NE5532x, SA5532x Dual Low-Noise Operational Amplifiers

1 Features

- Equivalent Input Noise Voltage: 5 nV/$\sqrt{\text{Hz}}$ Typ at 1 kHz
- Unity-Gain Bandwidth: 10 MHz Typ
- Common-Mode Rejection Ratio: 100 dB Typ
- High DC Voltage Gain: 100 V/mV Typ
- Peak-to-Peak Output Voltage Swing 26 V Typ With $V_{CC\pm}$ = ±15 V and R_L = 600 Ω
- High Slew Rate: 9 V/μs Typ

2 Applications

- AV Receivers
- Embedded PCs
- Netbooks
- Video Broadcasting and Infrastructure: Scalable Platforms
- DVD Recorders and Players
- Multichannel Video Transcoders
- Pro Audio Mixers

3 Description

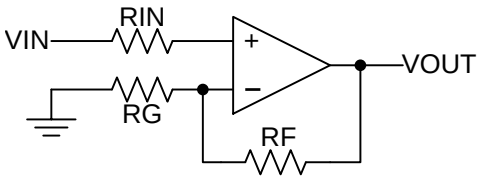
The NE5532, NE5532A, SA5532, and SA5532A devices are high-performance operational amplifiers combining excellent DC and AC characteristics. They feature very low noise, high output-drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are compensated internally for unity-gain operation. These devices have specified maximum limits for equivalent input noise voltage.

Device Information[1]

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
NE5532x, SA5532x	SOIC (8)	4.90 mm × 3.91 mm
NE5532x, SA5532x	PDIP (8)	9.81 mm × 6.35 mm
NE5532x	SO (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Simplified Schematic ... 1
5 Revision History ... 2
6 Pin Configuration and Functions ... 3
7 Specifications ... 4
7.1 Absolute Maximum Ratings ... 4
7.2 ESD Ratings ... 4
7.3 Recommended Operating Conditions ... 4
7.4 Thermal Information ... 4
7.5 Electrical Characteristics ... 5
7.6 Operating Characteristics ... 5
7.7 Typical Characteristics ... 6
8 Detailed Description ... 7
8.1 Overview ... 7
8.2 Functional Block Diagram ... 7
8.3 Feature Description ... 7
8.4 Device Functional Modes ... 7
9 Application and Implementation ... 8
9.1 Typical Application ... 8
10 Power Supply Recommendations ... 11
11 Layout ... 11
11.1 Layout Guidelines ... 11
11.2 Layout Example ... 11
12 Device and Documentation Support ... 13
12.1 Related Links ... 13
12.2 Trademarks ... 13
12.3 Electrostatic Discharge Caution ... 13
12.4 Glossary ... 13
13 Mechanical, Packaging, and Orderable Information ... 13

5 Revision History

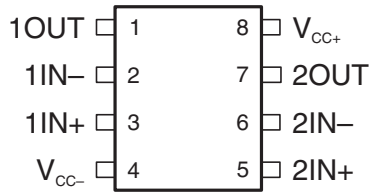
Changes from Revision I (April 2009) to Revision J **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1

Copyright © 1979–2015, Texas Instruments Incorporated

6 Pin Configuration and Functions

NE5532, NE5532A . . . D, P, OR PS PACKAGE
SA5532, SA5532A . . . D OR P PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
1IN+	3	I	Noninverting input
1IN-	2	I	Inverting Input
OUT1	1	O	Output
2IN+	5	I	Noninverting input
2IN-	6	I	Inverting Input
2OUT	7	O	Output
VCC+	8	—	Positive Supply
VCC-	4	—	Negative Supply

Copyright © 1979–2015, Texas Instruments Incorporated

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	V_{CC+}	0	22	V
		V_{CC-}	–22	0	V
	Input voltage, either input(2)(3)		V_{CC-}	V_{CC+}	V
	Input current(4)		–10	10	mA
	Duration of output short circuit(5)		Unlimited		
T_J	Operating virtual-junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
(4) Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
(5) The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC+}	Supply voltage		5	15	V
V_{CC-}	Supply voltage		–5	–15	V
T_A	Operating free-air temperature	NE5532, NE5532A	0	70	°C
		SA5532, SA5532A	–40	85	

7.4 Thermal Information

THERMAL METRIC(1)		NE5532, NE5532A, SA5532, and SA5532A			UNIT
		D	P	PS	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance (2)(3)	97	85	95	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The package thermal impedance is calculated in accordance with JESD 51-7.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A) / \theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

Copyright © 1979–2015, Texas Instruments Incorporated

7.5 Electrical Characteristics

$V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0	T_A = 25°C		0.5	4	mV
			T_A = Full range(2)			5	
I_{IO}	Input offset current	T_A = 25°C			10	150	nA
		T_A = Full range(2)				200	
I_{IB}	Input bias current	T_A = 25°C			200	800	nA
		T_A = Full range(2)				1000	
V_{ICR}	Common-mode input-voltage range			±12	±13		V
V_{OPP}	Maximum peak-to-peak output-voltage swing	R_L ≥ 600 Ω, $V_{CC\pm}$ = ±15 V		24	26		V
A_{VD}	Large-signal differential-voltage amplification	R_L ≥ 600 Ω, V_O = ±10 V	T_A = 25°C	15	50		V/mV
			T_A = Full range(2)	10			
		R_L ≥ 2 kΩ, V_O±10 V	T_A = 25°C	25	100		
			T_A = Full range(2)	15			
A_{vd}	Small-signal differential-voltage amplification	f = 10 kHz			2.2		V/mV
B_{OM}	Maximum output-swing bandwidth	R_L = 600 Ω, V_O = ±10 V			140		kHz
B_1	Unity-gain bandwidth	R_L = 600 Ω, C_L = 100 pF			10		MHz
r_i	Input resistance			30	300		kΩ
z_o	Output impedance	A_{VD} = 30 dB, R_L = 600 Ω, f = 10 kHz			0.3		Ω
CMRR	Common-mode rejection ratio	V_{IC} = V_{ICR} min		70	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC\pm}$ = ±9 V to ±15 V, V_O = 0		80	100		dB
I_{OS}	Output short-circuit current			10	38	60	mA
I_{CC}	Total supply current	V_O = 0, No load			8	16	mA
	Crosstalk attenuation (V_{O1}/V_{O2})	V_{01} = 10 V peak, f = 1 kHz			110		dB

(1) All characteristics are measured under open-loop conditions, with zero common-mode input voltage, unless otherwise specified.
(2) Full temperature ranges are: –40°C to 85°C for the SA5532 and SA5532A devices, and 0°C to 70°C for the NE5532 and NE5532A devices.

7.6 Operating Characteristics

$V_{CC\pm}$ = ±15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	NE5532, SA5532			NE5532A, SA5532A			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain			9			9		V/μs
	Overshoot factor	V_I = 100 mV, R_L = 600 Ω, A_{VD} = 1, C_L = 100 pF		10			10		%
V_n	Equivalent input noise voltage	f = 30 Hz		8			8	10	nV/√Hz
		f = 1 kHz		5			5	6	
I_n	Equivalent input noise current	f = 30 Hz		2.7			2.7		pA/√Hz
		f = 1 kHz		0.7			0.7		

Copyright © 1979–2015, Texas Instruments Incorporated

7.7 Typical Characteristics

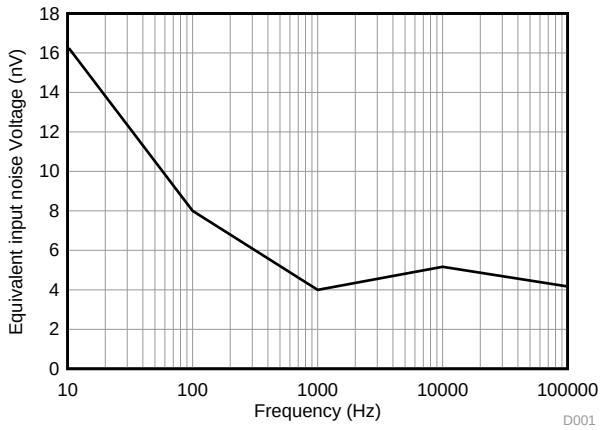


Figure 1. Equivalent Input Noise Voltage vs Frequency

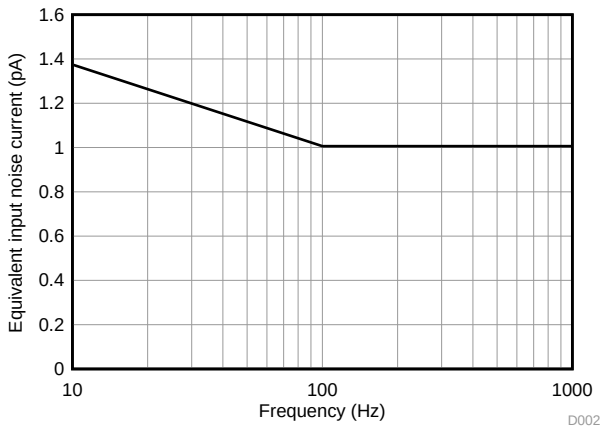


Figure 2. Equivalent Input Noise Current vs Frequency

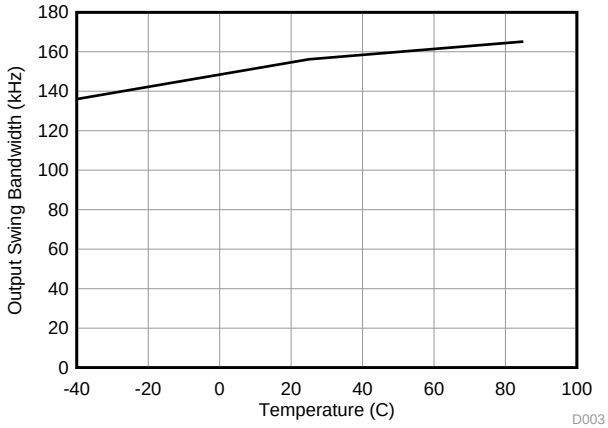


Figure 3. Output Swing Bandwidth vs Temperature at V_{CC} = ±10 V

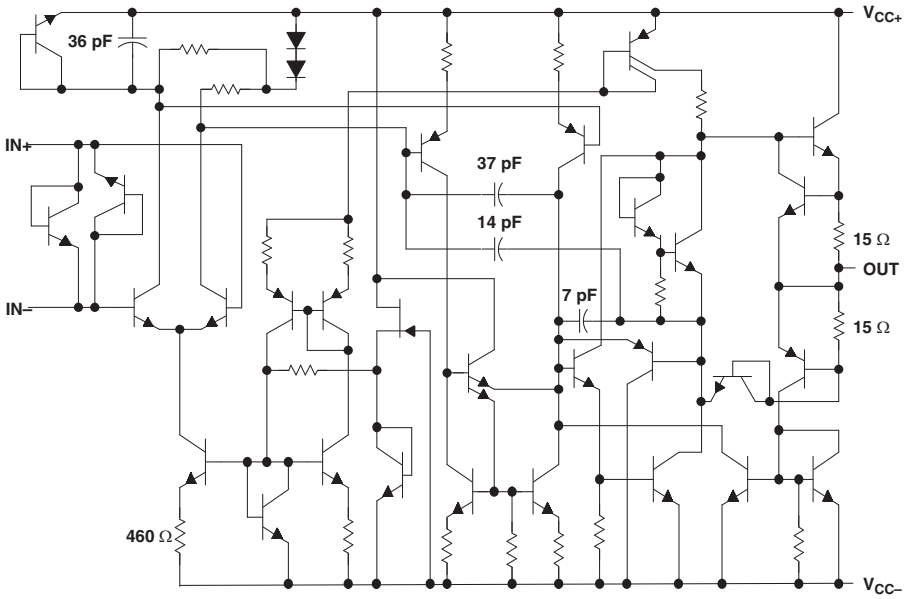
Copyright © 1979–2015, Texas Instruments Incorporated

8 Detailed Description

8.1 Overview

The NE5532, NE5532A, SA5532, and SA5532A devices are high-performance operational amplifiers combining excellent dc and ac characteristics. They feature very low noise, high output-drive capability, high unity-gain and maximum-output-swing bandwidths, low distortion, high slew rate, input-protection diodes, and output short-circuit protection. These operational amplifiers are compensated internally for unity-gain operation. These devices have specified maximum limits for equivalent input noise voltage.

8.2 Functional Block Diagram



Component values shown are nominal.

8.3 Feature Description

8.3.1 Unity-Gain Bandwidth

The unity-gain bandwidth is the frequency up to which an amplifier with a unity gain may be operated without greatly distorting the signal. The NE5532, NE5532A, SA5532, and SA5532A devices have a 10-MHz unity-gain bandwidth.

8.3.2 Common-Mode Rejection Ratio

The common-mode rejection ratio (CMRR) of an amplifier is a measure of how well the device rejects unwanted input signals common to both input leads. It is found by taking the ratio of the change in input offset voltage to the change in the input voltage and converting to decibels. Ideally the CMRR would be infinite, but in practice, amplifiers are designed to have it as high as possible. The CMRR of the NE5532, NE5532A, SA5532, and SA5532A devices is 100 dB.

8.3.3 Slew Rate

The slew rate is the rate at which an operational amplifier can change its output when there is a change on the input. The NE5532, NE5532A, SA5532, and SA5532A devices have a 9-V/ms slew rate.

8.4 Device Functional Modes

The NE5532, NE5532A, SA5532, and SA5532A devices are powered on when the supply is connected. Each of these devices can be operated as a single supply operational amplifier or dual supply amplifier depending on the application.

Copyright © 1979–2015, Texas Instruments Incorporated

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Typical Application

Some applications require differential signals. Figure 4 shows a simple circuit to convert a single-ended input of 2 V to 10 V into differential output of ±8 V on a single 15-V supply. The output range is intentionally limited to maximize linearity. The circuit is composed of two amplifiers. One amplifier acts as a buffer and creates a voltage, V_{OUT+}. The second amplifier inverts the input and adds a reference voltage to generate V_{OUT-}. Both V_{OUT+} and V_{OUT-} range from 2 V to 10 V. The difference, V_{DIFF}, is the difference between V_{OUT+} and V_{OUT-}.

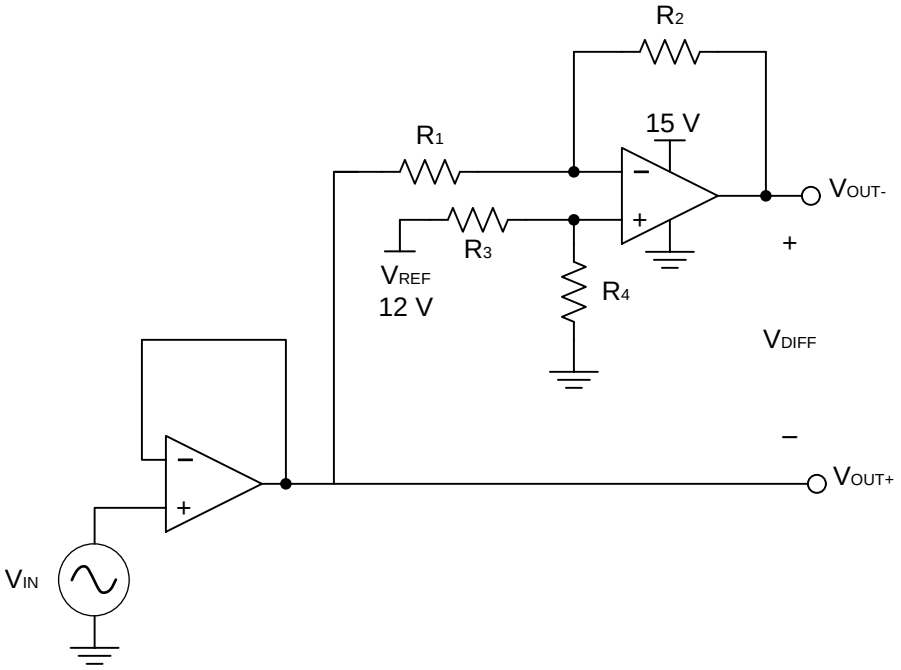


Figure 4. Schematic for Single-Ended Input to Differential Output Conversion

9.1.1 Design Requirements

The design requirements are as follows:

- Supply voltage: 15 V
- Reference voltage: 12V
- Input: 2 V to 10 V
- Output differential: ±8 V

Copyright © 1979–2015, Texas Instruments Incorporated

Typical Application (continued)

9.1.2 Detailed Design Procedure

The circuit in Figure 4 takes a single-ended input signal, V_{IN}, and generates two output signals, V_{OUT+} and V_{OUT-} using two amplifiers and a reference voltage, V_{REF}. V_{OUT+} is the output of the first amplifier and is a buffered version of the input signal, V_{IN} Equation 1. V_{OUT-} is the output of the second amplifier which uses V_{REF} to add an offset voltage to V_{IN} and feedback to add inverting gain. The transfer function for V_{OUT-} is Equation 2.

$$V_{OUT+} = V_{IN} \tag{1}$$

$$V_{out-} = V_{ref} \times \left(\frac{R4}{R3+R4}\right) \times \left(1+\frac{R2}{R1}\right) - V_{in} \times \frac{R2}{R1} \tag{2}$$

The differential output signal, V_{DIFF}, is the difference between the two single-ended output signals, V_{OUT+} and V_{OUT-}. Equation 3 shows the transfer function for V_{DIFF}. By applying the conditions that $R_1 = R_2$ and $R_3 = R_4$, the transfer function is simplified into Equation 6. Using this configuration, the maximum input signal is equal to the reference voltage and the maximum output of each amplifier is equal to the V_{REF}. The differential output range is $2 \times V_{REF}$. Furthermore, the common mode voltage will be one half of V_{REF} (see Equation 7).

$$V_{DIFF} = V_{OUT+} - V_{OUT-} = V_{IN} \times \left(1 + \frac{R_2}{R_1}\right) - V_{REF} \times \left(\frac{R_4}{R_3 + R_4}\right)\left(1 + \frac{R_2}{R_1}\right) \tag{3}$$

$$V_{OUT+} = V_{IN} \tag{4}$$

$$V_{OUT-} = V_{REF} - V_{IN} \tag{5}$$

$$V_{DIFF} = 2 \times V_{IN} - V_{REF} \tag{6}$$

$$V_{cm} = \left(\frac{V_{OUT+} + V_{OUT-}}{2}\right) = \frac{1}{2} V_{REF} \tag{7}$$

9.1.2.1 Amplifier Selection

Linearity over the input range is key for good dc accuracy. The common mode input range and the output swing limitations determine the linearity. In general, an amplifier with rail-to-rail input and output swing is required. Bandwidth is a key concern for this design. Since the NE5532 has a bandwidth of 10 MHz, this circuit will only be able to process signals with frequencies of less than 10 MHz.

9.1.2.2 Passive Component Selection

Because the transfer function of V_{OUT-} is heavily reliant on resistors (R_1, R_2, R_3, and R_4), use resistors with low tolerances to maximize performance and minimize error. This design used resistors with resistance values of 36 kΩ with tolerances measured to be within 2%. But, if the noise of the system is a key parameter, the user can select smaller resistance values (6 kΩ or lower) to keep the overall system noise low. This ensures that the noise from the resistors is lower than the amplifier noise.

9.1.3 Application Curves

The measured transfer functions in Figure 5, Figure 6, and Figure 7 were generated by sweeping the input voltage from 0 V to 12V. However, this design should only be used between 2 V and 10 V for optimum linearity.

Copyright © 1979–2015, Texas Instruments Incorporated

Typical Application (continued)

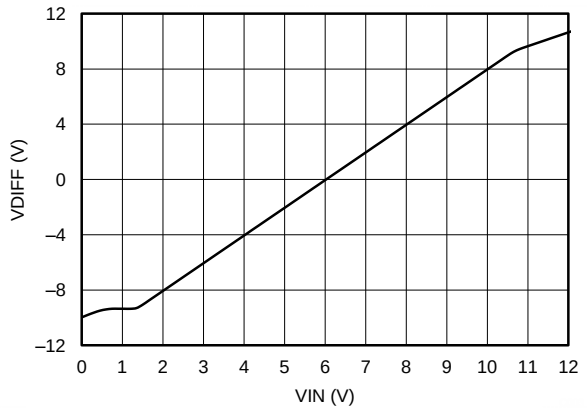


Figure 5. Differential Output Voltage vs Input Voltage

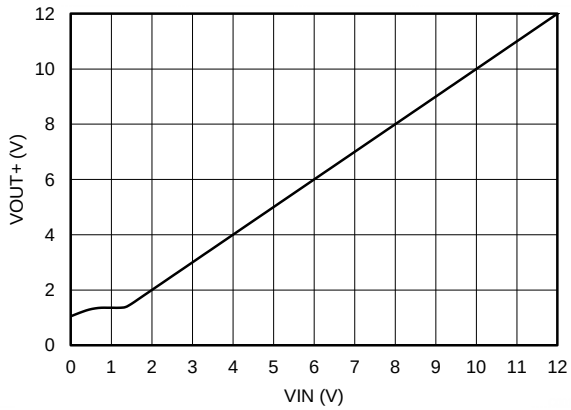


Figure 6. Positive Output Voltage Node vs Input Voltage

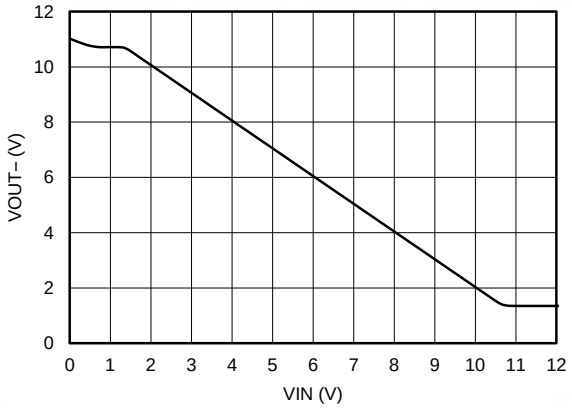


Figure 7. Positive Output Voltage Node vs Input Voltage

Copyright © 1979–2015, Texas Instruments Incorporated

10 Power Supply Recommendations

The NE5532x and SA5532x devices are specified for operation over the range of ±5 to ±15 V; many specifications apply from 0°C to 70°C (NE5532x) and -40°C to 85°C (SA5532x). The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages outside of the ±22 V range can permanently damage the device (see the *Absolute Maximum Ratings*).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to Circuit Board Layout Techniques, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in *Layout Example*.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

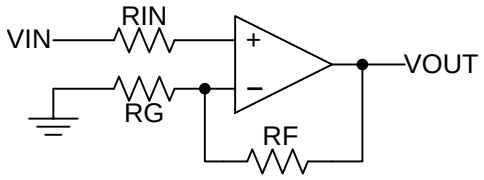


Figure 8. Operational Amplifier Schematic for Noninverting Configuration

Layout Example (continued)

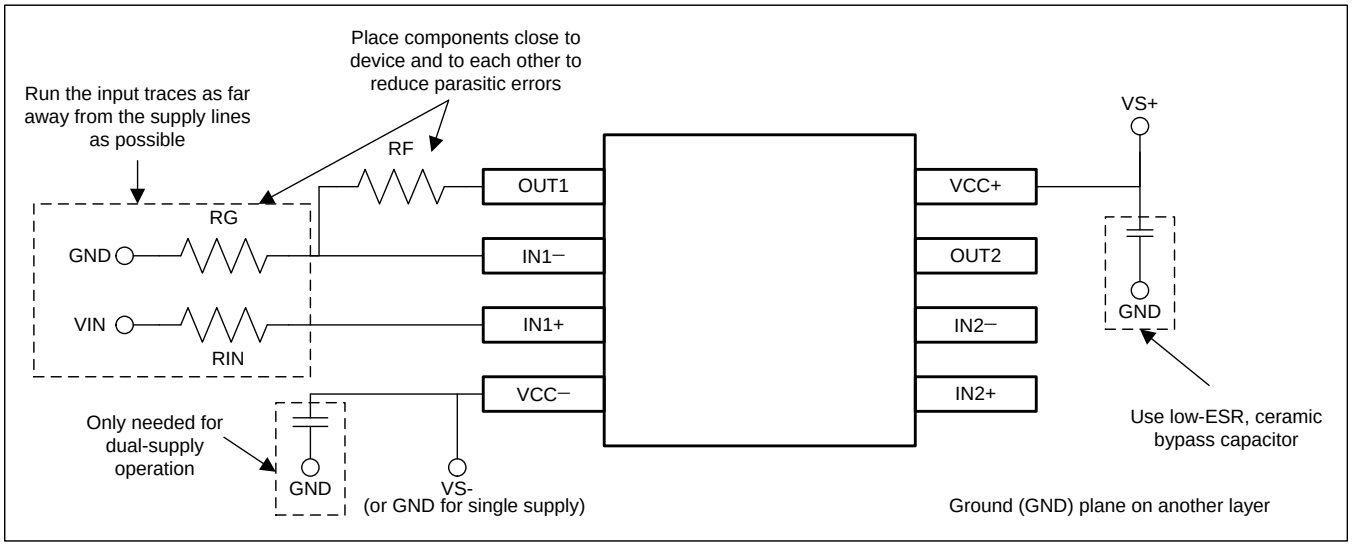


Figure 9. Operational Amplifier Board Layout for Noninverting Configuration

Copyright © 1979–2015, Texas Instruments Incorporated

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

Parts	Product Folder	Sample & Buy	Technical Documents	Tools & Software	Support & Community
NE5532	Click here	Click here	Click here	Click here	Click here
NE5532A	Click here	Click here	Click here	Click here	Click here
SA5532	Click here	Click here	Click here	Click here	Click here
SA5532A	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.4 Glossary

SLYZ022 — *TI Glossary.*

This glossary lists and explains terms, acronyms and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

Copyright © 1979–2015, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
NE5532AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532ADRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532AP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	NE5532AP	Samples
NE5532APE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	NE5532AP	Samples
NE5532APSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532APSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532A	Samples
NE5532D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	Samples
NE5532DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	N5532	Samples
NE5532DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	Samples
NE5532DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	Samples
NE5532P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	NIPDAU | SN	N / A for Pkg Type	0 to 70	NE5532P	Samples
NE5532PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	NIPDAU	N / A for Pkg Type	0 to 70	NE5532P	Samples
NE5532PSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	N5532	Samples
SA5532AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A	Samples
SA5532ADG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SA5532ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532A	Samples
SA5532AP	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	SA5532AP	Samples
SA5532APE4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	SA5532AP	Samples
SA5532D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532	Samples
SA5532DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SA5532	Samples
SA5532P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-40 to 85	SA5532P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

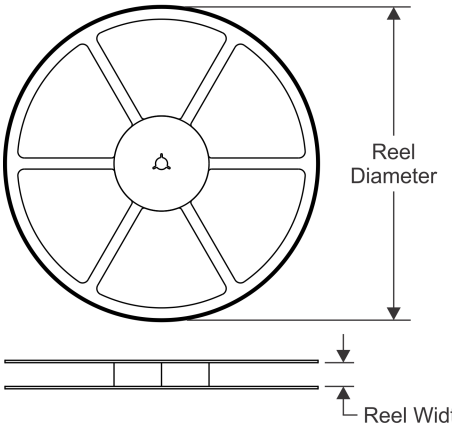
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

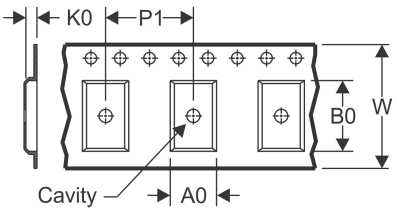
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

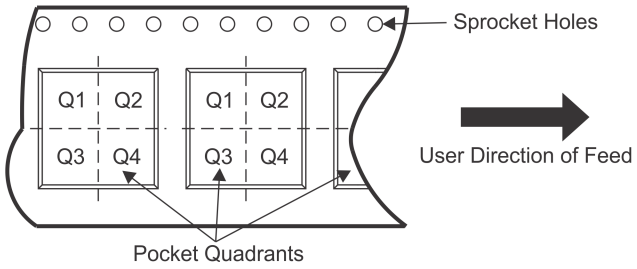


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

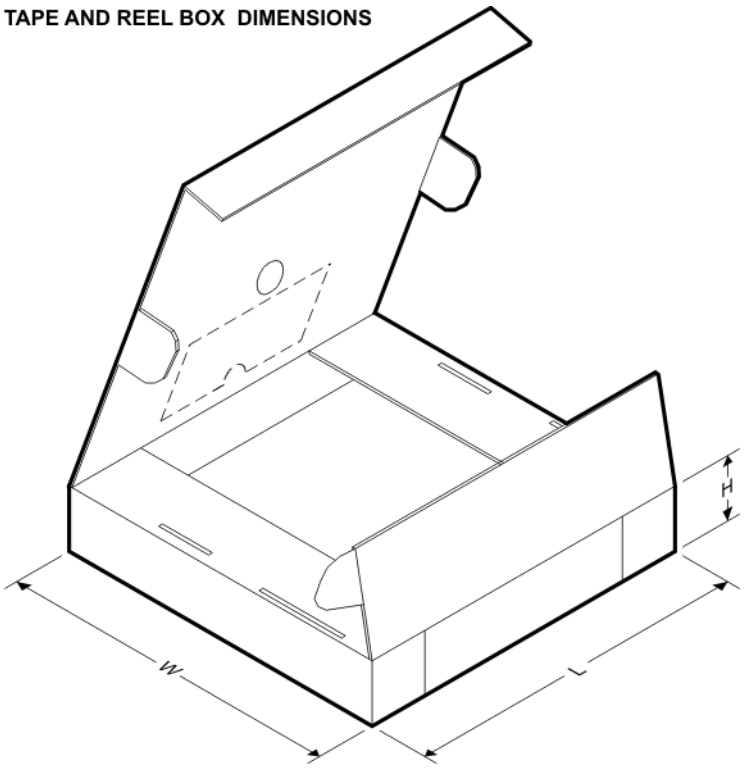
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

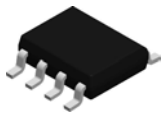
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
NE5532ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5532DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
NE5532DR	SOIC	D	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
NE5532DRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA5532ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SA5532DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
NE5532ADR	SOIC	D	8	2500	340.5	338.1	20.6
NE5532DR	SOIC	D	8	2500	340.5	338.1	20.6
NE5532DR	SOIC	D	8	2500	364.0	364.0	27.0
NE5532DRG4	SOIC	D	8	2500	340.5	338.1	20.6
SA5532ADR	SOIC	D	8	2500	340.5	338.1	20.6
SA5532DR	SOIC	D	8	2500	340.5	338.1	20.6

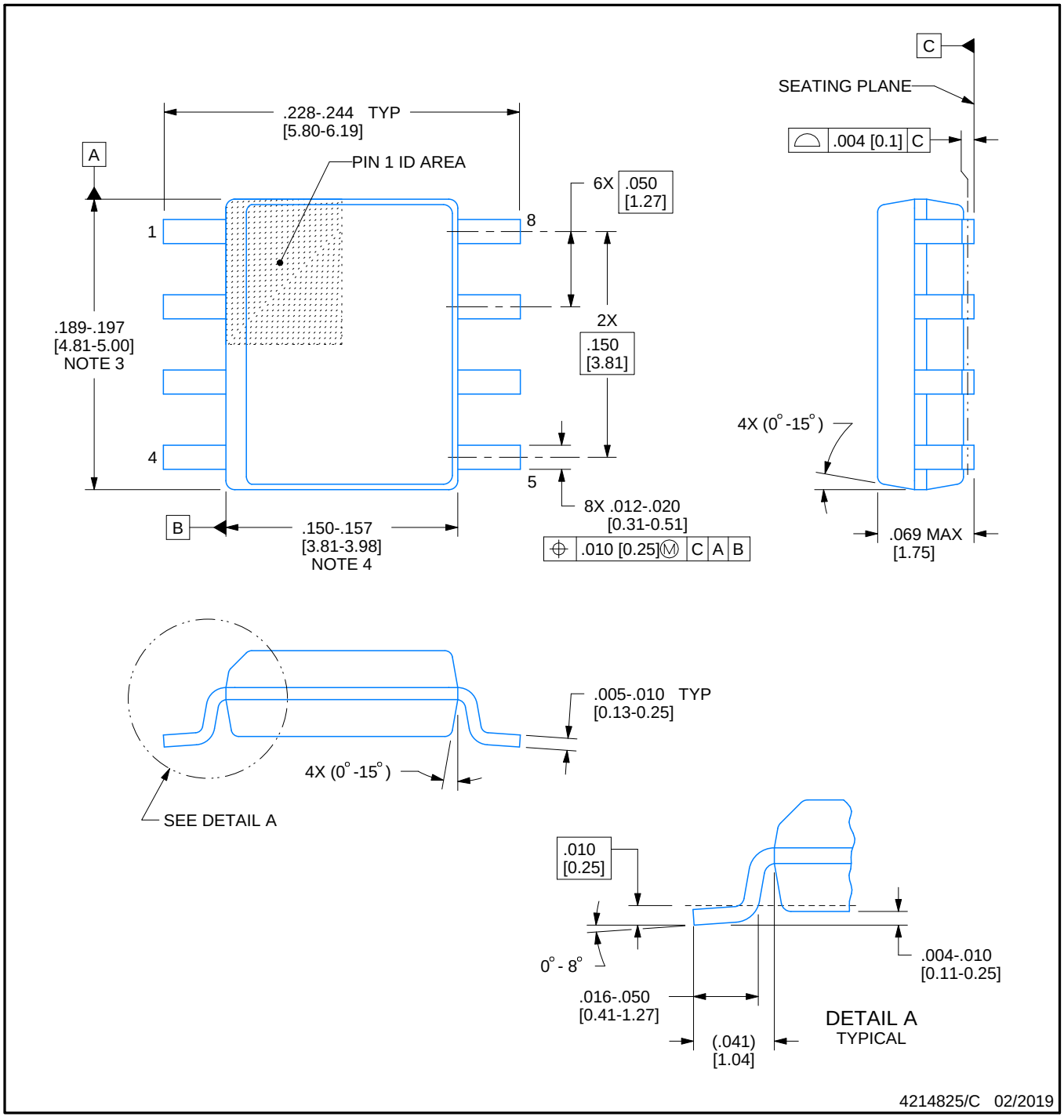


PACKAGE OUTLINE

D0008A

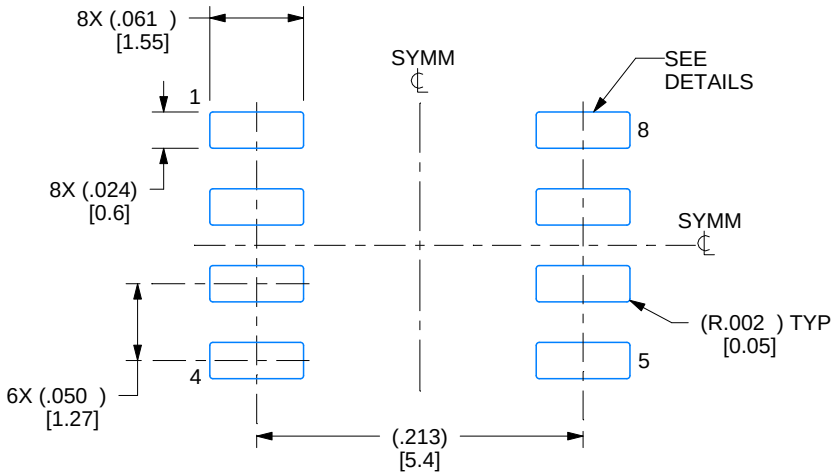
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

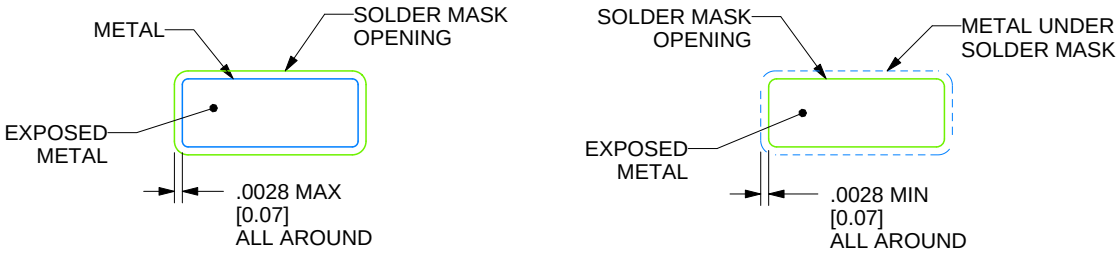


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

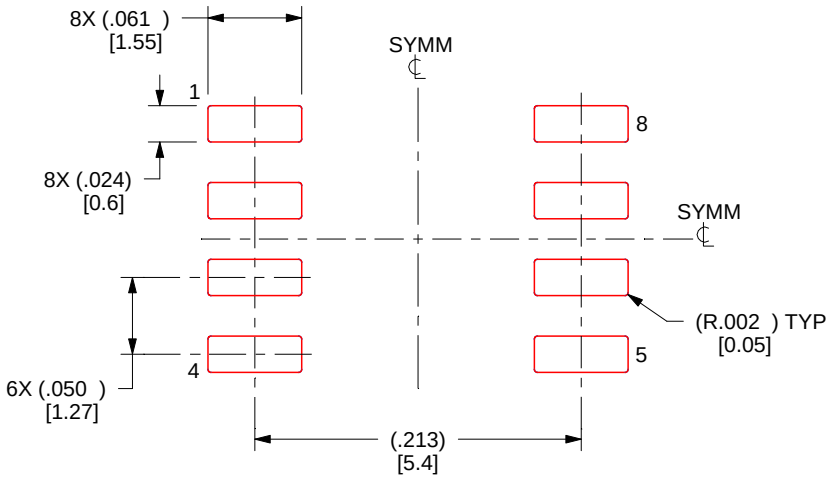
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

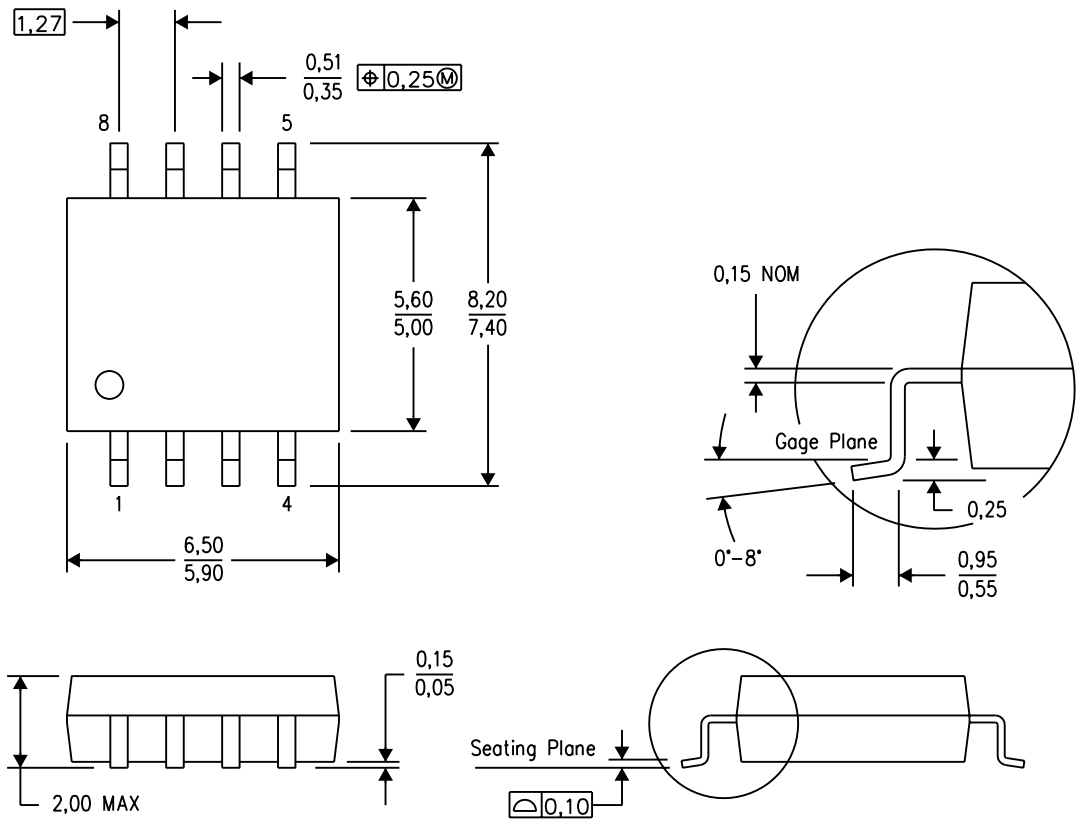
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

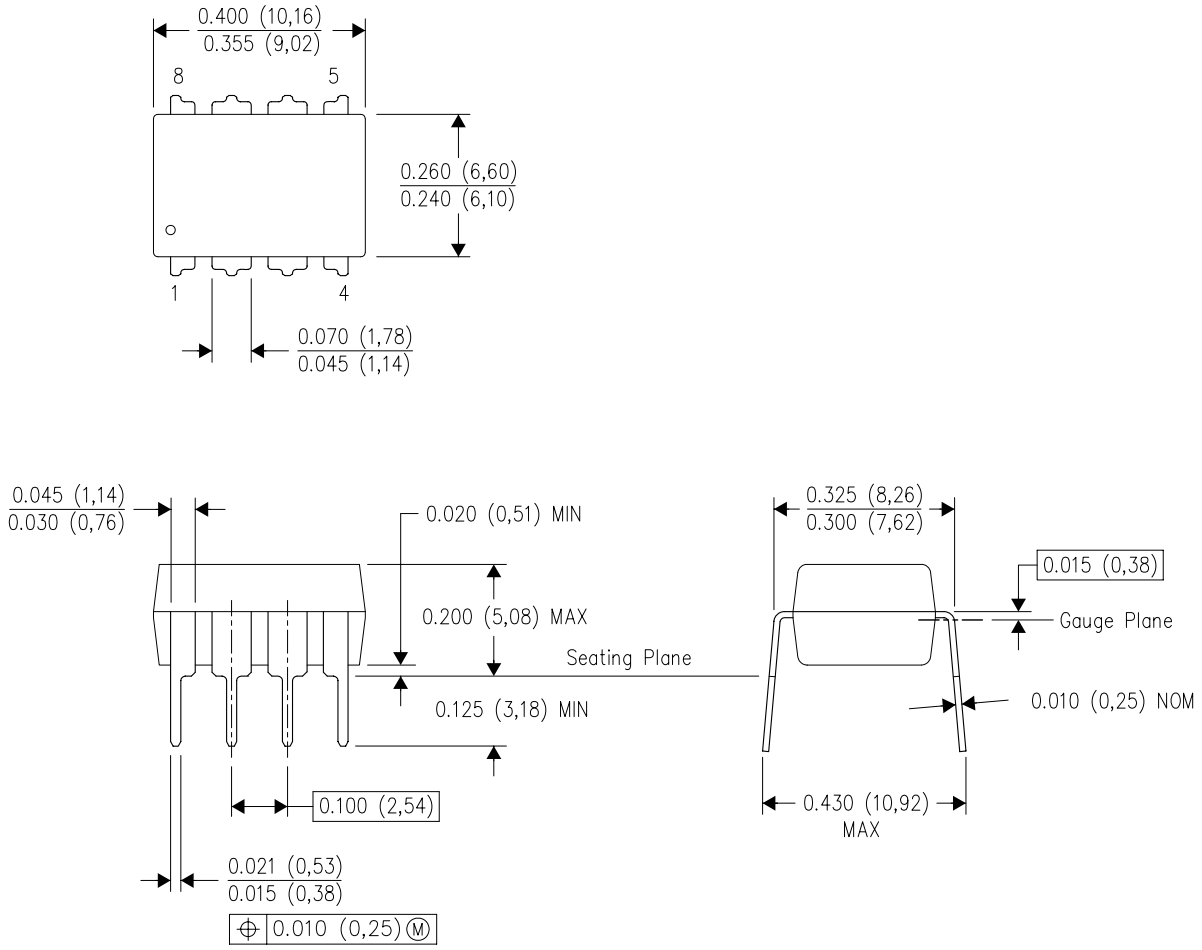
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated