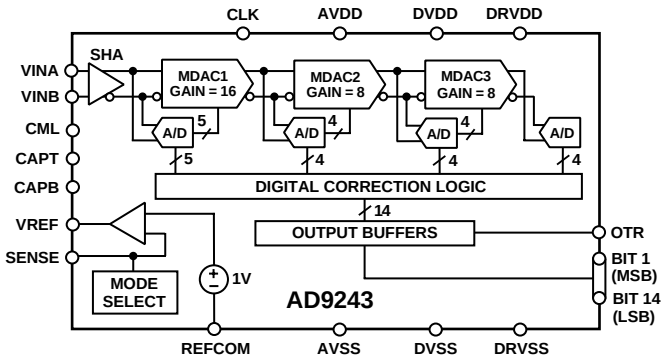
Complete 14-Bit, 3.0 MSPS Monolithic A/D Converter

AD9243

FEATURES

Monolithic 14-Bit, 3 MSPS A/D Converter
Low Power Dissipation: 110 mW
Single +5 V Supply
Integral Nonlinearity Error: 2.5 LSB
Differential Nonlinearity Error: 0.6 LSB
Input Referred Noise: 0.36 LSB
Complete: On-Chip Sample-and-Hold Amplifier and Voltage Reference
Signal-to-Noise and Distortion Ratio: 79.0 dB
Spurious-Free Dynamic Range: 91.0 dB
Out-of-Range Indicator
Straight Binary Output Data
44-Lead MQFP

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9243 is a 3 MSPS, single supply, 14-bit analog-to-digital converter (ADC). It combines a low cost, high speed CMOS process and a novel architecture to achieve the resolution and speed of existing hybrid implementations at a fraction of the power consumption and cost. It is a complete, monolithic ADC with an on-chip, high performance, low noise sample-and-hold amplifier and programmable voltage reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of the application. The device uses a multistage differential pipelined architecture with digital output error correction logic to guarantee no missing codes over the full operating temperature range.

The input of the AD9243 is highly flexible, allowing for easy interfacing to imaging, communications, medical, and data-acquisition systems. A truly differential input structure allows for both single-ended and differential input interfaces of varying input spans. The sample-and-hold amplifier (SHA) is equally suited for both multiplexed systems that switch full-scale voltage levels in successive channels as well as sampling single-channel inputs at frequencies up to and beyond the Nyquist rate. Also, the AD9243 performs well in communication systems employing Direct-IF Down Conversion since the SHA in the differential input mode can achieve excellent dynamic performance *well beyond* its specified Nyquist frequency of 1.5 MHz.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range (OTR) signal indicates an overflow condition which can be used with the most significant bit to determine low or high overflow.

PRODUCT HIGHLIGHTS

The AD9243 offers a complete single-chip sampling 14-bit, analog-to-digital conversion function in a 44-lead Metric Quad Flatpack.

Low Power and Single Supply

The AD9243 consumes only 110 mW on a single +5 V power supply.

Excellent DC Performance Over Temperature

The AD9243 provides no missing codes, and excellent temperature drift performance over the full operating temperature range.

Excellent AC Performance and Low Noise

The AD9243 provides nearly 13 ENOB performance and has an input referred noise of 0.36 LSB rms.

Flexible Analog Input Range

The versatile onboard sample-and-hold (SHA) can be configured for either single ended or differential inputs of varying input spans.

Flexible Digital Outputs

The digital outputs can be configured to interface with +3 V and +5 V CMOS logic families.

REV. A

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 World Wide Web Site: http://www.analog.com
Fax: 781/326-8703
© Analog Devices, Inc., 1998

AD9243–SPECIFICATIONS

DC SPECIFICATIONS (AVDD = +5 V, DVDD = +5 V, DRVDD = +5 V, f_{SAMPLE} = 3 MSPS, VREF = 2.5 V, VINB = 2.5 V, T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	AD9243	Units
RESOLUTION	14	Bits min
MAX CONVERSION RATE	3	MHz min
INPUT REFERRED NOISE		
V_{REF} = 1 V	0.9	LSB rms typ
V_{REF} = 2.5 V	0.36	LSB rms typ
ACCURACY		
Integral Nonlinearity (INL)	±2.5	LSB typ
Differential Nonlinearity (DNL)	±0.6	LSB typ
	±1.0	LSB max
INL[1]	±2.5	LSB typ
DNL[1]	±0.7	LSB typ
No Missing Codes	14	Bits Guaranteed
Zero Error (@ +25°C)	0.3	% FSR max
Gain Error (@ +25°C)[2]	1.5	% FSR max
Gain Error (@ +25°C)[3]	0.75	% FSR max
TEMPERATURE DRIFT		
Zero Error	3.0	ppm/°C typ
Gain Error[2]	20.0	ppm/°C typ
Gain Error[3]	5.0	ppm/°C typ
POWER SUPPLY REJECTION	0.1	% FSR max
ANALOG INPUT		
Input Span (with V_{REF} = 1.0 V)	2	V p-p min
(with V_{REF} = 2.5 V)	5	V p-p max
Input (VINA or VINB) Range	0	V min
	AVDD	V max
Input Capacitance	16	pF typ
INTERNAL VOLTAGE REFERENCE		
Output Voltage (1 V Mode)	1	Volts typ
Output Voltage Tolerance (1 V Mode)	±14	mV max
Output Voltage (2.5 V Mode)	2.5	Volts typ
Output Voltage Tolerance (2.5 V Mode)	±35	mV max
Load Regulation[4]	2.0	mV max
REFERENCE INPUT RESISTANCE	5	kΩ typ
POWER SUPPLIES		
Supply Voltages		
AVDD	+5	V (±5% AVDD Operating)
DVDD	+5	V (±5% DVDD Operating)
DRVDD	+5	V (±5% DRVDD Operating)
Supply Current		
IAVDD	23.0	mA max (20 mA typ)
IDRVDD	1.0	mA max (0.5 mA typ)
IDVDD	5.0	mA max (3.5 mA typ)
POWER CONSUMPTION	110	mW typ
	145	mW max

NOTES
[1]V_{REF} =1 V.
[2]Including internal reference.
[3]Excluding internal reference.
[4]Load regulation with 1 mA load current (in addition to that required by the AD9243).

Specification subject to change without notice.

AC SPECIFICATIONS (AVDD = +5 V, DVDD= +5 V, DRVDD = +5 V, f_{SAMPLE} = 3 MSPS, VREF = 2.5 V, A_{IN} = –0.5 dBFS, AC Coupled/ Differential Input, T_{MIN} to T_{MAX} unless otherwise noted)

Parameter	AD9243	Units
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)		
f_{INPUT} = 500 kHz	75.0	dB min
	79.0	dB typ
f_{INPUT} = 1.5 MHz	77.0	dB typ
EFFECTIVE NUMBER OF BITS (ENOB)		
f_{INPUT} = 500 kHz	12.3	Bits min
	12.8	Bits typ
f_{INPUT} = 1.5 MHz	12.5	Bits typ
SIGNAL-TO-NOISE RATIO (SNR)		
f_{INPUT} = 500 kHz	76.0	dB min
	80.0	dB typ
f_{INPUT} = 1.5 MHz	79.0	dB typ
TOTAL HARMONIC DISTORTION (THD)		
f_{INPUT} = 500 kHz	–78.0	dB max
	–87.0	dB typ
f_{INPUT} = 1.5 MHz	–82.0	dB typ
SPURIOUS FREE DYNAMIC RANGE		
f_{INPUT} = 500 kHz	91.0	dB typ
f_{INPUT} = 1.5 MHz	84.0	dB typ
DYNAMIC PERFORMANCE		
Full Power Bandwidth	40	MHz typ
Small Signal Bandwidth	40	MHz typ
Aperture Delay	1	ns typ
Aperture Jitter	4	ps rms typ
Acquisition to Full-Scale Step (0.0025%)	80	ns typ
Overvoltage Recovery Time	167	ns typ

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS (AVDD = +5 V, DVDD = +5 V, T_{MIN} to T_{MAX} unless otherwise noted)

Parameters	Symbol	AD9243	Units
LOGIC INPUTS			
High Level Input Voltage	V_{IH}	+3.5	V min
Low Level Input Voltage	V_{IL}	+1.0	V max
High Level Input Current (V_{IN} = DVDD)	I_{IH}	±10	μA max
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	±10	μA max
Input Capacitance	C_{IN}	5	pF typ
LOGIC OUTPUTS (with DRVDD = 5 V)			
High Level Output Voltage (I_{OH} = 50 μA)	V_{OH}	+4.5	V min
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	+2.4	V min
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}	+0.4	V max
Low Level Output Voltage (I_{OL} = 50 μA)	V_{OL}	+0.1	V max
Output Capacitance	C_{OUT}	5	pF typ
LOGIC OUTPUTS (with DRVDD = 3 V)			
High Level Output Voltage (I_{OH} = 50 μA)	V_{OH}	+2.4	V min
Low Level Output Voltage (I_{OL} = 50 μA)	V_{OL}	+0.7	V max

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (T_{MIN} to T_{MAX} with AVDD = +5 V, DVDD = +5 V, DRVDD = +5 V, C_L = 20 pF)

Parameters	Symbol	AD9243	Units
Clock Period[1]	t_C	333	ns min
CLOCK Pulsewidth High	t_{CH}	150	ns min
CLOCK Pulsewidth Low	t_{CL}	150	ns min
Output Delay	t_{OD}	8	ns min
		13	ns typ
		19	ns max
Pipeline Delay (Latency)		3	Clock Cycles

NOTES
[1]The clock period may be extended to 1 ms without degradation in specified performance @ +25 °C.

Specifications subject to change without notice.

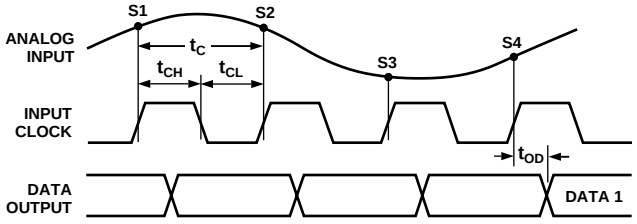


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Units
AVDD	AVSS	–0.3	+6.5	V
DVDD	DVSS	–0.3	+6.5	V
AVSS	DVSS	–0.3	+0.3	V
AVDD	DVDD	–6.5	+6.5	V
DRVDD	DRVSS	–0.3	+6.5	V
DRVSS	AVSS	–0.3	+0.3	V
REFCOM	AVSS	–0.3	+0.3	V
CLK	DVSS	–0.3	DVDD + 0.3	V
Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
VINA, VINB	AVSS	–0.3	AVDD + 0.3	V
VREF	AVSS	–0.3	AVDD + 0.3	V
SENSE	AVSS	–0.3	AVDD + 0.3	V
CAPB, CAPT	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			+150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			+300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

THERMAL CHARACTERISTICS

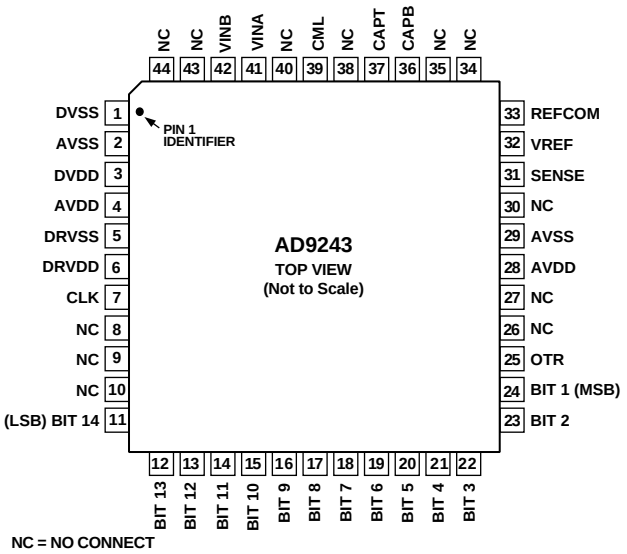
Thermal Resistance
44-Lead MQFP
θ_{JA} = 53.2°C/W
θ_{JC} = 19°C/W

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option*
AD9243AS	–40°C to +85°C	44-Lead MQFP	S-44
AD9243EB	Evaluation Board		

*S = Metric Quad Flatpack.

PIN CONNECTIONS



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9243 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN DESCRIPTION

Pin Number	Name	Description
1	DVSS	Digital Ground
2, 29	AVSS	Analog Ground
3	DVDD	+5 V Digital Supply
4, 28	AVDD	+5 V Analog Supply
5	DRVSS	Digital Output Driver Ground
6	DRVDD	Digital Output Driver Supply
7	CLK	Clock Input Pin
8–10	NC	No Connect
11	BIT 14	Least Significant Data Bit (LSB)
12–23	BIT 13–BIT 2	Data Output Bits
24	BIT 1	Most Significant Data Bit (MSB)
25	OTR	Out of Range
26, 27, 30	NC	No Connect
31	SENSE	Reference Select
32	VREF	Reference I/O
33	REFCOM	Reference Common
34, 35, 38	NC	No Connect
40, 43, 44		
36	CAPB	Noise Reduction Pin
37	CAPT	Noise Reduction Pin
39	CML	Common-Mode Level (Midsupply)
41	VINA	Analog Input Pin (+)
42	VINB	Analog Input Pin (–)

DEFINITIONS OF SPECIFICATION

INTEGRAL NONLINEARITY (INL)

INL refers to the deviation of each individual code from a line drawn from "negative full scale" through "positive full scale." The point used as "negative full scale" occurs 1/2 LSB before the first code transition. "Positive full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

DIFFERENTIAL NONLINEARITY (DNL, NO MISSING CODES)

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 14-bit resolution indicates that all 16384 codes, respectively, must be present over all operating ranges.

ZERO ERROR

The major carry transition should occur for an analog value 1/2 LSB below VINA = VINB. Zero error is defined as the deviation of the actual transition from that point.

GAIN ERROR

The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

OVERVOLTAGE RECOVERY TIME

Overvoltage recovery time is defined as that amount of time required for the ADC to achieve a specified accuracy after an overvoltage (50% greater than full-scale range), measured from the time the overvoltage signal reenters the converter's range.

TEMPERATURE DRIFT

The temperature drift for zero error and gain error specifies the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

APERTURE DELAY

Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D, SINAD) RATIO

S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

EFFECTIVE NUMBER OF BITS (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits.

Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

SIGNAL-TO-NOISE RATIO (SNR)

SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

TWO-TONE SFDR

The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal level is lowered), or in dBFS (always related back to converter full scale).

Typical Differential AC Characterization Curves/Plots

(AVDD = +5 V, DVDD = +5 V, DRVDD = +5 V, f_{SAMPLE} = 3.00 MSPS, T_A = +25°C, Differential Input)

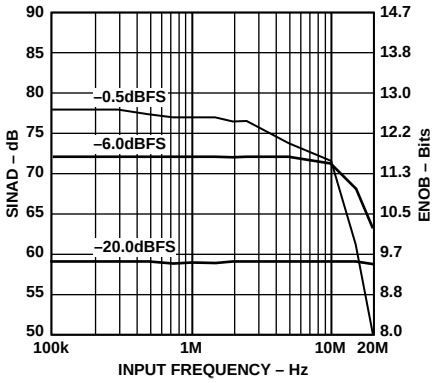


Figure 2. SINAD vs. Input Frequency (Input Span = 5 V, V_{CM} = 2.5 V)

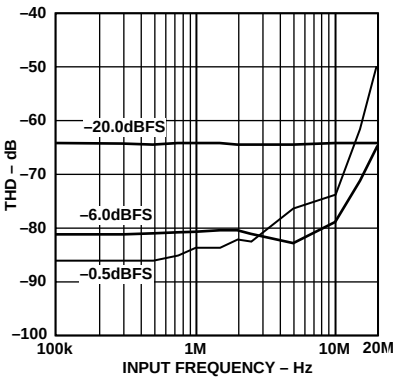


Figure 3. THD vs. Input Frequency (Input Span = 5 V, V_{CM} = 2.5 V)

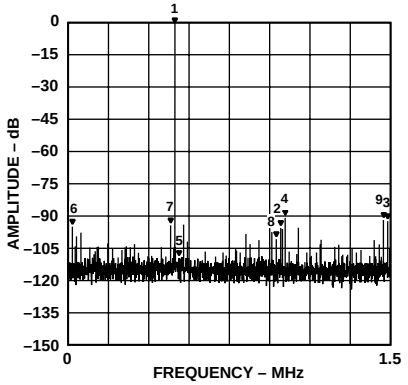


Figure 4. Typical FFT, f_{IN} = 500 kHz (Input Span = 5 V, V_{CM} = 2.5 V)

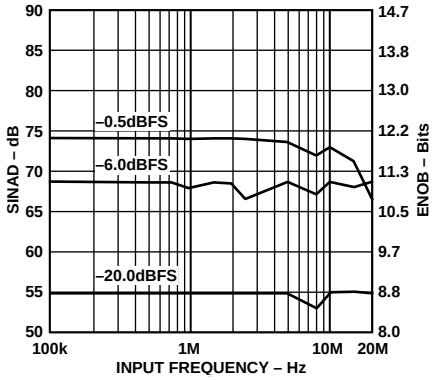


Figure 5. SINAD vs. Input Frequency (Input Span = 2 V, V_{CM} = 2.5 V)

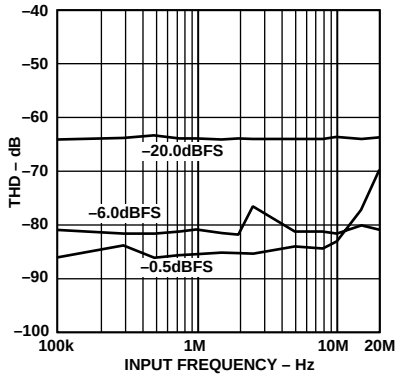


Figure 6. THD vs. Input Frequency (Input Span = 2 V, V_{CM} = 2.5 V)

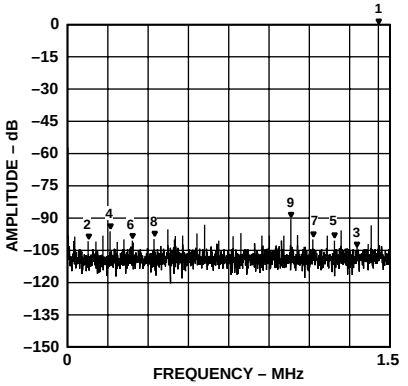


Figure 7. Typical FFT, f_{IN} = 1.50 MHz (Input Span = 2 V, V_{CM} = 2.5 V)

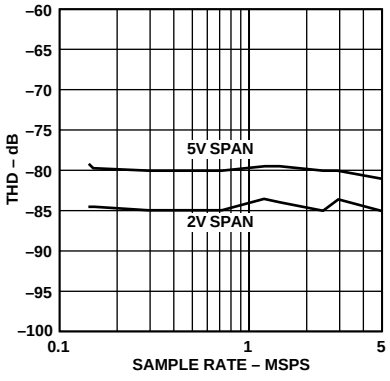


Figure 8. THD vs. Sample Rate (f_{IN} = 1.5 MHz, A_{IN} = –0.5 dBFS, V_{CM} = 2.5 V)

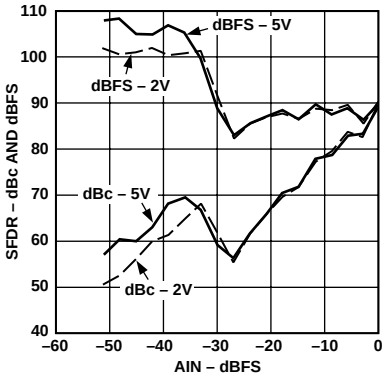


Figure 9. Single Tone SFDR (f_{IN} = 1.5 MHz, V_{CM} = 2.5 V)

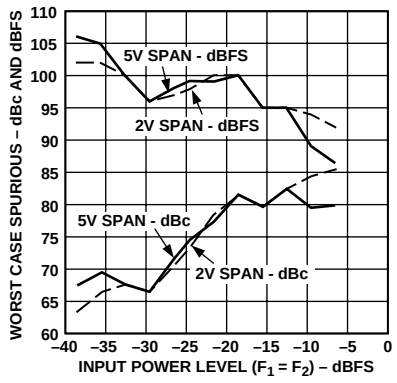


Figure 10. Dual Tone SFDR (f_1 = 0.95 MHz, f_2 = 1.04 MHz, V_{CM} = 2.5 V)

Other Characterization Curves/Plots

(AVDD = +5 V, DVDD = +5 V, DRVDD = +5 V, f_{SAMPLE} = 3.00 MSPS, T_A = +25°C, Single-Ended Input)

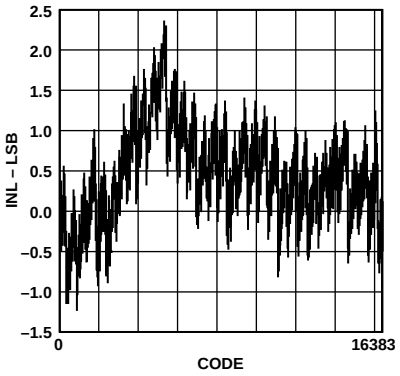


Figure 11. Typical INL (Input Span = 5 V)

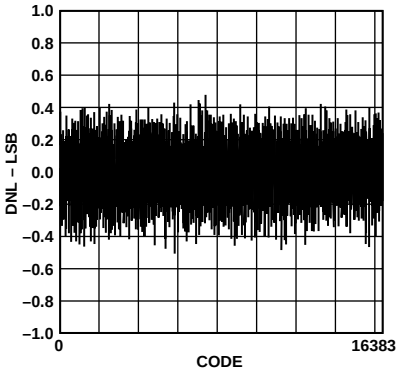


Figure 12. Typical DNL (Input Span = 5 V)

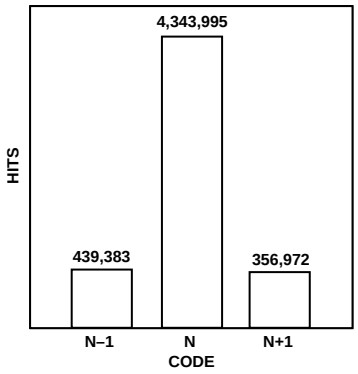


Figure 13. "Grounded-Input" Histogram (Input Span = 5 V)

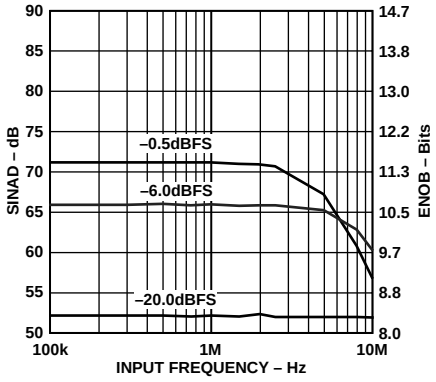


Figure 14. SINAD vs. Input Frequency (Input Span = 2 V, V_{CM} = 2.5 V)

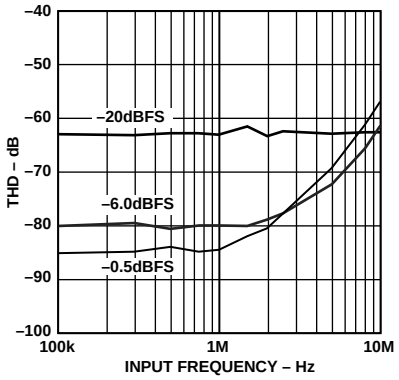


Figure 15. THD vs. Input Frequency (Input Span = 2 V, V_{CM} = 2.5 V)

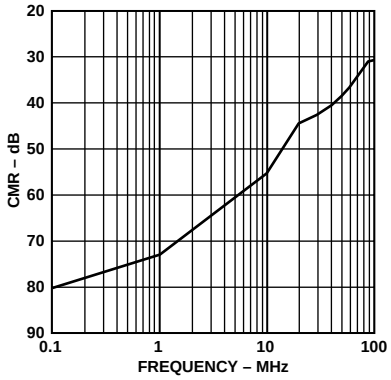


Figure 16. CMR vs. Input Frequency (Input Span = 2 V, V_{CM} = 2.5 V)

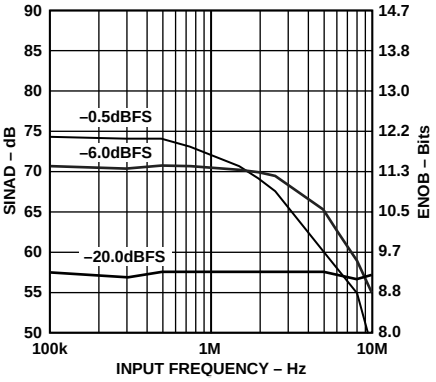


Figure 17. SINAD vs. Input Frequency (Input Span = 5 V, V_{CM} = 2.5 V)

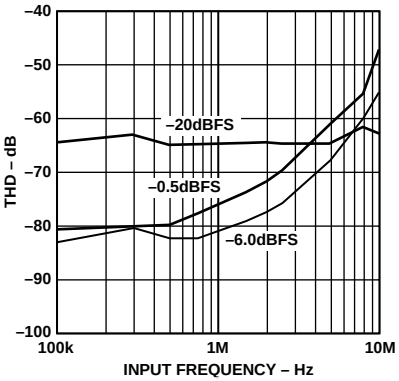


Figure 18. THD vs. Input Frequency (Input Span = 5 V, V_{CM} = 2.5 V)

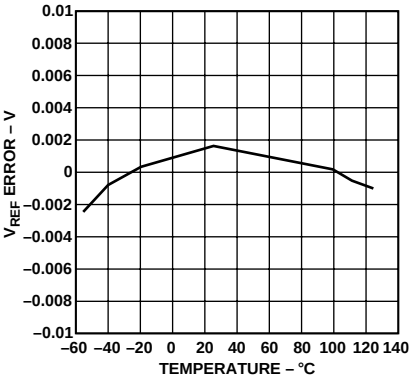


Figure 19. Typical Voltage Reference Error vs. Temperature

INTRODUCTION

The AD9243 utilizes a four-stage pipeline architecture with a wideband input sample-and-hold amplifier (SHA) implemented on a cost-effective CMOS process. Each stage of the pipeline, excluding the last stage, consists of a low resolution flash A/D connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier amplifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash A/D.

The pipeline architecture allows a greater throughput rate at the expense of pipeline delay or latency. This means that while the converter is capable of capturing a new input sample every clock cycle, it actually takes three clock cycles for the conversion to be fully processed and appear at the output. This latency is not a concern in most applications. The digital output, together with the out-of-range indicator (OTR), is latched into an output buffer to drive the output pins. The output drivers can be configured to interface with +5 V or +3.3 V logic families.

The AD9243 uses both edges of the clock in its internal timing circuitry (see Figure 1 and specification page for exact timing requirements). The A/D samples the analog input on the rising edge of the clock input. During the clock low time (between the falling edge and rising edge of the clock), the input SHA is in the sample mode; during the clock high time it is in the hold mode. System disturbances just prior to the rising edge of the clock and/or excessive clock jitter may cause the input SHA to acquire the wrong value, and should be minimized.

ANALOG INPUT AND REFERENCE OVERVIEW

Figure 20, a simplified model of the AD9243, highlights the relationship between the analog inputs, VINA, VINB, and the reference voltage, VREF. Like the voltage applied to the top of the resistor ladder in a flash A/D converter, the value VREF defines the maximum input voltage to the *A/D core*. The minimum input voltage to the *A/D core* is automatically defined to be –VREF.

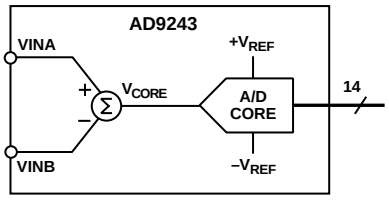


Figure 20. AD9243 Equivalent Functional Input Circuit

The addition of a differential input structure gives the user an additional level of flexibility that is not possible with traditional flash converters. The input stage allows the user to easily configure the inputs for either single-ended operation or differential operation. The A/D's input structure allows the dc offset of the input signal to be varied independently of the input span of the converter. Specifically, the input to the *A/D core* is the difference of the voltages applied at the VINA and VINB input pins.

Therefore, the equation,

$$V_{CORE} = VINA - VINB \quad (1)$$

defines the output of the differential input stage and provides the input to the A/D core.

The voltage, V_{CORE}, must satisfy the condition,

$$-VREF \le V_{CORE} \le VREF \quad (2)$$

where *VREF* is the voltage at the *VREF* pin.

While an infinite combination of VINA and VINB inputs exist that satisfy Equation 2, there is an additional limitation placed on the inputs by the power supply voltages of the AD9243. The power supplies bound the valid operating range for VINA and VINB. The condition,

$$AVSS - 0.3\ V < VINA < AVDD + 0.3\ V \quad (3)$$
$$AVSS - 0.3\ V < VINB < AVDD + 0.3\ V$$

where *AV*SS is nominally 0 V and *AV*DD is nominally +5 V, defines this requirement. Thus, the range of valid inputs for VINA and VINB is any combination that satisfies both Equations 2 and 3.

For additional information showing the relationship between VINA, VINB, VREF and the digital output of the AD9243, see Table IV.

Refer to Table I and Table II for a summary of the various analog input and reference configurations**.**

ANALOG INPUT OPERATION

Figure 21 shows the equivalent analog input of the AD9243 which consists of a differential sample-and-hold amplifier (SHA). The differential input structure of the SHA is highly flexible, allowing the devices to be easily configured for either a differential or single-ended input. The dc offset, or common-mode voltage, of the input(s) can be set to accommodate either single-supply or dual supply systems. Also, note that the analog inputs, VINA and VINB, are interchangeable with the exception that reversing the inputs to the VINA and VINB pins results in a polarity inversion.

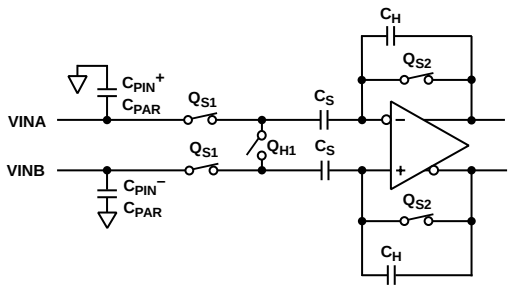


Figure 21. AD9243 Simplified Input Circuit

The input SHA of the AD9243 is optimized to meet the performance requirements for some of the most demanding communication, imaging, and data acquisition applications while maintaining low power dissipation. Figure 22 is a graph of the full-power bandwidth of the AD9243, typically 40 MHz. Note that the small signal bandwidth is the same as the full-power bandwidth. The settling time response to a full-scale stepped input is shown in Figure 23 and is typically 80 ns to 0.0025%. The low input referred noise of 0.36 LSB's rms is displayed via a grounded histogram and is shown in Figure 13.

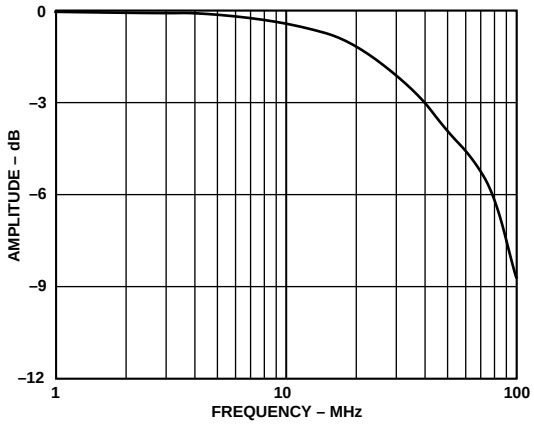


Figure 22. Full-Power Bandwidth

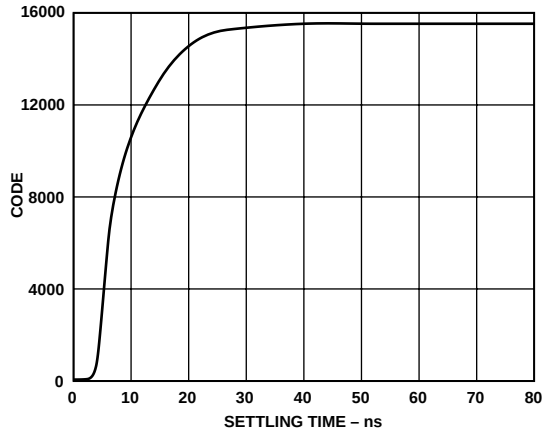


Figure 23. Settling Time

The SHA's optimum *distortion* performance for a differential or single-ended input is achieved under the following two conditions: (1) the common-mode voltage is centered around mid supply (i.e., AVDD/2 or approximately 2.5 V) and (2) the input signal voltage span of the SHA is set at its lowest (i.e., 2 V input span). This is due to the sampling switches, Q_{S1}, being CMOS switches whose R_{ON} resistance is very low but has some signal dependency which causes frequency dependent ac distortion while the SHA is in the track mode. The R_{ON} resistance of a CMOS switch is typically lowest at its midsupply but increases symmetrically as the input signal approaches either AVDD or AVSS. A lower input signal voltage span centered at midsupply reduces the degree of R_{ON} modulation.

Figure 24 compares the AD9243's THD vs. frequency performance for a 2 V input span with a common-mode voltage of 1 V and 2.5 V. Note the difference in the amount of degradation in THD performance as the input frequency increases. Similarly, note how the THD performance at lower frequencies becomes less sensitive to the common-mode voltage. As the input frequency approaches dc, the distortion will be dominated by static nonlinearities such as INL and DNL. It is important to note that these dc static nonlinearities are independent of any R_{ON} modulation.

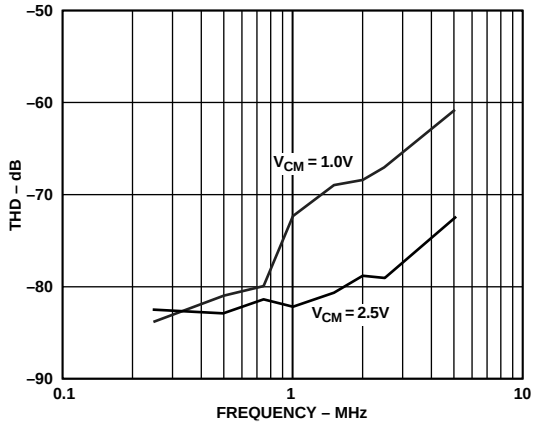


Figure 24. AD9243 THD vs. Frequency for V_{CM} = 2.5 V and 1.0 V (A_{IN} = –0.5 dB, Input Span = 2.0 V p-p)

Due to the high degree of symmetry within the SHA topology, a significant improvement in distortion performance for differential input signals with frequencies up to and beyond Nyquist can be realized. This inherent symmetry provides excellent cancellation of both common-mode distortion and noise. Also, the required input signal voltage span is reduced by a half which further reduces the degree of R_{ON} modulation and its effects on distortion.

The optimum *noise and dc linearity* performance for either differential or single-ended inputs is achieved with the largest input signal voltage span (i.e., 5 V input span) and matched input impedance for VINA and VINB. Note that only a slight degradation in dc linearity performance exists between the 2 V and 5 V input span as specified in the AD9243 "DC SPECIFICATIONS."

Referring to Figure 21, the differential SHA is implemented using a switched-capacitor topology. Hence, its input impedance and its subsequent effects on the input drive source should be understood to maximize the converter's performance. The combination of the pin capacitance, C_{PIN}, parasitic capacitance $C_{PAR,}$ and the sampling capacitance, C_S, is typically less than 16 pF. When the SHA goes into track mode, the input source must charge or discharge the voltage stored on C_S to the new input voltage. This action of charging and discharging C_S which is approximately 4 pF, averaged over a period of time and for a given sampling frequency, F_S, makes the input impedance appear to have a benign resistive component (i.e., 83 kΩ at F_S = 3.0 MSPS). However, if this action is analyzed within a sampling period (i.e., T = <1/F_S), the input impedance is dynamic due to the instantaneous requirement of charging and discharging C_S. A series resistor inserted between the input drive source and the SHA input as shown in Figure 25 provides the effective isolation.

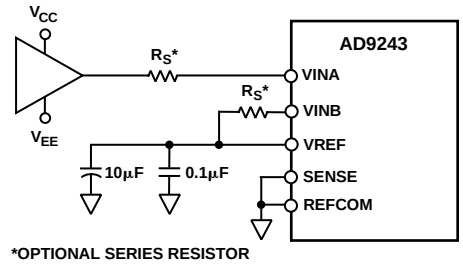


Figure 25. Series Resistor Isolates Switched-Capacitor SHA Input from Op Amp. Matching Resistors Improve SNR Performance

The optimum size of this resistor is dependent on several factors which include the AD9243 sampling rate, the selected op amp, and the particular application. *In most applications, a 30 Ω to 50 Ω resistor is sufficient.* However, some applications may require a larger resistor value to reduce the noise bandwidth or possibly limit the fault current in an overvoltage condition. Other applications may require a larger resistor value as part of an anti-aliasing filter. In any case, since the THD performance is dependent on the series resistance and the above mentioned factors, optimizing this resistor value for a given application is encouraged.

A slight improvement in SNR performance and dc offset performance is achieved by matching the input resistance connected to VINA and VINB. The degree of improvement is dependent on the resistor value and the sampling rate. For series resistor values greater than 100 Ω, the use of a matching resistor is encouraged.

The noise or small-signal bandwidth of the AD9243 is the same as its full-power bandwidth. For noise sensitive applications, the excessive bandwidth may be detrimental and the addition of a series resistor and/or shunt capacitor can help limit the wideband noise at the A/D's input by forming a low-pass filter. Note, however, that the combination of this series resistance with the equivalent input capacitance of the AD9243 should be evaluated for those time-domain applications that are sensitive to the input signal's absolute settling time. In applications where harmonic distortion is not a primary concern, the series resistance may be selected in combination with the SHA's nominal 16 pF of input capacitance to set the filter's 3 dB cutoff frequency.

A better method of reducing the noise bandwidth, while possibly establishing a real pole for an antialiasing filter, is to add some additional shunt capacitance between the input (i.e., VINA and/or VINB) and analog ground. Since this additional shunt capacitance combines with the equivalent input capacitance of the AD9243, a lower series resistance can be selected to establish the filter's cutoff frequency while not degrading the distortion performance of the device. The shunt capacitance also acts like a charge reservoir, sinking or sourcing the additional charge required by the hold capacitor, C_H, further reducing current transients seen at the op amp's output.

The effect of this increased capacitive load on the op amp driving the AD9243 should be evaluated. To optimize performance when noise is the primary consideration, increase the shunt capacitance as much as the transient response of the input signal will allow. Increasing the capacitance too much may adversely affect the op amp's settling time, frequency response, and distortion performance.

Table I. Analog Input Configuration Summary

Input Connection	Coupling	Input Span (V)	Input Range (V) VINA[1]	Input Range (V) VINB[1]	Figure #	Comments
Single-Ended	DC	2	0 to 2	1	32, 33	Best for stepped input response applications, suboptimum THD and noise performance, requires ±5 V op amp.
		2 × VREF	0 to 2 × VREF	VREF	32, 33	Same as above but with improved noise performance due to increase in dynamic range. Headroom/settling time requirements of ±5 op amp should be evaluated.
		5	0 to 5	2.5	32, 33	Optimum noise performance, excellent THD performance. Requires op amp with VCC > +5 V due to insufficient headroom @ 5 V.
		2 × VREF	2.5 – VREF to 2.5 + VREF	2.5	39	Optimum THD performance with VREF = 1, noise performance improves while THD performance degrades as VREF increases to 2.5 V. Single supply operation (i.e., +5 V) for many op amps.
Single-Ended	AC	2 or 2 × VREF	0 to 1 or 0 to 2 × VREF	1 or VREF	34	Suboptimum ac performance due to input common-mode level not biased at optimum midsupply level (i.e., 2.5 V).
		5	0 to 5	2.5	34	Optimum noise performance, excellent THD performance.
		2 × VREF	2.5 – VREF to 2.5 + VREF	2.5	35	Flexible input range, Optimum THD performance with VREF = 1. Noise performance improves while THD performance degrades as VREF increases to 2.5 V.
Differential	AC or DC	2	2 to 3	3 to 2	29–31	Optimum full-scale THD and SFDR performance well beyond the A/Ds Nyquist frequency.
		2 × VREF	2.5 – VREF/2 to 2.5 + VREF/2	2.5 + VREF/2 to 2.5 – VREF/2	29–31	Same as 2 V to 3 V input range with the exception that full-scale THD and SFDR performance can be traded off for better noise performance.
		5	1.75 to 3.25	3.25 to 1.75	29–31	Widest dynamic range (i.e., ENOBs) due to Optimum Noise performance.

NOTE
[1]VINA and VINB can be interchanged if signal inversion is required.

REFERENCE OPERATION

The AD9243 contains an onboard bandgap reference that provides a pin-strappable option to generate either a 1 V or 2.5 V output. With the addition of two external resistors, the user can generate reference voltages other than 1 V and 2.5 V. Another alternative is to use an external reference for designs requiring enhanced accuracy and/or drift performance. See Table II for a summary of the pin-strapping options for the AD9243 reference configurations.

Figure 26 shows a simplified model of the internal voltage reference of the AD9243. A pin-strappable reference amplifier buffers a 1 V fixed reference. The output from the reference amplifier, A1, appears on the VREF pin. The voltage on the VREF pin determines the full-scale input span of the A/D. This input span equals,

Full-Scale Input Span = 2 × VREF

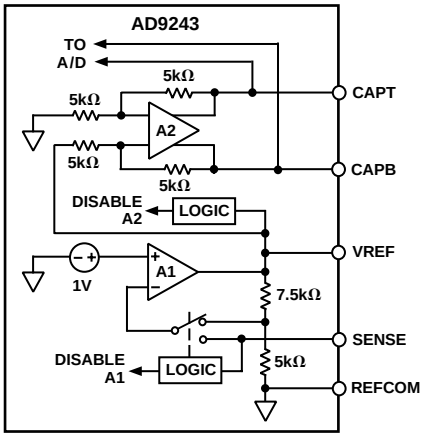


Figure 26. Equivalent Reference Circuit

The voltage appearing at the VREF pin as well as the state of the internal reference amplifier, A1, are determined by the voltage appearing at the SENSE pin. The logic circuitry contains two comparators which monitor the voltage at the SENSE pin. The comparator with the lowest set point (approximately 0.3 V) controls the position of the switch within the feedback path of A1. If the SENSE pin is tied to REFCOM, the switch is connected to the internal resistor network thus providing a VREF of 2.5 V. If the SENSE pin is tied to the VREF pin via a short or resistor, the switch is connected to the SENSE pin. A short will provide a VREF of 1.0 V while an external resistor network will provide an alternative VREF between 1.0 V and 2.5 V. The other comparator controls internal circuitry which will disable the reference amplifier if the SENSE pin is tied AVDD. Disabling the reference amplifier allows the VREF pin to be driven by an external voltage reference.

The actual reference voltages used by the internal circuitry of the AD9243 appear on the CAPT and CAPB pins. For proper operation when using the internal or an external reference, it is necessary to add a capacitor network to decouple these pins. Figure 27 shows the recommended decoupling network. This capacitive network performs the following three functions: (1) along with the reference amplifier, A2, it provides a low source impedance over a large frequency range to drive the A/D internal circuitry, (2) it provides the necessary compensation for A2, and (3) it bandlimits the noise contribution from the reference. The turn-on time of the reference voltage appearing between CAPT and CAPB is approximately 15 ms and should be evaluated in any power-down mode of operation.

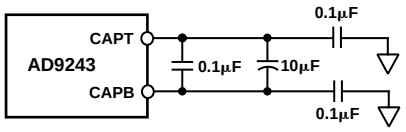


Figure 27. Recommended CAPT/CAPB Decoupling Network

The A/D's input span may be varied dynamically by changing the differential reference voltage appearing across CAPT and CAPB symmetrically around 2.5 V (i.e., midsupply). To change the reference at speeds beyond the capabilities of A2, it will be necessary to drive CAPT and CAPB with two high speed, low noise amplifiers. In this case, both internal amplifiers (i.e., A1 and A2) must be disabled by connecting SENSE to AVDD and VREF to REFCOM and the capacitive decoupling network removed. The external voltages applied to CAPT and CAPB must be 2.5 V + Input Span/4 and 2.5 V – Input Span/4 respectively in which the input span can be varied between 2 V and 5 V. Note that those samples within the pipeline A/D during any reference transition will be corrupted and should be discarded.

Table II. Reference Configuration Summary

Reference Operating Mode	Input Span (VINA–VINB) (V p-p)	Required VREF (V)	Connect	To
INTERNAL	2	1	SENSE	VREF
INTERNAL	5	2.5	SENSE	REFCOM
INTERNAL	2 ≤ SPAN ≤ 5 AND SPAN = 2 × VREF	1 ≤ VREF ≤ 2.5 AND VREF = (1 + R1/R2)	R1 R2	VREF AND SENSE SENSE AND REFCOM
EXTERNAL (NONDYNAMIC)	2 ≤ SPAN ≤ 5	1 ≤ VREF ≤ 2.5	SENSE VREF	AVDD EXT. REF.
EXTERNAL (DYNAMIC)	2 ≤ SPAN ≤ 5	CAPT and CAPB Externally Driven	SENSE VREF EXT. REF. EXT. REF.	AVDD REFCOM CAPT CAPB

DRIVING THE ANALOG INPUTS

INTRODUCTION

The AD9243 has a highly flexible input structure allowing it to interface with single-ended or differential input interface circuitry. The applications shown in sections "Driving the Analog Inputs" and "Reference Configurations" along with the information presented in "Input and Reference Overview" of this data sheet, give examples of both single-ended and differential operation. Refer to Tables I and II for a list of the different possible input and reference configurations and their associated figures in the data sheet.

The optimum mode of operation, analog input range, and associated interface circuitry will be determined by the particular applications performance requirements as well as power supply options. For example, a dc coupled single-ended input may be appropriate for many data acquisition and imaging applications. Also, many communication applications which require a dc coupled input for proper demodulation can take advantage of the excellent single-ended distortion performance of the AD9243. The input span should be configured such that the system's performance objectives and the headroom requirements of the driving op amp are simultaneously met.

Alternatively, the differential mode of operation provides the best THD and SFDR performance over a wide frequency range. A transformer coupled differential input should be considered for the most demanding spectral-based applications which allow ac coupling (e.g., Direct IF to Digital Conversion). The dc-coupled differential mode of operation also provides an enhancement in distortion and noise performance at higher input spans. Furthermore, it allows the AD9243 to be configured for a 5 V span using op amps specified for +5 V or ±5 V operation.

Single-ended operation requires that VINA be ac or dc coupled to the input signal source while VINB of the AD9243 be biased to the appropriate voltage corresponding to a midscale code transition. Note that signal inversion may be easily accomplished by transposing VINA and VINB.

Differential operation requires that VINA and VINB be simultaneously driven with two equal signals that are in and out of phase versions of the input signal. Differential operation of the AD9243 offers the following benefits: (1) Signal swings are smaller and therefore linearity requirements placed on the input signal source may be easier to achieve, (2) Signal swings are smaller and therefore may allow the use of op amps which may otherwise have been constrained by headroom limitations, (3) Differential operation minimizes even-order harmonic products, and (4) Differential operation offers noise immunity based on the device's common-mode rejection as shown in Figure 16.

As is typical of most CMOS devices, exceeding the supply limits will turn on internal parasitic diodes resulting in transient currents within the device. Figure 28 shows a simple means of clamping a dc coupled input with the addition of two series resistors and two diodes. Note that a larger series resistor could be used to limit the fault current through D1 and D2 but should be evaluated since it can cause a degradation in overall performance.

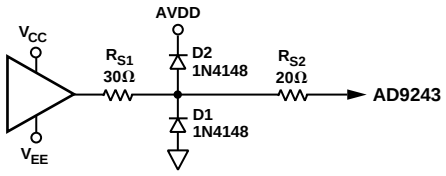


Figure 28. Simple Clamping Circuit

DIFFERENTIAL MODE OF OPERATION

Since not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended-to-differential conversion. A single-ended-to-differential conversion can be realized with an RF transformer or a dual op amp differential driver. The optimum method depends on whether the application requires the input signal to be ac or dc coupled to AD9243.

AC Coupling via an RF Transformer

In applications that do not need to be dc coupled, an RF transformer with a center tap is the best method to generate differential inputs for the AD9243. It provides all the benefits of operating the A/D in the differential mode without contributing additional noise or distortion. An RF transformer has the added benefit of providing electrical isolation between the signal source and the A/D.

Figure 29 shows the schematic of the suggested transformer circuit. The circuit uses a Mini-Circuits RF transformer, model #T4-6T, which has an impedance ratio of four (turns ratio of 2). The schematic assumes that the signal source has a 50 Ω source impedance. The 1:4 impedance ratio requires the 200 Ω secondary termination for optimum power transfer and VSWR. The centertap of the transformer provides a convenient means of level shifting the input signal to a desired common-mode voltage. Optimum performance can be realized when the centertap is tied to CML of the AD9243 which is the common-mode bias level of the internal SHA.

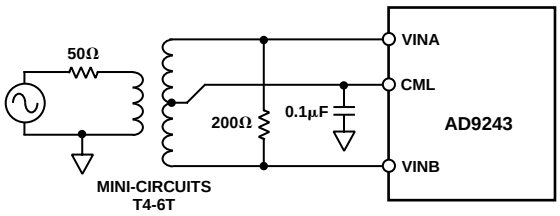


Figure 29. Transformer Coupled Input

Transformers with other turns ratios may also be selected to optimize the performance of a given application. For example, a given input signal source or amplifier may realize an improvement in distortion performance at reduced output power levels and signal swings. Hence, selecting a transformer with a higher impedance ratio (i.e., Mini-Circuits T16-6T with a 1:16 impedance ratio) effectively "steps up" the signal level, further reducing the driving requirements of the signal source.

DC Coupling with Op Amps

Applications that require dc coupling can also benefit by driving the AD9243 differentially. Since the signal swing requirements of each input is reduced by a factor of two in the differential mode, the AD9243 can be configured for a 5 V input span in a +5 V or ±5 V system. This allows various high performance op amps specified for +5 V and ±5 V operation to be configured in various differential driver topologies. The optimum op amp driver topology depends on whether the common-mode voltage of the single-ended-input signal requires level-shifting.

Figure 30 shows a cross-coupled differential driver circuit best suited for systems in which the common-mode signal of the input is already biased to approximately midsupply (i.e., 2.5 V). The common-mode voltage of the differential output is set by the voltage applied to the "+" input of A2. The closed loop gain of this symmetrical driver can be easily set by R_{IN} and R_F. For more insight into the operation of this cross-coupled driver, please refer to the AD8042 data sheet.

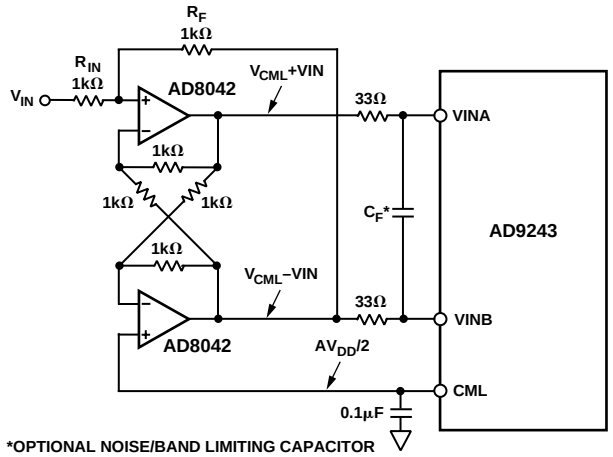


Figure 30. Cross-Coupled Differential Driver

The driver circuit shown in Figure 31 is best suited for systems in which the bipolar input signal is referenced to AGND and requires proper level shifting. This driver circuit provides the ability to level-shift the input signal to within the common-mode range of the AD9243. The two op amps are configured as matched difference amplifiers with the input signal applied to opposing inputs to provide the differential output. The common-mode offset voltage is applied to the noninverting resistor network which provides the proper level shifting. The circuit also employs optional diodes and pull-up resistors which may help improve the op amps' distortion performance by reducing their headroom requirements. Rail-to-rail output amplifiers like the AD8042 have sufficient headroom and thus do not require these optional components.

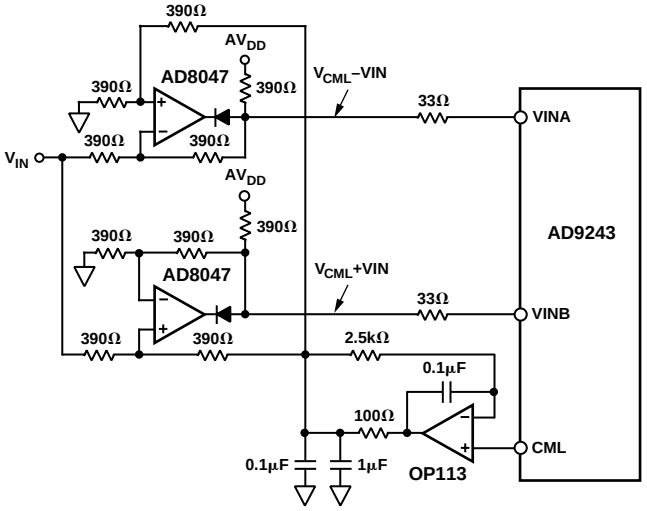


Figure 31. Differential Driver with Level-Shifting

SINGLE-ENDED MODE OF OPERATION

The AD9243 can be configured for single-ended operation using dc or ac coupling. In either case, the input of the A/D must be driven from an operational amplifier that will not degrade the A/D's performance. Because the A/D operates from a single supply, it will be necessary to level shift ground-based bipolar signals to comply with its input requirements. Both dc and ac coupling provide this necessary function, but each method results in different interface issues which may influence the system design and performance.

DC COUPLING AND INTERFACE ISSUES

Many applications require the analog input signal to be dc coupled to the AD9243. An operational amplifier can be configured to rescale and level shift the input signal so that it is compatible with the selected input range of the A/D. The input range to the A/D should be selected on the basis of system performance objectives as well as the analog power supply availability since this will place certain constraints on the op amp selection.

Many of the new high performance op amps are specified for only ±5 V operation and have limited input/output swing capabilities. Hence, the selected input range of the AD9243 should be sensitive to the headroom requirements of the particular op amp to prevent clipping of the signal. Also, since the output of a dual supply amplifier can swing below –0.3 V, clamping its output should be considered in some applications.

In some applications, it may be advantageous to use an op amp specified for single supply +5 V operation since it will inherently limit its output swing to within the power supply rails. Rail-to-rail output amplifiers such as the AD8041 allow the AD9243 to be configured with larger input spans which improves the noise performance.

If the application requires the largest single-ended input range (i.e., 0 V to 5 V) of the AD9243, the op amp will require larger supplies to drive it. Various high speed amplifiers in the "Op Amp Selection Guide" of this data sheet can be selected to accommodate a wide range of supply options. Once again, clamping the output of the amplifier should be considered for these applications. Alternatively, a single-ended to differential op amp driver circuit using the AD8042 could be used to achieve the 5 V input span while operating from a single +5 V supply.

Two dc coupled op amp circuits using a noninverting and inverting topology are discussed below. Although not shown, the noninverting and inverting topologies can be easily configured as part of an antialiasing filter by using a Sallen-Key or Multiple-Feedback topology, respectively. An additional R-C network can be inserted between the op amp's output and the AD9243 input to provide a real pole.

Simple Op Amp Buffer

In the simplest case, the input signal to the AD9243 will already be biased at levels in accordance with the selected input range. It is simply necessary to provide an adequately low source impedance for the VINA and VINB analog input pins of the A/D. Figure 32 shows the recommended configuration for a single-ended drive using an op amp. In this case, the op amp is shown in a noninverting unity gain configuration driving the VINA pin. The internal reference drives the VINB pin. Note that the addition of a small series resistor of 30 Ω to 50 Ω connected to VINA and VINB will be beneficial in nearly all cases. Refer to section "Analog Input Operation" for a discussion on resistor selection. Figure 32 shows the proper connection for a 0 V to 5 V input range. Alternative single ended input ranges of 0 V to 2 × VREF can also be realized with the proper configuration of VREF (refer to the section "Using the Internal Reference").

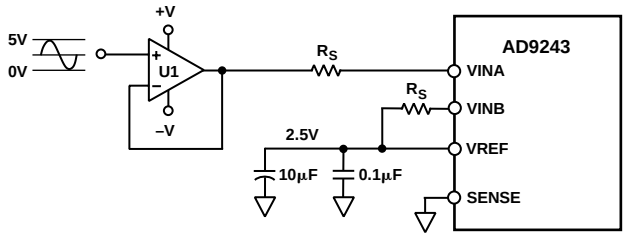


Figure 32. Single-Ended AD9243 Op Amp Drive Circuit

Op Amp with DC Level Shifting

Figure 33 shows a dc-coupled level shifting circuit employing an op amp, A1, to sum the input signal with the desired dc offset. Configuring the op amp in the inverting mode with the given resistor values results in an ac signal gain of –1. If the signal inversion is undesirable, interchange the VINA and VINB connections to reestablish the original signal polarity. The dc voltage at VREF sets the common-mode voltage of the AD9243. For example, when VREF = 2.5 V, the output level from the op amp will also be centered around 2.5 V. The use of ratio matched, thin-film resistor networks will minimize gain and offset errors. Also, an optional pull-up resistor, R_P, may be used to reduce the output load on VREF to ±1 mA.

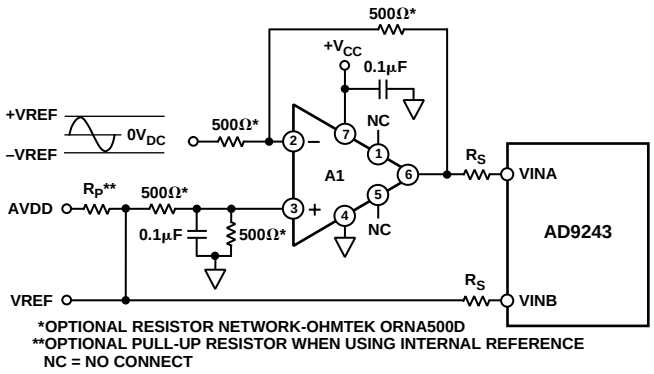


Figure 33. Single-Ended Input With DC-Coupled Level Shift

AC COUPLING AND INTERFACE ISSUES

For applications where ac coupling is appropriate, the op amp's output can be easily level shifted to the common-mode voltage, V_{CM}, of the AD9243 via a coupling capacitor. This has the advantage of allowing the op amps common-mode level to be symmetrically biased to its midsupply level (i.e., $(V_{CC} + V_{EE})/2$). Op amps which operate symmetrically with respect to their power supplies typically provide the best ac performance as well as greatest input/output span. Hence, various high speed/performance amplifiers which are restricted to +5 V/–5 V operation and/or specified for +5 V single-supply operation can be easily configured for the 5 V or 2 V input span of the AD9243, respectively. The best ac distortion performance is achieved when the A/D is configured for a 2 V input span and common-mode voltage of 2.5 V. Note that differential transformer coupling, which is another form of ac coupling, should be considered for optimum ac performance.

Simple AC Interface

Figure 34 shows a typical example of an ac-coupled, single-ended configuration. The bias voltage shifts the bipolar, ground-referenced input signal to approximately VREF. The value for C1 and C2 will depend on the size of the resistor, R. The capacitors, C1 and C2, are typically a 0.1 µF ceramic and 10 µF tantalum capacitor in parallel to achieve a low cutoff frequency while maintaining a low impedance over a wide frequency range. The combination of the capacitor and the resistor form a high-pass filter with a high-pass –3 dB frequency determined by the equation,

$$f_{-3\,dB} = 1/(2 \times \pi \times R \times (C1 + C2))$$

The low impedance VREF voltage source biases both the VINB input and provides the bias voltage for the VINA input. Figure 34 shows the VREF configured for 2.5 V. Thus the input range

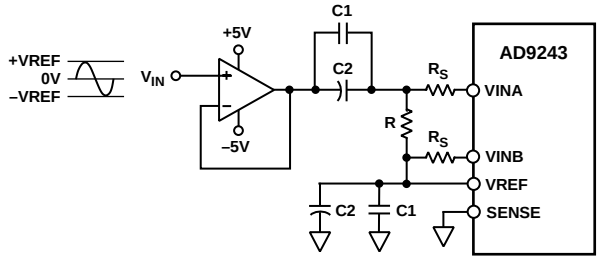


Figure 34. AC-Coupled Input

of the A/D is 0 V to 5 V. Other input ranges could be selected by changing VREF but the A/D's distortion performance will degrade slightly as the input common-mode voltage deviates from its optimum level of 2.5 V.

Alternative AC Interface

Figure 35 shows a flexible ac coupled circuit which can be configured for different input spans. Since the common-mode voltage of VINA and VINB are biased to midsupply independent of VREF, VREF can be pin-strapped or reconfigured to achieve input spans between 2 V and 5 V p-p. The AD9243's CMRR along with the symmetrical coupling R-C networks will reject both power supply variations and noise. The resistors, R, establish the common-mode voltage. They may have a high value (e.g., 5 kΩ) to minimize power consumption and establish a low cutoff frequency. The capacitors, C1 and C2, are typically a 0.1 μF ceramic and 10 μF tantalum capacitor in parallel to achieve a low cutoff frequency while maintaining a low impedance over a wide frequency range. R_S isolates the buffer amplifier from the A/D input. The optimum performance is achieved when VINA and VINB are driven via symmetrical networks. The high pass $f_{-3\ dB}$ point can be approximated by the equation,

$$f_{-3\ dB} = 1/(2 \times \pi \times R/2 \times (C1 + C2))$$

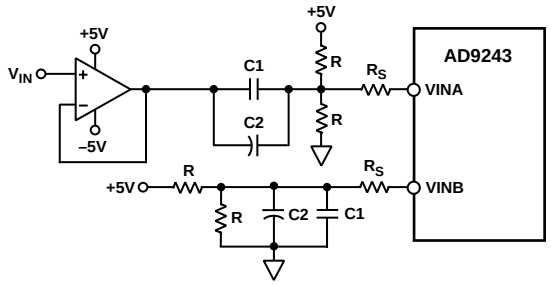


Figure 35. AC-Coupled Input-Flexible Input Span, V_{CM} = 2.5 V

OP AMP SELECTION GUIDE

Op amp selection for the AD9243 is highly dependent on a particular application. In general, the performance requirements of any given application can be characterized by either time domain or frequency domain parameters. In either case, one should carefully select an op amp which preserves the performance of the A/D. This task becomes challenging when one considers the AD9243's high performance capabilities coupled with other external system level requirements such as power consumption and cost.

The ability to select the optimal op amp may be further complicated by either limited power supply availability and/or limited *acceptable* supplies for a desired op amp. Newer, high performance op amps typically have input and output range limitations in accordance with their lower supply voltages. As a result, some op amps will be more appropriate in systems where ac-coupling is allowable. When dc-coupling is required, op amps without headroom constraints such as rail-to-rail op amps or ones where larger supplies can be used should be considered. The following section describes some op amps currently available from Analog Devices. The system designer is *always* encouraged to contact the factory or local sales office to be updated on Analog Devices' latest amplifier product offerings. Highlights of the areas where the op amps excel and where they may limit the performance of the AD9243 are also included.

AD812: Dual, 145 MHz Unity GBW, Single-Supply Current Feedback, +5 V to ±15 V Supplies
Best Applications: Differential and/or Low Impedance Input Drivers
Limits: THD above 1 MHz

AD8011: $f_{-3\ dB}$ = 300 MHz, +5 V or ±5 V Supplies, Current Feedback
Best Applications: Single-Supply, AC/DC-Coupled, Good AC Specs, Low Noise, Low Power (5 mW)
Limits: THD above 5 MHz, Usable Input/Output Range

AD8013: Triple, $f_{-3\ dB}$ = 230 MHz, +5 V or ±5 V supplies, Current Feedback, Disable Function
Best Applications: 3:1 Multiplexer, Good AC Specs
Limits: THD above 5 MHz, Input Range

AD9631: 220 MHz Unity GBW, 16 ns Settling to 0.01%, ±5 V Supplies
Best Applications: Best AC Specs, Low Noise, AC-Coupled
Limits: Usable Input/Output Range, Power Consumption

AD8047: 130 MHz Unity GBW, 30 ns Settling to 0.01%, ±5 V Supplies
Best Applications: Good AC Specs, Low Noise, AC-Coupled
Limits: THD > 5 MHz, Usable Input Range

AD8041: Rail-to-Rail, 160 MHz Unity GBW, 55 ns Settling to 0.01%, +5 V Supply, 26 mW
Best Applications: Low Power, Single-Supply Systems, DC-Coupled, Large Input Range
Limits: Noise with 2 V Input Range

AD8042: Dual AD8041
Best Applications: Differential and/or Low Impedance Input Drivers
Limits: Noise with 2 V Input Range

REFERENCE CONFIGURATIONS

The figures associated with this section on internal and external reference operation do not show recommended matching series resistors for VINA and VINB for the purpose of simplicity. Please refer to section "Driving the Analog Inputs, Introduction" for a discussion of this topic. Also, the figures do not show the decoupling network associated with the CAPT and CAPB pins. Please refer to the section "Reference Operation" for a discussion of the internal reference circuitry and the recommended decoupling network shown in Figure 27.

USING THE INTERNAL REFERENCE

Single-Ended Input with 0 to 2 × VREF Range

Figure 36 shows how to connect the AD9243 for a 0 V to 2 V or 0 V to 5 V input range via pin strapping the SENSE pin. An intermediate input range of 0 to 2 × VREF can be established using the resistor programmable configuration in Figure 38 and connecting VREF to VINB.

In either case, both the common-mode voltage and input span are directly dependent on the value of VREF. More specifically, the common-mode voltage is equal to VREF while the input span is equal to 2 × VREF. Thus, the valid input range extends from 0 to 2 × VREF. When VINA is ≤ 0 V, the digital output will be 0000 Hex; when VINA is ≥ 2 × VREF, the digital output will be 3FFF Hex.

Shorting the VREF pin directly to the SENSE pin places the internal reference amplifier in unity-gain mode and the resultant VREF output is 1 V. Therefore, the valid input range is 0 V to 2 V. However, shorting the SENSE pin directly to the REFCOM pin configures the internal reference amplifier for a gain of 2.5 and the resultant VREF output is 2.5 V. Thus, the valid input range becomes 0 V to 5 V. The VREF pin should be bypassed to the REFCOM pin with a 10 µF tantalum capacitor in parallel with a low-inductance 0.1 µF ceramic capacitor.

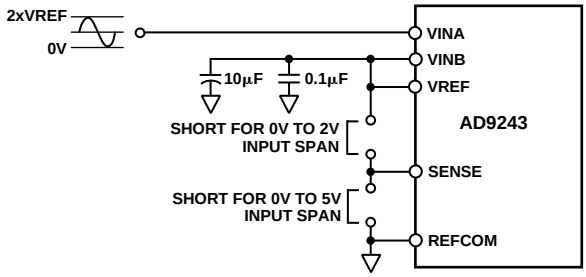


Figure 36. Internal Reference (2 V p-p Input Span, V_{CM} = 1 V, or 5 V p-p Input Span, V_{CM} = 2.5 V)

Single-Ended or Differential Input, V_{CM} = 2.5 V

Figure 37 shows the single-ended configuration that gives the best SINAD performance. To optimize dynamic specifications, center the common-mode voltage of the analog input at approximately by 2.5 V by connecting VINB to VREF, a low-impedance 2.5 V source. As described above, shorting the SENSE pin directly to the REFCOM pin results in a 2.5 V reference voltage and a 5 V p-p input span. The valid range for input signals is 0 V to 5 V. The VREF pin should be bypassed to the REFCOM pin with a 10 µF tantalum capacitor in parallel with a low inductance 0.1 µF ceramic capacitor.

This reference configuration could also be used for a differential input in which VINA and VINB are driven via a transformer as shown in Figure 29. In this case, the common-mode voltage, V_{CM}, is set at midsupply by connecting the transformers center tap to CML of the AD9243. VREF can be configured for 1 V or 2.5 V by connecting SENSE to either VREF or REFCOM respectively. Note that the valid input range for each of the differential inputs is one half of the single-ended input and thus becomes V_{CM} – VREF/2 to V_{CM} + VREF/2.

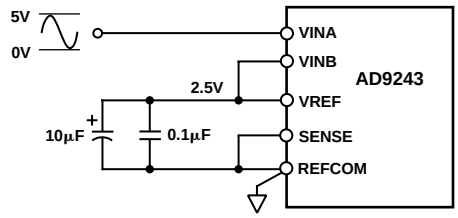


Figure 37. Internal Reference—5 V p-p Input Span, V_{CM} = 2.5 V

Resistor Programmable Reference

Figure 38 shows an example of how to generate a reference voltage other than 1 V or 2.5 V with the addition of two external resistors and a bypass capacitor. Use the equation,

$$VREF = 1\ V \times (1 + R1/R2),$$

to determine appropriate values for R1 and R2. These resistors should be in the 2 kΩ to 100 kΩ range. For the example shown, R1 equals 2.5 kΩ and R2 equals 5 kΩ. From the equation above, the resultant reference voltage on the VREF pin is 1.5 V. This sets the input span to be 3 V p-p. To assure stability, place a 0.1 µF ceramic capacitor in parallel with R1.

The common-mode voltage can be set to VREF by connecting VINB to VREF to provide an input span of 0 to 2 × VREF. Alternatively, the common-mode voltage can be set to 2.5 V by connecting VINB to a low impedance 2.5 V source. For the example shown, the valid input single range for VINA is 1 V to 4 V since VINB is set to an external, low impedance 2.5 V source. The VREF pin should be bypassed to the REFCOM pin with a 10 µF tantalum capacitor in parallel with a low inductance 0.1 µF ceramic capacitor.

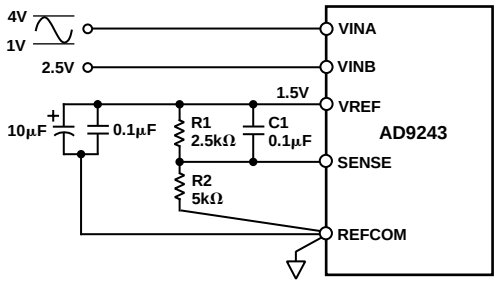


Figure 38. Resistor Programmable Reference (3 V p-p Input Span, V_{CM} = 2.5 V)

USING AN EXTERNAL REFERENCE

Using an external reference may enhance the dc performance of the AD9243 by improving drift and accuracy. Figures 39 through 41 show examples of how to use an external reference with the A/D. Table III is a list of suitable voltage references from Analog Devices. To use an external reference, the user must disable the internal reference amplifier and drive the VREF pin. Connecting the SENSE pin to AVDD disables the internal reference amplifier.

Table III. Suitable Voltage References

	Output Voltage	Drift (ppm/°C)	Initial Accuracy % (max)	Operating Current (µA)
Internal	1.00	26	1.4	N/A
AD589	1.235	10–100	1.2–2.8	50
AD1580	1.225	50–100	0.08–0.8	50
REF191	2.048	5–25	0.1–0.5	45
Internal	2.50	26	1.4	N/A
REF192	2.50	5–25	0.08–0.4	45
REF43	2.50	10–25	0.06–0.1	600
AD780	2.50	3–7	0.04–0.2	1000

The AD9243 contains an internal reference buffer, A2 (see Figure 26), that simplifies the drive requirements of an external reference. The external reference must be able to drive a ≈5 kΩ (±20%) load. Note that the bandwidth of the reference buffer is deliberately left small to minimize the reference noise contribution. As a result, it is not possible to change the reference voltage rapidly in this mode without the removal of the CAPT/CAPB Decoupling Network, and driving these pins directly.

Variable Input Span with V_{CM} = 2.5 V

Figure 39 shows an example of the AD9243 configured for an input span of 2 × VREF centered at 2.5 V. An external 2.5 V reference drives the VINB pin thus setting the common-mode voltage at 2.5 V. The input span can be independently set by a voltage divider consisting of R1 and R2 which generates the VREF signal. A1 buffers this resistor network and drives VREF. Choose this op amp based on accuracy requirements. It is essential that a minimum of a 10 µF capacitor in parallel with a 0.1 µF low inductance ceramic capacitor decouple the reference output to ground.

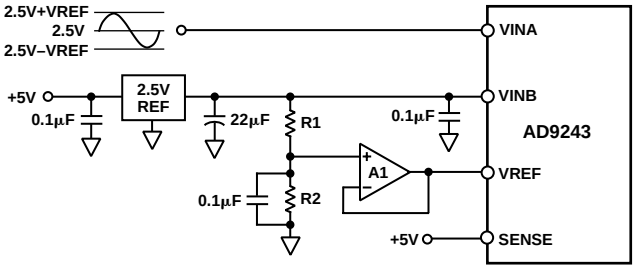


Figure 39. External Reference, V_{CM} = 2.5 V (2.5 V on VINB, Resistor Divider to Make VREF)

Single-Ended Input with 0 to 2 × VREF Range

Figure 40 shows an example of an external reference driving both VINB and VREF. In this case, both the common mode voltage and input span are directly dependent on the value of VREF. More specifically, the common-mode voltage is equal to VREF while the input span is equal to 2 × VREF. Thus, the valid input range extends from 0 to 2 × VREF. For example, if the REF191, a 2.048 external reference was selected, the valid input range extends from 0 V to 4.096 V. In this case, 1 LSB of the AD9243 corresponds to 0.250 mV. It is essential that a minimum of a 10 µF capacitor in parallel with a 0.1 µF low inductance ceramic capacitor decouple the reference output to ground.

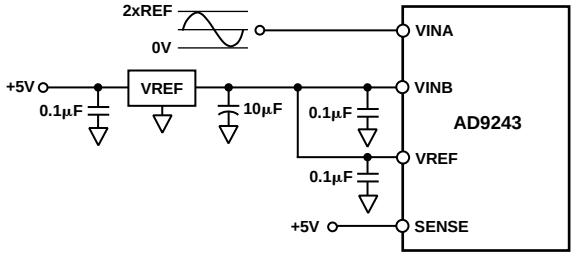


Figure 40. Input Range = 0 V to 2 × VREF

Low Cost/Power Reference

The external reference circuit shown in Figure 41 uses a low cost 1.225 V external reference (e.g., AD580 or AD1580) along with an op amp and transistor. The 2N2222 transistor acts in conjunction with 1/2 of an OP282 to provide a very low impedance drive for VINB. The selected op amp need not be a high speed op amp and may be selected based on cost, power, and accuracy.

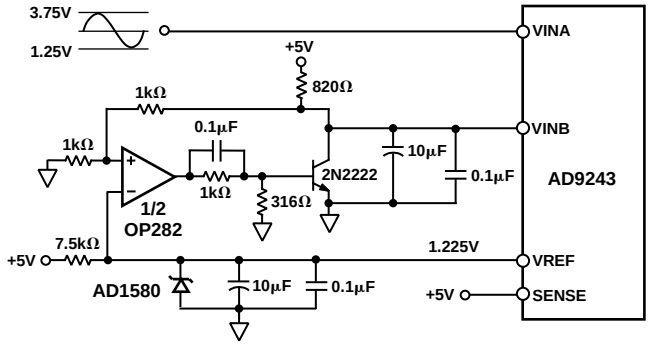


Figure 41. External Reference Using the AD1580 and Low Impedance Buffer

DIGITAL INPUTS AND OUTPUTS

Digital Outputs

The AD9243 output data is presented in positive true straight binary for all input ranges. Table IV indicates the output data formats for various input ranges regardless of the selected input range. A twos complement output data format can be created by inverting the MSB.

Table IV. Output Data Format

Input (V)	Condition (V)	Digital Output	OTR
VINA –VINB	< – VREF	00 0000 0000 0000	1
VINA –VINB	= – VREF	00 0000 0000 0000	0
VINA –VINB	= 0	10 0000 0000 0000	0
VINA –VINB	= + VREF – 1 LSB	11 1111 1111 1111	0
VINA –VINB	≥ + VREF	11 1111 1111 1111	1

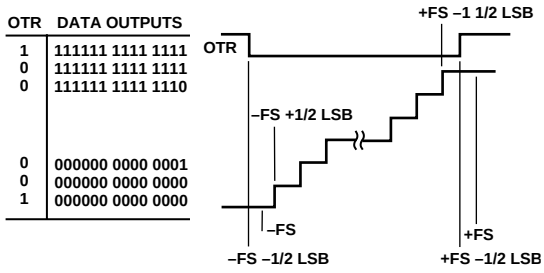


Figure 42. Output Data Format

Out Of Range (OTR)

An out-of-range condition exists when the analog input voltage is beyond the input range of the converter. OTR is a digital output that is updated along with the data output corresponding to the particular sampled analog input voltage. Hence, OTR has the same pipeline delay (latency) as the digital data. It is LOW when the analog input voltage is within the analog input range. It is HIGH when the analog input voltage exceeds the input range as shown in Figure 42. OTR will remain HIGH

until the analog input returns within the input range and another conversion is completed. By logical ANDing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table V is a truth table for the over/underrange circuit in Figure 43 which uses NAND gates. Systems requiring programmable gain conditioning of the AD9243 input signal can immediately detect an out-of-range condition, thus eliminating gain selection iterations. Also, OTR can be used for digital offset and gain calibration.

Table V. Out-of-Range Truth Table

OTR	MSB	Analog Input Is
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

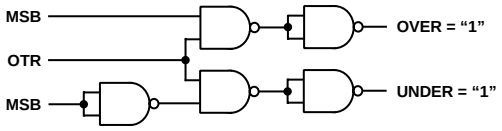


Figure 43. Overrange or Underrange Logic

Digital Output Driver Considerations (DRVDD)

The AD9243 output drivers can be configured to interface with +5 V or 3.3 V logic families by setting DRVDD to +5 V or 3.3 V respectively. The AD9243 output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause glitches on the supplies and may affect SINAD performance. Applications requiring the AD9243 to drive large capacitive loads or large fanout may require additional decoupling capacitors on DRVDD. In extreme cases, external buffers or latches may be required.

Clock Input and Considerations

The AD9243 internal timing uses the two edges of the clock input to generate a variety of internal timing signals. The clock input must meet or exceed the minimum specified pulsewidth high and low (t_{CH} and t_{CL}) specifications for the given A/D as defined in the Switching Specifications at the beginning of the data sheet to meet the rated performance specifications. For example, the clock input to the AD9243 operating at 3 MSPS may have a duty cycle between 45% to 55% to meet this timing requirement since the minimum specified t_{CH} and t_{CL} is 150 ns.

For clock rates below 3 MSPS, the duty cycle may deviate from this range to the extent that both t_{CH} and t_{CL} are satisfied.

All high speed high resolution A/Ds are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{IN}) due to only aperture jitter (t_A) can be calculated with the following equation:

$$SNR = 20 \log_{10} [1/(2 \pi f_{IN} t_A)]$$

In the equation, the rms aperture jitter, t_A, represents the root-sum square of all the jitter sources which include the clock input, analog input signal, and A/D aperture jitter specification. For example, if a 1.5 MHz full-scale sine wave is sampled by an A/D with a total rms jitter of 15 ps, the SNR performance of the A/D will be limited to 77 dB. Undersampling applications are particularly sensitive to jitter.

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9243. As such, supplies for clock drivers should be separated from the A/D output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other method), it should be retimed by the original clock at the last step.

Most of the power dissipated by the AD9243 is from the analog power supply. However, lower clock speeds will reduce digital current slightly. Figure 44 shows the relationship between power and clock rate.

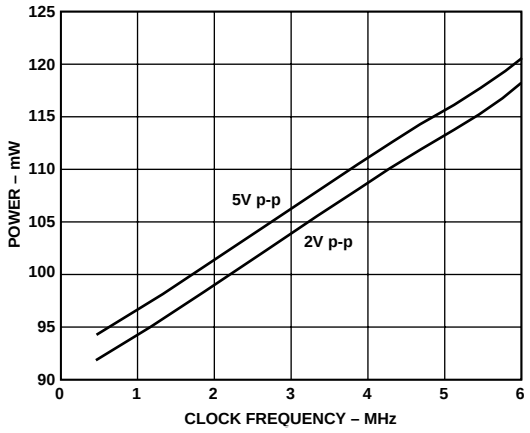


Figure 44. AD9243 Power Consumption vs. Clock Frequency

GROUNDING AND DECOUPLING

Analog and Digital Grounding

Proper grounding is essential in any high speed, high resolution system. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power schemes. The use of ground and power planes offers distinct advantages:

1. The minimization of the loop area encompassed by a signal and its return path.
2. The minimization of the impedance associated with ground and power paths.
3. The inherent distributed capacitor formed by the power plane, PCB insulation, and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. While the AD9243 features separate analog and digital ground pins, it should be treated as an analog component. *The AVSS, DVSS and DRVSS pins must be joined together directly under the AD9243.* A solid ground plane under the A/D is acceptable if the power and ground return currents are managed carefully. Alternatively, the ground plane under the A/D may contain serrations to *steer* currents in predictable directions where cross-coupling between analog and digital would otherwise be unavoidable. The AD9243/EB ground layout, shown in Figure 54, depicts the serrated type of arrangement. The analog and digital grounds are connected by a jumper below the A/D.

Analog and Digital Supply Decoupling

The AD9243 features separate analog and digital supply and ground pins, helping to minimize digital corruption of sensitive analog signals.

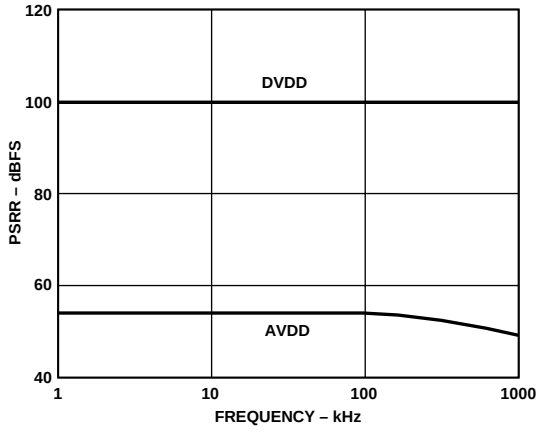


Figure 45. AD9243 PSSR vs. Frequency

Figure 45 shows the power supply rejection ratio vs. frequency for a 200 mV p-p ripple applied to both AVDD and DVDD.

In general, AVDD, the analog supply, should be decoupled to AVSS, the analog common, as close to the chip as physically possible. Figure 46 shows the recommended decoupling for the analog supplies; 0.1 µF ceramic chip capacitors should provide adequately low impedance over a wide frequency range. Note that the AVDD and AVSS pins are co-located on the AD9243 to simplify the layout of the decoupling capacitors and provide the shortest possible PCB trace lengths. The AD9243/EB power plane layout, shown in Figure 55 depicts a typical arrangement using a multilayer PCB.

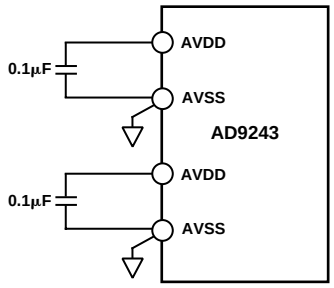


Figure 46. Analog Supply Decoupling

The CML is an internal analog bias point used internally by the AD9243. This pin must be decoupled with at least a 0.1 µF capacitor as shown in Figure 47. The dc level of CML is approximately AVDD/2. This voltage should be buffered if it is to be used for any external biasing.

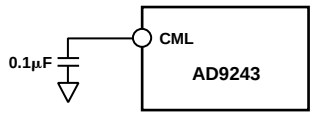


Figure 47. CML Decoupling

The digital activity on the AD9243 chip falls into two general categories: correction logic, and output drivers. The internal correction logic draws relatively small surges of current, mainly during the clock transitions. The output drivers draw large current impulses while the output bits are changing. The size and duration of these currents are a function of the load on the output bits: large capacitive loads are to be avoided. Note that the internal correction logic of the AD9243 is referenced DVDD while the output drivers are referenced to DRVDD.

The decoupling shown in Figure 48, a 0.1 µF ceramic chip capacitor, is appropriate for a reasonable capacitive load on the digital outputs (typically 20 pF on each pin). Applications involving greater digital loads should consider increasing the digital decoupling proportionally, and/or using external buffers/latches.

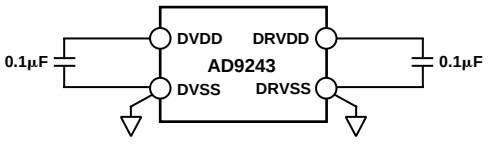


Figure 48. Digital Supply Decoupling

A complete decoupling scheme will also include large tantalum or electrolytic capacitors on the PCB to reduce low-frequency ripple to negligible levels. Refer to the AD9243/EB schematic and layouts in Figures 51–55 for more information regarding the placement of decoupling capacitors.

APPLICATIONS

DIRECT IF DOWN CONVERSION USING THE AD9243

As previously noted, the AD9243's performance in the differential mode of operation extends well beyond its baseband region and into several Nyquist zone regions. Hence, the AD9243 may be well suited as a mix down converter in both narrow and wideband applications. Various IF frequencies exist over the frequency range in which the AD9243 maintains excellent dynamic performance (e.g., refer to Figure 5 and 6). The IF signal will be aliased to the ADC's baseband region due to the sampling process in a similar manner that a mixer will down convert an IF signal. For signals in various Nyquist zones, the following equation may be used to determine the final frequency after aliasing.

$$f_{1\ NYQUIST} = f_{SIGNAL}$$
$$f_{2\ NYQUIST} = f_{SAMPLE} - f_{SIGNAL}$$
$$f_{3\ NYQUIST} = abs\ (f_{SAMPLE} - f_{SIGNAL})$$
$$f_{4\ NYQUIST} = 2 \times f_{SAMPLE} - f_{SIGNAL}$$
$$f_{5\ NYQUIST} = abs\ (2 \times f_{SAMPLE} - f_{SIGNAL})$$

There are several potential benefits in using the ADC to alias (i.e., mix) down a narrowband or wideband IF signal. First and foremost is the elimination of a complete mixer stage with its associated amplifiers and filters, reducing cost and power dissipation. Second is the ability to apply various DSP techniques to perform such functions as filtering, channel selection, quadrature demodulation, data reduction, and detection.

One common example is the digitization of a 10.7 MHz IF using a low jitter 2.5 MHz sample clock. Using the equation above for the fifth Nyquist zone, the resultant frequency after sampling is 700 kHz. Figure 49 shows the typical performance of the AD9243 operating under these conditions. Figure 50 demonstrates how the AD9243 is still able to maintain a high degree of linearity and SFDR over a wide amplitude.

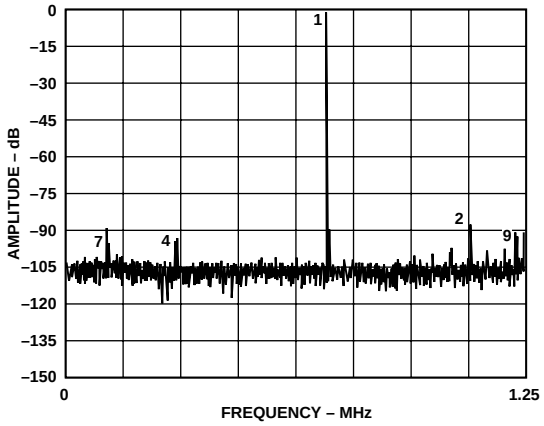


Figure 49. IF Sampling a 10.7 MHz Input Using the AD9243 (V_{CM} = 2.5 V, Input Span = 2 V p-p)

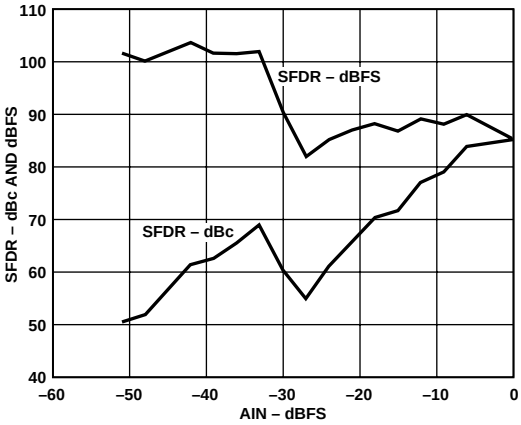


Figure 50. AD9243 Differential Input SNR/SFDR vs. Input Amplitude (AIN) @ 10.7 MHz

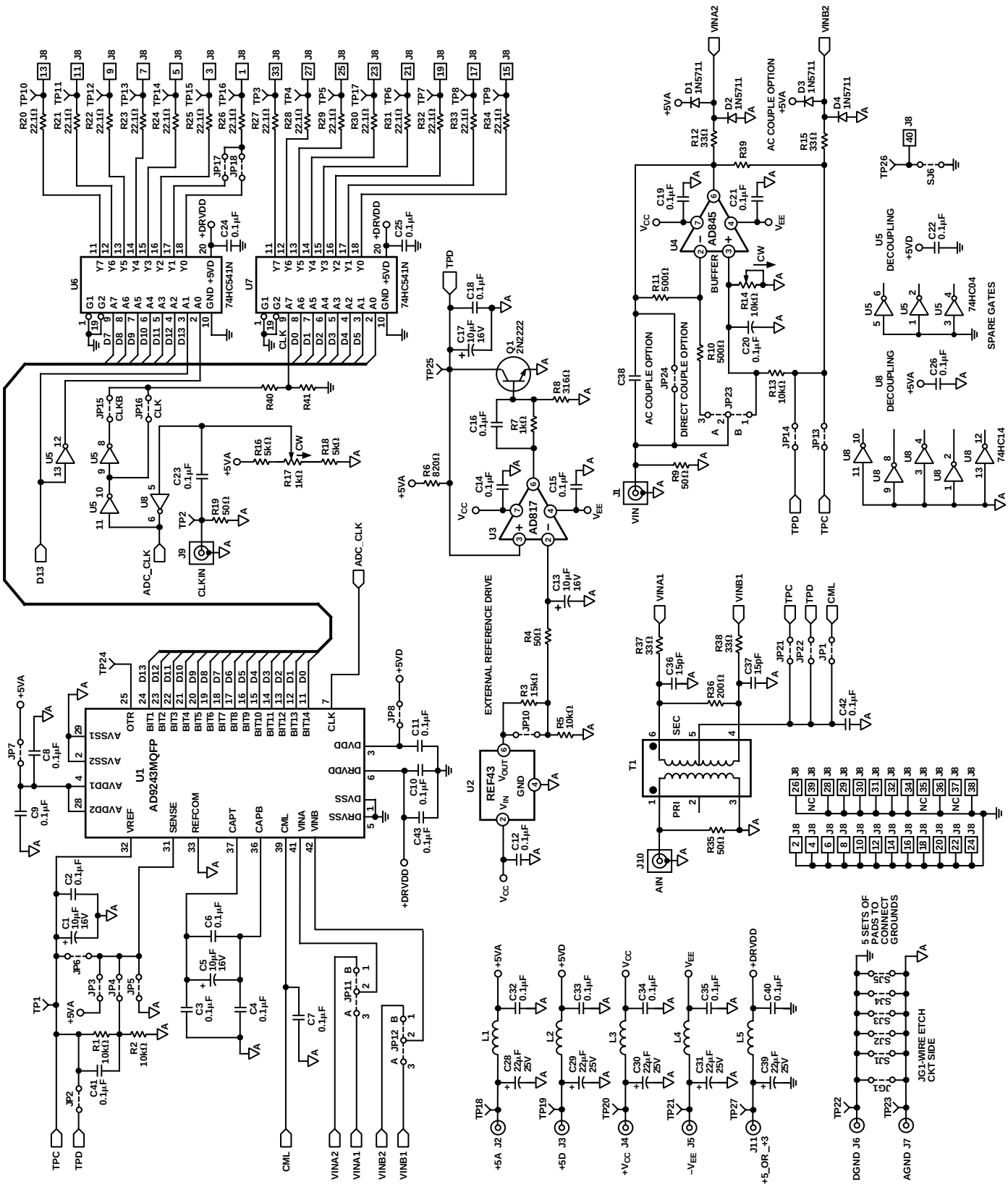


Figure 51. Evaluation Board Schematic

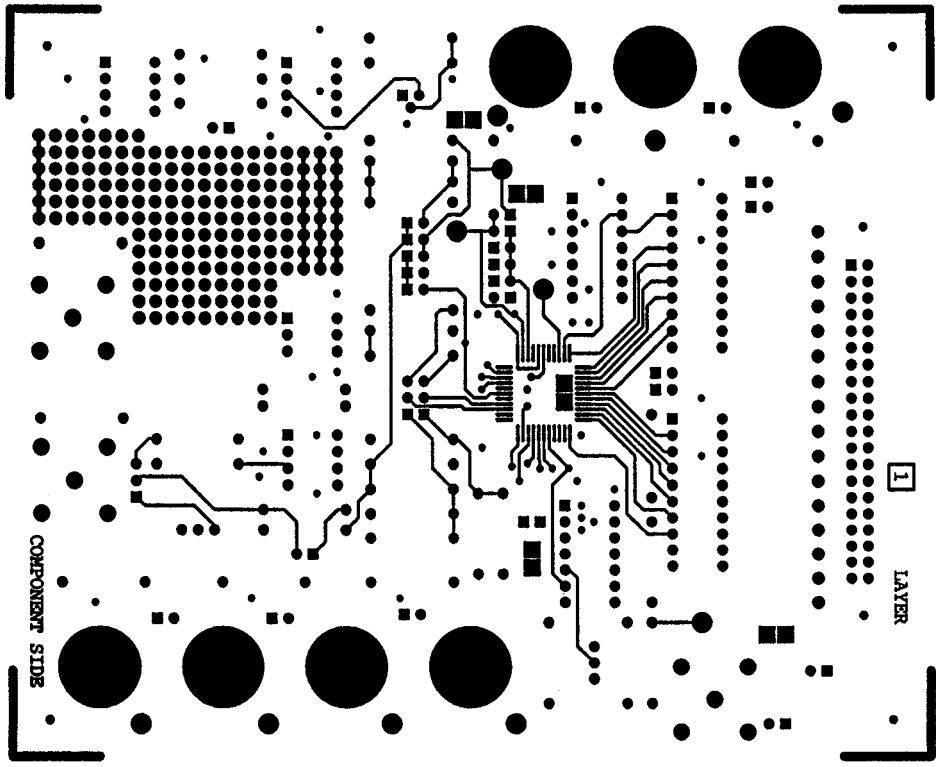


Figure 52. Evaluation Board Component Side Layout (Not to Scale)

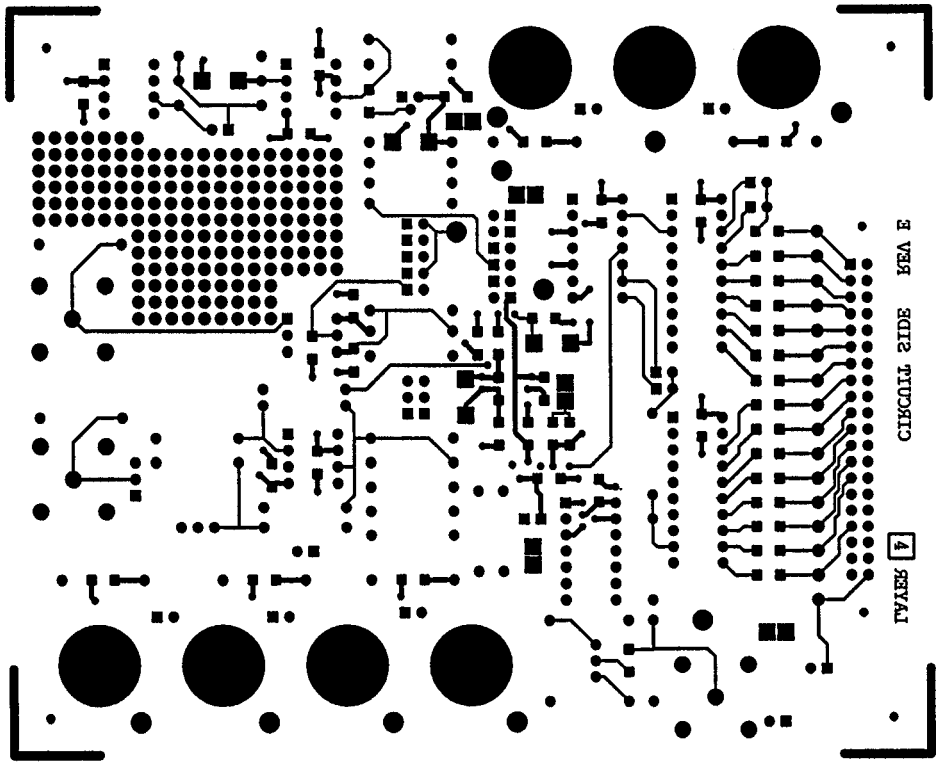


Figure 53. Evaluation Board Solder Side Layout (Not to Scale)

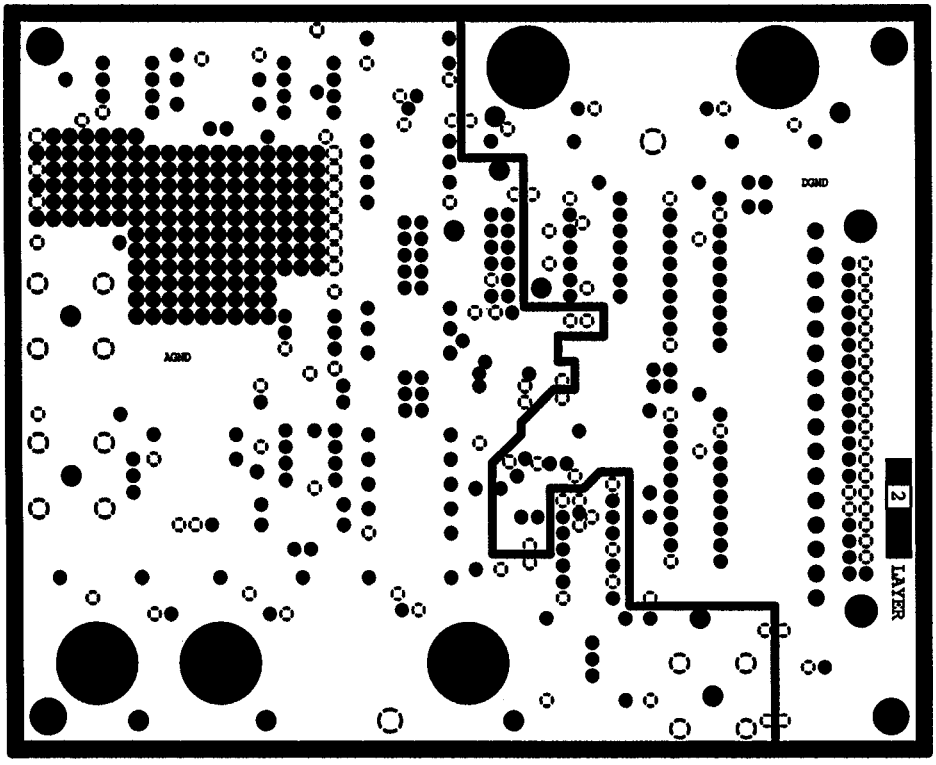


Figure 54. Evaluation Board Ground Plane Layout (Not to Scale)

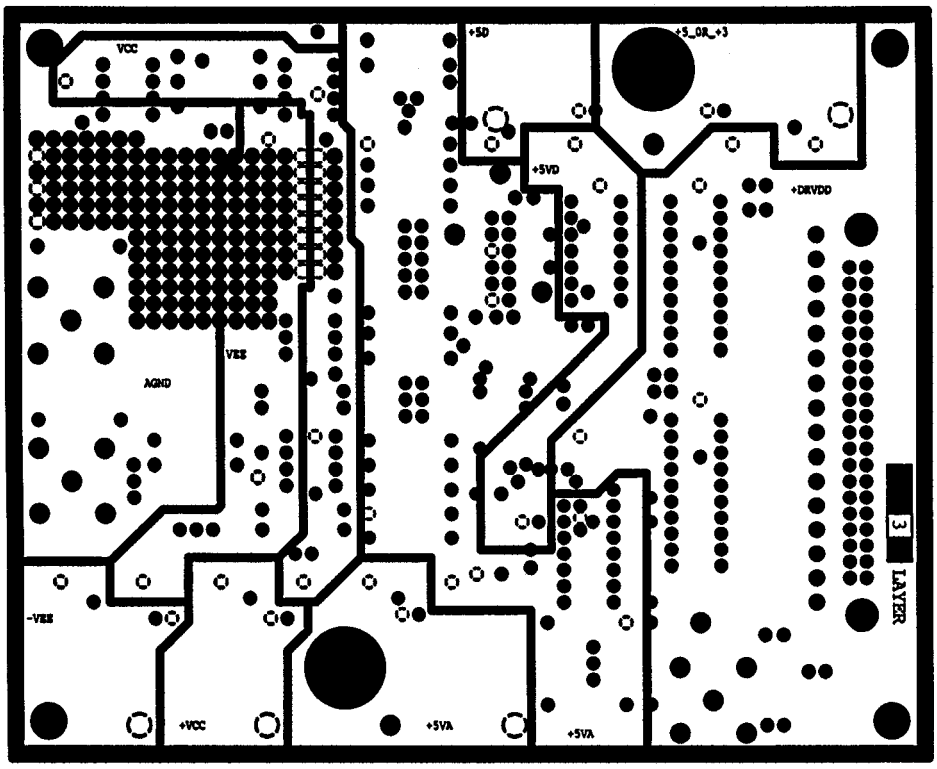
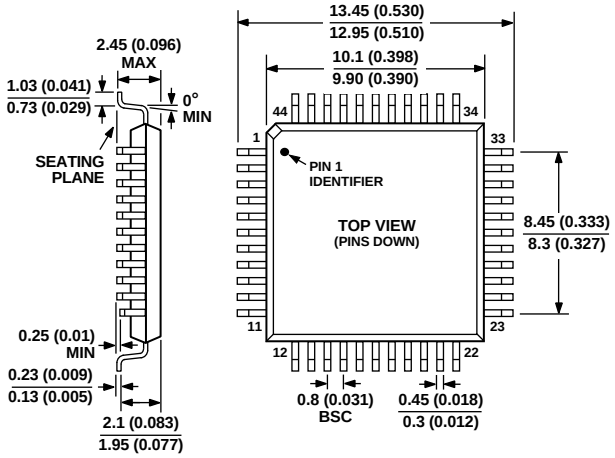


Figure 55. Evaluation Board Power Plane Layout (Not to Scale)

OUTLINE DIMENSIONS

Dimensions shown in mm and (inches).

44-Lead Metric Quad Flatpack (MQFP)
(S-44)



C2202a–0–5/98

PRINTED IN U.S.A.