LDC1001 Inductance-to-Digital Converter

1 Features

- Magnet-free operation
- Sub-micron precision
- Adjustable sensing range (through coil design)
- Lower system cost
- Remote sensor placement (decoupling the LDC from harsh environments)
- High durability (by virtue of contact-less operation)
- Insensitivity to environmental interference (such as dirt, dust, water, oil)
- Supply voltage, analog: 4.75 V to 5.25 V
- Supply voltage, I/O: 1.8 V to 5.25 V
- Supply current (without LC tank): 1.7 mA
- R_P resolution: 16 bit
- L resolution: 24 bit
- LC frequency range: 5 kHz to 5 MHz

2 Applications

- Touch buttons
- Angular position sensing
- Linear position sensing
- Metal proximity sensing

3 Description

The LDC1001 device is a 4.75-V to 5.25-V inductance-to-digital converter designed for parallel resistance (Rp) and inductance (L) measurements. Inductive sensing technology enables precise measurement of linear or angular position of metal targets in automotive and industrial applications.

Inductive sensing is a contactless, short-range sensing technology that can enable high-resolution sensing of conductive targets in the presence of dust, dirt, oil, and moisture, which can be used by applications in harsh environments.

The LDC1001 system consists of an inductive sensor, typically a PCB coil, and a conductive target.

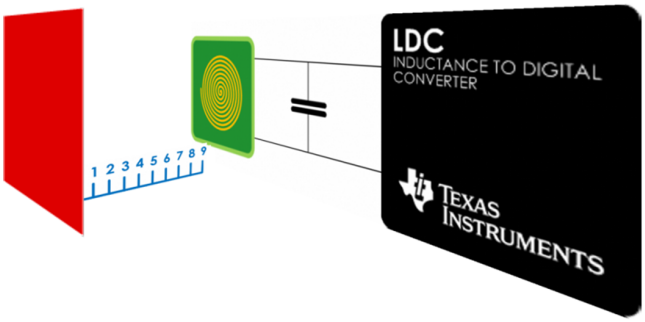
The LDC1001 is available in a 16-pin WSON package and offers several modes of operation. A serial peripheral interface (SPI) simplifies connection to an MCU.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LDC1001	WSON (16)	5.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Axial Distance Sensing Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 4
6.3 Recommended Operating Condition ... 4
6.4 Thermal Information ... 4
6.5 Electrical Characteristics ... 5
6.6 Timing Requirements ... 6
6.7 Typical Characteristics ... 7
7 Detailed Description ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Feature Description ... 8
7.4 Device Functional Modes ... 12
7.5 Programming ... 15
7.6 Register Maps ... 17
8 Application and Implementation ... 24
8.1 Application Information ... 24
8.2 Typical Application ... 25
9 Power Supply Recommendations ... 28
10 Layout ... 28
10.1 Layout Guidelines ... 28
10.2 Layout Example ... 29
11 Device and Documentation Support ... 30
11.1 Documentation Support ... 30
11.2 Support Resources ... 30
11.3 Trademarks ... 30
11.4 Electrostatic Discharge Caution ... 30
11.5 Glossary ... 30
12 Mechanical, Packaging, and Orderable Information ... 30

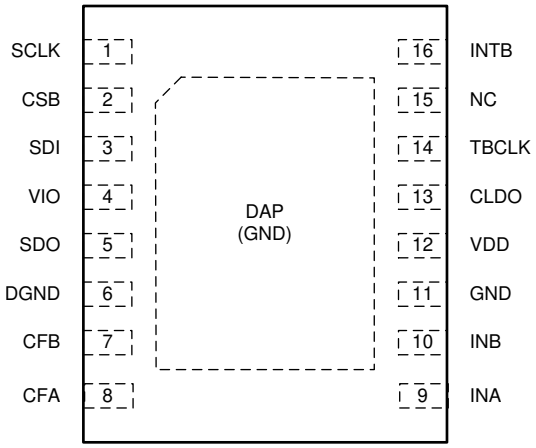
4 Revision History

DATE	VERSION	NOTES
November 2019	*	Initial release.

Copyright © 2019, Texas Instruments Incorporated

5 Pin Configuration and Functions

NHR Package
16-Pin WSON
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	SCLK	DI	SPI clock input. SCLK is used to clock-out/clock-in the data from/into the chip.
2	CSB	DI	SPI CSB. Multiple devices can be connected on the same SPI bus with each device having a dedicated CSB connection to the MCU so that each device can be uniquely selected.
3	SDI	DI	SPI Slave Data In (Master Out Slave In). This should be connected to the Master Out Slave In of the master.
4	VIO	P	Digital IO Supply
6	DGND	P	Digital ground
5	SDO	DO	SPI Slave Data Out (Master In Slave Out). This pin is high-Z when CSB is high.
7	CFB	A	LDC filter capacitor
8	CFA	A	LDC filter capacitor
9	INA	A	External LC Tank. Connected to external LC tank
10	INB	A	External LC Tank. Connected to external LC tank
11	GND	P	Analog ground
12	VDD	P	Analog supply
13	CLDO	A	LDO bypass capacitor. A 56-nF capacitor should be connected from this pin to GND.
14	TBCLK	DI/A	External time-base clock
15	NC	NC	This pin should be left floating.
16	INTB	DO	Configurable interrupt output.
—	DAP	P	Connect to GND for improved thermal performance.(2)

(1) DO: Digital Output, DI: Digital Input, P: Power, A: Analog
(2) There is an internal electrical connection between the exposed Die Attach Pad (DAP) and the GND pin of the device. Although the DAP can be left floating, for best performance the DAP should be connected to the same potential as the devices's GND pin. Do no use the DAP as the primary ground for the device. The device GND pin must always be connected to ground.

Copyright © 2019, Texas Instruments Incorporated

6 Specifications

6.1 Absolute Maximum Ratings[1]

	MIN	MAX	UNIT
Analog supply voltage (V_{DD} – GND)		6	V
IO supply voltage (V_{IO} – GND)		6	V
Voltage on any analog pin	–0.3	V_{DD} + 0.3	V
Voltage on any digital pin	–0.3	V_{IO} + 0.3	V
Input current on INA and INB		8	mA
Junction temperature, T_J[2]		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} – T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB. The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Condition

	MIN	MAX	UNIT
Analog Supply Voltage (V_{DD} – GND)	4.75	5.25	V
IO Supply Voltage (V_{IO} – GND)	1.8	5.25	V
$V_{DD} – V_{IO}$	≥0		V
Operating Temperature, T_A	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LDC1001 NHR (WSON) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	28	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} – T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB. The package thermal impedance is calculated in accordance with JESD 51-7.

Copyright © 2019, Texas Instruments Incorporated

6.5 Electrical Characteristics

Unless otherwise specified, all limits ensured for $T_A = T_J = 25°C$, $V_{DD} = 5$ V, $V_{IO} = 3.3$ V[1][2]

PARAMETER		TEST CONDITIONS	MIN[3]	TYP[4]	MAX[3]	UNIT
POWER						
V_{DD}	Analog supply voltage		4.75	5	5.25	V
V_{IO}	IO supply voltage	$V_{IO} \le V_{DD}$	1.8	3.3	5.25	V
I_{DD}	Supply current on VDD pin	PWR_MODE = 1, no sensor connected		1.7	2.3	mA
I_{VIO}	IO supply current	Static current			14	µA
I_{DD_LP}	Standby mode supply current on VDD pin	PWR_MODE = 0, no sensor connected		250		µA
t_{START}	Start-up time	From POR to ready-to-convert.		2		ms
LDC						
f_{SENSOR_MIN}	Minimum sensor frequency			5		kHz
f_{SENSOR_MAX}	Maximum sensor frequency			5		MHz
A_{SENSOR_MIN}	Minimum sensor amplitude			1		V_{PP}
A_{SENSOR_MAX}	Maximum sensor amplitude			4		V_{PP}
t_{REC}	Recovery time	Oscillation start-up time after R_P under-range condition		10		$1/f_{sensor}$
R_{P_MIN}	Minimum sensor R_P range			798		Ω
R_{P_MAX}	Maximum sensor R_P range			3.93		MΩ
R_{P_RES}	R_P measurement resolution			16		Bits
L Res	Inductance measurement resolution	RESPONSE_TIME = b111 (6144), f_{EXT} = 8 MHz, f_{SENSOR} = 5 kHz		24		Bits
t_{S_MIN}	Minimum response time	Minimum programmable settling time of digital filter		$192/f_{SENSOR}$		s
t_{S_MAX}	Maximum response time	Maximum programmable settling time of digital filter		$6144/f_{SENSOR}$		s
EXTERNAL CLOCK FOR FREQUENCY COUNTER						
External Clock	Frequency				8	MHz
	Clock input high voltage				V_{IO}	V
DIGITAL I/O CHARACTERISTICS						
V_{IH}	Logic 1 input voltage		$0.8 \times V_{IO}$			V
V_{IL}	Logic 0 input voltage				$0.2 \times V_{IO}$	V
V_{OH}	Logic 1 output voltage	I_{SOURCE} = 400 µA		V_{IO}–0.3		V
V_{OL}	Logic 0 output voltage	I_{SINK} = 400 µA			0.3	V
I_{IOHL}	Digital IO leakage current		–500		500	nA

(1) *Electrical Characteristics* table values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is $P_{DMAX} = (T_{J(MAX)} - T_A)/ R_{\theta JA}$. All numbers apply for packages soldered directly onto a PCB. The package thermal impedance is calculated in accordance with JESD 51-7.

(3) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.

(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.

Copyright © 2019, Texas Instruments Incorporated

6.6 Timing Requirements

Unless otherwise noted, all limits specified at T_A = 25°C, V_{DD} = 5 V, V_{IO} = 3.3 V, 10-pF capacitive load in parallel with a 10-kΩ load on SDO. Specified by design; not production tested.

			MIN	NOM	MAX	UNIT
f_{SCLK}	Serial clock frequency				4	MHz
t_{PH}	SCLK pulse width high	f_{SCLK} = 4 MHz	0.4 / f_{SCLK}			s
t_{PL}	SCLK pulse width low	f_{SCLK} = 4 MHz	0.4 / f_{SCLK}			s
t_{SU}	SDI setup time		10			ns
t_H	SDI hold time		10			ns
t_{ODZ}	SDO driven-to-tristate time	Measured at 10% / 90% point			20	ns
t_{OZD}	SDO tristate-to-driven time	Measured at 10% / 90% point			20	ns
t_{OD}	SDO output delay time				20	ns
t_{CSS}	CSB setup time		20			ns
t_{CSH}	CSB hold time		20			ns
t_{IAG}	Inter-access gap		100			ns
t_{DRDYB}	Data ready pulse width	Data ready pulse at every 1 / ODR if no data is read		1 / f_{sensor}		s

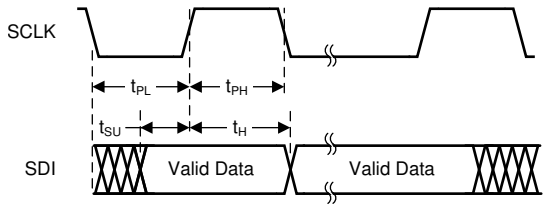


Figure 1. Write Timing Diagram

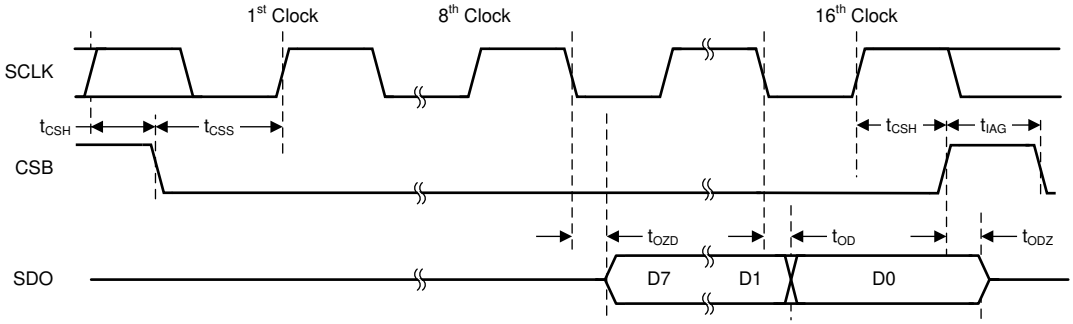
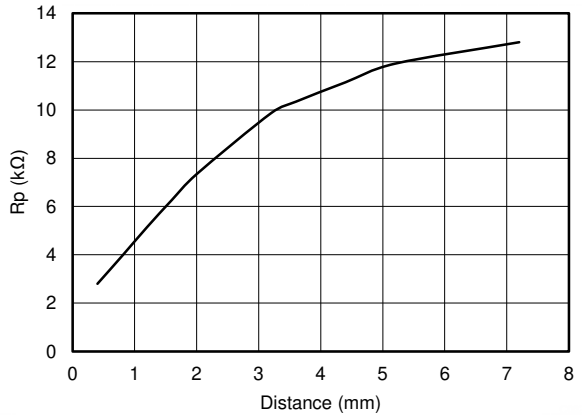


Figure 2. Read Timing Diagram

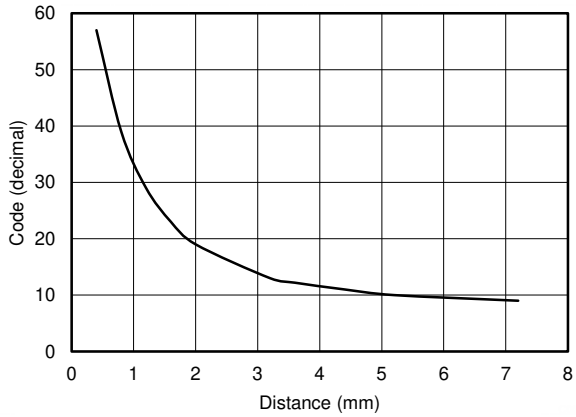
Copyright © 2019, Texas Instruments Incorporated

6.7 Typical Characteristics



Sensor Details:	Table 23	R_P_MIN:	1.347 kΩ
Target Material:	Stainless Steel	R_P_MAX:	38.785 kΩ

Figure 3. R_P vs Distance



Sensor Details:	Table 23	R_P_MIN:	1.347 kΩ
Target Material:	Stainless Steel	R_P_MAX:	38.785 kΩ

Figure 4. Proximity Data vs Distance

7 Detailed Description

7.1 Overview

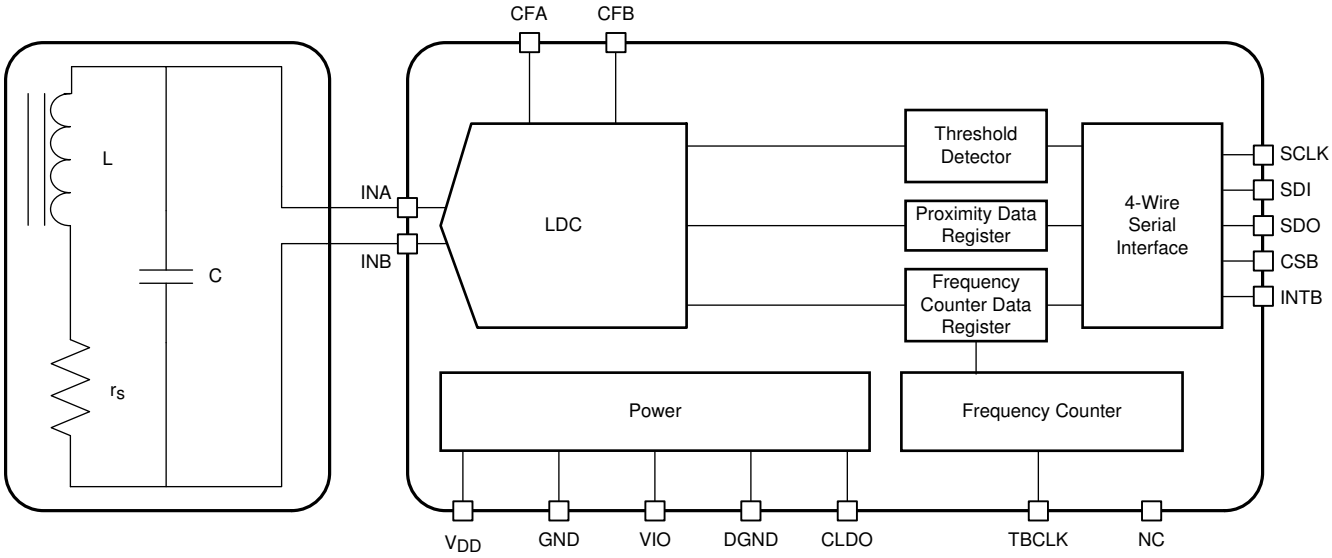
The LDC1001 is an Inductance-to-Digital Converter that measures the parallel impedance of an LC resonator. The device accomplishes this task by regulating the oscillation amplitude in a closed-loop configuration to a constant level, while monitoring the energy dissipated by the resonator. By monitoring the amount of power injected into the resonator, the LDC1001 can determine the value of R_P. When the value is determined, the device returns this as a digital value which is inversely proportional to R_P.

The threshold detector block provides a comparator with hysteresis. With the threshold registers programed and comparator enabled, proximity data register is compared with threshold registers and INTB pin indicates the output.

The device has a simple 4-wire SPI interface. The INTB pin provides multiple functions which are programmable with SPI.

The device has separate analog and I/O supplies. The analog supply operates at 5 V and the I/O operates at 1.8 to 5 V. The integrated LDO requires a 56-nF capacitor connected from the CLDO pin to GND.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Inductive Sensing

An AC current flowing through an inductor will generate an AC magnetic field. If a conductive material, such as a metal target, is brought into the vicinity of the coil, this magnetic field will induce circulating currents (eddy currents) on the surface of the target. These eddy currents are a function of the distance, size, and composition of the target. The eddy currents then generate their own magnetic field, which opposes the original field generated by the coil. This mechanism is best compared to a transformer, where the coil is the primary core and the eddy current is the secondary core. The inductive coupling between both cores depends on distance and shape. Hence the resistance and inductance of the secondary core (eddy current), shows up as a distant dependent resistive and inductive component on the primary side (coil). Figure 5 and Figure 8 show a simplified circuit model.

Copyright © 2019, Texas Instruments Incorporated

Feature Description (continued)

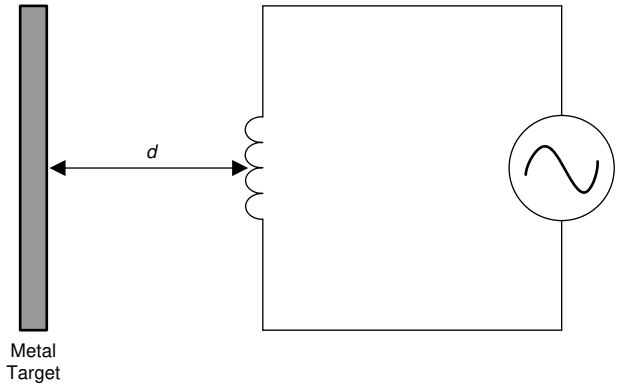


Figure 5. Inductor With a Metal Target

Eddy currents generated on the surface of the target can be modeled as a transformer as shown in Figure 6. The coupling between the primary and secondary coils is a function of the distance and the characteristics of the conductor. In Figure 6, the inductance L_S is the inductance of the coil, and R_S is the parasitic series resistance of the coil. The inductance L(*d*), which is a function of sensor to target distance, *d*, is the coupled inductance of the metal target. Likewise, R(*d*) is the parasitic resistance of the eddy currents and is also a function of distance.

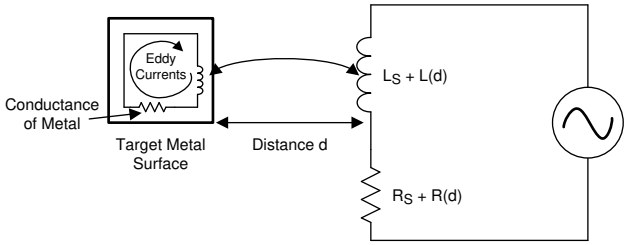


Figure 6. Metal Target Modeled as L and R With Circulating Eddy Currents

Generating an alternating magnetic field with just an inductor will consume a large amount of power. This power consumption can be reduced by adding a parallel capacitor, turning it into a resonator as shown in Figure 7. In this manner the power consumption is reduced to the eddy and inductor losses R_S + R(*d*) only.

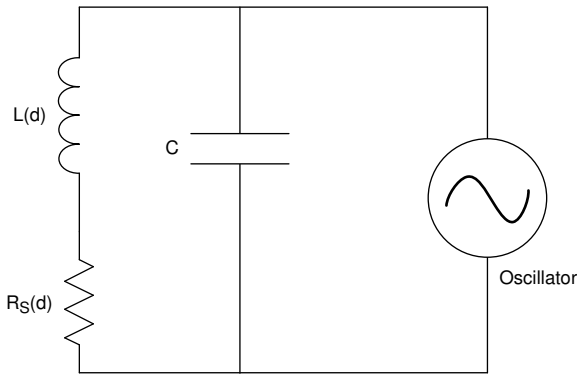


Figure 7. LC Tank Connected to Oscillator

Feature Description (continued)

The LDC1001 doesn't measure the series resistance directly; instead it measures the equivalent parallel resonance impedance R_P (see Figure 8). This representation is equivalent to the one shown in Figure 8, where the parallel resonance impedance $R_P(d)$ is given by Equation 1:

$$R_P(d) = \frac{L_S + L(d)}{[R_S + R(d)] \times C} \quad (1)$$

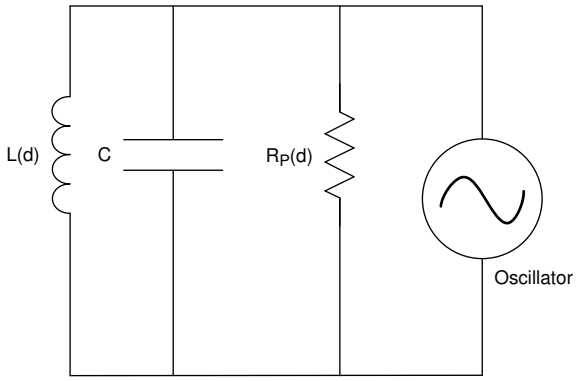


Figure 8. Equivalent Resistance of R_S in Parallel With LC Tank

Figure 9 shows the variation in R_P as a function of distance for a 14-mm diameter PCB coil (refer to the sensor characteristics in Table 23). The target in this example is a section of a 2-mm thick stainless steel disk.

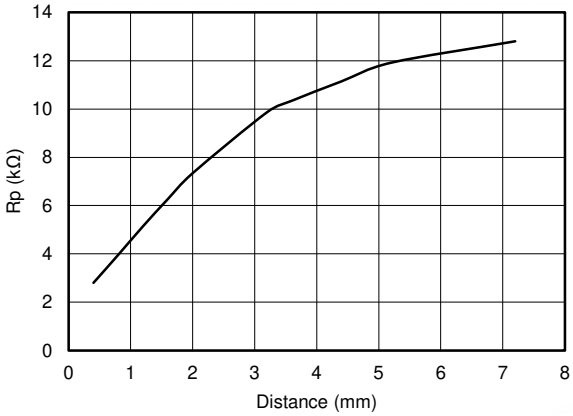


Figure 9. Typical R_P vs Distance With 14-mm PCB Coil

7.3.2 Measuring R_P With LDC1001

The LDC1001 supports a wide range of LC combinations, with oscillation frequencies ranging from 5 kHz to 5 MHz and R_P ranging from 798 Ω to 3.93 MΩ. This range of R_P can be viewed as the maximum input range of an ADC. As shown in Figure 9, the range of R_P is typically much smaller than the maximum input range supported by the LDC1001. To get better resolution in the desired sensing range, the LDC1001 offers a programmable input range through the R_P_MIN and R_P_MAX registers. Refer to *Calculation of R_P_MIN and R_P_MAX* for information on setting these registers.

When the resonance impedance R_P of the sensor drops below the programed R_P_MIN, the R_P output of the LDC will clip at its full scale output. This situation could, for example, happen when a target comes too close to the coil.

Copyright © 2019, Texas Instruments Incorporated

Feature Description (continued)

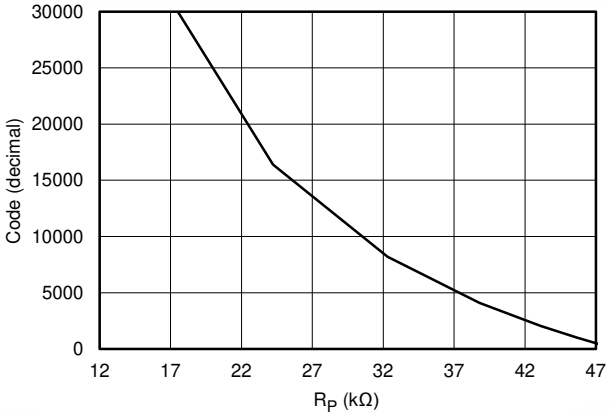


Figure 10. Transfer Characteristics of LDC1001 With R_P_MIN = 16.160 kΩ and R_P_MAX = 48.481 kΩ

Use Equation 2 to calculate the resonance impedance from the digital output code:

$$R_P = \frac{R_P_MAX \times R_P_MIN}{[R_P_MIN \times (1 - Y)] + (R_P_MAX \times Y)}$$

Where:

- R_P = Measured sensor parallel resistance in kΩ.
- R_P_MIN is the resistance (in kΩ) selected in register 0x02
- R_P_MAX is the resistance (in kΩ) selected in register 0x01
- Y = Proximity Data÷2^{15}
- Proximity data is the LDC R_P output = (Contents of Register 0x22) × 2^8 + (Contents of register 0x21). (2)

Example: If Proximity data (address 0x22:0x21) is 5000, R_P_MIN is 2.394 kΩ, and R_P_MAX is 38.785 kΩ ,the resonance impedance is given by:

Y = 5000/2^{15} = 0.1526

R_P = (38785 × 2394) ÷ (2394 × (1 – 0.1526) + 38785 × 0.1526) = (92851290 ÷ (2028.675 + 5918.591))

R_P = 11.683 kΩ

7.3.3 Measuring Inductance With LDC1001

LDC1001 measures the sensor's frequency of oscillation using a frequency counter. The frequency counter timing is set by an external clock applied on TBCLK pin. The sensor frequency can be calculated from the frequency counter register value (see registers 0x23 through 0x25) in Equation 3:

$$f_{SENSOR} = \frac{f_{EXT} \times RESPONSE_TIME}{3 \times FCOUNT}$$

Where:

- f_{SENSOR} is the measured sensor frequency
- f_{EXT} is the frequency of the external clock.
- FCOUNT is the value obtained from the Frequency Counter Data registers (address 0x23,0x24,0x25).
- RESPONSE_TIME is the programmed response time (set in the LDC configuration register, address 0x04). (3)

Copyright © 2019, Texas Instruments Incorporated

Feature Description (continued)

Use Equation 4 to determine the sensor inductance:

$$L = \frac{1}{C \times (2\pi \times f_{SENSOR})^2} \quad (4)$$

where

- C is the parallel sensor capacitance
- f_{SENSOR} is the sensor frequency calculated in Equation 3

Example: If f_{EXT} = 6MHz, RESPONSE_TIME = 6144, C = 100 pF and measured Fcount = 3000 (dec) (address 0x23 through 0x25)

f_{sensor}=(1/3) × (6000000/3000) × (6144)= 4.096 MHz

Using the f_{sensor} = 4.096 MHz example for Equation 4, the sensor inductance L = 15.098 µH.

NOTE

The accuracy of a measurement largely depends upon the frequency of the external time-base clock (TBCLK). A higher frequency will provide better measurement accuracy. The maximum supported frequency is 8 MHz.

7.4 Device Functional Modes

7.4.1 Power Modes

The LDC1001 has two power modes:

- Active Mode: In this mode the LDC1001 is performing conversions. Changing any device configuration settings except PWR_MODE or INTB_MODE when the LDC1001 is in active mode is not recommended. This mode is selected when PWR_MODE = 1.
- Standby Mode: This is the default mode on device power up. In the mode the LDC1001 power consumption is lower than when in Active mode, however the LDC1001 is not performing conversions. The SPI of the device is enabled, and the device should be configured in this mode. This mode is selected when PWR_MODE = 0.

7.4.2 INTB Pin Modes

The INTB pin is a configurable output pin which can be used to drive an interrupt on an MCU. This mode is selected by setting INTB_MODE. The LDC1001 provides three different modes on INTB pin:

1. Comparator Mode
2. Wake-Up Mode
3. DRDY Mode

LDC1001 has a built-in High and Low trigger threshold which registers as a comparator with programmable hysteresis or a special mode which can be used to wake up an MCU.

Copyright © 2019, Texas Instruments Incorporated

Device Functional Modes (continued)

7.4.2.1 Comparator Mode

In the Comparator mode, the INTB pin is asserted or deasserted when the proximity register value increases above Threshold High or decreases below Threshold Low registers, respectively. In this mode, the LDC1001 essentially behaves as a proximity switch with programmable hysteresis.

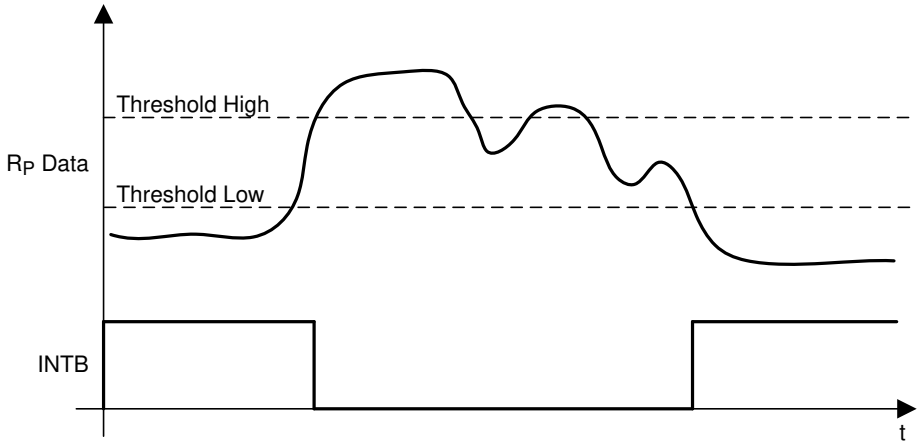


Figure 11. Behavior of INTB Pin in Comparator Mode

7.4.2.2 Wake-Up Mode

In Wake-up mode, the INTB pin is asserted when proximity register value increases above Threshold High and deasserted when wake-up mode is disabled in INTB pin mode register.

This mode can be used to wake up an MCU that is in sleep mode to conserve power.

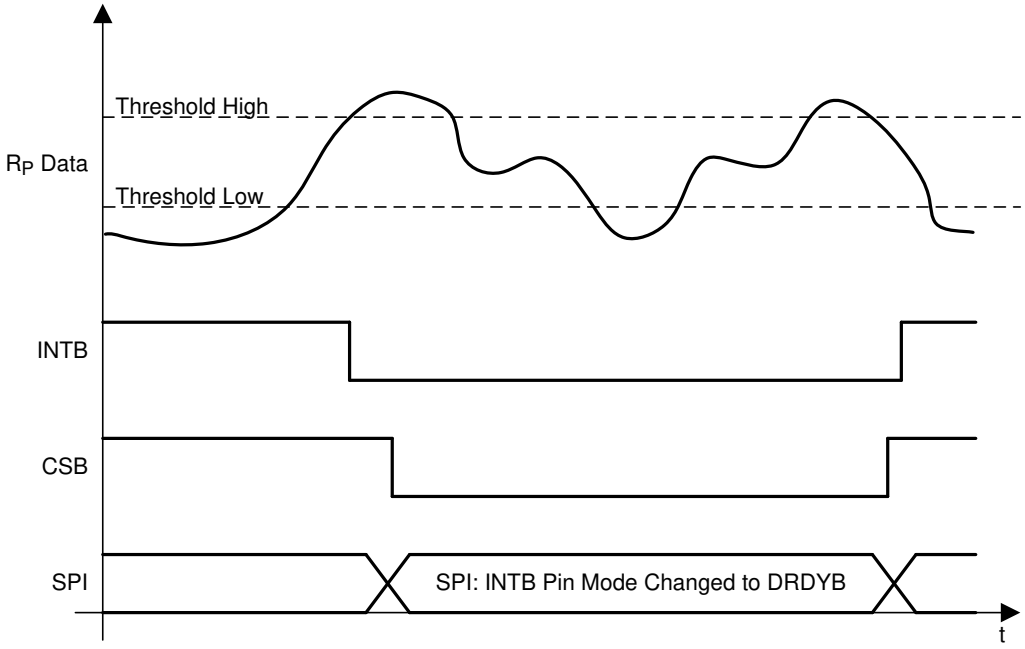


Figure 12. Behavior of INTB Pin in Wake-Up Mode

Device Functional Modes (continued)

7.4.2.3 DRDY Mode

In DRDY mode, the INTB pin is asserted every time the conversion data is available and deasserted once the read command on register 0x21 is registered internally; if the read is in progress, the pin is pulsed instead. TI recommends to configure this setting after PWR_MODE has been set to 1 (the LDC1001 is in Active Mode).

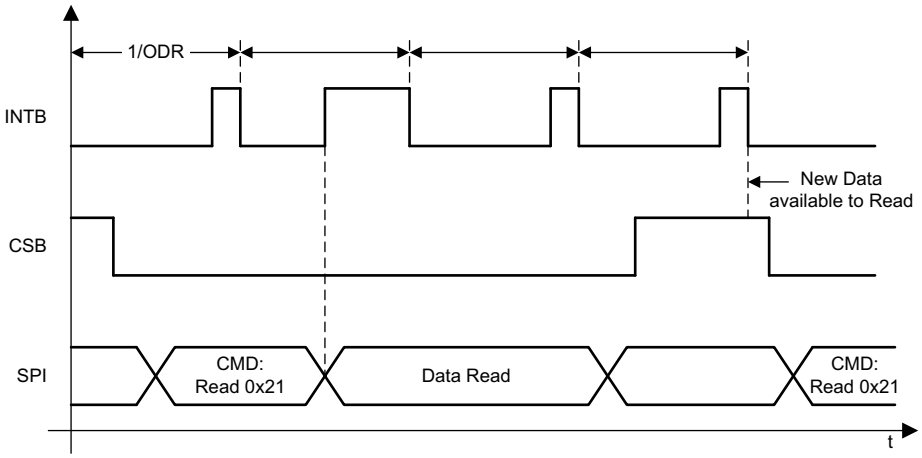


Figure 13. Behavior of INTB pin in DRDY Mode With SPI Extending Beyond Subsequent Conversions

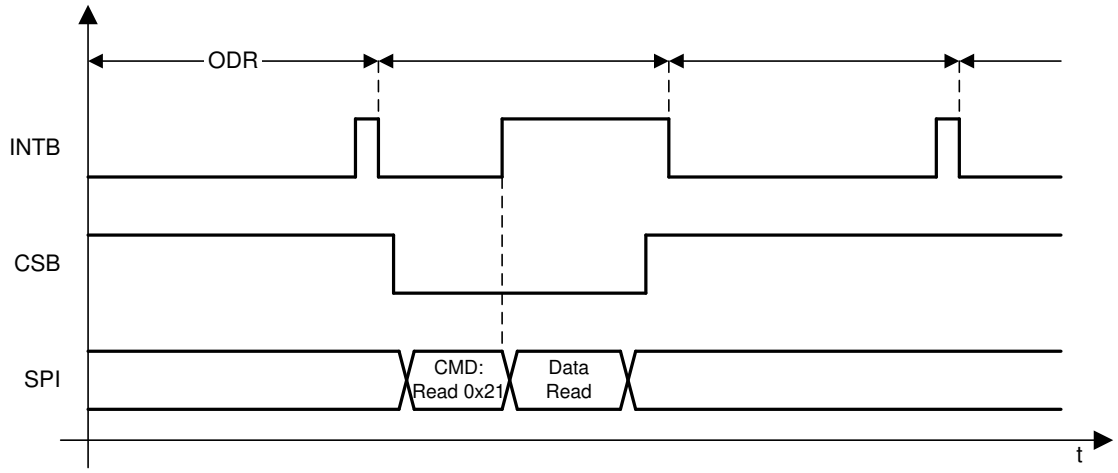


Figure 14. Behavior of INTB Pin in DRDY Mode With SPI Reading the Data Within Subsequent Conversion

Copyright © 2019, Texas Instruments Incorporated

7.5 Programming

The LDC1001 uses a 4-wire SPI to access control and data registers. The LDC1001 is a SPI slave device and does not initiate any transactions.

7.5.1 SPI Description

A typical serial interface transaction begins with an 8-bit instruction, which is comprised of a read/write bit (MSB, R=1) and a 7-bit address of the register, followed by a Data field which is typically 8 bits. However, the data field can be extended to a multiple of 8 bits by providing sufficient SPI clocks. Refer to the *Extended SPI Transactions* section for more information.

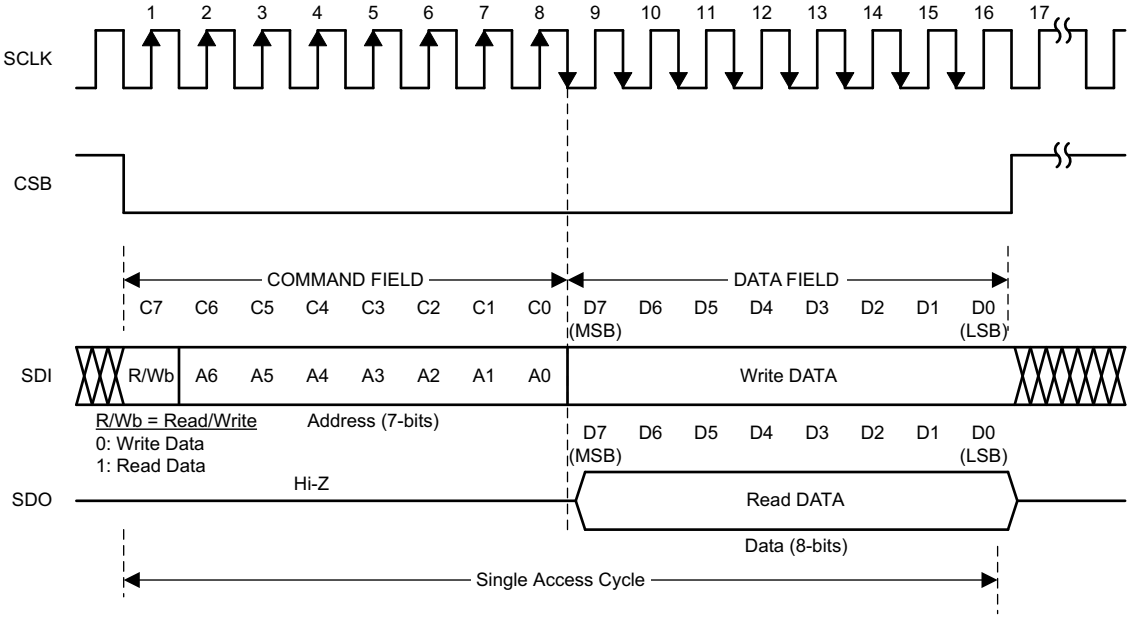


Figure 15. Serial Interface Protocol

Each assertion of chip select bar (CSB) starts a new register access. The R/Wb bit in the command field configures the type of the access. A value of 0 indicates a write operation, and a value of 1 indicates a read operation. All output data is driven on the falling edge of the serial clock (SCLK), and all input data is sampled on the rising edge of the serial clock (SCLK). Data is written into the register on the rising edge of the 16th clock. It is required to deassert CSB after the 16th clock. Remember that if CSB is deasserted before the 16th clock, no data write will occur.

The LDC1001 utilizes a 4-wire SPI interface to access control and data registers. The LDC1001 is an SPI slave device and does not initiate any transactions.

7.5.1.1 Extended SPI Transactions

A SPI transaction may be extended to multiple registers by keeping the CSB asserted for more than 16 pulses on SCLK. In this mode, the register addresses increment automatically. CSB must be remain asserted during 8*(1+N) clock cycles of SCLK, where N is the amount of bytes to write or read during the transaction.

During an extended read access, SDO outputs the register contents every 8 clock cycles after the initial 8 clocks of the command field. During an extended write access, the data is written to the registers every 8 clock cycles after the initial 8 clocks of the command field.

Extended transactions can be used to read 16 bits of proximity data and 24 bits of frequency data all in one SPI transaction by initiating a read from register 0x21.

Copyright © 2019, Texas Instruments Incorporated

Programming (continued)

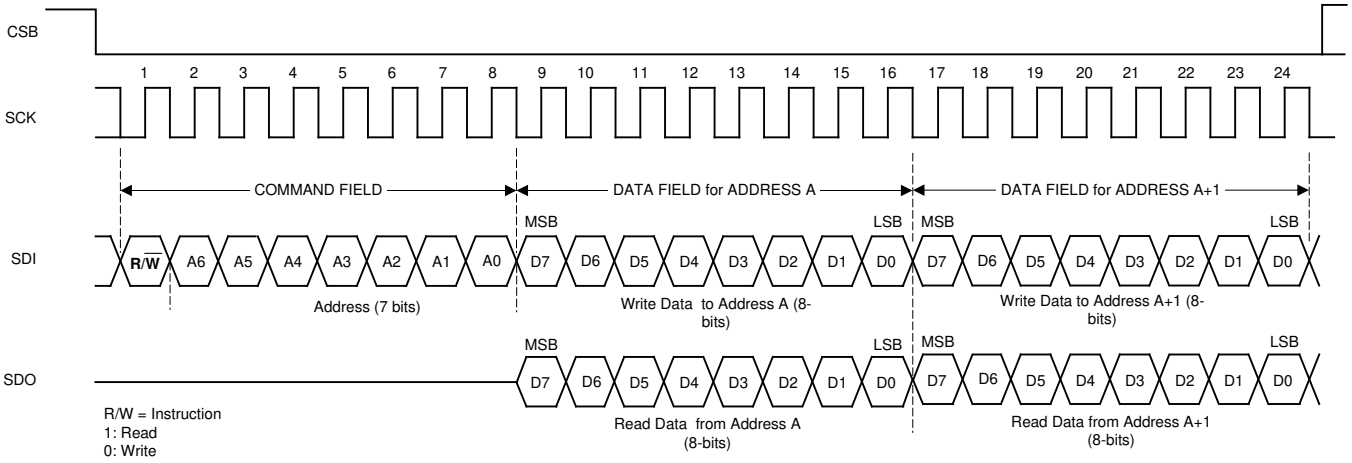


Figure 16. Extended SPI Transaction

Copyright © 2019, Texas Instruments Incorporated

7.6 Register Maps

Table 1. Register Map(1)(2)

REGISTER NAME	ADDRESS	TYPE(3)	DEFAULT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Device ID	0x00	RO	0x84	Device ID							
R_P_MAX	0x01	R/W	0x0E	R_P Maximum							
R_P_MIN	0x02	R/W	0x14	R_P Minimum							
Watchdog Timer Frequency	0x03	R/W	0x45	Min Sensor Frequency							
LDC Configuration	0x04	R/W	0x1B	Reserved (000)			Amplitude		RESPONSE_TIME		
Clock Configuration	0x05	R/W	0x01	Reserved (00'0000)						CLK_SEL	CLK_PD
Comparator Threshold High LSB	0x06	R/W	0xFF	Threshold High LSB							
Comparator Threshold High MSB	0x07	R/W	0xFF	Threshold High MSB							
Comparator Threshold Low LSB	0x08	R/W	0x00	Threshold Low LSB							
Comparator Threshold Low MSB	0x09	R/W	0x00	Threshold Low MSB							
INTB pin Configuration	0x0A	R/W	0x00	Reserved (0'0000)					INTB_MODE		
Power Configuration	0x0B	R/W	0x00	Reserved (000'0000)							PWR_MODE
Status	0x20	RO		OSC Dead	DRDY	Wake-up	Comparator	Don't Care			
Proximity	0x21	RO		Proximity Data[7:0] Data LSB							
Proximity	0x22	RO		Proximity Data [15:8] Data MSB							
Frequency Counter Data LSB	0x23	RO		FCOUNT LSB							
Frequency Counter Data Mid-Byte	0x24	RO		FCOUNT Mid Byte							
Frequency Counter Data MSB	0x25	RO		FCOUNT MSB							

(1) Values of register fields which are unused should be set to default values only.
(2) Registers 0x01 through 0x05 are Read Only when the part is awake (PWR_MODE bit is SET)
(3) R/W: Read/Write. RO: Read Only. WO: Write Only.

Copyright © 2019, Texas Instruments Incorporated

7.6.1 Register Description

7.6.1.1 Revision ID (Address = 0x00)

Table 2. Revision ID

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	Revision ID	RO	0x80	RevisionID of Silicon.

7.6.1.2 R_P_MAX (Address = 0x01)

Table 3. R_P_MAX

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	R_P Maximum	R/W	0x0E	Maximum Sensor R_P that LDC1001 needs to measure. Configures the input dynamic range of LDC1001. See Table 4 for register settings.

Table 4. Register Settings for R_P_MAX

REGISTER SETTING	R_P MAXIMUM SENSOR DRIVE (kΩ)
0x00	3926.991
0x01	3141.593
0x02	2243.995
0x03	1745.329
0x04	1308.997
0x05	981.748
0x06	747.998
0x07	581.776
0x08	436.332
0x09	349.066
0x0A	249.333
0x0B	193.926
0x0C	145.444
0x0D	109.083
0x0E	83.111
0x0F	64.642
0x10	48.481
0x11	38.785
0x12	27.704
0x13	21.547
0x14	16.160
0x15	12.120
0x16	9.235
0x17	7.182
0x18	5.387
0x19	4.309
0x1A	3.078
0x1B	2.394
0x1C	1.796
0x1D	1.347
0x1E	1.026

Copyright © 2019, Texas Instruments Incorporated

Table 4. Register Settings for R_P_MAX (continued)

REGISTER SETTING	R_P MAXIMUM SENSOR DRIVE (kΩ)
0x1F	0.798

7.6.1.3 R_P_MIN (Address = 0x02)

Table 5. R_P_MIN

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	R_P Minimum	R/W	0x14	Minimum Sensor R_P that LDC1001 needs to measure. Configures the input dynamic range of LDC1001. See Table 6 for register settings.(1)

(1) This register needs a mandatory write as it defaults to 0x14.

Table 6. Register Settings for R_P_MIN

REGISTER SETTING	R_P MINIMUM SENSOR DRIVE (kΩ)
0x20	3926.991
0x21	3141.593
0x22	2243.995
0x23	1745.329
0x24	1308.997
0x25	981.748
0x26	747.998
0x27	581.776
0x28	436.332
0x29	349.066
0x2A	249.333
0x2B	193.926
0x2C	145.444
0x2D	109.083
0x2E	83.111
0x2F	64.642
0x30	48.481
0x31	38.785
0x32	27.704
0x33	21.547
0x34	16.160
0x35	12.120
0x36	9.235
0x37	7.182
0x38	5.387
0x39	4.309
0x3A	3.078
0x3B	2.394
0x3C	1.796
0x3D	1.347
0x3E	1.026
0x3F	0.798

Copyright © 2019, Texas Instruments Incorporated

7.6.1.4 Watchdog Timer Frequency (Address = 0x03)

Table 7. Watchdog Timer Frequency

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	Min Sensor Frequency	R/W	0x45	Sets the watchdog timer. The Watchdog timer should be set based on the lowest sensor frequency. If this field is set to too high a value, then the LDC1001 may incorrectly determine a sensor oscillation timeout. $M = 68.94 \times \log_{10}\left(\frac{f_{SENSOR}}{2500}\right)$ where: • f_{SENSOR} is the sensor frequency • M is the register value to program for Min Sensor Frequency. (5) Example: With a Sensor frequency is 1 MHz Min Sensor Frequency = 68.94 × $\log_{10}$(1 × 10^6/2500) = Round to nearest integer (179.38) = 179

7.6.1.5 LDC Configuration (Address = 0x04)

Table 8. LDC Configuration

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:5	Reserved	R/W	0x1B	Reserved to 000
4:3	Amplitude			Sets the oscillation amplitude 00: 1 V 01: 2 V 10: 4 V **11: Reserved**
2:0	RESPONSE_TIME			000: Reserved 001: Reserved 010: 192 **011: 384** 100: 768 101: 1536 110: 3072 111: 6144

7.6.1.6 Clock Configuration (Address = 0x05)

Table 9. Clock Configuration

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:2	Reserved	R/W	0x01	Reserved to 00'0000.
1	CLK_SEL			**0: External time-based clock used for frequency counter (TBCLK)** 1: Do not use
0	CLK_PD			0: Enable external time base clock **1: Disable external time base clock (for lower power consumption in standby mode)**

Copyright © 2019, Texas Instruments Incorporated

7.6.1.7 Comparator Threshold High LSB (Address = 0x06)

Table 10. Comparator Threshold High LSB

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	Threshold High	R/W	0xFF	Threshold High Register LSB. Combine with contents of register 0x07 to set upper threshold.

7.6.1.8 Comparator Threshold High MSB (Address = 0x07)

Table 11. Comparator Threshold High MSB

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	Threshold High	R/W	0xFF	Threshold High Register MSB.

7.6.1.9 Comparator Threshold Low LSB (Address = 0x08)

Table 12. Comparator Threshold Low LSB

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	Threshold Low	R/W	0x00	Threshold Low Register LSB. Combine with contents of register 0x09 to set lower threshold.

7.6.1.10 Comparator Threshold Low MSB (Address = 0x09)

Table 13. Comparator Threshold Low MSB

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	Threshold Low	R/W	0x00	Threshold Low Register MSB.

7.6.1.11 INTB Pin Configuration (Address = 0x0A)

Table 14. INTB Pin Configuration

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:3	Reserved	R/W	0x00	Reserved to 00'000
2:0	INTB_MODE			**000: All modes disabled**. No signal output on INTB pin. 001: Wake-up Enabled on INTB pin 010: INTB pin indicates the status of Comparator output 100: DRDY Enabled on INTB pin All other combinations are Reserved

7.6.1.12 Power Configuration (Address = 0x0B)

Table 15. Power Configuration

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:1	Reserved	R/W	0x00	Reserved to 000'0000.
0	PWR_MODE			**0: Standby mode: LDC1001 is in a lower power mode but not actively converting. TI recommends to configure the LDC1001 while in this mode.** 1: Active Mode. Conversion is Enabled Refer to *Power Modes* for more details.

Copyright © 2019, Texas Instruments Incorporated

7.6.1.13 Status (Address = 0x20)

Table 16. Status

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7	OSC Status	RO	N/A	1: Indicates sensor oscillation timeout. This can be caused by a sensor with an R_P below R_P_MIN or setting Min Sensor Frequency too high. 0: Sensor oscillation timeout not detected.
6	Data Ready			1: No new data available 0: Data is ready to be read
5	Wake-up			1: Wake-up disabled 0: Wake-up triggered. Proximity data is more than Threshold High value.
4	Comparator			1: Proximity data is less than Threshold Low value 0: Proximity data is more than Threshold High value
3:0	Don't Care			Don't care

7.6.1.14 Proximity Data LSB (Address = 0x21)

TI recommends to read register 0x21 immediately after any read of register 0x20.

Table 17. Proximity Data LSB

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	Proximity Data[7:0]	RO	N/A	Least Significant Byte of Proximity Data

7.6.1.15 Proximity Data MSB (Address = 0x22)

Conversion data is updated to the proximity register only when a read is initiated on 0x21 register. If the read is delayed between subsequent conversions, these registers are not updated until another read is initiated on 0x21.

Table 18. Proximity Data MSB

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	Proximity data [15:8]	RO	N/A	Most Significant Byte of Proximity data

7.6.1.16 Frequency Counter LSB (Address = 0x23)

Table 19. Frequency Counter LSB

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FCOUNT LSB (FCOUNT[7:0])	RO	N/A	LSB of Frequency Counter. Sensor frequency can be calculated using the output data rate. Refer to the *Measuring Inductance With LDC1001* for more information.

7.6.1.17 Frequency Counter Mid-Byte (Address = 0x24)

Table 20. Frequency Counter Mid-Byte

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FCOUNT Mid byte (FCOUNT[15:8])	RO	N/A	Middle Byte of Output data rate

Copyright © 2019, Texas Instruments Incorporated

7.6.1.18 Frequency Counter MSB (Address = 0x25)

Table 21. Frequency Counter MSB

BIT	FIELD	TYPE	DEFAULT	DESCRIPTION
7:0	FCOUNT MSB (FCOUNT[23:16])	RO	N/A	MSB of Output data rate

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Calculation of R_P_MIN and R_P_MAX

Different sensing applications may have a different range of the resonance impedance R_P to measure. The LDC1001 measurement range of R_P is controlled by setting 2 registers – R_P_MIN and R_P_MAX. For a given application, R_P must never be outside the range set by these register values, otherwise the measured value will be clipped. For optimal sensor resolution, the range of R_P_MIN to R_P_MAX should not be unnecessarily large. The following procedure is recommended to determine the R_P_MIN and R_P_MAX register values.

8.1.1.1 R_P_MAX

R_P_MAX sets the upper limit of the LDC1001 resonant impedance input range.

- Configure the sensor such that the eddy current losses are minimized. As an example, for a proximity sensing application, set the distance between the sensor and the target to the maximum sensing distance.
- Measure the sensor impedance R_P using an impedance analyzer.
- Multiply R_P by 2 and use the next higher value from Table 7.

Setting R_P_MAX to a value not listed in Table 7 can result in indeterminate behavior.

8.1.1.2 R_P_MIN

R_P_MIN sets the lower limit of the LDC1001 resonant impedance input range.

- Configure the sensor such that the eddy current losses are maximized. As an example, for a proximity sensing application, set the distance between the sensor and the metal target to the minimum sensing distance.
- Measure the sensor impedance R_P using an impedance analyzer.
- Divide the R_P value by 2 and then select the next lower R_P value from Table 10.

Note that setting R_P_MIN to a value not listed on Table 10 can result in indeterminate behavior. In addition, R_P_MIN powers on with a default value of 0x14 which must be changed to a value from Table 10 prior to powering on the LDC.

8.1.2 Output Data Rate

The output data rate of (or the conversion time) LDC1001 depends on the sensor frequency, f_{sensor} and RESPONSE_TIME field in LDC Configuration register(Address:0x04). The maximum sample rate requires a RESPONSE_TIME setting of 192 and a sensor frequency of 5 MHz.

$$SR = \frac{3 \times f_{SENSOR}}{RESPONSE_TIME} \quad (6)$$

8.1.3 Choosing Filter Capacitor (CFA and CFB Pins)

The filter capacitor is critical to the operation of the LDC1001. The capacitor should be low leakage, temperature stable, and it must not generate any piezoelectric noise (the dielectrics of many capacitors exhibit piezoelectric characteristics and any such noise is coupled directly through R_P into the converter). The optimal capacitance values range from 20 pF to 100 nF. The value of the capacitor is based on the time constant and resonating frequency of the sensor.

Copyright © 2019, Texas Instruments Incorporated

Application Information (continued)

If a ceramic capacitor is used, then a C0G (or NP0) grade dielectric is recommended. The voltage rating should be ≥10 V. The traces connecting CFA and CFB to the capacitor should be as short as possible to minimize any parasitics.

For optimal performance, the selected filter capacitor connected between pins CFA and CFB must be as small as possible, but large enough such that the active filter does not saturate. The size of this capacitor depends on the time constant of the sense coil, which is given by L/R_S, (L=inductance, R_S=series resistance of the inductor at oscillation frequency). The larger this time constant, the larger filter capacitor is required. Hence, this time constant reaches its maximum when there is no target present in front of the sensor.

The following procedure can be used to find the optimal filter capacitance:

1. Start with a large filter capacitor. For a ferrite core coil, 10 nF is usually large enough. For an air coil or PCB coil, a value of 100 pF is usually large enough.
2. Power on the LDC1001 and set the desired register values. Minimize the eddy currents losses by minimizing the amount of conductive target covering the sensor. For an axial sensing application, the target should be at the farthest distance from coil. For a lateral or angular position sensing application, the target coverage of the coil should be minimized.
3. Observe the signal on the CFB pin using a scope. Because this node is very sensitive to capacitive loading, the use an active probe is recommended. As an alternative, a passive probe with a 1-kΩ series resistance between the tip and the CFB pin can be used. The time scale of the scope should be set so that 10-100 cycles of the sensor oscillation frequency are visible. For example, if the sensor frequency is 1 MHz, the timescale per division of the oscilloscope should be set to 0.1 ms.
4. Vary the values of the filter capacitor until that the signal observed on the CFB pin has an amplitude of approximate 1 V_{PP}. This signal scales linearly with the reciprocal of the filter capacitance. For example, if a 100-pF filter capacitor is applied and the signal observed on the CFB pin has a peak-to-peak value of 200 mV, the desired 1-V_{PP} value is obtained using a filter capacitor value that is calculated in Equation 7.

$$200\ mV / 1\ V \times 100\ pF = 20\ pF \quad (7)$$

8.2 Typical Application

8.2.1 Axial Distance Sensing Using a PCB Sensor With LDC1001

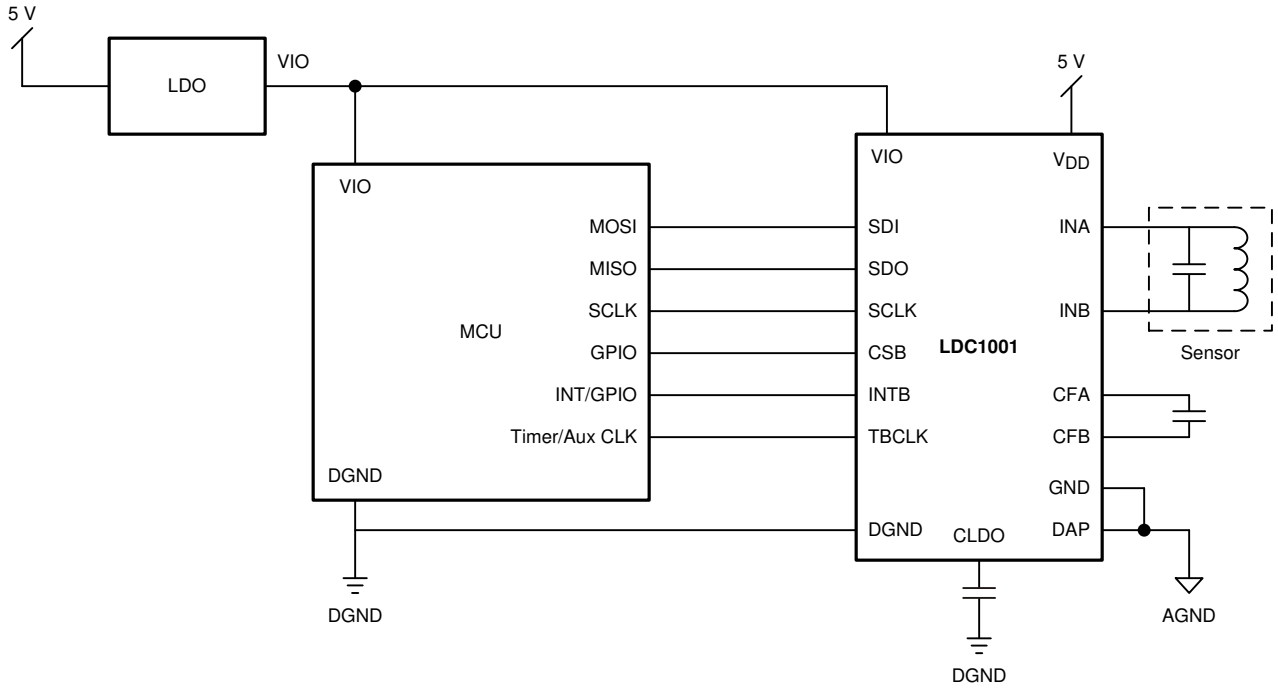


Figure 17. Typical Application Schematic

Typical Application (continued)

8.2.1.1 Design Requirements

For this design example, use the design parameters listed in Table 22 as the input parameters.

Table 22. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum sensing distance	1 mm
Maximum sensing distance	7 mm
Sample rate	28 KSPS
Number of PCB layers for sensor	2 layers with 62 mil (1.8 mm) PCB thickness
Sensor diameter	551 mil (14 mm)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Sensor and Target

In this example, consider a PCB sensor with the characteristics listed in Table 23:

Table 23. Sensor Characteristics

PARAMETER	VALUE
Thickness of PCB copper	1 oz (35 µm)
Coil shape	Circular
Number of turns	23
Trace thickness	4 mil (0.102 mm)
Trace spacing	4 mil (0.102 mm)
PCB core material	FR4
R_P at 1-mm target-sensor distance	5 kΩ
R_P at 7-mm target-sensor distance	12.5 kΩ
Nominal sensor Inductance	18 µH

The target is a stainless steel disk of 15-mm diameter and has a thickness of 1 mm.

8.2.1.2.2 Calculating Sensor Capacitor

Sensor frequency depends on various factors in the application. In this example, use Equation 8 to calculate the sensor frequency to achieve an output data rate of 28 KSPS per the design parameter.

$$SR = \frac{3 \times f_{SENSOR}}{RESPONSE_TIME} \tag{8}$$

With an LDC1001 RESPONSE_TIME setting of 384 and an output data rate specification of 28 KSPS, the sensor frequency calculated in Equation 8 is 3.6 MHz.

Using Equation 9, the sensor capacitor is 108 pF with the sensor inductance of 18 µH. A 100-pF sensor capacitor will slightly increase the sensor frequency to 3.75 MHz and provide a sample rate of 29.3 KSPS.

$$L = \frac{1}{C \times (2\pi \times f_{SENSOR})^2} \tag{9}$$

As the target interacts with the sensor inductance, the apparent inductance will decrease. When the target is at the 1-mm minimum distance for this application, the maximum interaction will occur, and the sensor frequency will increase to 3.95 MHz.

Copyright © 2019, Texas Instruments Incorporated

8.2.1.2.3 Choosing Filter Capacitor

Following the steps listed in the *Choosing Filter Capacitor (CFA and CFB Pins)* section, the filter capacitor for the example sensor is 20 pF. Figure 18 and Figure 19 show the pattern on CFB pin with a 100-pF and 20-pF filter capacitor. Notice that the timescale of scope traces is sufficient to vew the waveform over many cycles of the sensor oscillation.

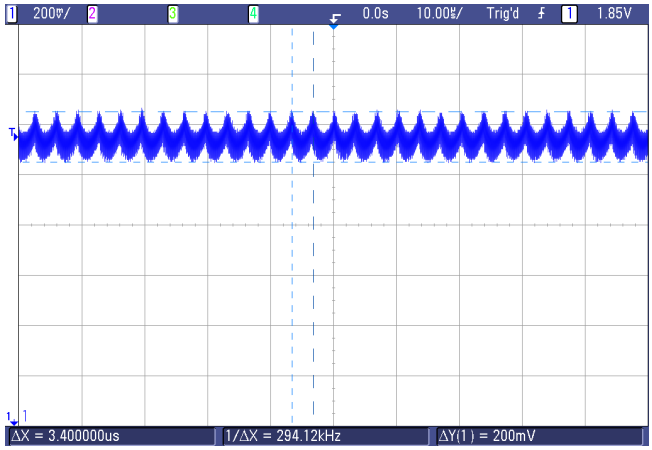


Figure 18. Waveform on CFB With 100 pF

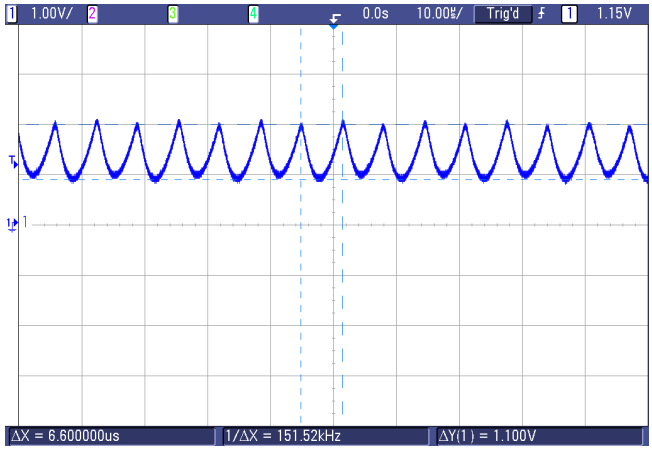


Figure 19. Waveform on CFB With 20 pF

8.2.1.2.4 Setting R_P_MIN and R_P_MAX

Calculating value for R_P_MAX Register : R_P at 8 mm is 12.5 kΩ, 12500 × 2 = 25000. 27.704 kΩ is the nearest value larger than 25 kΩ, which corresponds to the R_P_MAX setting of 0x12 in Table 4.

Calculating value for R_P_MIN Register : R_P at 1 mm is 5 kΩ, 5000 / 2 = 2500. 2.394 kΩ is the nearest value lower than 2.5 kΩ, which corresponds to the R_P_MIN setting of 0x3B in Table 6.

8.2.1.2.5 Calculating Minimum Sensor Frequency

Use Equation 10 to calculate the minimum sensor frequency.

$$M = 68.94 \times \log_{10}\left(\frac{f_{SENSOR}}{2500}\right) \tag{10}$$

In Equation 10, M is 218.96, which rounds to 219 decimal. This value should to be written into Watchdog Timer Register (address 0x03).

The LDC1001 includes a watchdog which monitors the sensor oscillation and flags an error in the STATUS register if no transitions occur on the sensor in a given time window. The time window is controlled by the Min Frequency setting. If the Min Sensor Frequency is programmed for too high a frequency, the watchdog will erroneously indicate that the sensor has stopped oscillating. If the Min Sensor Frequency is set too low, then the LDC1001 will take a longer time to detect if the sensor oscillation has stopped.

Copyright © 2019, Texas Instruments Incorporated

8.2.1.3 Application Curve

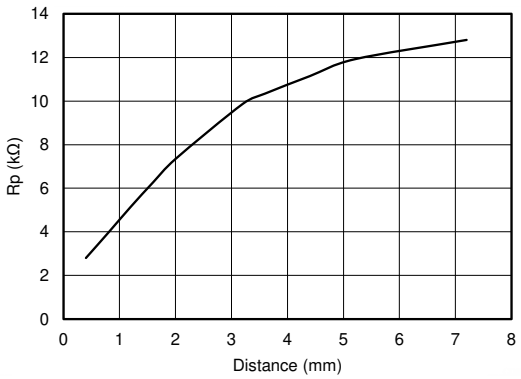


Figure 20. R_P vs Distance

9 Power Supply Recommendations

The LDC1001 is designed to operate from an analog supply range of 4.75 V to 5.25 V and digital I/O supply range of 1.8 V to 5.25 V. The analog supply voltage should be greater than or equal to the digital supply voltage for proper operation of the device. The supply voltage should be well regulated. If the supply is placed more than a few centimeters from the LDC1001, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A capacitor with a value of 10 µF is usually sufficient.

10 Layout

10.1 Layout Guidelines

- The VDD and VIO pin should be bypassed to ground with a low-ESR ceramic bypass capacitor. The typical recommended bypass capacitance is a 0.1-µF ceramic X5R or X7R dielectric capacitor. Some applications may require additional supply bypassing for optimal LDC1001 operation. For these applications, the smallest-valued capacitor should be placed closest to the corresponding supply pin.
- The optimum placement is closest to the VDD/VIO and GND/DGND pins of the device. Take care to minimize the loop area formed by the bypass capacitor connection, the VDD/VIO pin, and the GND/DGND pin of the IC. See Figure 21 for a PCB layout example.
- The CLDO pin should be bypassed to digital ground (DGND) with a 56-nF ceramic bypass capacitor.
- Connect the filter capacitor selected for the application using the procedure described in *Choosing Filter Capacitor (CFA and CFB Pins)* between the two CFA and CFB pins. Place the filter capacitor close to the CFA and CFB pins. Do not use any ground or power plane below the capacitor and the trace connecting the capacitor and the CFA /CFB pins.
- Use separate ground planes for the GND and DGND with a star connection. See Figure 21 for a PCB layout example.
- The sensor capacitor should be a C0G capacitor placed as close as possible to the sensor coil.
- See the *LDC Sensor Design* application report for more details.

Copyright © 2019, Texas Instruments Incorporated

10.2 Layout Example

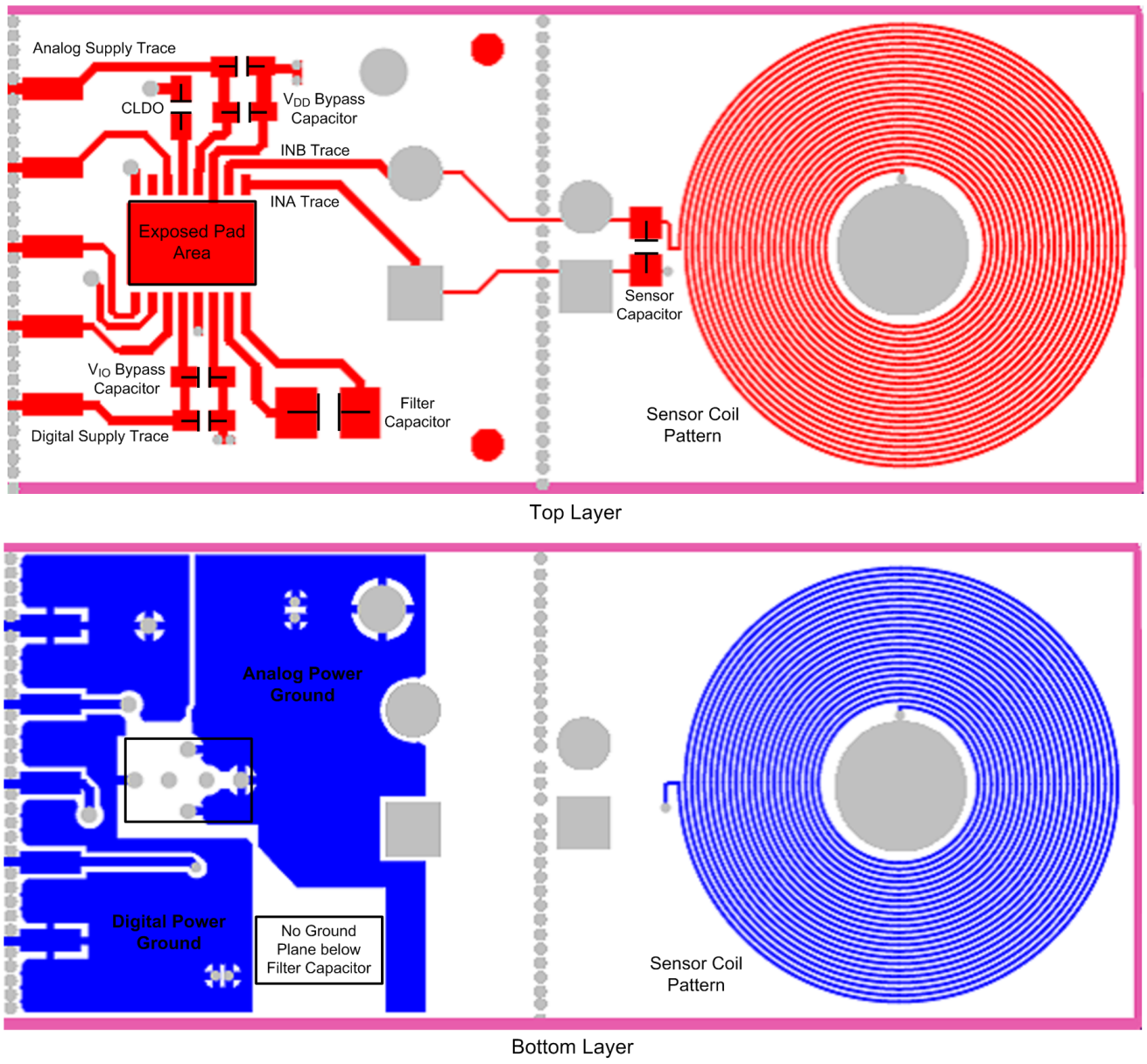


Figure 21. LDC1001 Board Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *Semiconductor and IC Package Thermal Metrics* (SPRA953)
- *LDC Sensor Design* (SNOA930)

11.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Copyright © 2019, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LDC1001NHRR	ACTIVE	WSON	NHR	16	1000	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-40 to 125	LDC1001	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LDC1001 :

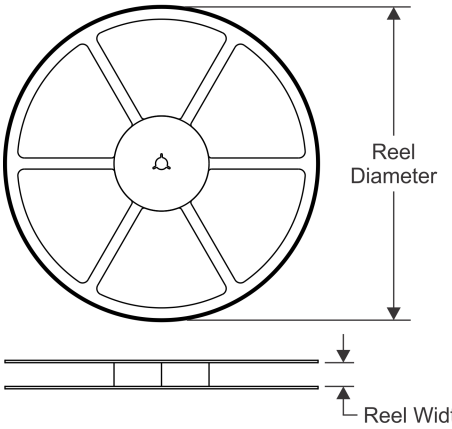
- Automotive: LDC1001-Q1

NOTE: Qualified Version Definitions:

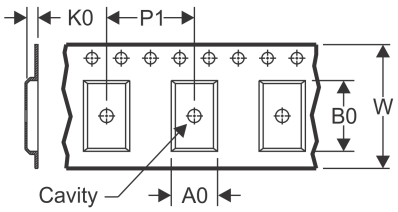
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

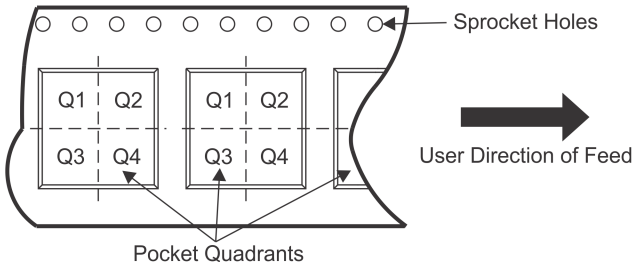


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

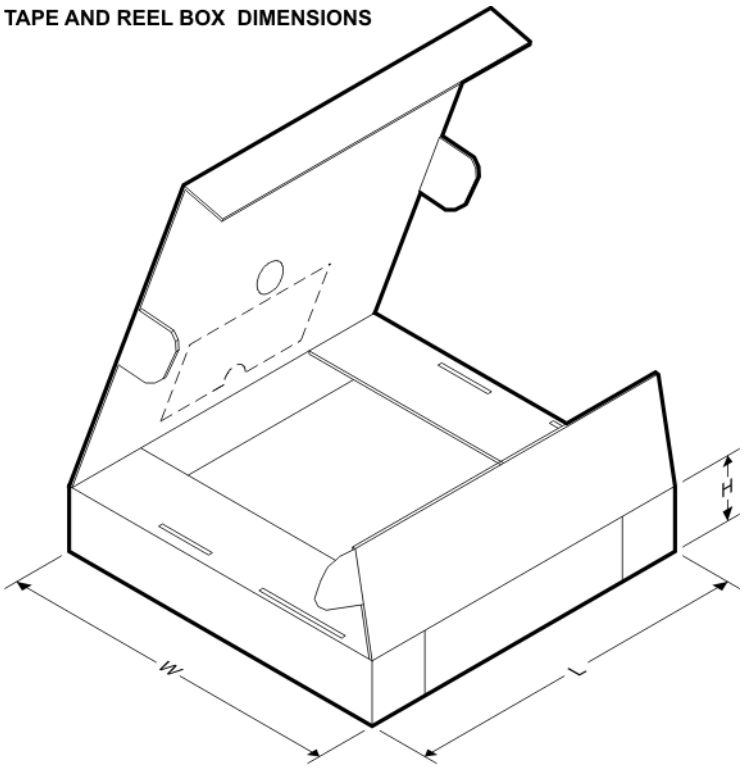
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LDC1001NHRR	WSON	NHR	16	1000	178.0	12.4	4.3	5.3	1.3	8.0	12.0	Q1

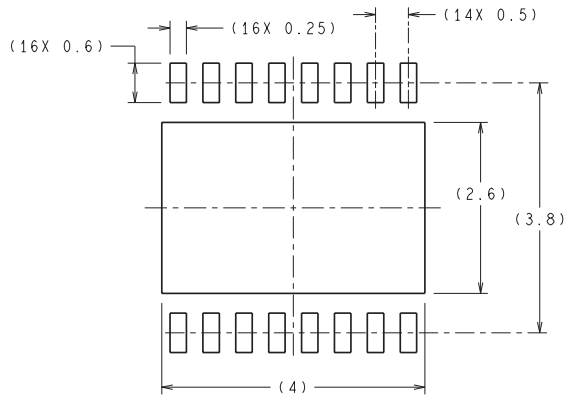
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

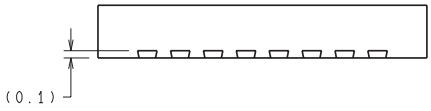
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LDC1001NHRR	WSON	NHR	16	1000	210.0	185.0	35.0

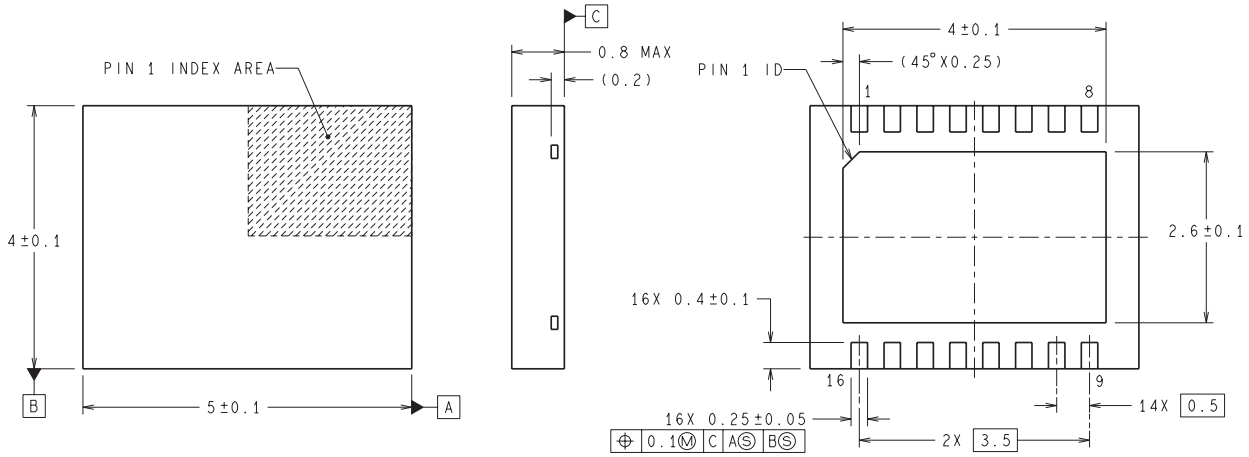
NHR0016B



RECOMMENDED LAND PATTERN

DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY





SDA16B (Rev A)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2020, Texas Instruments Incorporated