

DS25BR110 3.125 Gbps LVDS Buffer with Receive Equalization

Check for Samples: [DS25BR110](#)

FEATURES

- DC - 3.125 Gbps Low Jitter, High Noise Immunity, Low Power Operation
- Four Levels of Receive Equalization Reduce ISI Jitter
- On-Chip 100Ω Input and Output Termination Minimizes Insertion and Return Losses, Reduces Component Count, and Minimizes Board Space
- 7 kV ESD on LVDS I/O Pins Protects Adjoining Components
- Small 3 mm x 3 mm 8-WSON Space Saving Package

APPLICATIONS

- Clock and Data Buffering
- Metallic Cable Equalization
- FR-4 Equalization

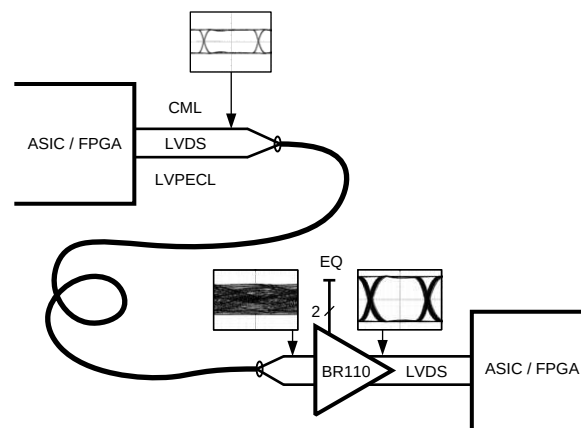
DESCRIPTION

The DS25BR110 is a single channel 3.125 Gbps LVDS buffer optimized for high-speed signal transmission over lossy FR-4 printed circuit board backplanes and balanced metallic cables. A fully differential signal path ensures exceptional signal integrity and noise immunity.

The DS25BR110 features four levels of receive equalization (EQ), making it ideal for use as a receiver device. Other LVDS devices with similar IO characteristics include the following products. The DS25BR120 features four levels of pre-emphasis for use as an optimized driver device, while the DS25BR100 features both pre-emphasis and equalization for use as an optimized repeater device. The DS25BR150 is a buffer/repeater with the lowest power consumption and does not feature transmit pre-emphasis nor receive equalization.

Wide input common mode range allows the receiver to accept signals with LVDS, CML and LVPECL levels; the output levels are LVDS. A very small package footprint requires minimal space on the board while the flow-through pinout allows easy board layout. The differential inputs and outputs are internally terminated with a 100Ω resistor to lower device input and output return losses, reduce component count, and further minimize board space.

Typical Application



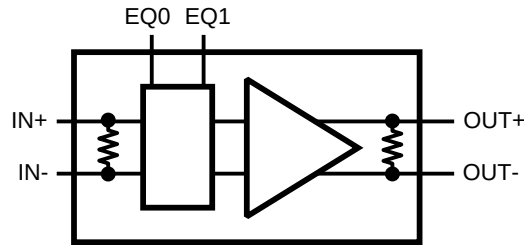
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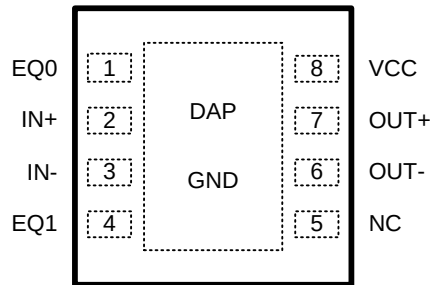
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Block Diagram



Pin Diagram



Pin Descriptions

Pin		Type	Description
Name	Number		
EQ0	1	Input	Equalizer select pin.
IN+	2	Input	Non-inverting LVDS input pin.
IN-	3	Input	Inverting LVDS input pin.
EQ1	4	Input	Equalizer select pin.
NC	5	NA	"NO CONNECT" pin.
OUT-	6	Output	Inverting LVDS output pin.
OUT+	7	Output	Non-inverting LVDS Output pin.
VCC	8	Power	Power supply pin.
GND	DAP	Power	Ground pad (DAP - die attach pad)

Control Pins (EQ0 and EQ1) Truth Tables

EQ1	EQ0	Equalization Level
0	0	Off
0	1	Low (Approx. 4 dB at 1.56 GHz)
1	0	Medium (Approx. 8 dB at 1.56 GHz)
1	1	High (Approx. 16 dB at 1.56 GHz)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})		–0.3V to +4V
LVCMOS Input Voltage (EQ0, EQ1)		–0.3V to ($V_{CC} + 0.3V$)
LVDS Input Voltage (IN+, IN–)		–0.3V to +4V
Differential Input Voltage VID		1.0V
LVDS Output Voltage (OUT+, OUT–)		–0.3V to ($V_{CC} + 0.3V$)
LVDS Differential Output Voltage ((OUT+) – (OUT–))		0V to 1.0V
LVDS Output Short Circuit Current Duration		5 ms
Junction Temperature		+150°C
Storage Temperature Range		–65°C to +150°C
Lead Temperature Range	Soldering (4 sec.)	+260°C
Maximum Package Power Dissipation at 25°C	NGQ0008A Package	2.08W
	Derate NGQ0008A Package	16.7 mW/°C above +25°C
Package Thermal Resistance	θ_{JA}	+60.0°C/W
	θ_{JC}	+12.3°C/W
ESD Susceptibility	HBM ⁽³⁾	≥7 kV
	MM ⁽⁴⁾	≥250V
	CDM ⁽⁵⁾	≥1250V

(1) “Absolute Maximum Ratings” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

(3) Human Body Model, applicable std. JESD22-A114C

(4) Machine Model, applicable std. JESD22-A115-A

(5) Field Induced Charge Device Model, applicable std. JESD22-C101-C

Recommended Operating Conditions

	Min	Typ	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Receiver Differential Input Voltage (V_{ID})			1.0	V
Operating Free Air Temperature (T_A)	–40	+25	+85	°C

DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. ⁽¹⁾⁽²⁾⁽³⁾

Parameter		Test Conditions	Min	Typ	Max	Units
LVCMOS INPUT DC SPECIFICATIONS (EQ0, EQ1)						
V _{IH}	High Level Input Voltage		2.0		V _{CC}	V
V _{IL}	Low Level Input Voltage		GND		0.8	V
I _{IH}	High Level Input Current	V _{IN} = 3.6V V _{CC} = 3.6V		0	±10	μA
I _{IL}	Low Level Input Current	V _{IN} = GND V _{CC} = 3.6V		0	±10	μA
V _{CL}	Input Clamp Voltage	I _{CL} = -18 mA, V _{CC} = 0V		-0.9	-1.5	V
LVDS OUTPUT DC SPECIFICATIONS (OUT+, OUT-)						
V _{OD}	Differential Output Voltage	R _L = 100Ω	250	350	450	mV
ΔV _{OD}	Change in Magnitude of V _{OD} for Complimentary Output States		-35		35	mV
V _{OS}	Offset Voltage	R _L = 100Ω	1.05	1.2	1.375	V
ΔV _{OS}	Change in Magnitude of V _{OS} for Complimentary Output States		-35		35	mV
I _{OS}	Output Short Circuit Current ⁽⁴⁾	OUT to GND		-35	-55	mA
		OUT to V _{CC}		7	55	mA
C _{OUT}	Output Capacitance	Any LVDS Output Pin to GND		1.2		pF
R _{OUT}	Output Termination Resistor	Between OUT+ and OUT-		100		Ω
LVDS INPUT DC SPECIFICATIONS (IN+, IN-)						
V _{ID}	Input Differential Voltage		0		1	V
V _{TH}	Differential Input High Threshold	V _{CM} = +0.05V or V _{CC} -0.05V		0	+100	mV
V _{TL}	Differential Input Low Threshold		-100	0		mV
V _{CMR}	Common Mode Voltage Range	V _{ID} = 100 mV	0.05		V _{CC} - 0.05	V
I _{IN}	Input Current	V _{IN} = 3.6V or 0V V _{CC} = 3.6V or 0V		±1	±10	μA
C _{IN}	Input Capacitance	Any LVDS Input Pin to GND		1.7		pF
R _{IN}	Input Termination Resistor	Between IN+ and IN-		100		Ω
SUPPLY CURRENT						
I _{CC}	Supply Current	EQ0 = 0, EQ1 = 0		35	43	mA

- (1) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or notes. Typical specifications are estimations only and are not ensured
- (2) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground except V_{OD} and ΔV_{OD}.
- (3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured
- (4) Output short circuit current (I_{OS}) is specified as magnitude only, minus sign indicates direction only.

AC Electrical Characteristics⁽¹⁾

Over recommended operating supply and temperature ranges unless otherwise specified.^{(2) (3)}

Parameter		Test Conditions		Min	Typ	Max	Units
LVDS OUTPUT AC SPECIFICATIONS (OUT+, OUT-)							
t _{PHLD}	Differential Propagation Delay High to Low	R _L = 100Ω			350	465	ps
t _{PLHD}	Differential Propagation Delay Low to High				350	465	ps
t _{SKD1}	Pulse Skew t _{PLHD} – t _{PHLD} ⁽⁴⁾				45	100	ps
t _{SKD2}	Part to Part Skew ⁽⁵⁾				45	150	ps
t _{LHT}	Rise Time	R _L = 100Ω			80	150	ps
t _{HLT}	Fall Time				80	150	ps
JITTER PERFORMANCE WITH EQ = OFF							
t _{RJ1A}	Random Jitter (RMS Value) No Test Channels ⁽⁶⁾	V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ) EQ0 = 0, EQ1 = 0	2.5 Gbps		0.5	1	ps
t _{RJ2A}				3.125 Gbps		0.5	1
t _{DJ1A}	Deterministic Jitter (Peak to Peak) No Test Channels ⁽⁷⁾	V _{ID} = 350 mV V _{CM} = 1.2V K28.5 (NRZ) EQ0 = 0, EQ1 = 0	2.5 Gbps		11	40	ps
t _{DJ2A}				3.125 Gbps		11	47
t _{TJ1A}	Total Jitter (Peak to Peak) No Test Channels ⁽⁸⁾	V _{ID} = 350 mV V _{CM} = 1.2V PRBS-23 (NRZ) EQ0 = 0, EQ1 = 0	2.5 Gbps		0.05	0.16	UI _{P-P}
t _{TJ2A}				3.125 Gbps		0.08	0.20
JITTER PERFORMANCE WITH EQ = LOW (Figure 5 and Figure 6)							
t _{RJ1B}	Random Jitter (RMS Value) Test Channel D ⁽⁶⁾	V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ) EQ0 = 1, EQ1 = 0	2.5 Gbps		0.5	1	ps
t _{RJ2B}				3.125 Gbps		0.5	1
t _{DJ1B}	Deterministic Jitter (Peak to Peak) Test Channel D ⁽⁷⁾	V _{ID} = 350 mV V _{CM} = 1.2V K28.5 (NRZ) EQ0 = 1, EQ1 = 0	2.5 Gbps		1	16	ps
t _{DJ2B}				3.125 Gbps		11	31
t _{TJ1B}	Total Jitter (Peak to Peak) Test Channel D ⁽⁸⁾	V _{ID} = 350 mV V _{CM} = 1.2V PRBS-23 (NRZ) EQ0 = 1, EQ1 = 0	2.5 Gbps		0.03	0.09	UI _{P-P}
t _{TJ2B}				3.125 Gbps		0.06	0.14
JITTER PERFORMANCE WITH EQ = MEDIUM (Figure 5 and Figure 6)							
t _{RJ1C}	Random Jitter (RMS Value) Test Channel E ⁽⁶⁾	V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ) EQ0 = 0, EQ1 = 1	2.5 Gbps		0.5	1	ps
t _{RJ2C}				3.125 Gbps		0.5	1
t _{DJ1C}	Deterministic Jitter (Peak to Peak) Test Channel E ⁽⁷⁾	V _{ID} = 350 mV V _{CM} = 1.2V K28.5 (NRZ) EQ0 = 0, EQ1 = 1	2.5 Gbps		10	29	ps
t _{DJ2C}				3.125 Gbps		27	43

(1) Specification is ensured by characterization and is not tested in production.

(2) The Electrical Characteristics tables list ensured specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or notes. Typical specifications are estimations only and are not ensured.

(3) Typical values represent most likely parametric norms for V_{CC} = +3.3V and T_A = +25°C, and at the Recommended Operation Conditions at the time of product characterization and are not ensured.

(4) t_{SKD1}, |t_{PLHD} – t_{PHLD}|, is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

(5) t_{SKD2}, Part to Part Skew, is defined as the difference between the minimum and maximum specified differential propagation delays. This specification applies to devices at the same V_{CC} and within 5°C of each other within the operating temperature range.

(6) Measured on a clock edge with a histogram and an accumulation of 1500 histogram hits. Input stimulus jitter is subtracted geometrically.

(7) Tested with a combination of the 1100000101 (K28.5+ character) and 0011111010 (K28.5- character) patterns. Input stimulus jitter is subtracted algebraically.

(8) Measured on an eye diagram with a histogram and an accumulation of 3500 histogram hits. Input stimulus jitter is subtracted.

AC Electrical Characteristics⁽¹⁾ (continued)Over recommended operating supply and temperature ranges unless otherwise specified.⁽²⁾⁽³⁾

Parameter		Test Conditions		Min	Typ	Max	Units
t _{TJ1C}	Total Jitter (Peak to Peak) Test Channel E ⁽⁸⁾	V _{ID} = 350 mV V _{CM} = 1.2V PRBS-23 (NRZ) EQ0 = 0, EQ1 = 1	2.5 Gbps		0.07	0.12	UI _{P-P}
t _{TJ2C}			3.125 Gbps		0.12	0.17	UI _{P-P}
JITTER PERFORMANCE WITH EQ = HIGH (Figure 5 and Figure 6)							
t _{RJ1D}	Random Jitter (RMS Value) Test Channel F ⁽⁶⁾	V _{ID} = 350 mV V _{CM} = 1.2V Clock (RZ) EQ0 = 1, EQ1 = 1	2.5 Gbps		1.6	2.1	ps
t _{RJ2D}			3.125 Gbps		1.7	2.3	ps
t _{DJ1D}	Deterministic Jitter (Peak to Peak) Test Channel F ⁽⁷⁾	V _{ID} = 350 mV V _{CM} = 1.2V K28.5 (NRZ) EQ0 = 1, EQ1 = 1	2.5 Gbps		30	45	ps
t _{DJ2D}			3.125 Gbps		43	59	ps
t _{TJ1D}	Total Jitter (Peak to Peak) Test Channel F ⁽⁸⁾	V _{ID} = 350 mV V _{CM} = 1.2V PRBS-23 (NRZ) EQ0 = 1, EQ1 = 1	2.5 Gbps		0.14	0.27	UI _{P-P}
t _{TJ2D}			3.125 Gbps		0.19	0.28	UI _{P-P}

DC TEST CIRCUITS

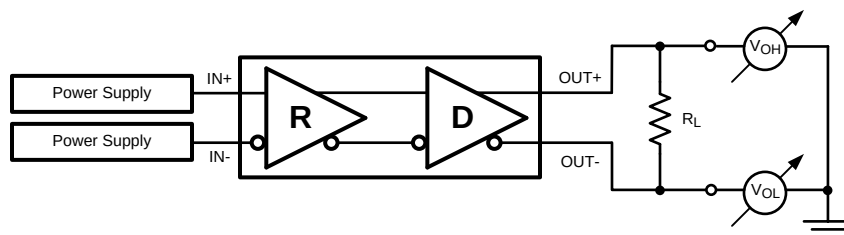


Figure 1. Differential Driver DC Test Circuit

AC Test Circuits and Timing Diagrams

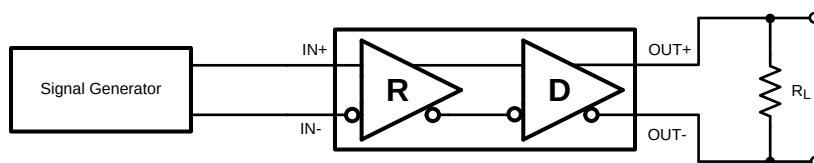


Figure 2. Differential Driver AC Test Circuit

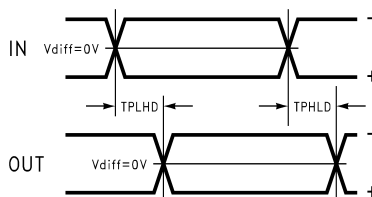


Figure 3. Propagation Delay Timing Diagram

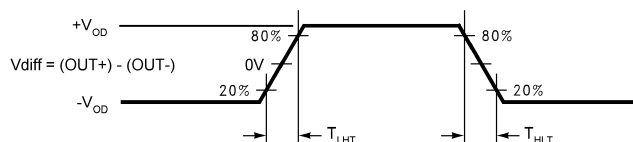


Figure 4. LVDS Output Transition Times

Equalization Test Circuits

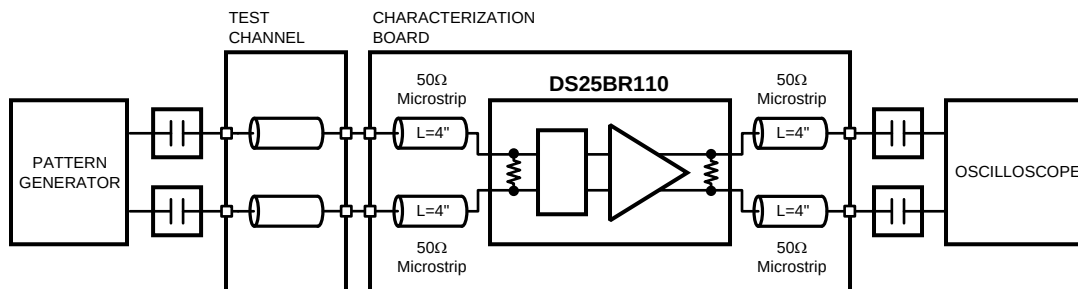


Figure 5. Equalization Performance Test Circuit

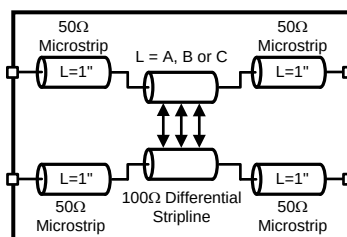


Figure 6. Test Channel Description

Test Channel Loss Characteristics

The test channel was fabricated with Polyclad PCL-FR-370-Laminate/PCL-FRP-370 Prepreg materials (Dielectric constant of 3.7 and Loss Tangent of 0.02). The edge coupled differential striplines have the following geometries: Trace Width (W) = 5 mils, Gap (S) = 5 mils, Height (B) = 16 mils.

Test Channel	Length (inches)	Insertion Loss (dB)					
		500 MHz	750 MHz	1000 MHz	1250 MHz	1500 MHz	1560 MHz
A	10	-1.2	-1.7	-2.0	-2.4	-2.7	-2.8
B	20	-2.6	-3.5	-4.1	-4.8	-5.5	-5.6
C	30	-4.3	-5.7	-7.0	-8.2	-9.4	-9.7
D	15	-1.6	-2.2	-2.7	-3.2	-3.7	-3.8
E	30	-3.4	-4.5	-5.6	-6.6	-7.7	-7.9
F	60	-7.8	-10.3	-12.4	-14.5	-16.6	-17.0

Device Operation

INPUT INTERFACING

The DS25BR110 accepts differential signals and allows simple AC or DC coupling. With a wide common mode range, the DS25BR110 can be DC-coupled with all common differential drivers (i.e., LVPECL, LVDS, CML). The following three figures illustrate typical DC-coupled interface to common differential drivers. Note that the DS25BR110 inputs are internally terminated with a 100Ω resistor.

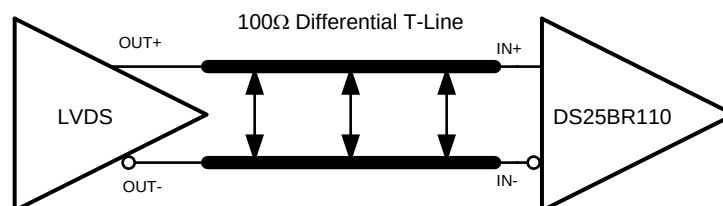


Figure 7. Typical LVDS Driver DC-Coupled Interface to DS25BR110 Input

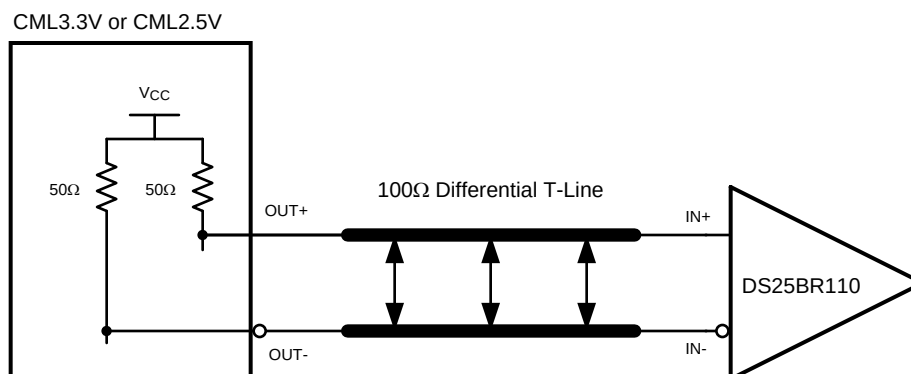


Figure 8. Typical CML Driver DC-Coupled Interface to DS25BR110 Input

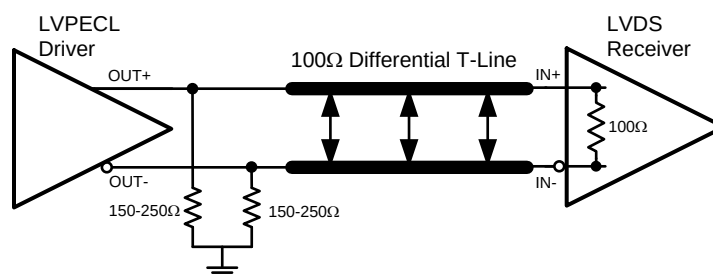


Figure 9. Typical LVPECL Driver DC-Coupled Interface to DS25BR110 Input

OUTPUT INTERFACING

The DS25BR110 outputs signals compliant to the LVDS standard. It can be DC-coupled to most common differential receivers. The following figure illustrates typical DC-coupled interface to common differential receivers and assumes that the receivers have high impedance inputs. While most differential receivers have a common mode input range that can accommodate LVDS compliant signals, it is recommended to check the respective receiver's datasheet prior to implementing the suggested interface implementation.

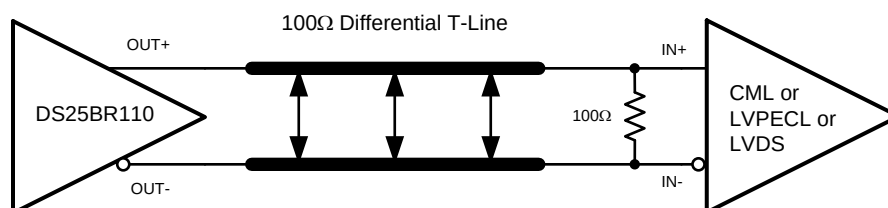


Figure 10. Typical DS25BR110 Output DC-Coupled Interface to an LVDS, CML or LVPECL Receiver

Typical Performance

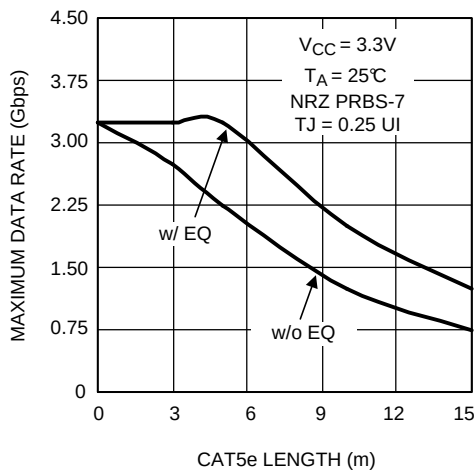


Figure 11. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length

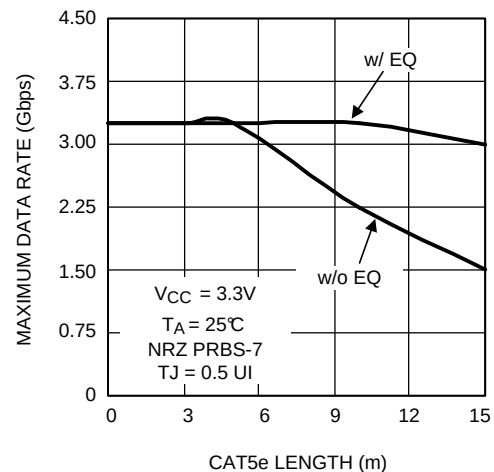
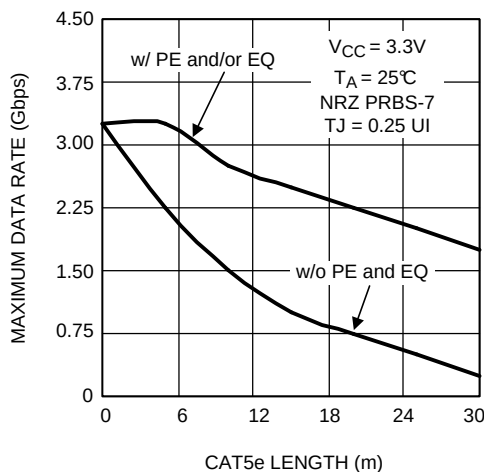


Figure 12. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length



**Figure 13. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length
DS25BR120 Used as a Driver
DS25BR110 Used as a Receiver**

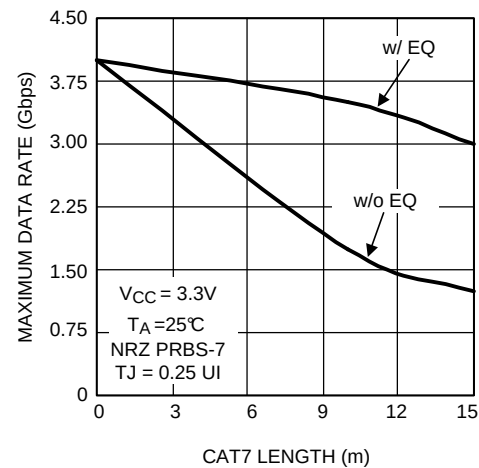
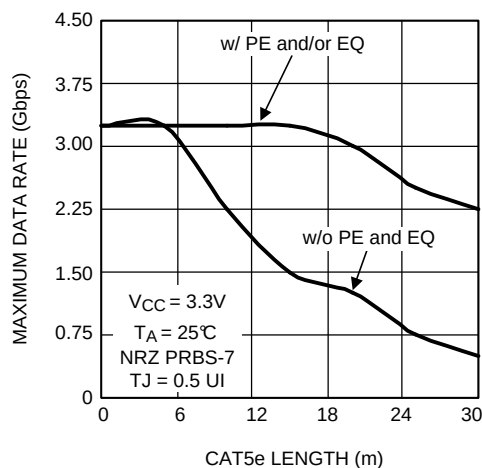


Figure 14. Maximum Data Rate as a Function of CAT7 (Siemon Tera) Length



**Figure 15. Maximum Data Rate as a Function of CAT5e (Belden 1700A) Length
DS25BR120 Used as a Driver
DS25BR110 Used as a Receiver**

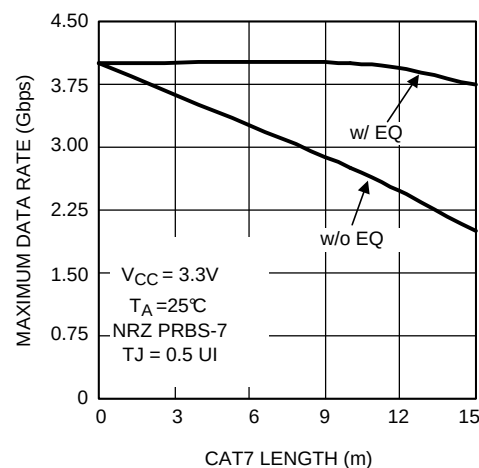
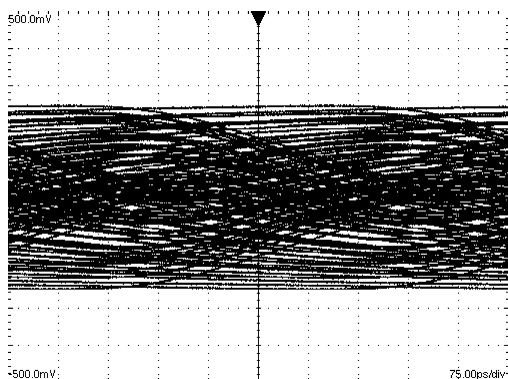
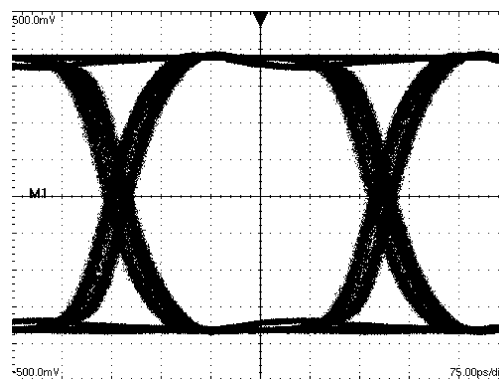


Figure 16. Maximum Data Rate as a Function of CAT7 (Slemon Tera) Length

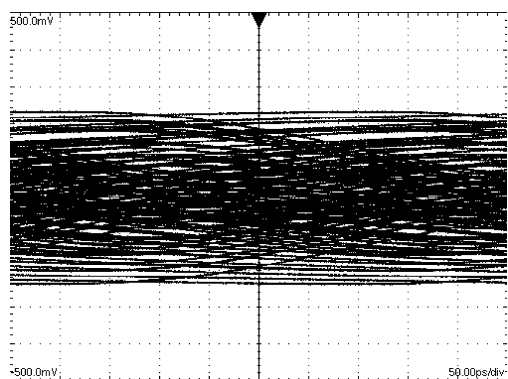
Typical Performance (continued)



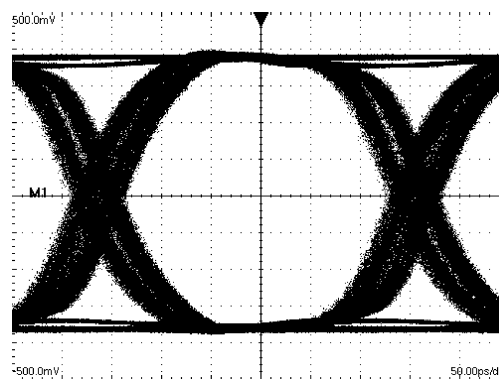
**Figure 17. A 2.5 Gbps NRZ PRBS-7 After 70"
Differential FR-4 Stripline
V:100 mV / DIV, H:75 ps / DIV**



**Figure 18. An Equalized 2.5 Gbps NRZ PRBS-7 After 70"
Differential FR-4 Stripline
V:100 mV / DIV, H:75 ps / DIV**



**Figure 19. A 3.125 Gbps NRZ PRBS-7 After 70"
Differential FR-4 Stripline
V:100 mV / DIV, H:50 ps / DIV**



**Figure 20. An Equalized 3.125 Gbps NRZ PRBS-7 After 70"
Differential FR-4 Stripline
V:100 mV / DIV, H:50 ps / DIV**

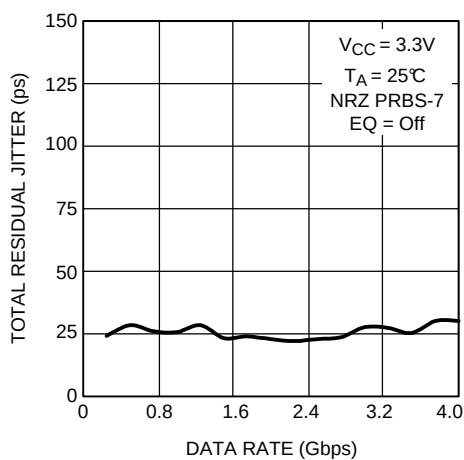


Figure 21. Total Jitter as a Function of Data Rate

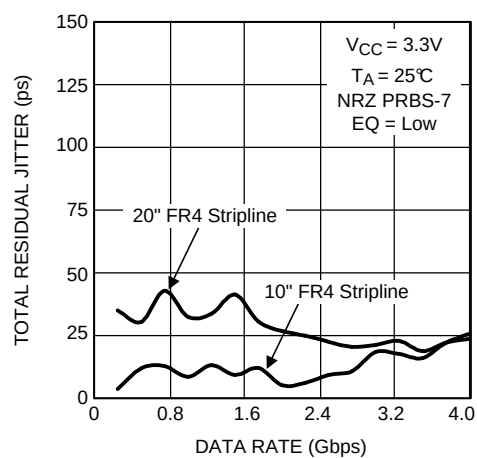


Figure 22. Total Jitter as a Function of Data Rate

Typical Performance (continued)

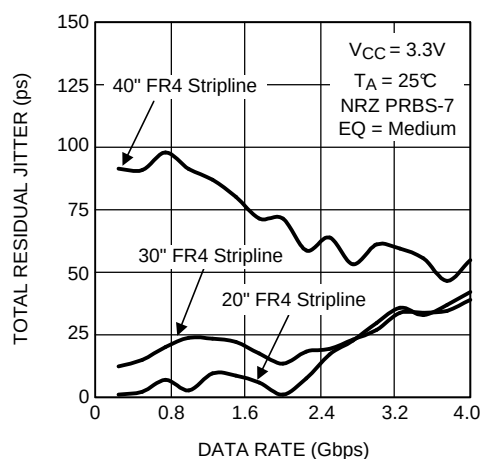


Figure 23. Total Jitter as a Function of Data Rate

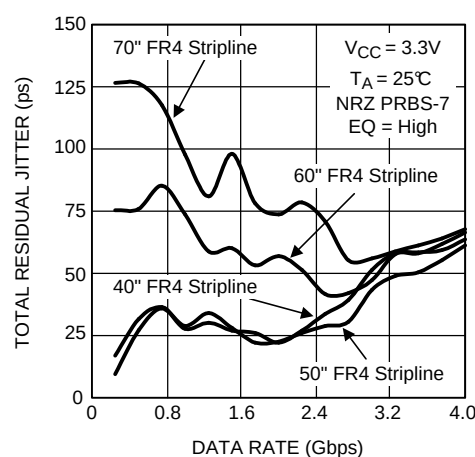


Figure 24. Total Jitter as a Function of Data Rate

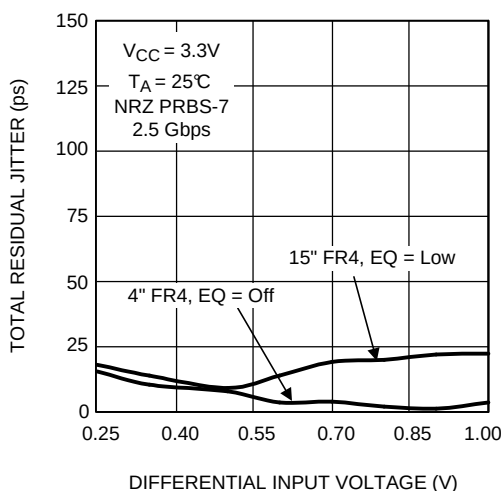


Figure 25. Total Jitter as a Function of Input Amplitude

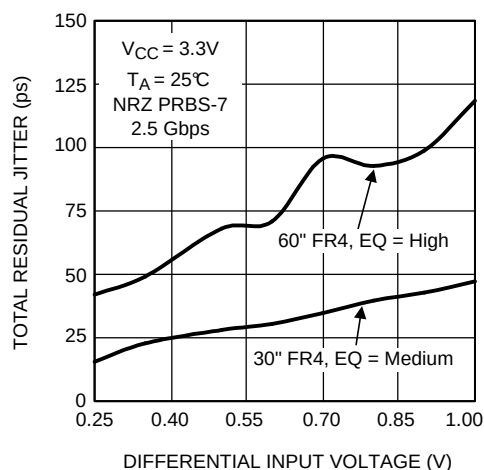


Figure 26. Total Jitter as a Function of Input Amplitude

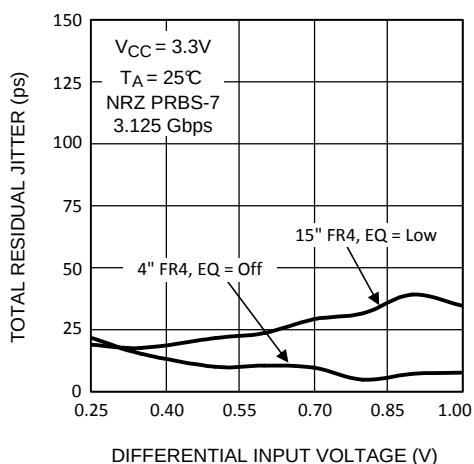


Figure 27. Total Jitter as a Function of Input Amplitude

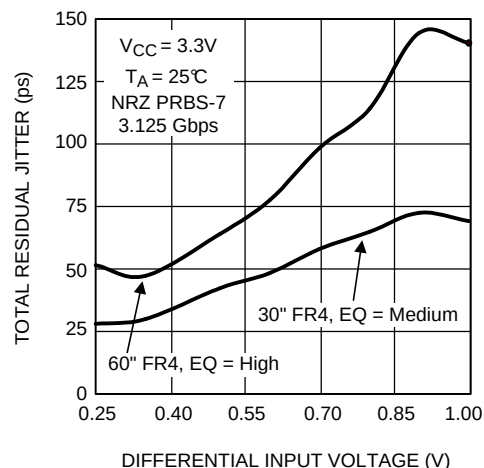


Figure 28. Total Jitter as a Function of Input Amplitude

REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS25BR110TSD/NOPB	ACTIVE	WS0N	NGQ	8	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	2R110	Samples
DS25BR110TSDX/NOPB	ACTIVE	WS0N	NGQ	8	4500	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	-40 to 85	2R110	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

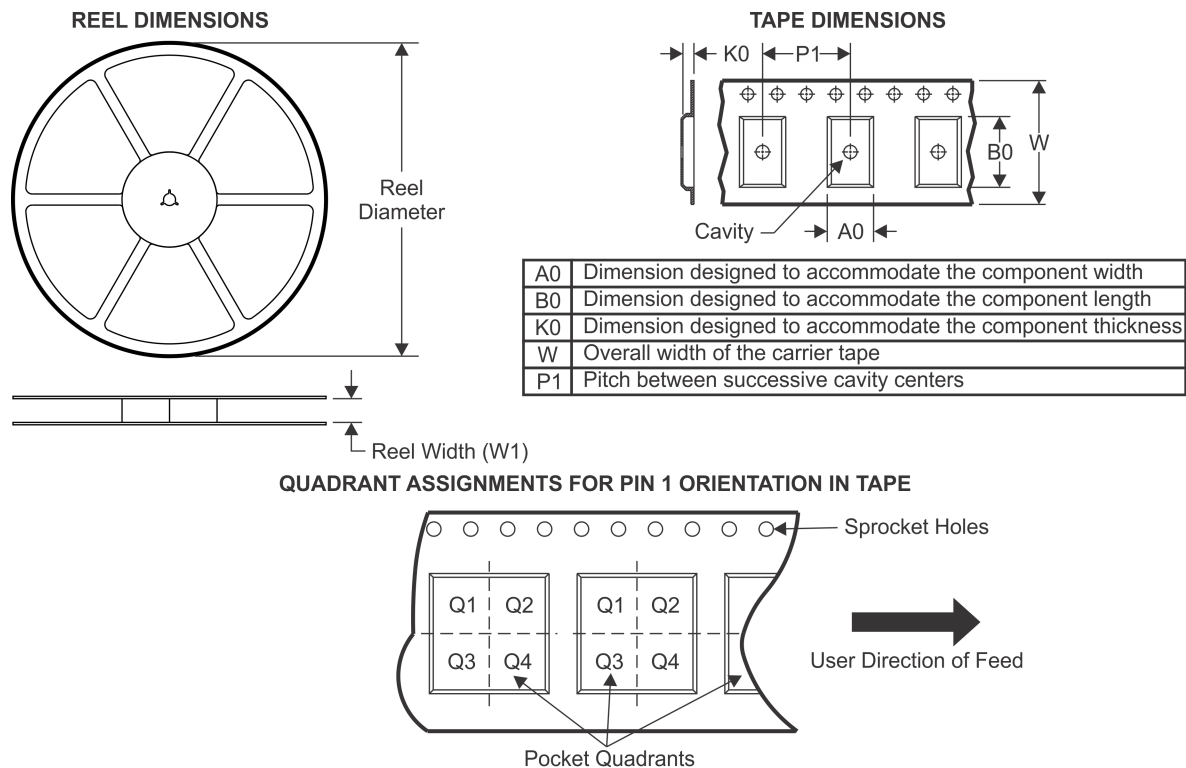
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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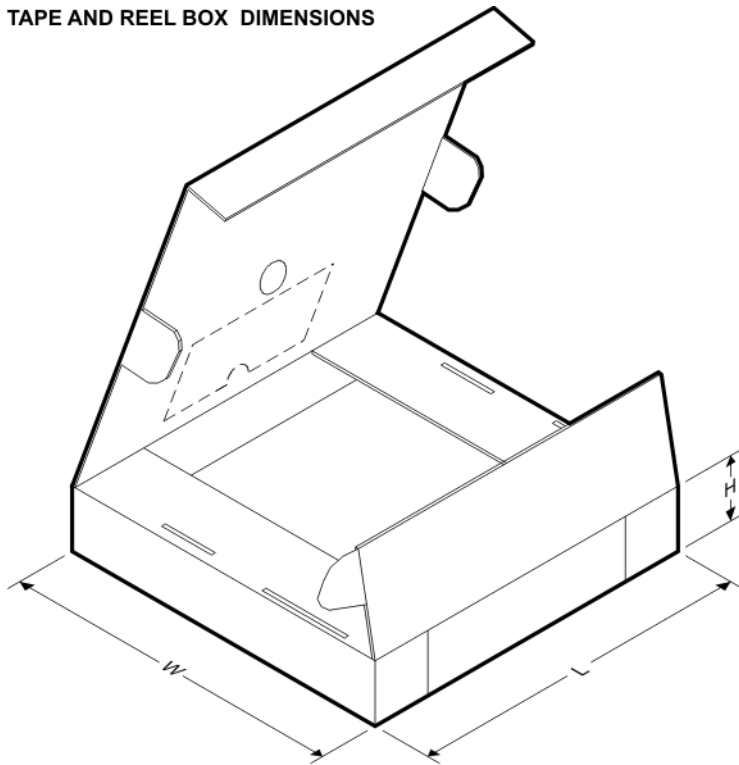
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS25BR110TSD/NOPB	WSO	NGQ	8	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
DS25BR110TSDX/NOPB	WSO	NGQ	8	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

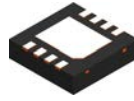
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS25BR110TSD/NOPB	WSO	NGQ	8	1000	210.0	185.0	35.0
DS25BR110TSDX/NOPB	WSO	NGQ	8	4500	367.0	367.0	35.0

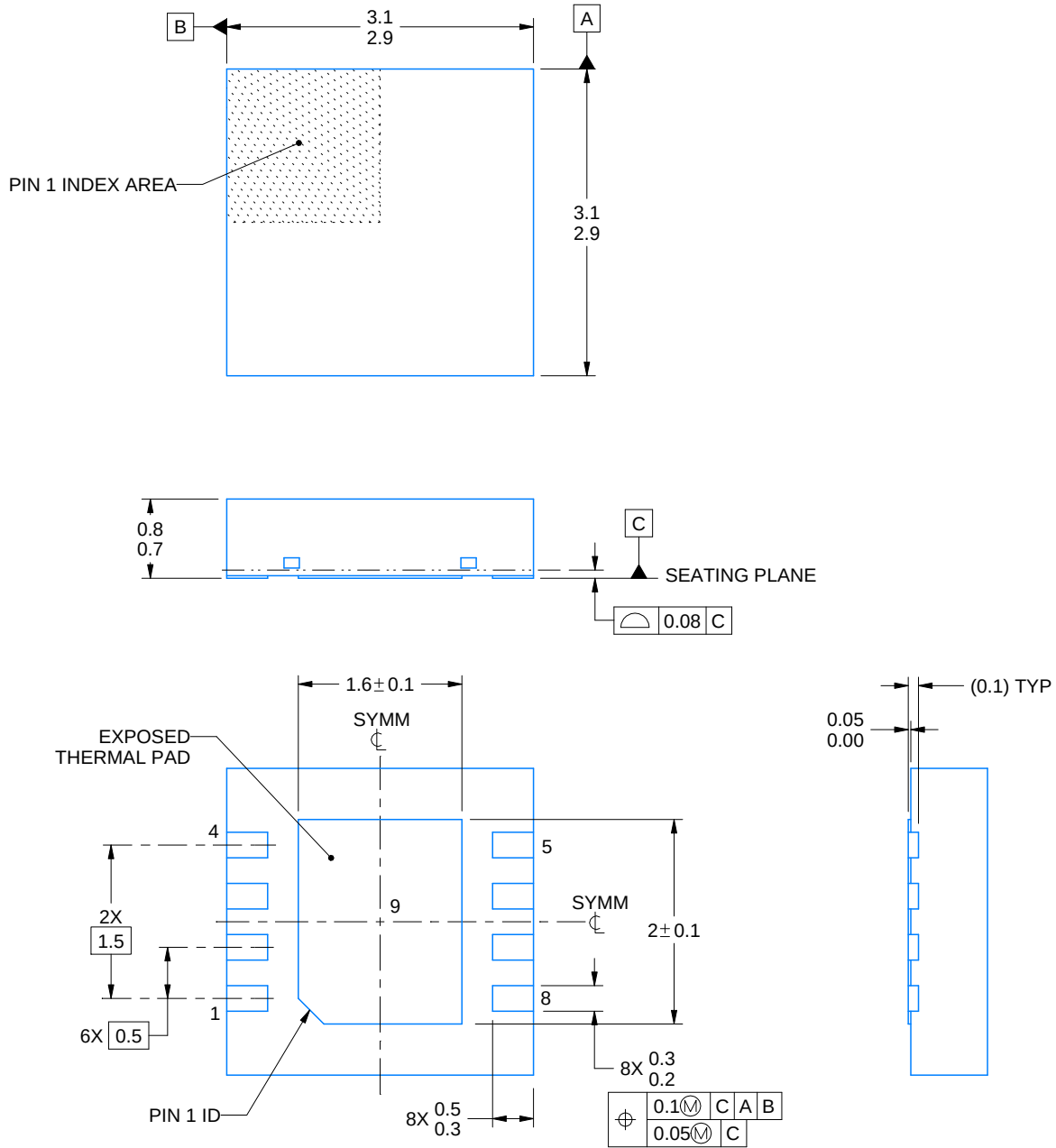
NGQ0008A



PACKAGE OUTLINE

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4214922/A 03/2018

NOTES:

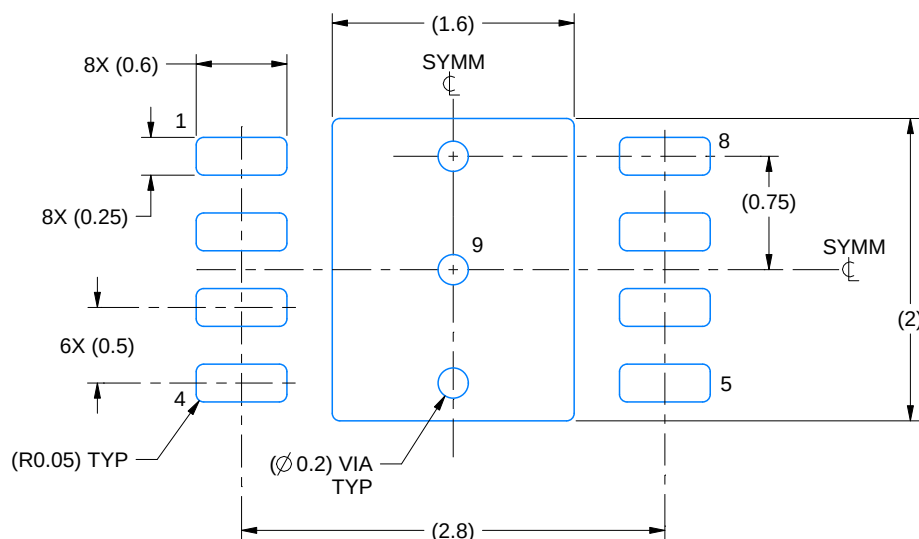
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

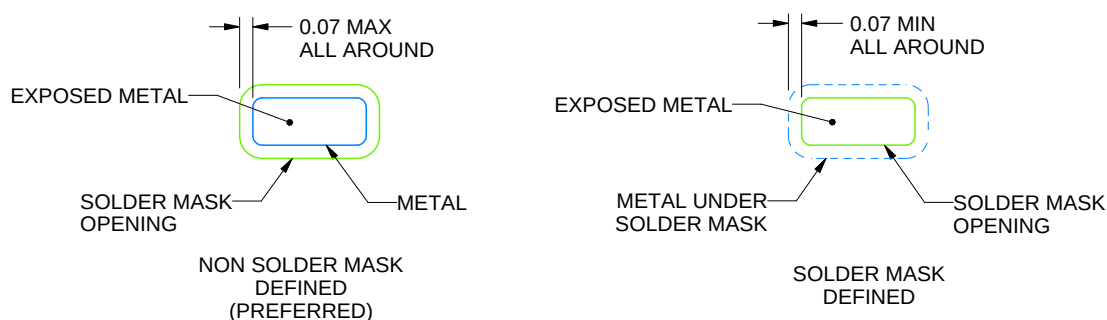
NGQ0008A

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

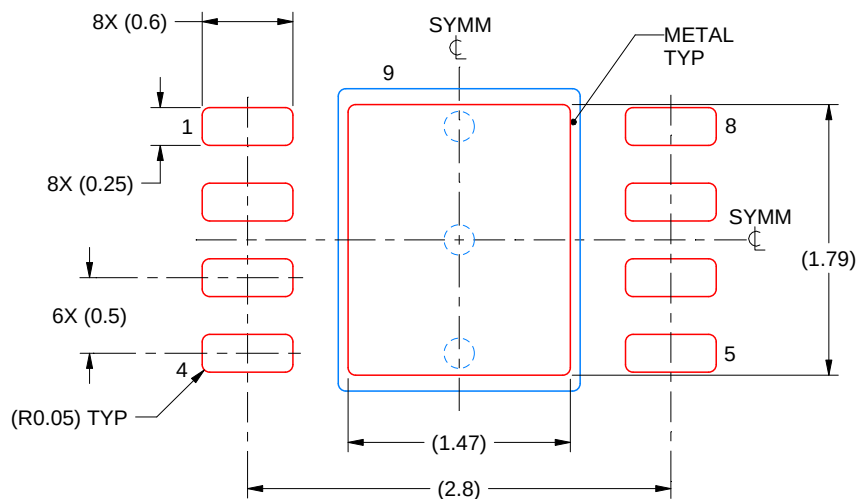
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

NGQ0008A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214922/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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