

## MAX98400A/MAX98400B

## Stereo, High-Power, Class D Amplifiers

### General Description

The MAX98400A/MAX98400B Class D amplifiers provide high-performance, thermally efficient amplifier solutions. The MAX98400A delivers 2x20W into 8Ω loads or 1x40W into a 4Ω load. The MAX98400B delivers 2x12W into 8Ω loads.

An integrated limiting circuit prevents output clipping distortion, protects small speakers from transient voltages, and reduces power dissipation.

A thermal-foldback feature can be enabled to automatically reduce the output power at above a junction temperature of +120°C. Traditional thermal protection is also available in addition to robust overcurrent protection.

The ICs operate from a single 8V to 28V supply and provide a high 67dB PSRR, eliminating the need for a regulated power supply. They offer up to 90% efficiency from a 12V supply.

Filterless modulation allows the ICs to pass EN55022B EMI limits with 1m cables using only a low-cost ferrite bead and small-value capacitor on each output.

Both devices feature eight digitally controlled gain settings.

Comprehensive click-and-pop reduction circuitry minimizes noise coming into and out of shutdown.

The MAX98400A/MAX98400B are available in 36-pin and 24-pin TQFN packages, respectively, and are specified over the -40°C to +85°C temperature range.

### Features

- Wide 8V to 28V Supply Voltage Range
- Single-Supply Operation
- Low EMI: Active Emissions Limiting
- Clipping Limiter
- Low Quiescent Current
- Thermal Foldback
- Thermal and Overcurrent Protection

### Applications

- LCD/PDP Televisions
- LCD Monitors
- MP3 Docking Stations
- Notebook PCs

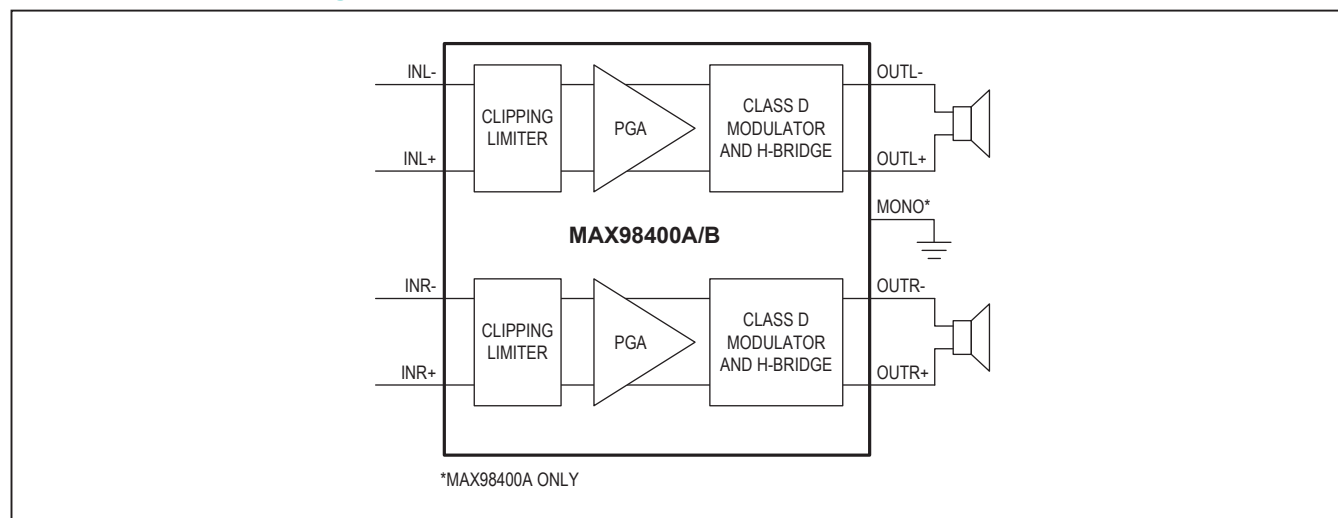
### Ordering Information

| PART                 | PIN-PACKAGE | SPEC  |
|----------------------|-------------|-------|
| <b>MAX98400AETX+</b> | 36 TQFN-EP* | 2x20W |
| <b>MAX98400BETG+</b> | 24 TQFN-EP* | 2x12W |

**Note:** Devices operate over the -40°C to +85°C temperature range.

\*EP = Exposed pad.

### Simplified Block Diagram



---

**TABLE OF CONTENTS**

---

|                                                   |    |
|---------------------------------------------------|----|
| Absolute Maximum Ratings . . . . .                | 4  |
| Electrical Characteristics . . . . .              | 4  |
| Typical Operating Characteristics . . . . .       | 7  |
| Pin Configurations . . . . .                      | 12 |
| Pin Descriptions . . . . .                        | 12 |
| Stereo Configuration for MAX98400A . . . . .      | 14 |
| Mono Configuration for MAX98400A . . . . .        | 15 |
| Detailed Description . . . . .                    | 15 |
| Efficiency . . . . .                              | 16 |
| Shutdown . . . . .                                | 16 |
| Click-and-Pop Suppression . . . . .               | 16 |
| Mono Configuration . . . . .                      | 16 |
| Clipping Limiter . . . . .                        | 16 |
| Limiter Threshold Control (LIM_TH) . . . . .      | 17 |
| Release Time Control (RELEASE) . . . . .          | 17 |
| Preamplifier Gain Setting . . . . .               | 18 |
| Protection . . . . .                              | 18 |
| Thermal Foldback . . . . .                        | 18 |
| Overtemperature Protection . . . . .              | 18 |
| Overcurrent Protection . . . . .                  | 18 |
| Applications Information . . . . .                | 18 |
| Filterless Class D Operation . . . . .            | 18 |
| Inductor-Based Output Filters . . . . .           | 19 |
| Component Selection . . . . .                     | 19 |
| Input Capacitor . . . . .                         | 19 |
| Power Supplies . . . . .                          | 19 |
| Internal Regulator Vs . . . . .                   | 19 |
| Supply Bypassing, Layout, and Grounding . . . . . | 19 |
| Chip Information . . . . .                        | 19 |
| Functional Diagrams . . . . .                     | 20 |
| Package Information . . . . .                     | 22 |
| Revision History . . . . .                        | 26 |

| LIST OF FIGURES                                                    |    |
|--------------------------------------------------------------------|----|
| Figure 1. MAX98400B EMI Performance . . . . .                      | 18 |
| Figure 2. MAX98400A Efficiency vs. Class AB Efficiency . . . . .   | 18 |
| Figure 3. Limiter Control, Mode3 Configuration (Table 1) . . . . . | 19 |
| Figure 4. Output Filter for PWM Mode . . . . .                     | 21 |

| LIST OF TABLES                                |    |
|-----------------------------------------------|----|
| Table 1. Limiter Control Modes . . . . .      | 19 |
| Table 2. Gain Selection . . . . .             | 20 |
| Table 3. Filter Component Selection . . . . . | 21 |

## Absolute Maximum Ratings

|                                                                            |                                     |
|----------------------------------------------------------------------------|-------------------------------------|
| PVDD to PGND                                                               | -0.3V to +30V                       |
| V <sub>S</sub> to GND                                                      | -0.3V to +6V                        |
| SHDN, MONO to GND                                                          | -0.3V to +6V                        |
| IN <sub>-</sub> to GND                                                     | -0.3V to +6V                        |
| G1, G2, RELEASE, TEMPLOCK,<br>LIM_TH to GND                                | -0.3V to (V <sub>S</sub> + 0.3V)    |
| OUT <sub>-</sub> to PGND                                                   | -0.3V to (V <sub>PVDD</sub> + 0.3V) |
| PGND to GND                                                                | -0.3V to +0.3V                      |
| Continuous Current into OUT <sub>-</sub>                                   | +2.4A                               |
| Continuous Current into PVDD, PGND                                         | +4.8A                               |
| Continuous Current into All Other Pins                                     | +10mA                               |
| Duration of OUT <sub>-</sub> Short Circuit to PVDD or PGND ... Continuous  |                                     |
| Duration of Short Circuit Between<br>OUT <sub>+</sub> and OUT <sub>-</sub> | Continuous                          |

|                                                                |                 |
|----------------------------------------------------------------|-----------------|
| Continuous Power Dissipation (T <sub>A</sub> = +70°C)          |                 |
| 36-Pin TQFN Multilayer Board<br>(derate 35.7mW/°C above +70°C) | 2857.1mW        |
| θ <sub>JA</sub> (Note 1)                                       | 28°C/W          |
| θ <sub>JC</sub> (Note 1)                                       | 1°C/W           |
| 24-Pin TQFN Multilayer Board<br>(derate 27.8mW/°C above +70°C) | 35.7mW          |
| θ <sub>JA</sub> (Note 1)                                       | 36°C/W          |
| θ <sub>JC</sub> (Note 1)                                       | 3°C/W           |
| Junction Temperature                                           | +150°C          |
| Operating Temperature Range                                    | -40°C to +85°C  |
| Storage Temperature Range                                      | -65°C to +150°C |
| Lead Temperature (soldering, 10s)                              | +300°C          |
| Soldering Temperature (reflow)                                 | +260°C          |

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Electrical Characteristics

(V<sub>PVDD</sub> = 18V, C<sub>IN</sub> = 1μF, V<sub>SHDN</sub> = 5V, LIM\_TH = V<sub>S</sub>, TEMPLOCK = unconnected; G1 = GND, G2 = open (gain = 20.1dB), C<sub>REL</sub> = 1μF, C1 = C2 = 1μF, R<sub>L</sub> = ∞, AC measurement bandwidth 20Hz to 20kHz, differential input signal, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted. Typical values are at T<sub>A</sub> = +25°C.) (Notes 2, 3)

| PARAMETER                               | SYMBOL                 | CONDITIONS                                                               | MIN  | TYP  | MAX  | UNITS            |
|-----------------------------------------|------------------------|--------------------------------------------------------------------------|------|------|------|------------------|
| <b>AMPLIFIER DC CHARACTERISTICS</b>     |                        |                                                                          |      |      |      |                  |
| PVDD Supply Voltage Range               | V <sub>PVDD</sub>      | Inferred from PVDD_PSR                                                   | 8    |      | 28   | V                |
| V <sub>S</sub> Supply Input Voltage     | V <sub>S</sub>         | Inferred from I <sub>VS</sub> test                                       | 4.75 |      | 5.5  | V                |
| Quiescent Current                       | I <sub>PVDD</sub>      | Dual-supply mode:<br>V <sub>S</sub> = 4.75V, T <sub>A</sub> = +25°C      |      | 10   | 15   | mA               |
|                                         | I <sub>VS</sub>        |                                                                          |      | 6    | 8.2  |                  |
| Single-Supply<br>Quiescent Current      | I <sub>PVDD</sub>      | Single-supply mode:<br>T <sub>A</sub> = +25°C                            |      | 16   | 23   | mA               |
|                                         |                        | R <sub>L</sub> = 8Ω (Note 3)                                             |      | 17   |      |                  |
| Shutdown Current                        | I <sub>SHDN_PVDD</sub> | V <sub>SHDN</sub> = 0V, T <sub>A</sub> = +25°C,<br>V <sub>S</sub> = 5.5V |      | 8    | 20   | μA               |
|                                         | I <sub>SHDN_VS</sub>   |                                                                          |      | 3    | 10   |                  |
| PVDD Undervoltage Lockout               | V <sub>UVLO</sub>      |                                                                          |      | 7    | 7.9  | V                |
| V <sub>S</sub> Regulator Output Voltage | V <sub>S</sub>         |                                                                          | 4.2  | 4.47 | 4.75 | V                |
| <b>INPUT STAGE</b>                      |                        |                                                                          |      |      |      |                  |
| Differential Input Voltage Range        |                        |                                                                          |      |      | 2    | V <sub>RMS</sub> |
| Single-Ended Input Voltage<br>Range     |                        |                                                                          |      |      | 1    | V <sub>RMS</sub> |
| Common-Mode Rejection Ratio             | CMRR                   |                                                                          |      | 60   |      | dB               |
| Input Resistance                        |                        | Differential V <sub>LIM_TH</sub> = 0V, gain = +35dB                      | 20   | 32   |      | kΩ               |

## Electrical Characteristics (continued)

(VPVDD = 18V, CIN = 1μF, VSHDN = 5V, LIM\_TH = VS, TEMPLOCK = unconnected; G1 = GND, G2 = open (gain = 20.1dB), CREL = 1μF, C1 = C2 = 1μF, RL = ∞, AC measurement bandwidth 20Hz to 20kHz, differential input signal, TA = TMIN to TMAX, unless otherwise noted. Typical values are at TA = +25°C.) (Notes 2, 3)

| PARAMETER                            | SYMBOL   | CONDITIONS                                                      | MIN  | TYP  | MAX | UNITS |
|--------------------------------------|----------|-----------------------------------------------------------------|------|------|-----|-------|
| <b>POWER STAGE</b>                   |          |                                                                 |      |      |     |       |
| Shutdown to Full Operation           | tSON     |                                                                 |      | 11   |     | ms    |
| Gain Accuracy                        |          |                                                                 | ±0.8 | ±4   |     | %     |
| Left-to-Right Gain Matching          |          | All gain settings                                               |      | ±2   |     | %     |
| Crosstalk                            |          | 1kHz                                                            |      | -85  |     | dB    |
|                                      |          | 10kHz                                                           |      | -68  |     |       |
| Output Offset Voltage                | VOS      | TA = +25°C                                                      | ±8   | ±45  |     | mV    |
| Click-and-Pop Level                  | KCP      | Peak voltage, 32 samples/s, A-weighted, TA = +25°C (Notes 4, 5) |      | -47  |     | dBV   |
|                                      |          | Into shutdown<br>Out of shutdown                                |      | -56  |     |       |
| PVDD Power-Supply Rejection Ratio    | PSRRPVDD | VPVDD = 8V to 28V                                               | 52   | 63   |     | dB    |
|                                      |          | 1kHz, 100mVp-p ripple                                           |      | 67   |     |       |
|                                      |          | 10kHz, 100mVp-p ripple                                          |      | 57   |     |       |
| VS Power-Supply Rejection Ratio      | PSRRVS   | VS = 4.75V to 5.5V                                              | 39   | 55   |     | dB    |
|                                      |          | 1kHz, 100mVp-p ripple                                           |      | 50   |     |       |
|                                      |          | 10kHz, 100mVp-p ripple                                          |      | 40   |     |       |
| MAX98400A Output Power               | POUT     | Stereo, RL = 8Ω, 10% THD+N, fIN = 1kHz (Note 3)                 |      | 22   |     | W     |
|                                      |          | Mono, RL = 4Ω, 10% THD+N, fIN = 1kHz (Note 3)                   |      | 44   |     |       |
| MAX98400B Output Power               | POUT     | Stereo, RL = 8Ω, 10% THD+N, fIN = 1kHz (Note 3)                 |      | 15   |     |       |
| Total Harmonic Distortion Plus Noise | THD+N    | POUT = 0.1W to POUT/2, fIN = 20Hz to 20kHz, RL = 8Ω             |      | 0.3  |     | %     |
|                                      |          | POUT/2, fIN = 1kHz, RL = 8Ω                                     |      | 0.03 |     |       |
| Output Noise                         | VN       | A-weighted                                                      |      | 100  |     | μVRMS |
| Efficiency                           | η        | POUT = 2x20W, RL = 8Ω (MAX98400A)<br>fIN = 1kHz (Note 3)        |      | 90   |     | %     |
| Current Limit                        | ILIM     |                                                                 | 3.5  | 5    |     | A     |
| Output FET Resistance                | RDSON    |                                                                 |      | 0.4  |     | Ω     |
| Switching Frequency                  | fsw      |                                                                 | 265  | 330  | 395 | kHz   |
| Peak Output Voltage                  |          | VPVDD = 28V                                                     | 20   | 26   |     | V     |
| <b>LIMITER</b>                       |          |                                                                 |      |      |     |       |
| Attack Time                          |          | V LIM_TH = 0V                                                   |      | 240  | 500 | μs    |
| Release Time                         |          | V LIM_TH = 0V                                                   |      | 0.8  |     | s     |
| Maximum Trigger Level                |          | VPVDD = 14V (Note 6)                                            | 4    |      |     | dBFS  |
| Minimum Trigger Level                |          | (Note 7)                                                        |      |      | -6  | dBFS  |
| Trigger Level                        |          | V LIM_TH = 0V                                                   | -1   | 0    | +1  | dBFS  |
| Compression Range                    |          | V LIM_TH = 0V                                                   | -12  |      |     | dB    |

## Electrical Characteristics (continued)

( $V_{PVDD} = 18V$ ,  $C_{IN} = 1\mu F$ ,  $\overline{SHDN} = 5V$ ,  $LIM\_TH = V_S$ ,  $TEMPLOCK = \text{unconnected}$ ;  $G1 = GND$ ,  $G2 = \text{open}$  (gain = 20.1dB),  $C_{REL} = 1\mu F$ ,  $C1 = C2 = 1\mu F$ ,  $R_L = \infty$ , AC measurement bandwidth 20Hz to 20kHz, differential input signal,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .) (Notes 2, 3)

| PARAMETER                                                                | SYMBOL    | CONDITIONS                                      | MIN               | TYP              | MAX               | UNITS      |
|--------------------------------------------------------------------------|-----------|-------------------------------------------------|-------------------|------------------|-------------------|------------|
| VGA Distortion                                                           |           | Compression = 0 to -12dB                        |                   | 3.5              |                   | %          |
| LIM_TH Input-Voltage Low (PVDD Tracking)                                 |           |                                                 | 0.15              |                  |                   | V          |
| LIM_TH Input-Voltage High (Limiter Off)                                  |           |                                                 |                   |                  | $V_S$<br>- 1      | V          |
| Channel-to-Channel Attenuation Tracking                                  |           |                                                 |                   | $\pm 1$          |                   | dB         |
| <b>THERMAL FOLDBACK</b>                                                  |           |                                                 |                   |                  |                   |            |
| Internal Templock Resistor                                               |           |                                                 | 120               | 205              | 310               | k $\Omega$ |
| Trigger Temperature                                                      |           |                                                 |                   | +130             |                   | $^\circ C$ |
| Hard Thermal Protection                                                  |           |                                                 |                   | +165             |                   | $^\circ C$ |
| <b>LOGIC INPUT (G1, G2)</b>                                              |           |                                                 |                   |                  |                   |            |
| Sink Current                                                             |           | $T_A = +25^\circ C$ , $V_{G1}$ , $V_{G2} = 0V$  | +2.5              | +5               | +8                | $\mu A$    |
| Source Current                                                           |           | $T_A = +25^\circ C$ , $V_{G1}$ , $V_{G2} = V_S$ | -8                | -5               | -2.5              | $\mu A$    |
| Input High Threshold                                                     |           |                                                 |                   |                  | $0.8 \times V_S$  | V          |
| Input Low Threshold                                                      |           |                                                 | $0.3 \times V_S$  |                  |                   | V          |
| Input Three-State Window                                                 |           |                                                 | $0.45 \times V_S$ | $0.5 \times V_S$ | $0.55 \times V_S$ | V          |
| <b>LOGIC INPUT (<math>\overline{SHDN}</math>, MONO (MAX98400A Only))</b> |           |                                                 |                   |                  |                   |            |
| Input Leakage Current                                                    | $I_{IN}$  | $T_A = +25^\circ C$                             |                   |                  | $\pm 10$          | $\mu A$    |
| Input High Threshold                                                     | $V_{INH}$ |                                                 | 2                 |                  |                   | V          |
| Input Low Threshold                                                      | $V_{INL}$ |                                                 |                   |                  | 0.4               | V          |
| Input-Voltage Hysteresis                                                 |           |                                                 |                   | 100              |                   | mV         |

**Note 2:** 100% production tested at  $T_A = +25^\circ C$ . Specifications over temperature limits are guaranteed by design.

**Note 3:** The MAX98400A stereo mode is specified with an 8 $\Omega$  resistive load in series with a 68 $\mu H$  inductive load connected across BTL outputs. The MAX98400A mono mode is specified with a 4 $\Omega$  resistive load in series with 33 $\mu H$  inductive load. The MAX98400B is specified with an 8 $\Omega$  resistive load in series with a 68 $\mu H$  inductive load connected across BTL outputs.

**Note 4:** Amplifier inputs AC-coupled to GND.

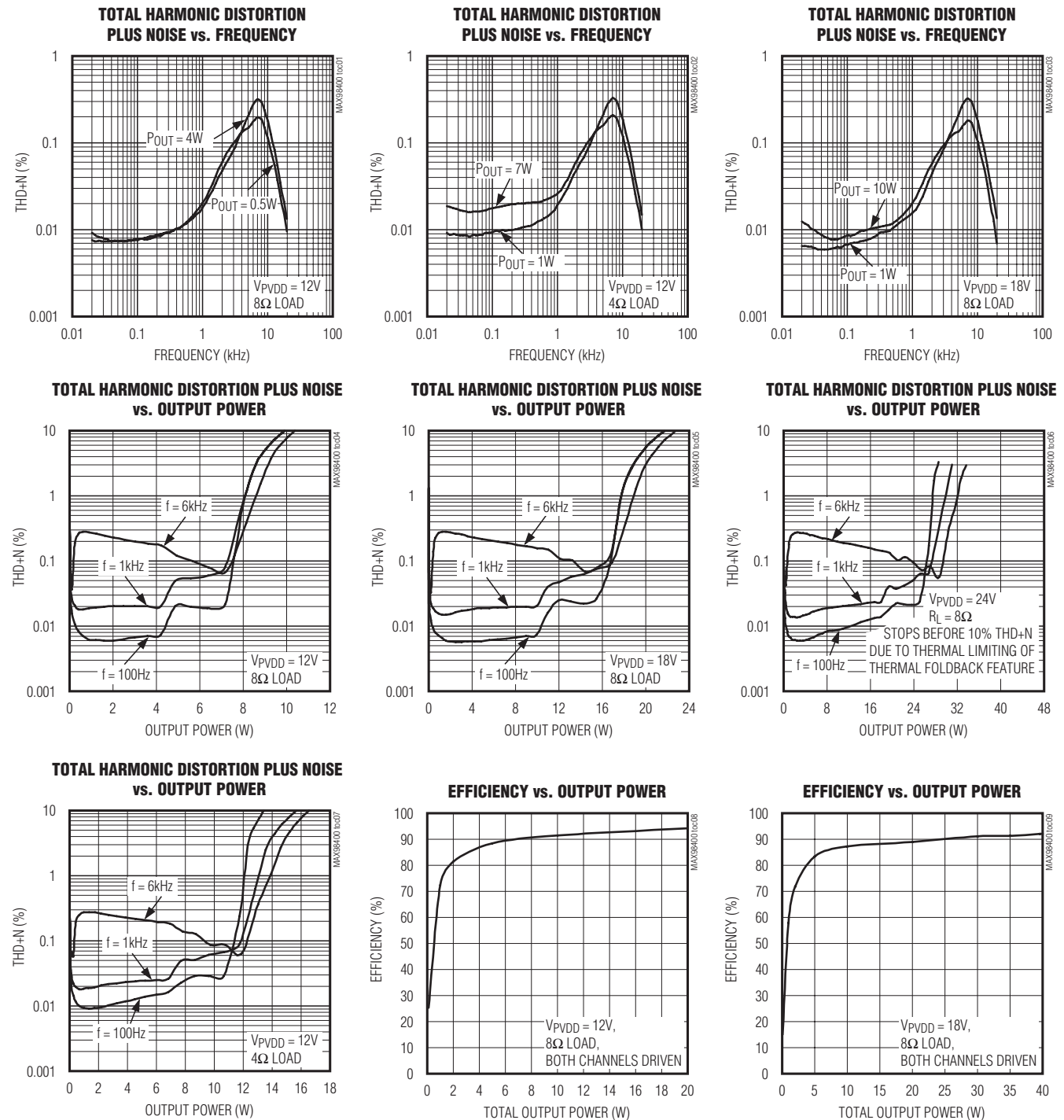
**Note 5:** Mode transitions controlled by  $\overline{SHDN}$ .

**Note 6:** Relative to equivalent full-scale undistorted output. Full scale (FS) =  $V_{PVDD} \times 0.95$ .

**Note 7:** Relative to equivalent full-scale undistorted output. Full scale (FS) =  $V_{PVDD}$ .

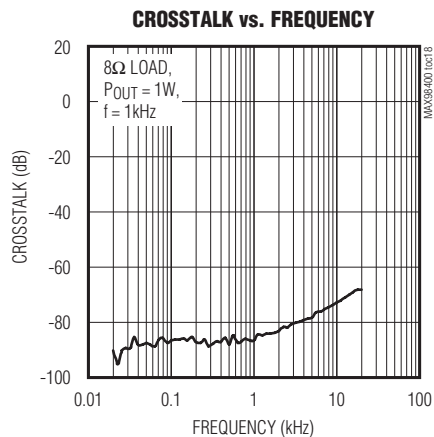
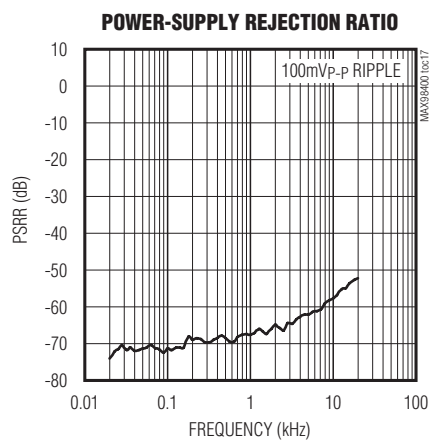
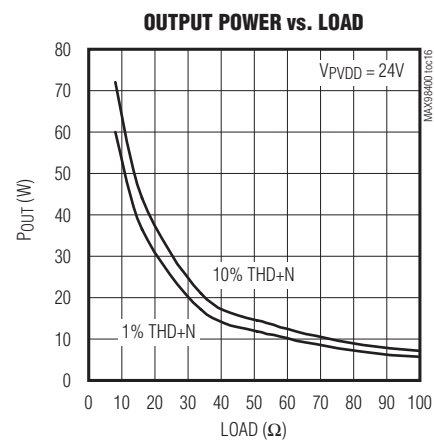
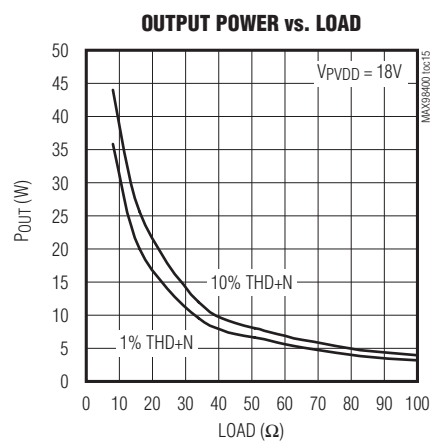
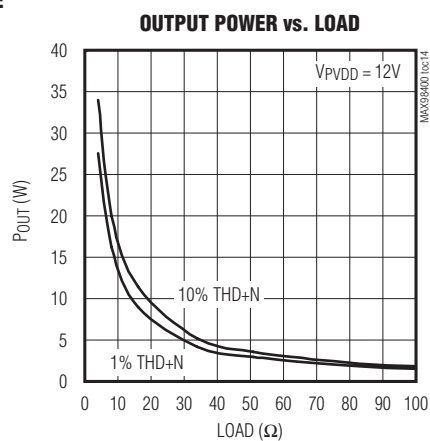
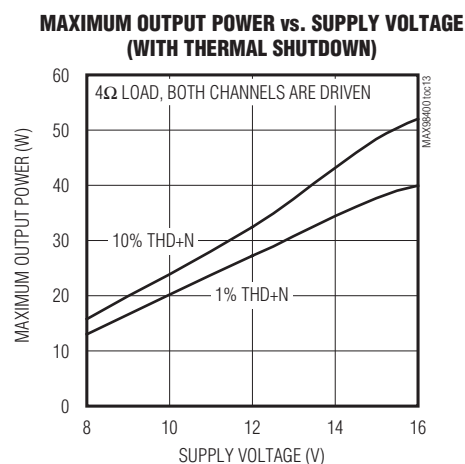
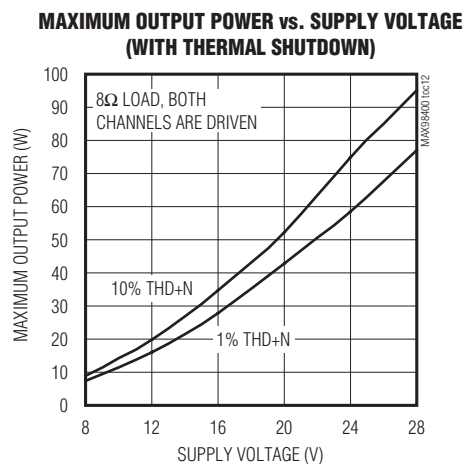
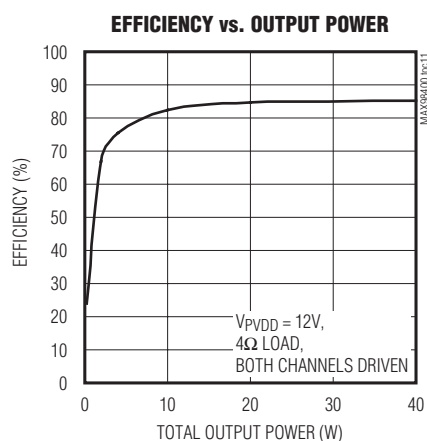
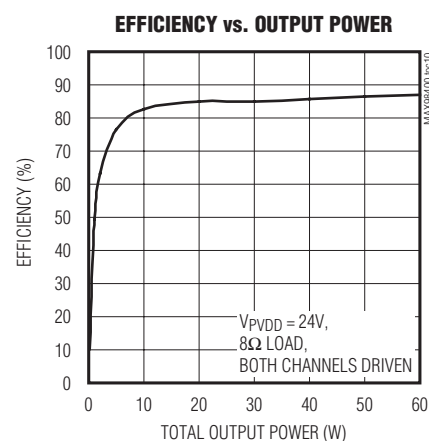
## Typical Operating Characteristics

(MAX98400A,  $V_{PVDD} = 18V$ ,  $V_{SHDN} = 5V$ ,  $LIM\_TH = V_S$ ,  $TEMPLOCK =$  unconnected;  $G1 = GND$ ,  $G2 =$  open (gain = 20.1dB),  $C_{IN} = C_{REL} = C1 = C2 = 1\mu F$ , typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)



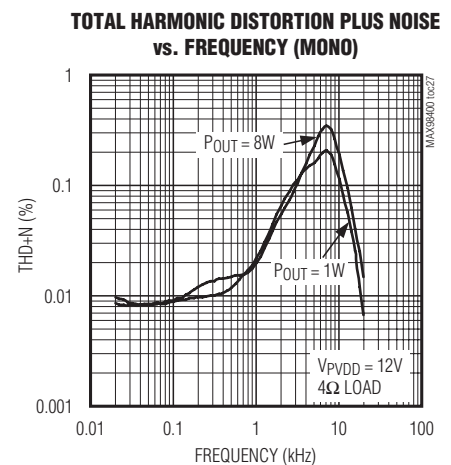
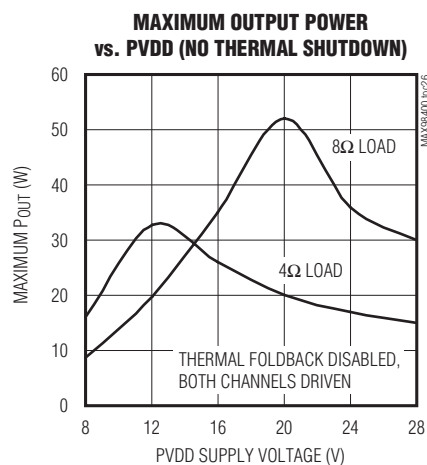
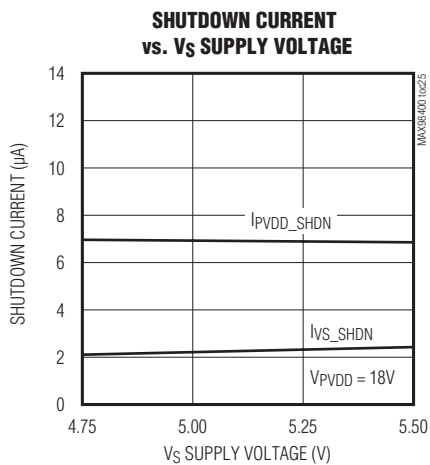
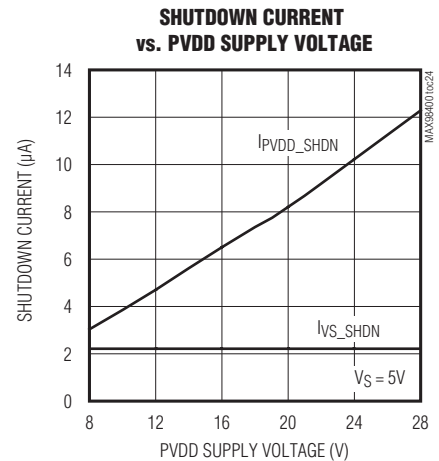
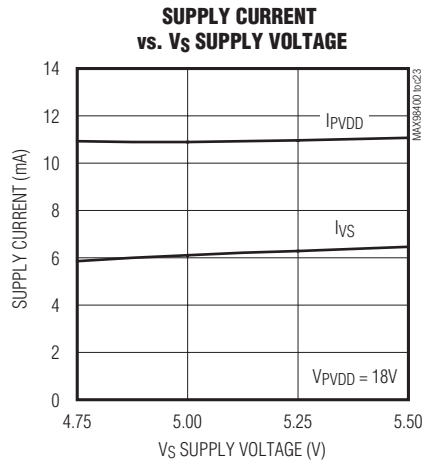
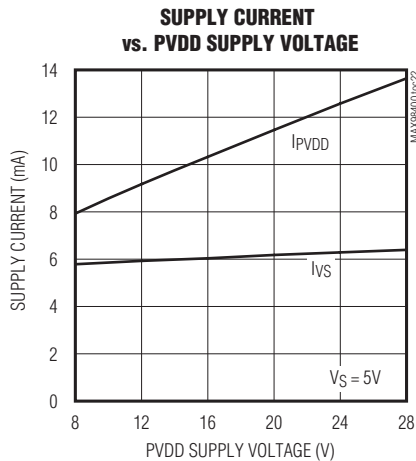
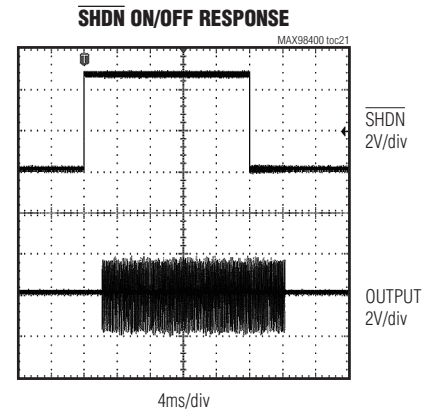
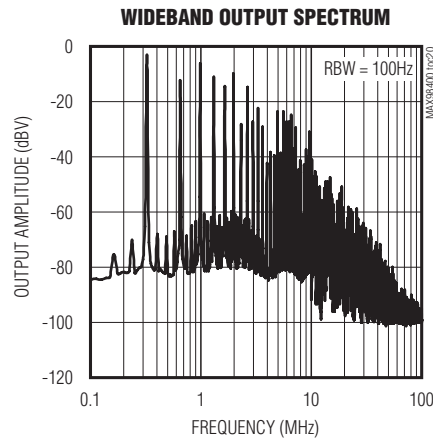
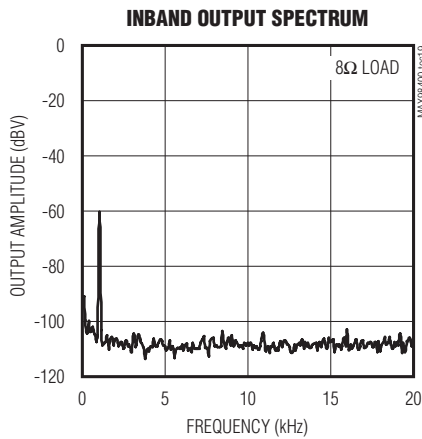
## Typical Operating Characteristics (continued)

(MAX98400A,  $V_{PVDD} = 18V$ ,  $V_{SHDN} = 5V$ ,  $LIM\_TH = V_S$ ,  $TEMPLOCK =$  unconnected;  $G1 = GND$ ,  $G2 =$  open (gain = 20.1dB),  $C_{IN} = C_{REL} = C1 = C2 = 1\mu F$ , typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)



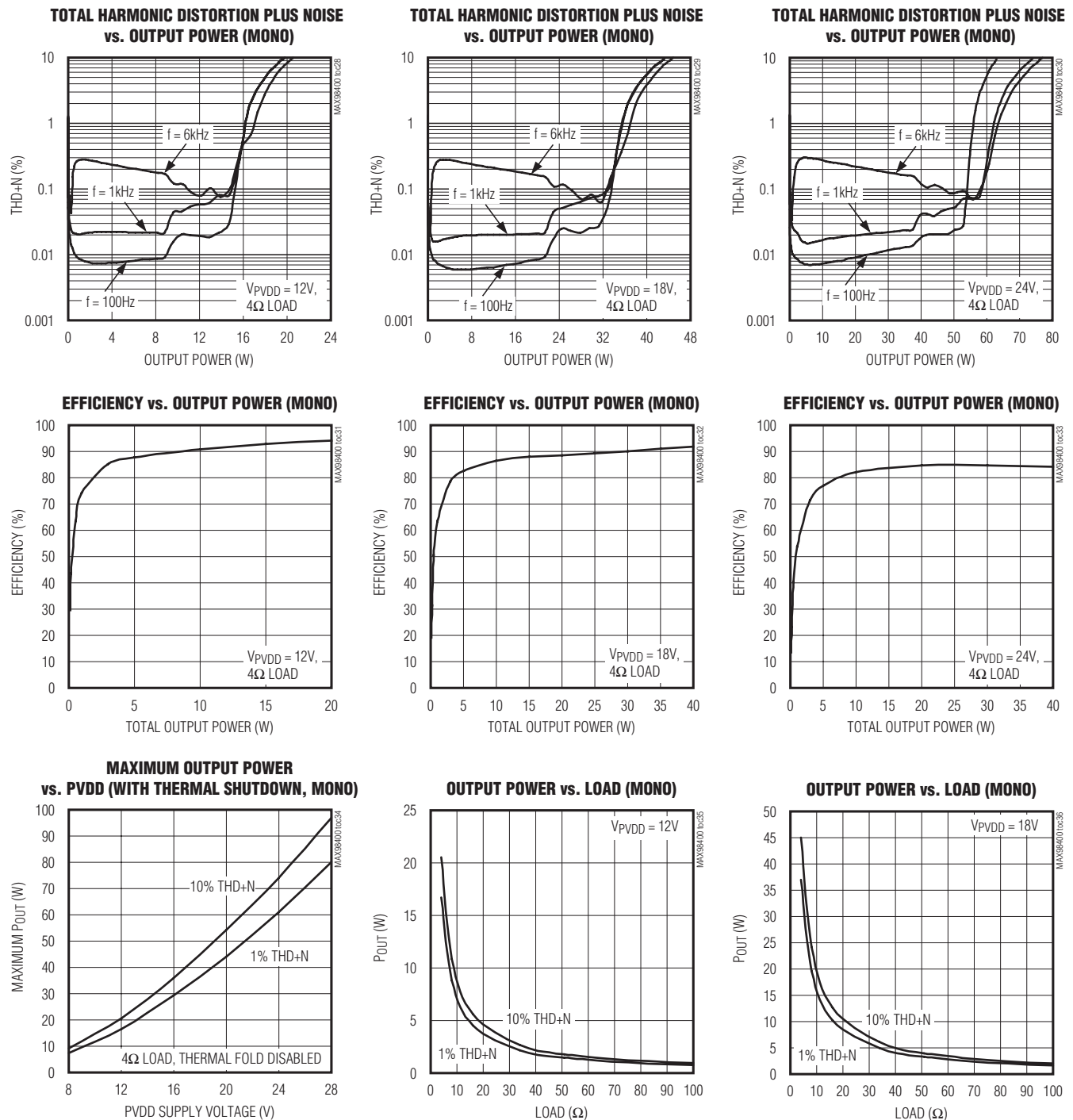
## Typical Operating Characteristics (continued)

(MAX98400A,  $V_{PVD D} = 18V$ ,  $V_{SHDN} = 5V$ ,  $LIM\_TH = V_S$ ,  $TEMPLOCK =$  unconnected;  $G1 = GND$ ,  $G2 =$  open (gain = 20.1dB),  $C_{IN} = C_{REL} = C1 = C2 = 1\mu F$ , typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)



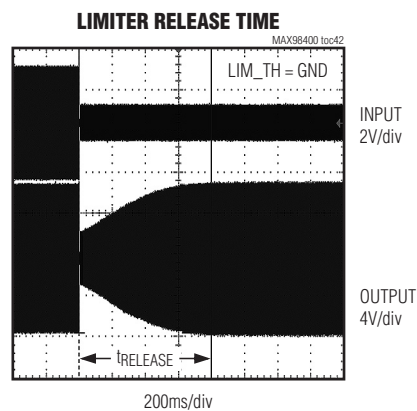
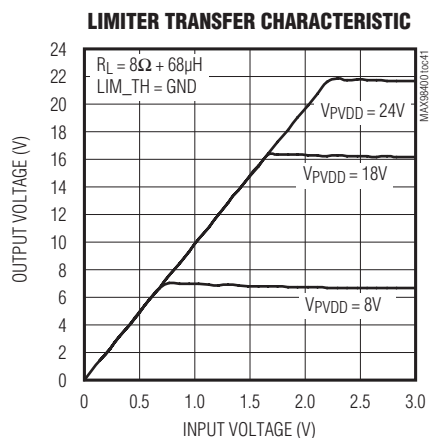
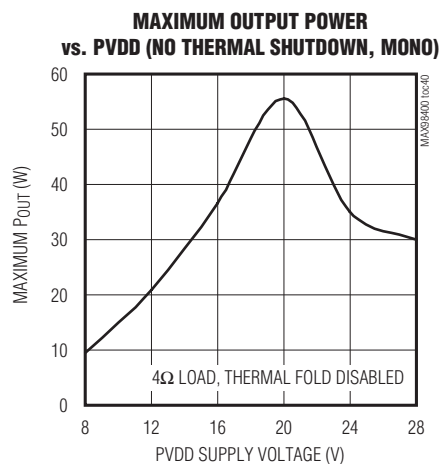
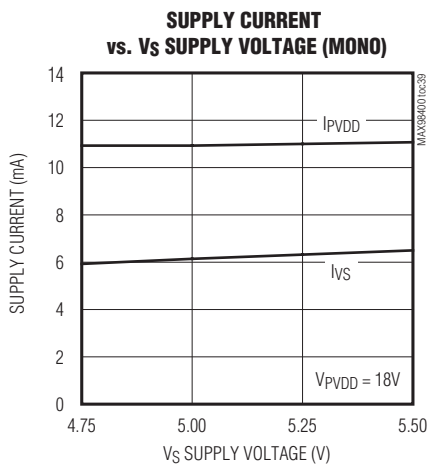
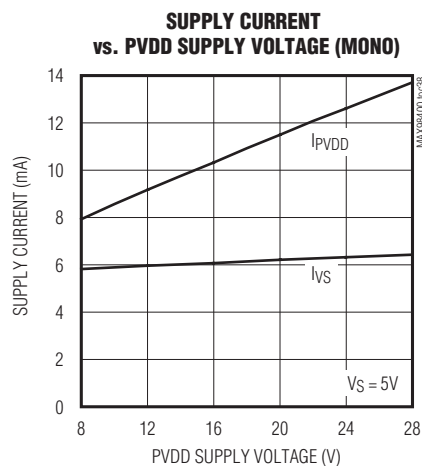
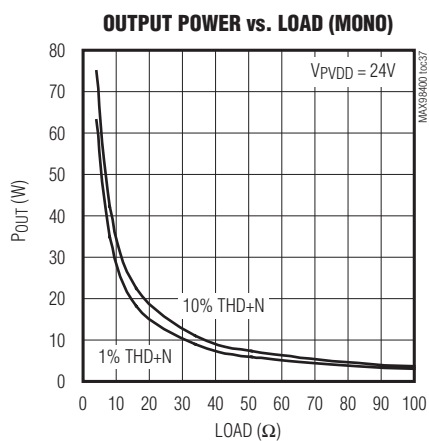
## Typical Operating Characteristics (continued)

(MAX98400A,  $V_{PVDD} = 18V$ ,  $V_{SHDN} = 5V$ ,  $LIM\_TH = V_S$ ,  $TEMPLOCK =$  unconnected;  $G1 = GND$ ,  $G2 =$  open (gain = 20.1dB),  $C_{IN} = C_{REL} = C1 = C2 = 1\mu F$ , typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)

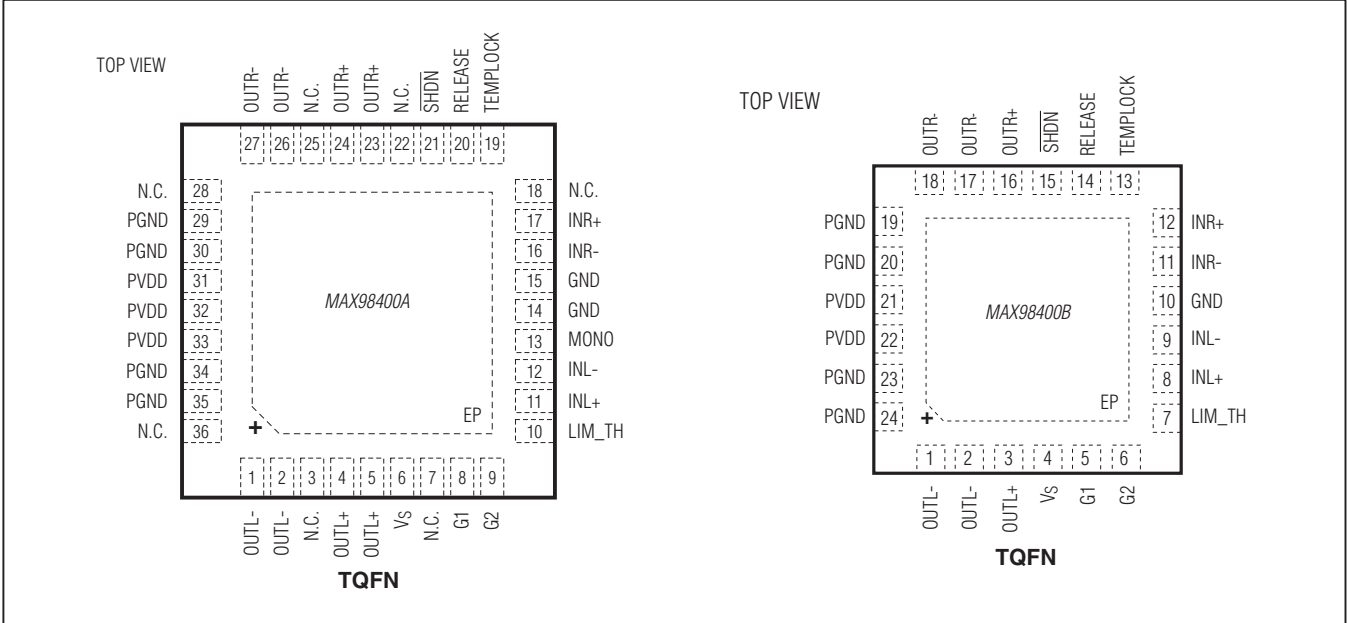


## Typical Operating Characteristics (continued)

(MAX98400A,  $V_{PVDD} = 18V$ ,  $V_{SHDN} = 5V$ ,  $LIM\_TH = V_S$ ,  $TEMPLOCK =$  unconnected;  $G1 = GND$ ,  $G2 =$  open (gain = 20.1dB),  $C_{IN} = C_{REL} = C1 = C2 = 1\mu F$ , typical values are at  $T_A = +25^\circ C$ , unless otherwise noted.)



Pin Configurations



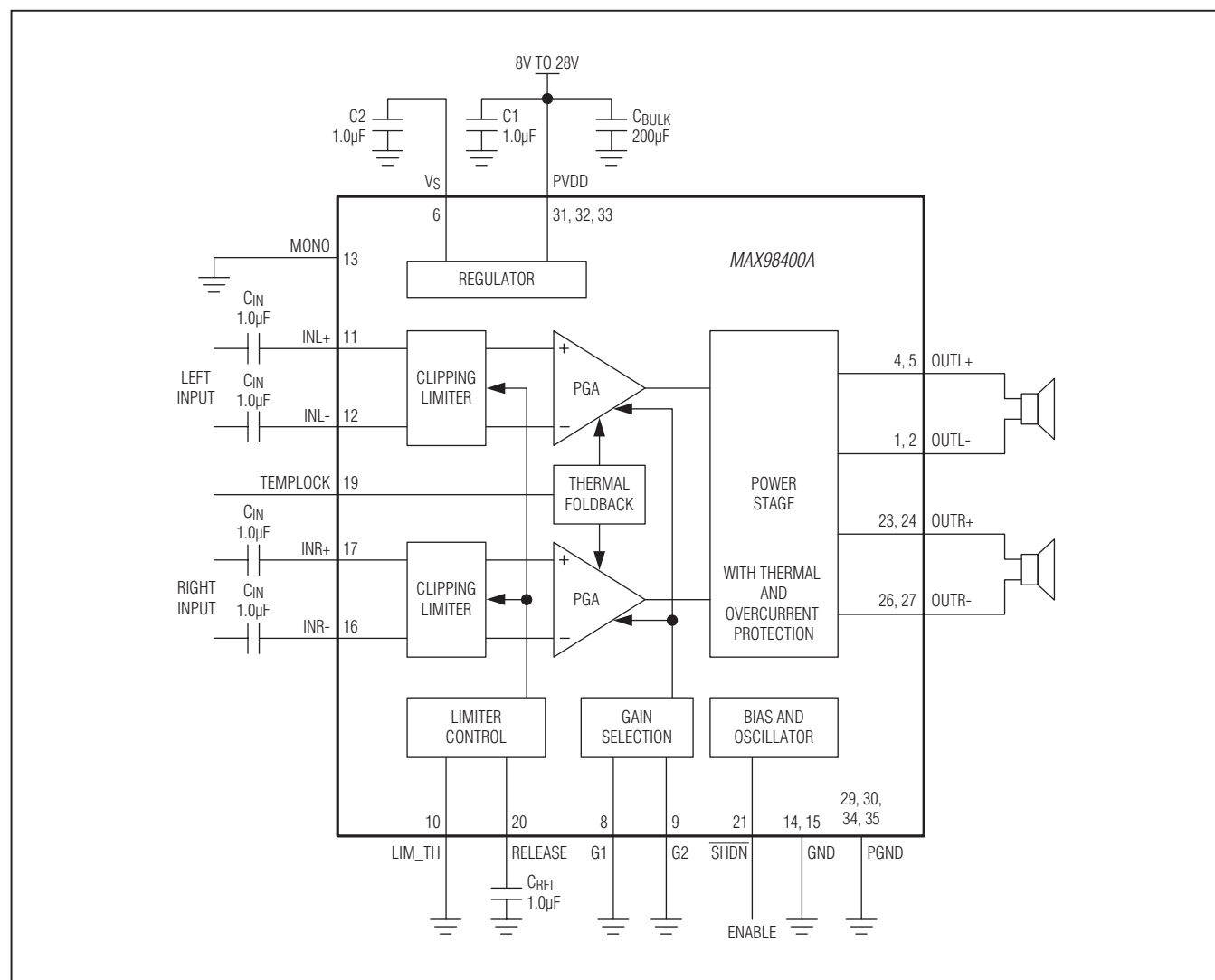
Pin Descriptions

| PIN                      |           | NAME   | FUNCTION                                                                                                                                                                                                                                                                                                                 |
|--------------------------|-----------|--------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| MAX98400A                | MAX98400B |        |                                                                                                                                                                                                                                                                                                                          |
| 1, 2                     | 1, 2      | OUTL-  | Negative Left Speaker Output                                                                                                                                                                                                                                                                                             |
| 3, 7, 18, 22, 25, 28, 36 | —         | N.C.   | No Connection                                                                                                                                                                                                                                                                                                            |
| 4, 5                     | 3         | OUTL+  | Positive Left Speaker Output                                                                                                                                                                                                                                                                                             |
| 6                        | 4         | VS     | 5V Regulator Supply. Bypass VS to GND with a 1μF capacitor. Connect to a +5V source for dual-supply operation.                                                                                                                                                                                                           |
| 8                        | 5         | G1     | Three-State Input for Gain Selection 1. See the <i>Detailed Description</i> section.                                                                                                                                                                                                                                     |
| 9                        | 6         | G2     | Three-State Input for Gain Selection 2. See the <i>Detailed Description</i> section.                                                                                                                                                                                                                                     |
| 10                       | 7         | LIM_TH | See the <i>Limiters Threshold Control (LIM_TH)</i> section for details. Connect to:<br>1) VS to disable limiter.<br>2) GND to have no clipping.<br>3) R <sub>LIM1</sub> resistor to GND to have a PVDD tracking threshold.<br>4) R <sub>LIM1</sub> and R <sub>LIM2</sub> resistor-divider to have an absolute threshold. |

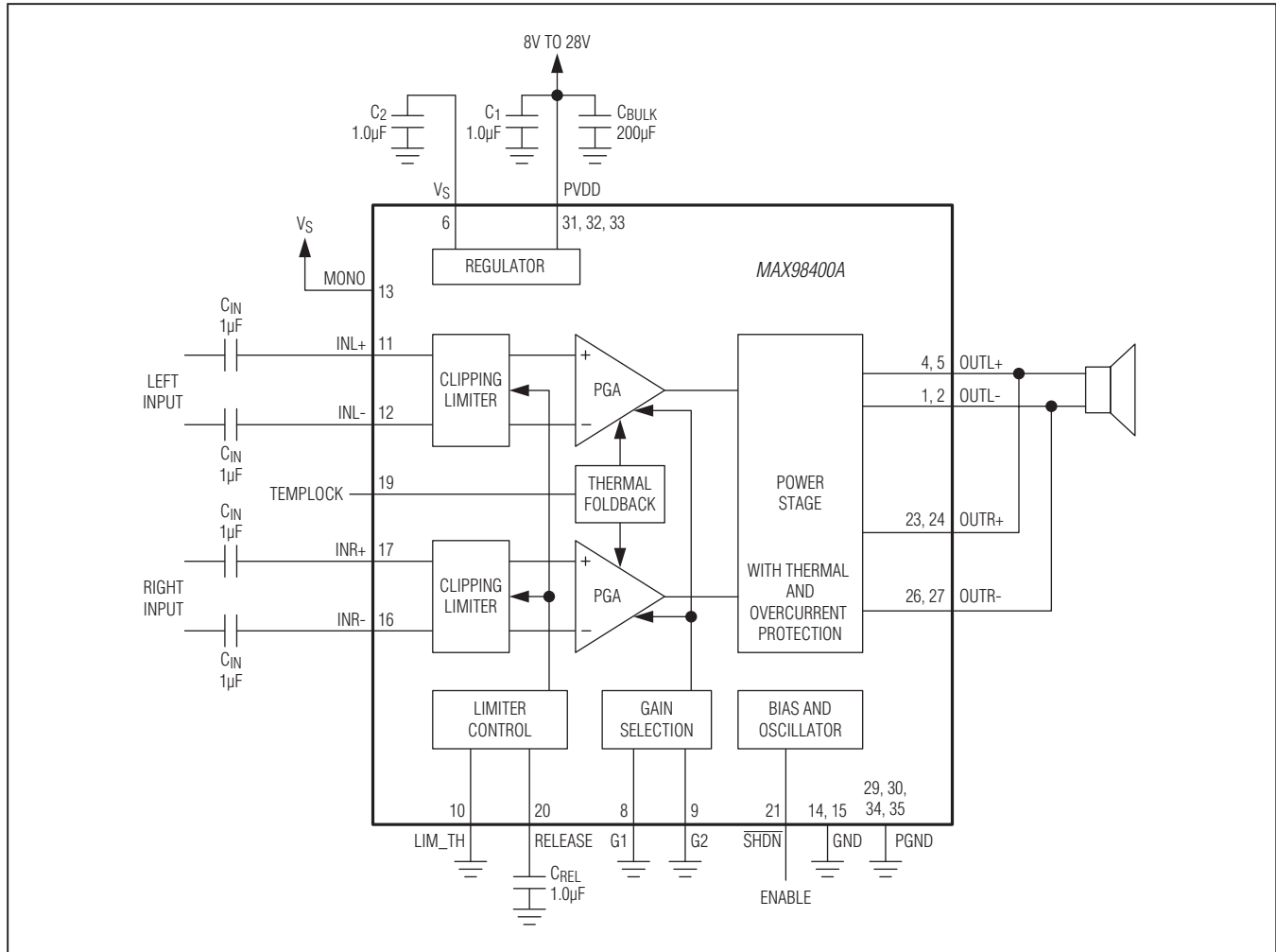
## Pin Descriptions (continued)

| PIN            |                | NAME                     | FUNCTION                                                                                                                                                |
|----------------|----------------|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|
| MAX98400A      | MAX98400B      |                          |                                                                                                                                                         |
| 11             | 8              | INL+                     | Left-Channel Positive Analog Input                                                                                                                      |
| 12             | 9              | INL-                     | Left-Channel Negative Analog Input                                                                                                                      |
| 13             | —              | MONO                     | Mono Operation. Connect MONO to GND for stereo operation. Connect MONO to $V_S$ for mono operation.                                                     |
| 14, 15         | 10             | GND                      | Analog Ground                                                                                                                                           |
| 16             | 11             | INR-                     | Right-Channel Negative Analog Input                                                                                                                     |
| 17             | 12             | INR+                     | Right-Channel Positive Analog Input                                                                                                                     |
| 19             | 13             | TEMPLOCK                 | See the <i>Thermal Foldback</i> section for details.<br>Connect to:<br>1) GND to disable thermal foldback.<br>2) Leave open to enable thermal foldback. |
| 20             | 14             | RELEASE                  | Sets the Limiter Time Constant. Connect to GND through 1 $\mu$ F.                                                                                       |
| 21             | 15             | $\overline{\text{SHDN}}$ | Active-Low Shutdown Input<br>Low = shutdown<br>High = enable                                                                                            |
| 23, 24         | 16             | OUTR+                    | Positive Right Speaker Output                                                                                                                           |
| 26, 27         | 17, 18         | OUTR-                    | Negative Right Speaker Output                                                                                                                           |
| 29, 30, 34, 35 | 19, 20, 23, 24 | PGND                     | Power Ground                                                                                                                                            |
| 31, 32, 33     | 21, 22         | PVDD                     | Power Supply. Bypass PVDD to PGND with 1 $\mu$ F and 200 $\mu$ F capacitors.                                                                            |
| —              | —              | EP                       | Exposed Pad. Connect to PGND for optimum thermal performance.                                                                                           |

## Stereo Configuration for MAX98400A



## Mono Configuration for MAX98400A



## Detailed Description

The MAX98400A/MAX98400B Class D amplifiers provide high-performance, thermally efficient amplifier solutions. The MAX98400A delivers 2x20W into 8Ω loads or 1x40W into a 4Ω load. The MAX98400B delivers 2x12W into 8Ω loads.

An integrated limiting circuit prevents output clipping distortion and protects small speakers from transient voltages.

A thermal-foldback feature can be enabled to automatically reduce the output power if the supply voltage, input signal, and/or ambient temperature are too high to operate within a junction temperature of +130°C. Traditional

thermal protection is also available in addition to robust overcurrent protection.

Both devices operate from an 8V to 28V supply and provide a high 67dB PSRR, eliminating the need for a regulated power supply. They offer up to 90% efficiency from a 12V supply.

Filterless modulation allows the ICs to pass EN55022B EMI limits with 1m cables using only a low-cost ferrite bead and small-value capacitor on each output (Figure 1).

Comprehensive click-and-pop reduction circuitry minimizes noise coming into and out of shutdown.

The MAX98400A/MAX98400B are available in 36-pin and 24-pin TQFN packages, respectively, and are specified over the -40°C to +85°C temperature range.

## Efficiency

The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. In a Class D amplifier, the output transistors act as switches and consume negligible power. Power loss associated with the Class D output stage is due to the  $I^2R$  loss of the MOSFET on-resistance, various switching losses, and quiescent current overhead.

The theoretical best efficiency of a linear amplifier is 78% at peak output power. Under typical music reproduction levels, the efficiency falls below 30%, whereas these ICs exhibit > 85% efficiency under the same conditions (Figure 2).

## Shutdown

The ICs feature a shutdown mode that reduces power consumption and extends battery life in portable applications. The shutdown mode reduces supply current to 8μA (typ). Drive  $\overline{\text{SHDN}}$  high for normal operation. Drive SHDN low to place the device in low-power shutdown mode. In shutdown mode, the outputs are high impedance and the common-mode voltage at the output decays to zero. The shutdown mode serves as a mute function.

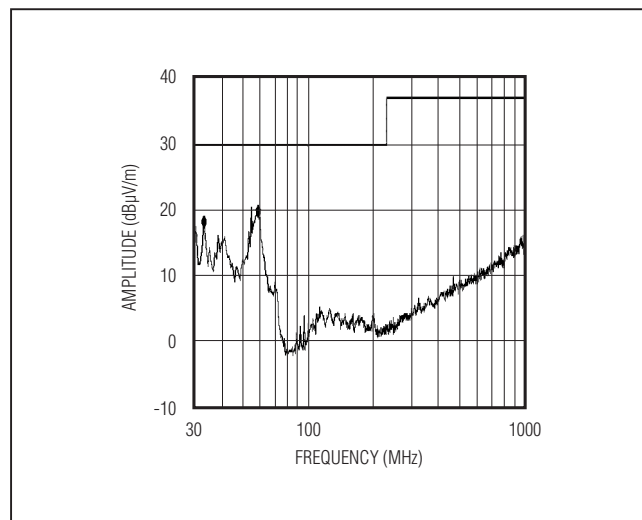


Figure 1. MAX98400B EMI Performance

## Click-and-Pop Suppression

The ICs feature comprehensive click-and-pop suppression that minimizes audible transients on startup and shutdown. While in shutdown, the H-bridge is in a high-impedance state.

## Mono Configuration

The MAX98400A features a mono mode that allows the right and left channels to operate in parallel, achieving up to 40W of output power. Apply a logic-high (Vs) to MONO to enable mono mode. In mono mode, an audio signal applied to the left channel (INL) is routed to the H-bridges of both channels. Connect OUTL+ to OUTR+ and OUTL- to OUTR- using heavy PCB traces as close as possible to the device. Driving MONO low (stereo mode) while the outputs are wired together in mono mode can trigger the short-circuit or thermal-overload protection, or both.

## Clipping Limiter

The ICs feature a programmable clipping limiter to prevent output clipping distortion and excessive power dissipation and to protect small speakers. All limiter functionality is controlled by two pins: LIM\_TH and RELEASE. The voltage applied at the LIM\_TH pin controls the threshold when the limiter acts, and the capacitor at the RELEASE pin controls the release time of the limiter. The limiter controls both left and right channels together.

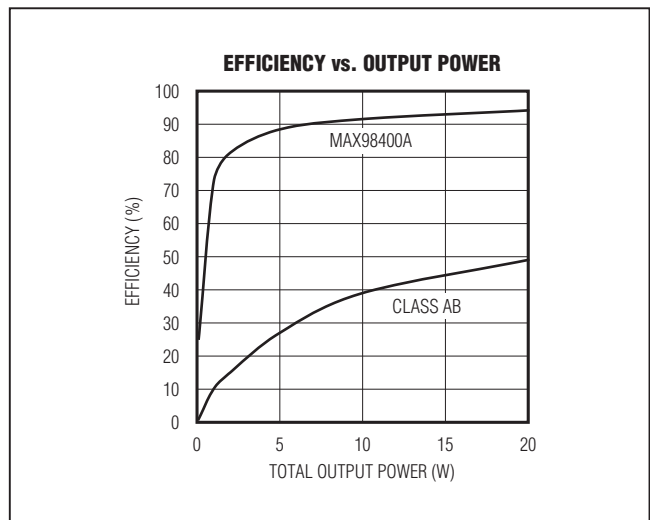


Figure 2. MAX98400A Efficiency vs. Class AB Efficiency

### Limiter Threshold Control (LIM\_TH)

There are three modes for the limiter, defined by  $V_{LIM\_TH}$ , the voltage applied to the LIM\_TH pin (Table 1).

In Mode1, the limiter is disabled. The output clips when output peak voltage reaches the voltage on PVDD, VPVDD.

In Mode2, the limiter threshold ( $V_{THRESH}$ ) tracks supply voltage, VPVDD. The peak output voltage is limited to approximately  $V_{THRESH} = VPVDD \times 0.95$ .

In Mode3, the limiter threshold,  $V_{THRESH}$ , is programmable.  $V_{LIM\_TH}$  can be set to a voltage proportional to the desired output threshold. The limiter threshold can be set down to  $0.5 \times VPVDD$  and up to  $1.6 \times VPVDD$ .  $V_{THRESH}$  cannot exceed 22V.

Threshold settings below VPVDD can be used to protect speakers; the peak output voltage is limited to a value of  $V_{THRESH} = V_{LIM\_TH} \times 6.4$ .

Threshold settings above VPVDD can be used to limit the output distortion; the peak output voltage is limited to a value of  $V_{THRESH} = V_{LIM\_TH} \times 6.4 \times 0.95$ . The 0.95 factor takes into account the voltage drop across the power FET that occurs when the amplifier is clipped. Choose  $R_{LIM1}$  and  $R_{LIM2}$  (Figure 3) to set the desired voltage at the LIM\_TH pin. For best accuracy, the parallel combination  $R_{LIM1} || R_{LIM2}$  should be approximately 100k $\Omega$ .

#### Example:

If the speaker in the application can handle only 12V peak, but VPVDD is higher, the threshold voltage ( $V_{THRESH}$ ) should be set to 12V:

$$V_{THRESH} = 12V$$

The voltage that needs to be applied to  $V_{LIM\_TH}$  is then defined as:

$$V_{LIM\_TH} = V_{THRESH}/6.4 = 12V/6.4 = 1.88V$$

For a 5V supply, a resistor-divider of  $R_{LIM1} = 165k\Omega$ / $R_{LIM2} = 270k\Omega$  gives both an unloaded voltage of 1.82V and the desired output resistance of approximately 100k $\Omega$ .

If only distortion limiting is desired, set  $V_{THRESH}$  to be 20% higher than VPVDD. This limits the output clipping levels to approximately 10% THD.

The attack time for the limiter is fixed, typically < 200 $\mu$ s.

### Release Time Control (RELEASE)

The release time for the limiter is set by an external capacitor at RELEASE ( $C_{REL}$ ) to GND. Choose  $C_{REL} = \text{Release Time [s]} \times 1\mu F$ . The  $C_{REL}$  limit is 2.2 $\mu F$ .

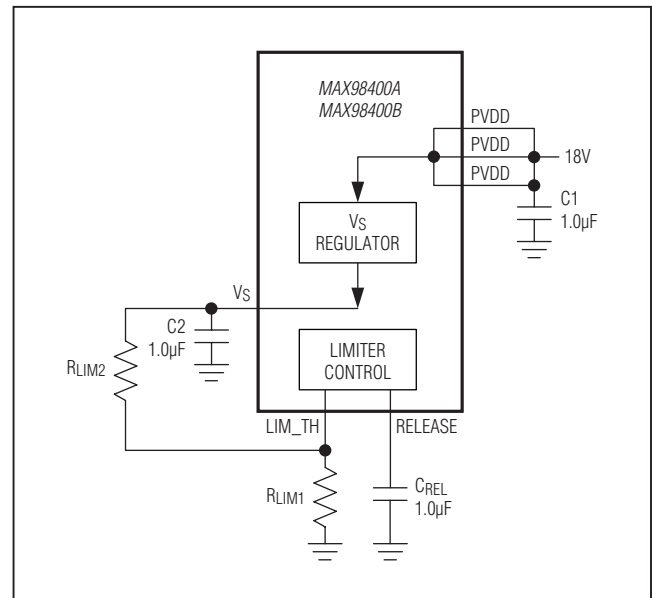


Figure 3. Limiter Control, Mode3 Configuration (Table 1)

Table 1. Limiter Control Modes

| MODE  | NAME          | FUNCTION                                                                                                                                                                                                                                                  | LIM_TH VOLTAGE RANGE               |
|-------|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|
| Mode1 | Disable       | The limiter is disabled when connecting LIM_TH to Vs or a voltage greater than 3.9V.                                                                                                                                                                      | $3.9V < V_{LIM\_TH} \leq V_S$      |
| Mode2 | PVDD tracking | The output peak voltage is limited to just below the supply voltage, VPVDD. $V_{THRESH} = VPVDD \times 0.95$ when LIM_TH is connected to ground or a voltage below 0.3V.                                                                                  | $V_{GND} \leq V_{LIM\_TH} < 0.15V$ |
| Mode3 | Programmable  | The output peak voltage, $V_{THRESH}$ , is limited to the threshold set by the voltage applied on the LIM_TH so that $V_{THRESH} = V_{LIM\_TH} \times 6.4$ . When $V_{THRESH}$ is set 20% higher than VPVDD, the output THD distortion is limited to 10%. | $0.6V \leq V_{LIM\_TH} \leq 3.8V$  |

**Note:**  $V_{THRESH}$  is the output peak limiting voltage (limiter threshold voltage).

### Preamplifier Gain Setting

The ICs offer eight pin-selectable gain settings, selectable through the G1 and G2 pins.

### Protection

The ICs feature overcurrent protection and two types of thermal protection: thermal foldback and overtemperature protection.

#### Thermal Foldback

The ICs feature thermal foldback that helps prevent unwanted thermal-shutdown events. If activated, thermal foldback attenuates the stereo output signal once the internal junction temperature exceeds +130°C. Attenuation is applied proportionally as the junction temperature ( $T_J$ ) exceeds the fixed +130°C threshold. The thermal-foldback mode is controlled by the TEMPLOCK pin.

#### Overtemperature Protection

The ICs feature an overtemperature protection that disables the amplifier if the junction temperature exceeds +165°C. Once the amplifier is disabled and the die temperature has cooled by 20°C, the devices enable again and resume normal operation.

#### Overcurrent Protection

When the output current reaches the current limit, 5A (typ), the ICs disable the outputs and initiate a recovering

sequence. The shutdown and recovering sequence is repeated until the output fault is removed.

## Applications Information

### Filterless Class D Operation

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filters add cost, increase the solution size of the amplifier, and can decrease efficiency and THD+N performance. The traditional PWM scheme uses large differential output swings ( $2 \times V_{DD}$  peak-to-peak) and causes large ripple currents. Any parasitic resistance in the filter components results in a loss of power, lowering the efficiency.

These ICs do not require an output filter. The devices rely on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output. Eliminating the output filter results in a smaller, lower cost solution.

Because the frequency of the ICs' output is well beyond the bandwidth of most speakers, voice coil movement due to the square-wave frequency is very small. For optimum results, use a speaker with a series inductance  $> 10\mu\text{H}$ . Typical  $8\Omega$  speakers exhibit series inductances in the  $20\mu\text{H}$  to  $100\mu\text{H}$  range.

**Table 2. Gain Selection**

| G1             | G2             | GAIN SETTING (dB) |
|----------------|----------------|-------------------|
| GND            | GND            | 9                 |
| Unconnected    | GND            | 13                |
| V <sub>S</sub> | GND            | 16.7              |
| GND            | Unconnected    | 20.1              |
| Unconnected    | Unconnected    | 23.3              |
| V <sub>S</sub> | Unconnected    | 26.4              |
| GND            | V <sub>S</sub> | 29.8              |
| Unconnected    | V <sub>S</sub> | 32.9              |
| V <sub>S</sub> | V <sub>S</sub> | Reserved          |

### Inductor-Based Output Filters

Some applications use the ICs with a full inductor-/capacitor-based (L/C) output filter. See Figure 4 for the correct connections of these components.

The load impedance of the speaker determines the filter component selection (Table 3).

Inductors L1 and L2 and capacitor C1 form the primary output filter. Capacitors C2 and C3 provide common-mode filtering to reduce radiated emissions. Capacitors C4 and C5, plus resistors R1 and R2, form a Zobel at the output. A Zobel corrects the output loading to compensate for the rising impedance of the loudspeaker. Without a Zobel, the filter exhibits a peak response near the cutoff frequency.

### Component Selection

#### Input Capacitor

The input AC-coupling capacitors allow the amplifier to automatically bias the signal to an optimum DC level. 1 $\mu$ F is recommended for the input capacitor.

#### Power Supplies

The ICs are designed to be operated from a single-supply voltage, V<sub>PVDD</sub>, which can range from 8V to 28V. Inside the ICs, this V<sub>PVDD</sub> supplies power for the output FETs and other high-power circuitry, while the low-power circuitry operates from V<sub>S</sub>, an internally generated 5V supply (4.6V typ). V<sub>S</sub> is internally generated from a linear regulator that is powered from V<sub>PVDD</sub>. Bypass both PVDD and V<sub>S</sub> pins to ground with a 1 $\mu$ F capacitor.

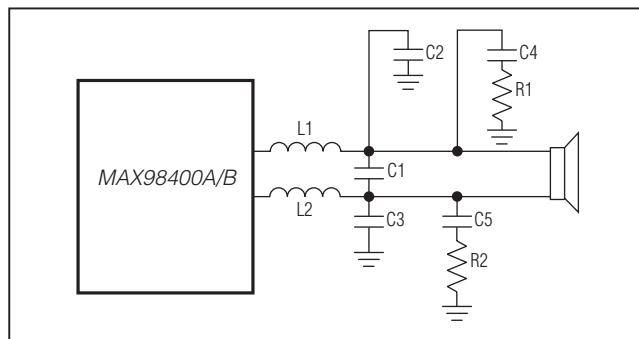


Figure 4. Output Filter for PWM Mode

Table 3. Filter Component Selection

| R <sub>L</sub> ( $\Omega$ ) | L1, L2 ( $\mu$ H) | C1 ( $\mu$ F) | C2, C3 ( $\mu$ F) | C4, C5 ( $\mu$ F) | R1, R2 ( $\Omega$ ) |
|-----------------------------|-------------------|---------------|-------------------|-------------------|---------------------|
| 4                           | 10                | 0.47          | 0.10              | 0.22              | 10                  |
| 8                           | 15                | 0.15          | 0.15              | 0.15              | 15                  |
| 16                          | 33                | 0.10          | 0.10              | 0.10              | 33                  |

### Internal Regulator V<sub>S</sub>

For highest efficiency operation and best thermal performance, especially at higher V<sub>PVDD</sub> levels, the V<sub>S</sub> can be supplied from an external 5V supply. To do this, connect a 5V source to the V<sub>S</sub> pin (4.75V to 5.5V). When a 5V supply is connected to the V<sub>S</sub> pin, the internal regulator is automatically disabled and the power dissipation of the ICs is reduced.

### Supply Bypassing, Layout, and Grounding

Proper layout and grounding are essential for optimum performance. Use wide traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents switching noise from coupling into the audio signal. Connect PGND and GND together at a single point on the PCB. Route all traces that carry switching transients away from GND and the traces/components in the audio signal path.

Bypass each PVDD pin with a 0.1 $\mu$ F capacitor to PGND. Place the bypass capacitors as close as possible to the ICs. Place a 220 $\mu$ F capacitor between PVDD and PGND. Bypass both PVDD and V<sub>S</sub> pins with a 1 $\mu$ F capacitor to GND.

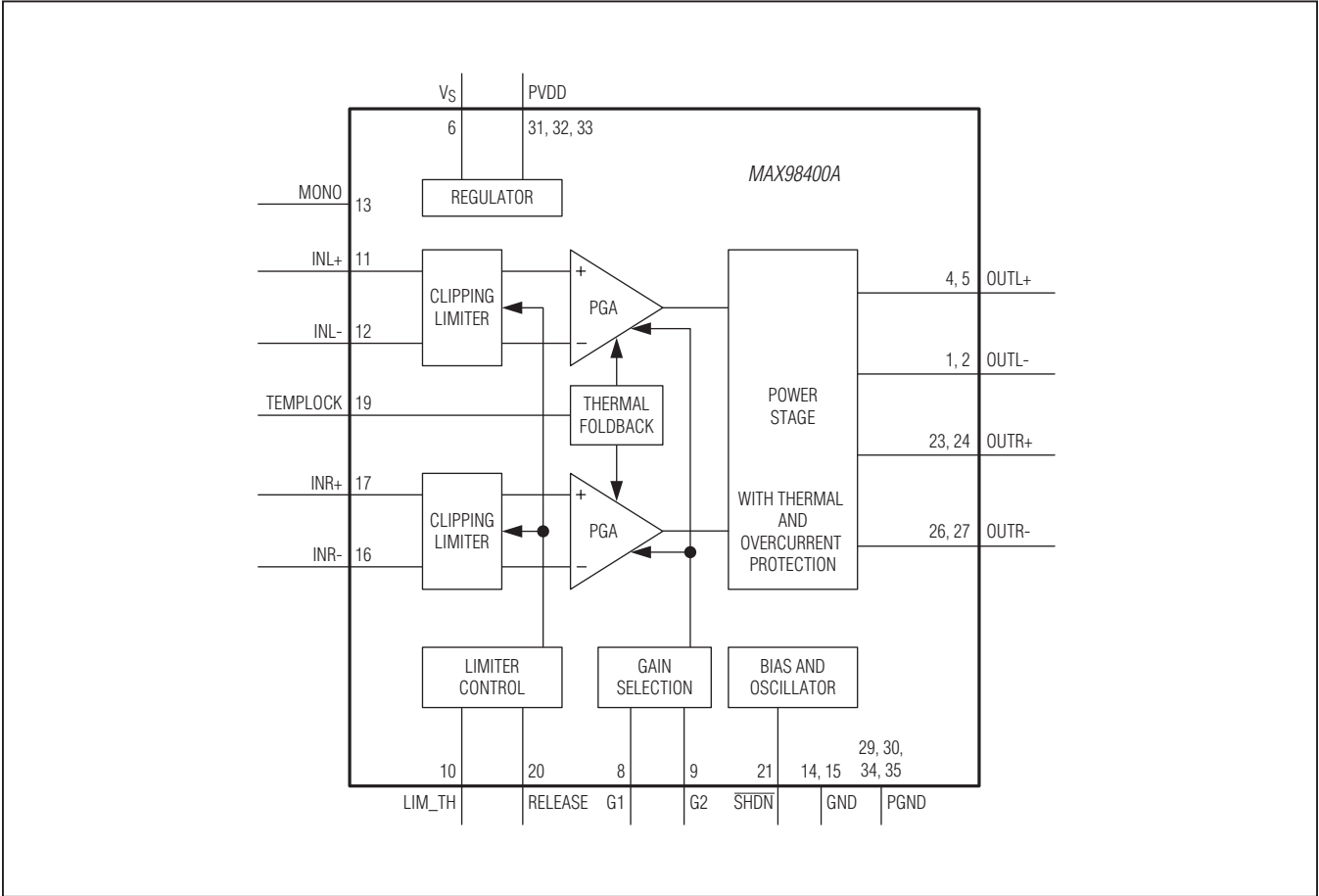
Use wide, low-resistance output traces. Current drawn from the outputs increases as load impedance decreases. High-output trace resistance decreases the power delivered to the load. The TQFN package features an exposed thermal pad on its underside. This pad lowers the package's thermal resistance by providing a heat conduction path from the die to the PCB. Connect the exposed thermal pad to PGND by using a large pad and multiple vias to the PGND plane.

For best optimum thermal performance, use 2oz copper and allow lots of PCB area around the device.

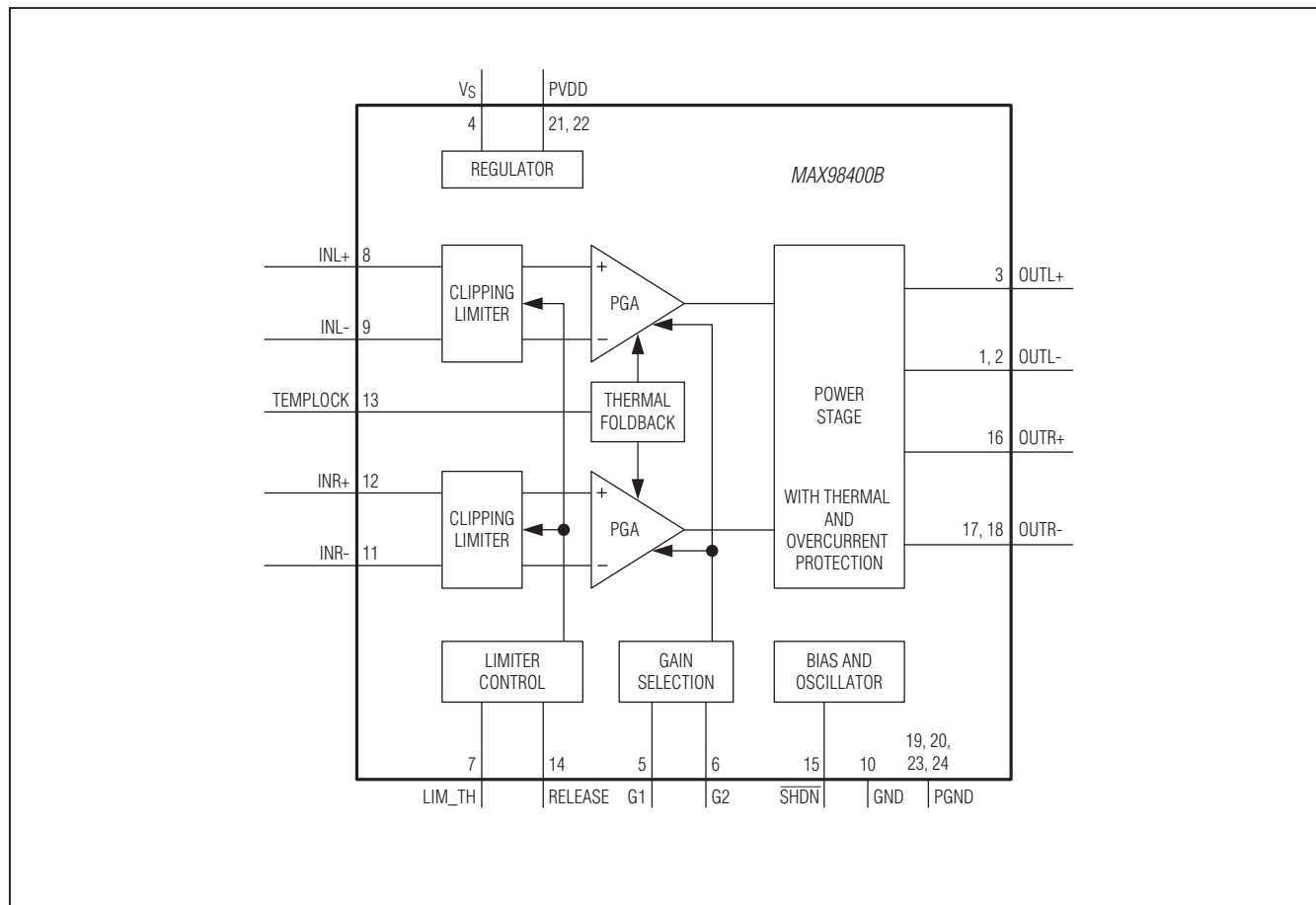
### Chip Information

PROCESS: CMOS

Functional Diagrams



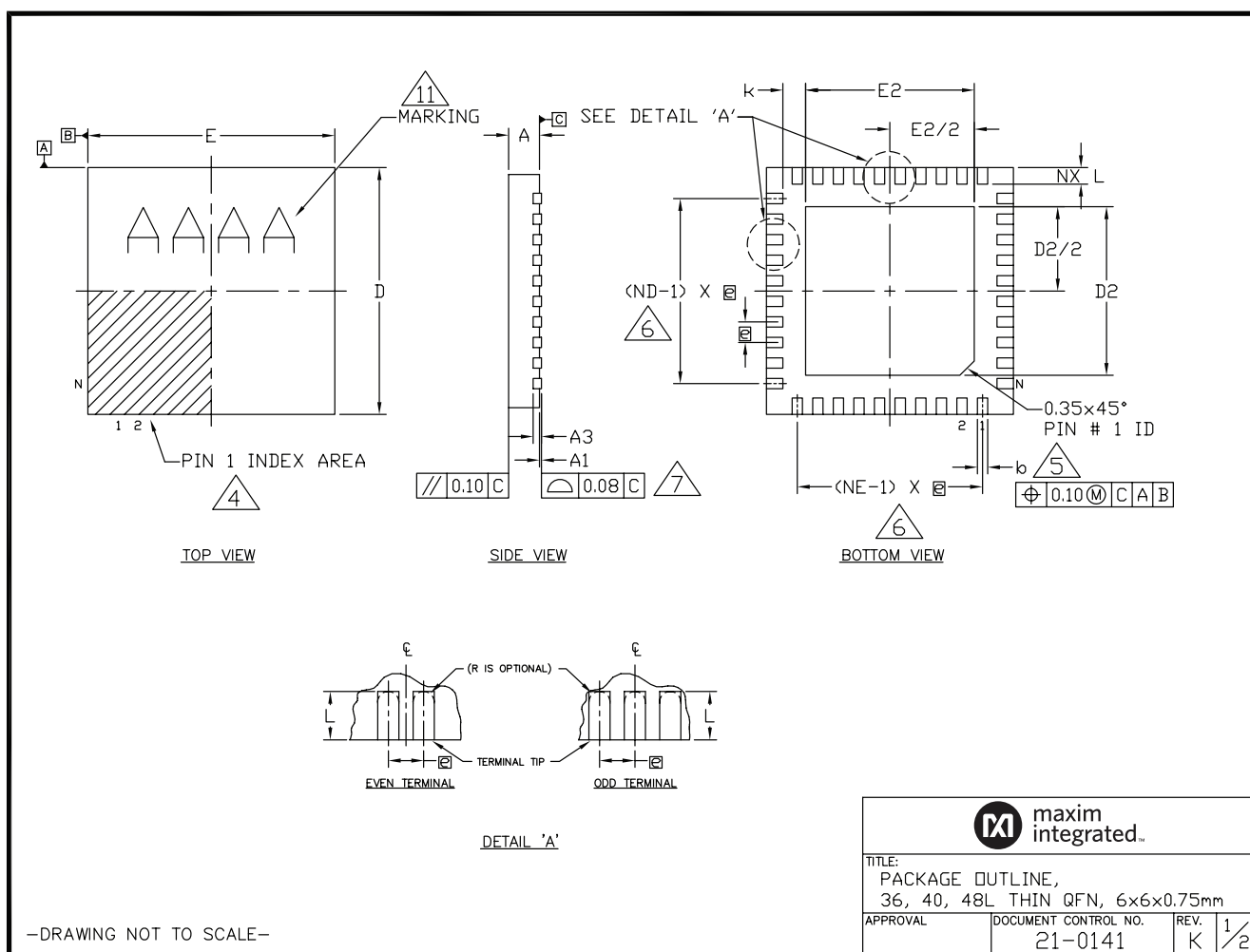
## Functional Diagrams (continued)



## Package Information

For the latest package outline information and land patterns, go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO.             | LAND PATTERN NO.        |
|--------------|--------------|-------------------------|-------------------------|
| 36 TQFN-EP   | T3666+2      | <a href="#">21-0141</a> | <a href="#">90-0049</a> |
| 24 TQFN-EP   | T2444+4      | <a href="#">21-0139</a> | <a href="#">90-0022</a> |



## Package Information (continued)

For the latest package outline information and land patterns, go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| COMMON DIMENSIONS |           |      |      |           |      |      |           |      |      |
|-------------------|-----------|------|------|-----------|------|------|-----------|------|------|
| PKG.              | 36L 6x6   |      |      | 40L 6x6   |      |      | 48L 6x6   |      |      |
| SYMBOL            | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. |
| A                 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 |
| A1                | 0         | 0.02 | 0.05 | 0         | 0.02 | 0.05 | 0         | —    | 0.05 |
| A3                | 0.20 REF. |      |      | 0.20 REF. |      |      | 0.20 REF. |      |      |
| b                 | 0.20      | 0.25 | 0.30 | 0.20      | 0.25 | 0.30 | 0.15      | 0.20 | 0.25 |
| D                 | 5.90      | 6.00 | 6.10 | 5.90      | 6.00 | 6.10 | 5.90      | 6.00 | 6.10 |
| E                 | 5.90      | 6.00 | 6.10 | 5.90      | 6.00 | 6.10 | 5.90      | 6.00 | 6.10 |
| e                 | 0.50 BSC. |      |      | 0.50 BSC. |      |      | 0.40 BSC. |      |      |
| k                 | 0.25      | —    | —    | 0.25      | —    | —    | 0.25      | —    | —    |
| L                 | 0.35      | 0.50 | 0.65 | 0.30      | 0.40 | 0.50 | 0.30      | 0.40 | 0.50 |
| N                 | 36        |      |      | 40        |      |      | 48        |      |      |
| ND                | 9         |      |      | 10        |      |      | 12        |      |      |
| NE                | 9         |      |      | 10        |      |      | 12        |      |      |
| JEDEC             | WJJD-1    |      |      | WJJD-2    |      |      | —         |      |      |

| EXPOSED PAD VARIATIONS |      |      |      |      |      |      |
|------------------------|------|------|------|------|------|------|
| PKG. CODES             | D2   |      |      | E2   |      |      |
|                        | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T3666-2                | 3.60 | 3.70 | 3.80 | 3.60 | 3.70 | 3.80 |
| T3666-3                | 3.60 | 3.70 | 3.80 | 3.60 | 3.70 | 3.80 |
| T3666N-1               | 3.60 | 3.70 | 3.80 | 3.60 | 3.70 | 3.80 |
| T3666MN-1              | 3.60 | 3.70 | 3.80 | 3.60 | 3.70 | 3.80 |
| T4066-2                | 4.00 | 4.10 | 4.20 | 4.00 | 4.10 | 4.20 |
| T4066-3                | 4.00 | 4.10 | 4.20 | 4.00 | 4.10 | 4.20 |
| T4066-5                | 4.00 | 4.10 | 4.20 | 4.00 | 4.10 | 4.20 |
| T4866-1                | 4.40 | 4.50 | 4.60 | 4.40 | 4.50 | 4.60 |
| T4866N-1               | 4.40 | 4.50 | 4.60 | 4.40 | 4.50 | 4.60 |
| T4866-2                | 4.40 | 4.50 | 4.60 | 4.40 | 4.50 | 4.60 |
| T4066MN-5              | 4.00 | 4.10 | 4.20 | 4.00 | 4.10 | 4.20 |

### NOTES:

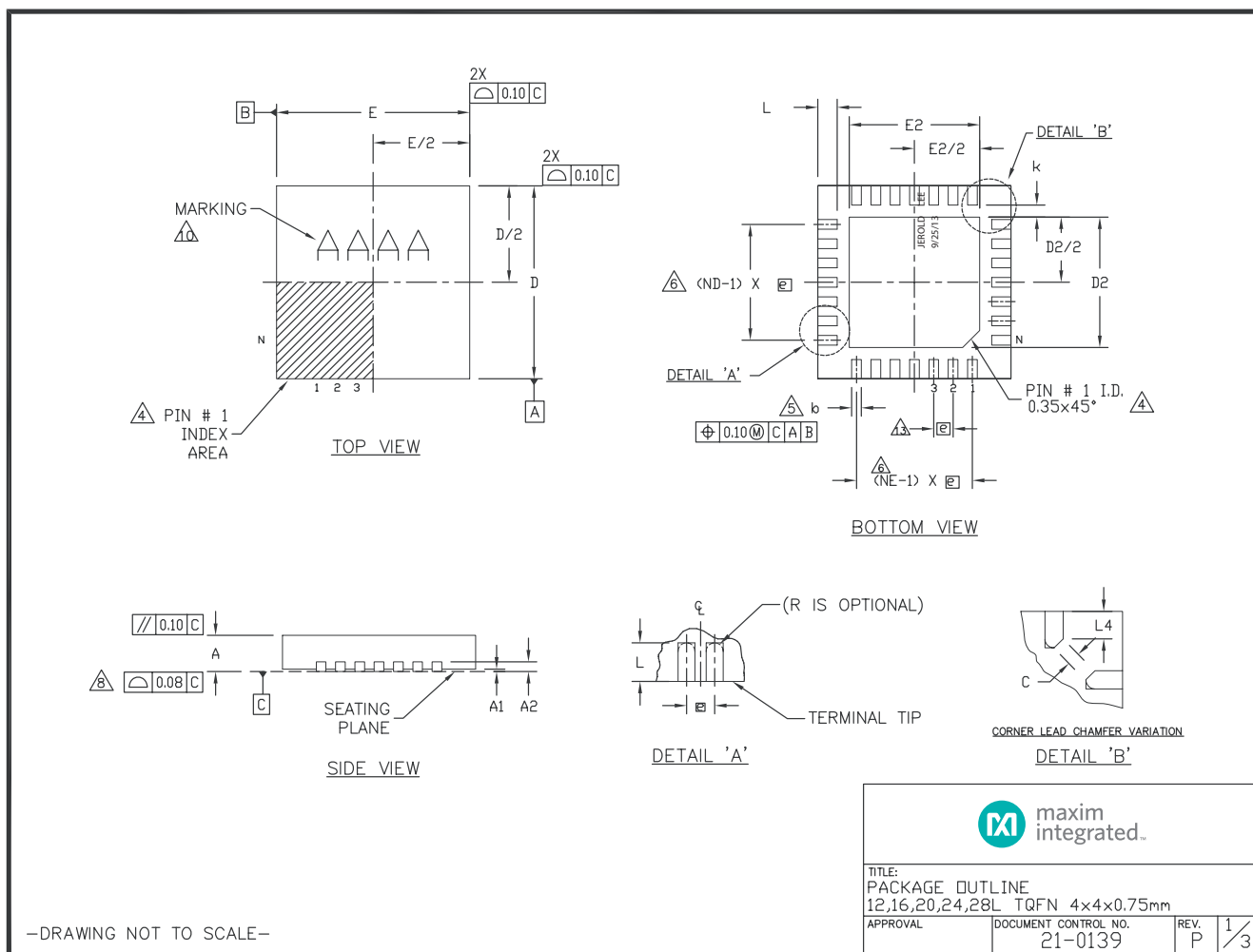
1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES IN DEGREES UNLESS OTHERWISE SPECIFIED
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE, RESPECTIVELY.
7. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
8. DRAWING CONFORMS TO JEDEC MQ220, EXCEPT FOR 0.4mm LEAD PITCH; PACKAGE T4866.
9. N IS THE TOTAL NUMBER OF TERMINALS.
10. WARPAGE SHALL NOT EXCEED 0.10mm.
11. MARKING IS FOR PACKAGE ORIENTATION PURPOSE ONLY.
12. NUMBER OF LEADS SHOWN FOR REFERENCE ONLY.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

|                                                                                                         |                                 |            |
|---------------------------------------------------------------------------------------------------------|---------------------------------|------------|
|  maxim integrated. |                                 |            |
| TITLE:<br>PACKAGE OUTLINE,<br>36, 40, 48L THIN QFN, 6x6x0.75mm                                          |                                 |            |
| APPROVAL                                                                                                | DOCUMENT CONTROL NO.<br>21-0141 | REV. K 2/2 |

## Package Information (continued)

For the latest package outline information and land patterns, go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



## Package Information (continued)

For the latest package outline information and land patterns, go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| COMMON DIMENSIONS |           |      |      |           |      |      |           |      |      |           |      |      |           |      |      |
|-------------------|-----------|------|------|-----------|------|------|-----------|------|------|-----------|------|------|-----------|------|------|
| PKG               | 12L 4x4   |      |      | 16L 4x4   |      |      | 20L 4x4   |      |      | 24L 4x4   |      |      | 28L 4x4   |      |      |
| REF.              | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. |
| A                 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 |
| A1                | 0.0       | 0.02 | 0.05 | 0.0       | 0.02 | 0.05 | 0.0       | 0.02 | 0.05 | 0.0       | 0.02 | 0.05 | 0.0       | 0.02 | 0.05 |
| A2                | 0.20 REF  |      |      | 0.20 REF  |      |      | 0.20 REF  |      |      | 0.20 REF  |      |      | 0.20 REF  |      |      |
| b                 | 0.25      | 0.30 | 0.35 | 0.25      | 0.30 | 0.35 | 0.20      | 0.25 | 0.30 | 0.18      | 0.23 | 0.30 | 0.15      | 0.20 | 0.25 |
| D                 | 3.90      | 4.00 | 4.10 | 3.90      | 4.00 | 4.10 | 3.90      | 4.00 | 4.10 | 3.90      | 4.00 | 4.10 | 3.90      | 4.00 | 4.10 |
| E                 | 3.90      | 4.00 | 4.10 | 3.90      | 4.00 | 4.10 | 3.90      | 4.00 | 4.10 | 3.90      | 4.00 | 4.10 | 3.90      | 4.00 | 4.10 |
| e                 | 0.80 BSC. |      |      | 0.65 BSC. |      |      | 0.50 BSC. |      |      | 0.50 BSC. |      |      | 0.40 BSC. |      |      |
| k                 | 0.25      | –    | –    | 0.25      | –    | –    | 0.25      | –    | –    | 0.25      | –    | –    | 0.25      | –    | –    |
| L                 | 0.45      | 0.55 | 0.65 | 0.45      | 0.55 | 0.65 | 0.45      | 0.55 | 0.65 | 0.30      | 0.40 | 0.50 | 0.30      | 0.40 | 0.50 |
| N                 | 12        |      |      | 16        |      |      | 20        |      |      | 24        |      |      | 28        |      |      |
| ND                | 3         |      |      | 4         |      |      | 5         |      |      | 6         |      |      | 7         |      |      |
| NE                | 3         |      |      | 4         |      |      | 5         |      |      | 6         |      |      | 7         |      |      |
| Jedec Var.        | WGGB      |      |      | WGGC      |      |      | WGGD-1    |      |      | WGGD-2    |      |      | WGGE      |      |      |

| DIMENSION VARIATIONS |      |      |      |      |      |      |      |      | R (LEAD TIP RADIUS) |           |
|----------------------|------|------|------|------|------|------|------|------|---------------------|-----------|
| PKG.<br>CODE         | D2   |      |      | E2   |      |      | L    |      |                     |           |
|                      | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. |                     | MAX.      |
| T2044-4              | 2.85 | 2.90 | 2.95 | 2.85 | 2.90 | 2.95 | 0.25 | 0.30 | 0.35                | 0.125 REF |
| T2044-5              | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 | 0.35 | 0.40 | 0.45                | 0.203 REF |

| EXPOSED PAD VARIATIONS |      |      |      |      |      |      |
|------------------------|------|------|------|------|------|------|
| PKG. CODES             | D2   |      |      | E2   |      |      |
|                        | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| T1244-3                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1244-4                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1644-3                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T1644-4                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2044-2                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2044-3                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2444-2                | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 |
| T2444-3                | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444-4                | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444-4C               | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444N-4               | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444M-1               | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2444MK-1              | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 |
| T2844-1                | 2.50 | 2.60 | 2.70 | 2.50 | 2.60 | 2.70 |
| T2844-1C               | 2.50 | 2.60 | 2.70 | 2.50 | 2.60 | 2.70 |
| T2844N-1               | 2.65 | 2.70 | 2.75 | 2.65 | 2.70 | 2.75 |

| CORNER LEAD CHAMFER VARIATION |                 |          |
|-------------------------------|-----------------|----------|
| PKG. CODES                    | C               | L4       |
| T2444-2                       | 0.120 X 45° REF | 0.31 REF |
| T2444-3                       | 0.120 X 45° REF | 0.31 REF |
| T2444-4                       | 0.120 X 45° REF | 0.31 REF |
| T2444-4C                      | 0.120 X 45° REF | 0.31 REF |
| T2444M-1                      | 0.120 X 45° REF | 0.31 REF |
| T2444MK-1                     | 0.120 X 45° REF | 0.31 REF |
| T2444N-4                      | 0.120 X 45° REF | 0.31 REF |

—DRAWING NOT TO SCALE—



|                                                              |                                 |           |     |
|--------------------------------------------------------------|---------------------------------|-----------|-----|
| TITLE:<br>PACKAGE OUTLINE<br>12,16,20,24,28L TQFN 4x4x0.75mm |                                 |           |     |
| APPROVAL                                                     | DOCUMENT CONTROL NO.<br>21-0139 | REV.<br>N | 2/3 |

Package Information (continued)

For the latest package outline information and land patterns, go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a “+”, “#”, or “-” in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

- NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
  2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
  3. N IS THE TOTAL NUMBER OF TERMINALS.
  4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
  5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
  6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
  7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
  8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
  9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
  10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
  11. COPLANARITY SHALL NOT EXCEED 0.08mm.
  12. WARPAGE SHALL NOT EXCEED 0.10mm.
  13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION “e”, ±0.05.
  14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
  15. MATERIAL MUST COMPLY WITH BANNED AND RESTRICTED SUBSTANCES SPEC # 10-0131.
  16. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-



TITLE:  
PACKAGE OUTLINE  
12,16,20,24,28L TQFN 4x4x0.75mm

|          |                                 |           |          |
|----------|---------------------------------|-----------|----------|
| APPROVAL | DOCUMENT CONTROL NO.<br>21-0139 | REV.<br>N | 3<br>/ 3 |
|----------|---------------------------------|-----------|----------|

## Revision History

| REVISION<br>NUMBER | REVISION<br>DATE | DESCRIPTION                    | PAGES<br>CHANGED |
|--------------------|------------------|--------------------------------|------------------|
| 0                  | 6/10             | Initial release                | —                |
| 1                  | 4/15             | Corrected Land Pattern numbers | 22               |

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at [www.maximintegrated.com](http://www.maximintegrated.com).

*Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.*