LTC6950
1.4GHz Low Phase Noise, Low Jitter PLL with Clock Distribution

DESCRIPTION

Demonstration circuit 1795A features the LTC®6950, a 1.4GHz low phase noise, low jitter PLL with clock distribution.

For ease of use, the DC1795A comes installed with a 100MHz reference and a 1GHz VCSO, voltage controlled SAW oscillator with sine wave output. All differential inputs and outputs have 0.5" spaced SMA connectors. The DC1795A has four AC coupled LVPECL outputs with 50Ω transmission lines making them suitable to drive 50Ω impedance instruments. The LVDS/CMOS output is DC coupled. The LTC6950's EZSync™ function is made available via a turret and an SMA connector.

For the evaluation of the LTC6950 with other VCOs and references, the DC1795A can be modified to accommodate different on-board or external components. It also allows the user the option of a passive or active loop filter.

A DC590 USB serial controller board is used for SPI communication with the LTC6950, controlled by the supplied ClockWizard™ software.

Design files for this circuit board are available at http://www.linear.com/demo/DC1795A

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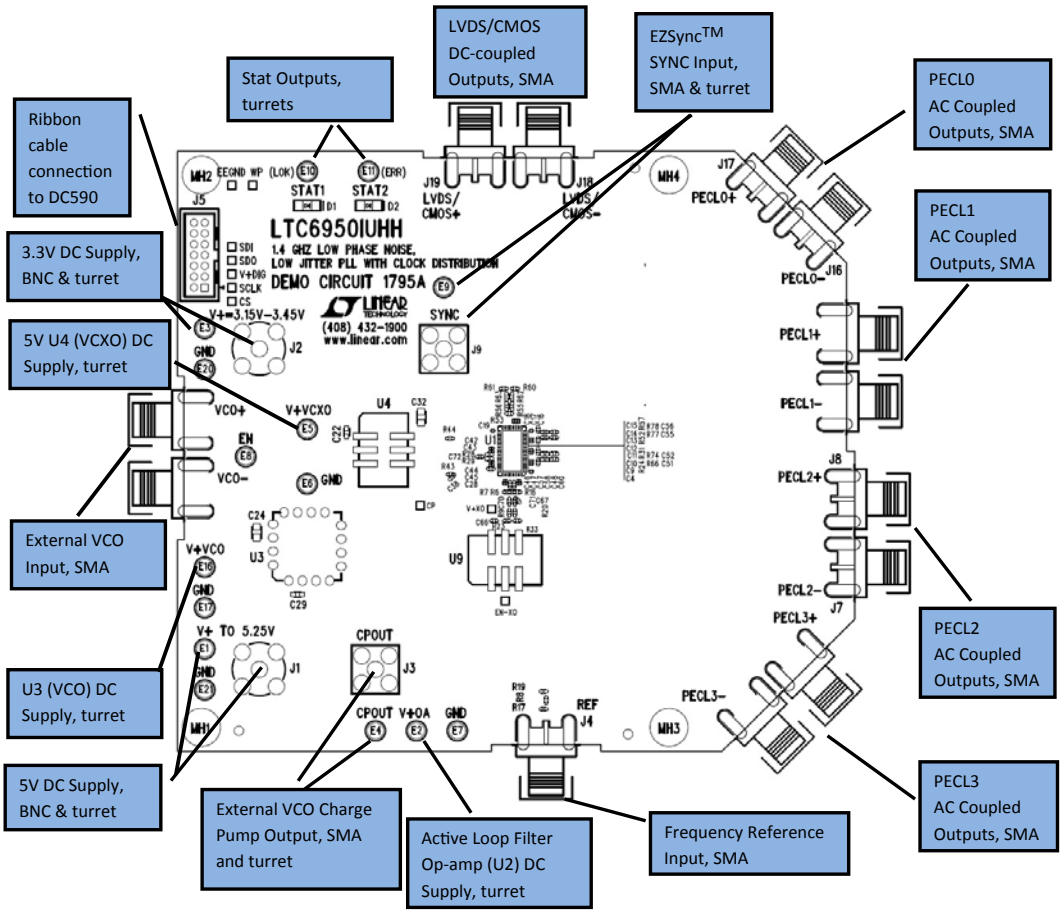


Figure 1. DC1795A Connections

QUICK START PROCEDURE

The DC1795A is easy to set up to evaluate the performance of the LTC6950. Follow the procedure below.

The DC590 and ClockWizard application are required to control the DC1795A through a personal computer (PC).

DC590 CONFIGURATION

Place the DC590 jumpers in the following positions (refer to Figure 2):

JP4: EE - Must be in the EN position.

JP5: ISO - ON must be selected.

JP5: SW - ON must be selected.

JP6: VCCIO - 3.3V or 5V must be selected. This sets the SPI port to 3.3V or 5V operation. 3.3V operation is recommended.

Connect the DC590 to one of your computer's USB ports with the included USB cable.

CLOCKWIZARD INSTALLATION

The ClockWizard software is used to communicate with the LTC6950. It uses the DC590 to translate between USB and SPI-compatible serial communications formats. It also includes advanced PLL design and simulation capabilities. The following are the ClockWizard system requirements:

- Windows Operating System: Windows XP, Windows 2003 Server, Windows Vista, Windows 7
- Microsoft .NET 3.5 SP1 or later
- Windows Installer 3.1 or later
- Linear Technology's DC590 hardware

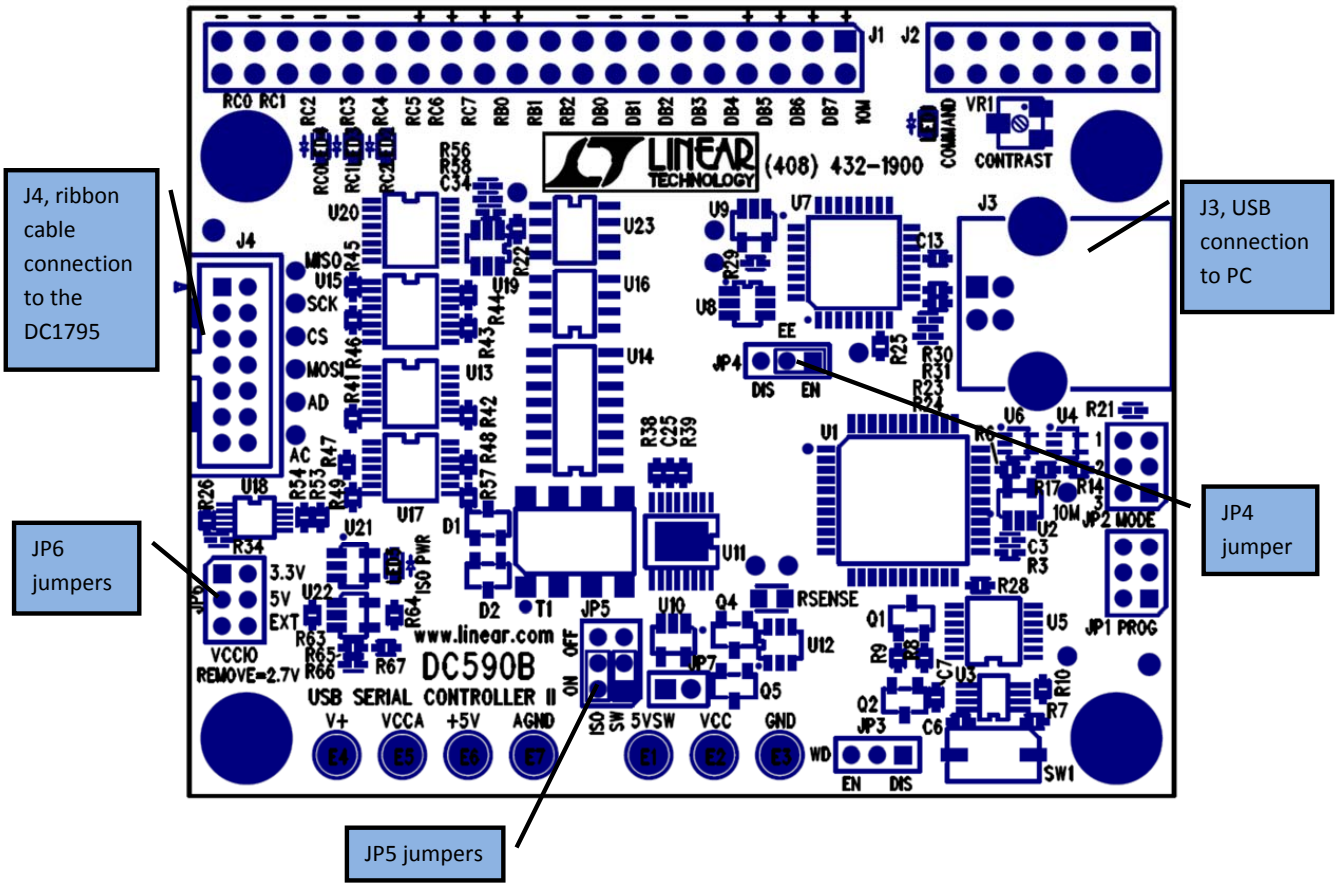


Figure 2. DC590 Jumper and Connector Locations

QUICK START PROCEDURE

Download the ClockWizard setup file at www.linear.com/ClockWizard.

Run the ClockWizard setup file and follow the instructions given on the screen. The setup file will verify and/or install Microsoft .NET and install the ClockWizard. Refer to the Help menu for software operation.

DC1795A CONFIGURATION

1. Connect the GND, V^+ = 3.15V to 3.45V, V^+ to 5.25V and V^+ VCXO turrets to a power supply and apply power (see Figure 1 and the Typical DC1795A Requirements and Characteristics table).
2. Connect the DC590 to the DC1795A with the provided ribbon cable.
3. Run the ClockWizard application.
4. In ClockWizard, click File > Load Settings and point to the “LTC6950_PECL0_250MHz.clkset” file.

The green “STAT1” LED on the DC1795A should turn on and the “STAT2” LED should turn off indicating that the loop is locked at 1000MHz. A 250MHz signal should be present on the PECL0 outputs.

Be sure to power down or terminate any unused RF output with 50Ω, or poor spurious performance may result.

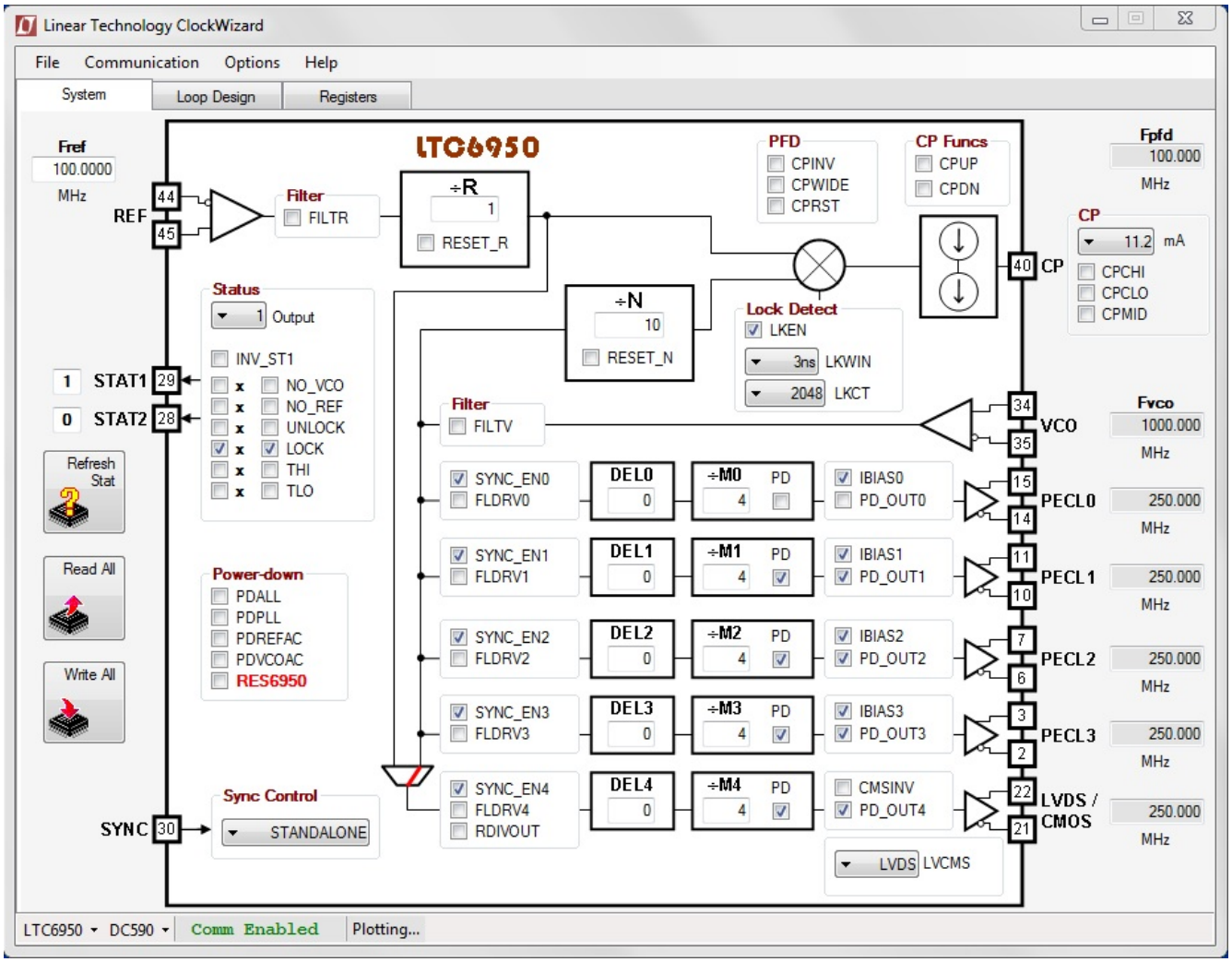


Figure 3. ClockWizard Screenshot

QUICK START PROCEDURE

TROUBLESHOOTING

If the green LED does not illuminate, follow the instructions below:

1. Verify that you are able to communicate with the DC1795A. The bottom status line in ClockWizard should read "LTC6950" and "Comm Enabled."
2. Verify that V^+ = 3.15V to 3.45V, V^+ to 5.25V and V^+ VCXO turrets have the correct voltages on them (see the Typical DC1795A Requirements and Characteristics table).
3. Select "Status" Output = 2 in ClockWizard's System Tab. Click "Read All." See if the NO_VCO or NO_REF boxes in the second column are checked.

a. If NO_REF is checked, verify the "V^+ XO" test point voltage is set to 3.3V. Verify R73 is installed (0 ohm)

b. IF NO_VCO is checked, verify the components between U4 and U1 match the default BOM.

Contact the factory for further troubleshooting.

DC1795A RECONFIGURATION

The DC1795A allows the use of a variety of references, VCOs and active or passive loop filters. The following covers the hardware reconfiguration of the DC1795A. Refer to ClockWizard and the LTC6950 data sheet to better understand how to change programmed parameters on the DC1795A.

LTC6950 CLKSET FILES

The ClockWizard provides three different clkset files for evaluation purposes. These files were made for the default bill of materials. If board modifications are made, these files or the loop filter may need to be modified for the LTC6950 to lock correctly.

1. LTC6950_PECL0_250MHz.clkset: Produces a 250MHz output on PECL0. All other outputs are powered down.
2. LTC6950_Figure16_250MHZ.clkset: Matches Figure 16 of the LTC6950 data sheet. To sync outputs, refer to the EZSync Function section.
3. LTC6950_ALL_CHAN_250MHz.clkset: Produces a 250MHz output on all five outputs. To sync outputs, refer to the EZSync Function section.

EZSync FUNCTION

Apply a 1ms or longer high pulse to the SYNC SMA connector to take advantage of the EZSync function. Refer to the LTC6950 data sheet for SYNC timing and level requirements.

LVPECL OUTPUT OPTIONS

The DC1795A has four AC coupled LVPECL outputs. Internal biasing (IBIASx = H) is required with this default termination network. The DC1795A has options for pull down or series resistors to accommodate the other LVPECL termination networks described in the data sheet.

LVDS/CMOS OUTPUT OPTIONS

The LVDS/CMOS output is DC coupled without on-board termination by default. The DC1795A provides pull down, series and a differential termination resistor options to accommodate other termination networks described in the data sheet.

DC1795A RECONFIGURATION

REFERENCE OPTIONS

Table 1 details the available reference options and board modifications for each available option. The CLKSET files described above assume the noise profile of the default reference. If a different reference is used, change the reference noise profile in ClockWizard before simulating the LTC6950 under the Loop Design tab.

VCO INPUT OPTIONS

Table 2 describes the available VCO input options. Board modifications and power requirements for each option are also provided in Table 2. There are two different oscillator footprints on the board: U3, which accommodates the popular 0.5" × 0.5" package, and U4, which accommodates another common 14mm × 9mm package with four or six pins. U4 also accommodates the smaller 5mm × 7.5mm package. An external connectorized VCO can also drive the LTC6950 through SMA connector J15. The CLKSET files described above assume the noise profile for the default VCO. If a different VCO is used, change the VCO noise profile in ClockWizard before simulating the LTC6950 under the Loop Design tab.

CLOCK FOLLOWER

When using the LTC6950 as a clock follower the LTC6950's PLL circuitry can be powered down by setting the PDPLL bit in ClockWizard. This will reduce the LTC6950's overall power consumption. Table 2 describes how to reconfigure the board for a differential external input when using the LTC6950 as a clock follower. Refer to the EZSync Function section and to the data sheet for more details on using the LTC6950 as a clock follower.

LOOP FILTER DESIGN AND INSTALLATION

Tables 3, 4 and 5 cross reference the loop filter options shown in ClockWizard's Loop Design tab with the DC1795A component reference designators. Table 3 is dedicated to the default oscillator, component U4. Table 4 is dedicated to another common oscillator footprint, component U3. Table 5 can be used with external oscillators. Use ClockWizard to select, design and simulate different loop filters.

Some VCO tuning voltage ranges are greater than the LTC6950 charge pump voltage range (refer to the LTC6950 data sheet). In such cases, an active loop filter using an op amp can deliver the required tuning voltage. When satisfied with the loop filter design, use Tables 3, 4 and 5 to help identify which components should be modified. The loop filter components are located on the bottom side of the DC1795A.

Table 1. Reference Options and Board Modifications

DEFAULT OPTION	REFERENCE OPTION	INSTALL	DEPOPULATE	LTC6950 PERFORMANCE	COMMENTS
●	On-Board	NA	NA	Limited by on board reference at frequency offsets <10kHz	U9 can accommodate any 5mm × 7.5mm or 9mm × 14mm oscillator package
	External	C67 0402 0.1µF	R73, C71	Best performance when using an ultralow noise external reference	For improved performance connect J4 to a very low noise reference, such as the Wenzel 501-04517D

DC1795A RECONFIGURATION

Table 2. VCO Input Options: Power Settings and Board Modifications

DEFAULT OPTION	OSCILLATOR	BOARD MODIFICATIONS		OSCILLATOR POWER SETTINGS				COMMENTS
		INSTALL	DEPOPULATE	V+ OA TURRET	V+ VXCO TURRET	V+ VCO TURRET	EN TURRET	
●	U4	NA (Default)	NA (Default)	[For Active Filters Only] Determined by U4 V_{TUNE} specification. 5V for Default U4. Must be less than 24V	Determined by U4 V_{CC} specification. 5V for Default U4. Must be less than 24V	-	Connects to pin 2 of U4. Not used with Default U4	Refer to Table 3: loop filter component selections for U4
	U3	U3, *C38 0402 0Ω	*R43	[For Active Filters Only] Determined by U3 V_{TUNE} specification. Must be less than 24V	-	Determined by U3 V_{CC} specification. Must be less than 24V	-	Refer to Table 4: loop filter component selections for U3
	Single-Ended External	*C25 0402 0Ω	*R25, R40, R41	[For Active Filters Only] Determined by External Oscillator V_{TUNE} specification, must be less than 24V	-	-	-	Connect signal to J15. Refer to Table 5: loop filter component selections.
	Differential External	*C25, C26 0402 0Ω C69 0402 ~100pF	*R25, R40, R41	[For Active Filters Only] Determined by External Oscillator V_{TUNE} specification, must be less than 24V	-	-	-	Connect signals to J14 and J15. [For External Oscillator Only] Refer to Table 5: loop filter component selections.

* General Recommendations: There are several termination and common mode options on the DC1795A for different input signal types. Refer to the DC1795A schematic, the LTC6950 data sheet and the data sheet for the VCO or clock distribution component used for an optimum termination network.

Table 3. Loop Filter Selection for U4 Oscillator (Refer to ClockWizard's Loop Design Tab)

DEFAULT OPTION	CLOCKWIZARD AND BOM CROSS REFERENCE							OTHER MODIFICATIONS		COMMENTS
	LOOP FILTER TYPE	RZ	CI	CP	R1	C2	L1	INSTALL	DEPOPULATE	
●	Filter 1 (Passive)	RZ_P	CI1_P + CI2_P	CP_P	-	-	-	-	-	RZ_P, CI1_P, CI2_P, CP_P populated with default values
	Filter 2 (Passive)	RZ_P	CI1_P + CI2_P	CP_P	R12	C22	-	-	-	
	Filter 3 (Passive)	RZ_P	CI1_P + CI2_P	CP_P	R72	C22	R12	-	-	
	Filter 4 (Active)	RZ_A	CI1_A + CI2_A	CP_A	R12	C22	-	R69, R71 (0402 0Ω)	R70, R72	Select CPINV under the ClockWizard System tab

Table 4. Loop Filter Selection for U3 Oscillator (Refer to ClockWizard's Loop Design Tab)

DEFAULT OPTION	CLOCKWIZARD AND BOM CROSS REFERENCE							OTHER MODIFICATIONS		COMMENTS
	LOOP FILTER TYPE	RZ	CI	CP	R1	C2	L1	INSTALL	DEPOPULATE	
	Filter 1 (Passive)	RZ_P	CI1_P + CI2_P	CP_P	-	-	-	R18 (0402 0Ω)	R12	
	Filter 2 (Passive)	RZ_P	CI1_P + CI2_P	CP_P	R18	C29	-		R12	
	Filter 3 (Passive)	RZ_P	CI1_P + CI2_P	CP_P	R72	C29	R18	-	R12	
	Filter 4 (Active)	RZ_A	CI1_A + CI2_A	CP_A	R18	C29	-	R69, R71 (0402 0Ω)	R12, R70, R72	Select CPINV under the ClockWizard System tab

DC1795A RECONFIGURATION

Table 5. Loop Filter Selection for External Oscillator (Refer to ClockWizard's Loop Design Tab)

DEFAULT OPTION	CLOCKWIZARD AND BOM CROSS REFERENCE				OTHER MODIFICATIONS		COMMENTS
	LOOP FILTER TYPE	RZ	CI	CP	INSTALL	DEPOPULATE	
	Filter 1 (Passive)	RZ_P	CI1_P + CI2_P	CP_P	R68 (0402 0Ω)	R72	Connect CPOUT turret to V_{TUNE} of external oscillator
	Filter 4 (Active)	RZ_A	CI1_A + CI2_A	CP_A	R67, R69 (0402 0Ω)	R70, R72	Select CPINV under the ClockWizard System tab. Connect CPOUT turret to V_{TUNE} of external oscillator

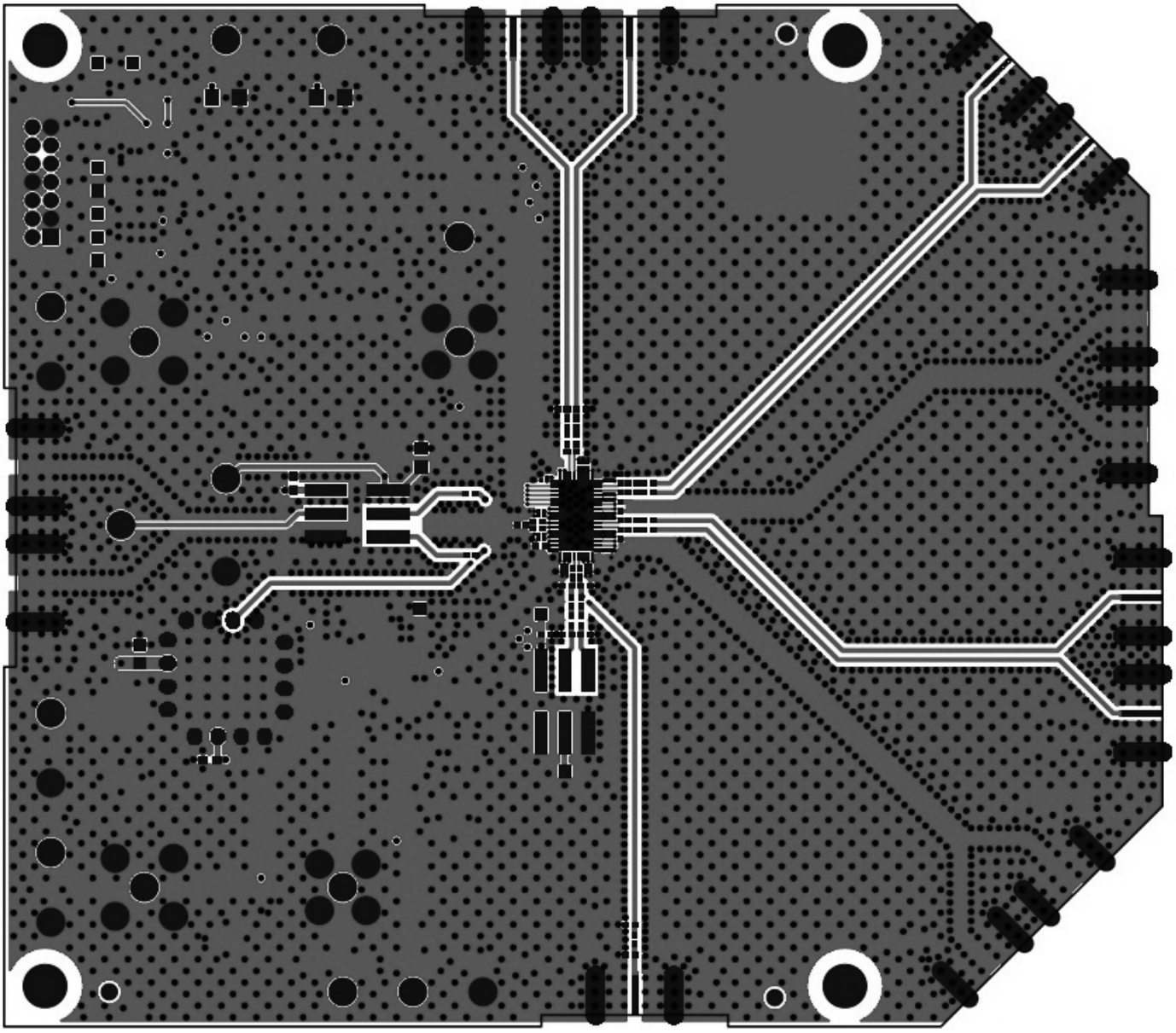
TYPICAL DC1795A REQUIREMENTS AND CHARACTERISTICS

PARAMETER	INPUT OR OUTPUT	PHYSICAL LOCATION	DETAILS
3.3V Power Supply	Input	J2 BNC connector, or V^+ = 3.15V to 3.45V turret	Low-noise and spur-free 3.3V, 500mA default (200mA configured*). Powers LTC6950, U6, U7, U8 and U9
Charge Pump Power Supply	Input	J1 BNC connector, or V^+ to 5.25V turret	Low-noise and spur-free 5V, 35mA*. Powers LTC6950 and provides common mode to U2
VCXO/VCSO Power Supply	Input	V^+ VCXO turret	Low-noise and spur-free 5V, 20mA*. Powers U4
LVDS/CMOS$^+$, LVDS/CMOS$^-$	Two Outputs	J19 and J18 SMA connectors**	DC coupled, 250MHz, (if enabled)*. Refer to LTC6950 data sheet for output levels for LVDS and CMOS option.
PECL0$^+$, PECL0$^-$	Two Outputs	J17 and J16 SMA connectors**	AC coupled, 250MHz, 800mV$_P$ differential*. Must have LTC6950's IBIAS0 = H with default BOM. DC1795A has options for an external pull down resistor if IBIAS0 = L.
PECL1$^+$, PECL1$^-$	Two Outputs	J13 and J12 SMA connectors**	AC coupled, 250MHz, 800mV$_P$ differential (if enabled)*. Must have LTC6950's IBIASX = H with default BOM. DC1795A has options for an external pull down resistor if IBIASX = L.
PECL2$^+$, PECL2$^-$	Two Outputs	J8 and J7 SMA connectors**	
PECL3$^+$, PECL3$^-$	Two Outputs	J11 and J10 SMA connectors**	
SYNC	Input	SYNC turret or J9 SMA connector	EZSync, 0V to 3.3V control signal, refer to the data sheet
STAT1, STAT2	Output	STAT1 and STAT2 turret	STAT1 GREEN LED, if ON LTC6950 is locked*. STAT2 RED LED, if ON indicates issue*. Refer to the troubleshooting section and data sheet
Loop Bandwidth	-	Set by loop filter component values	4.2kHz*
VCO Power Supply	Input	V^+ VCO turret	Board Modifications required for use, see Table 2
Active Loop Filter Supply	Input	V^+ OA turret	Board Modifications required for use, see Table 2
REF, External Reference	Input	J4 SMA connector	Board Modifications required for use, see Table 1
VCO$^+$, VCO$^-$, External VCO or Input for clock distribution	Input	J14 and J15 SMA connectors	Board Modifications required to use External VCO. See Tables 2 and 5. Clock Distribution, see Table 2 only
CPOUT	Output	CPOUT Turret	Used with External VCO, connect to external VCO's V_{TUNE} voltage

* These values are for the "LTC6950_PECL0_250MHz" file and the default on board VCO and Reference.

** Any unused RF output must be powered down or terminated with 50Ω, or poor spurious performance may result.

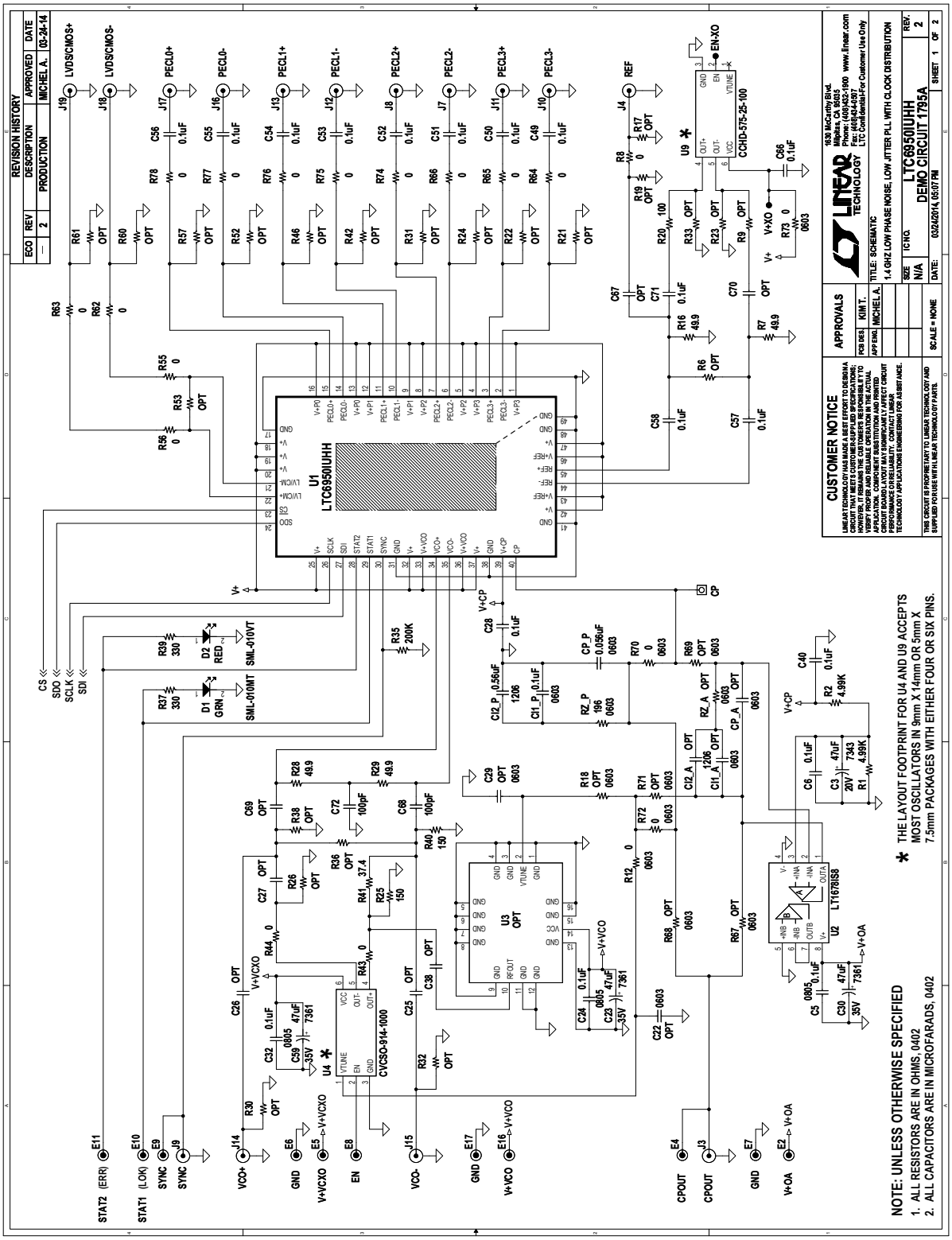
LAYOUT TOP LAYER



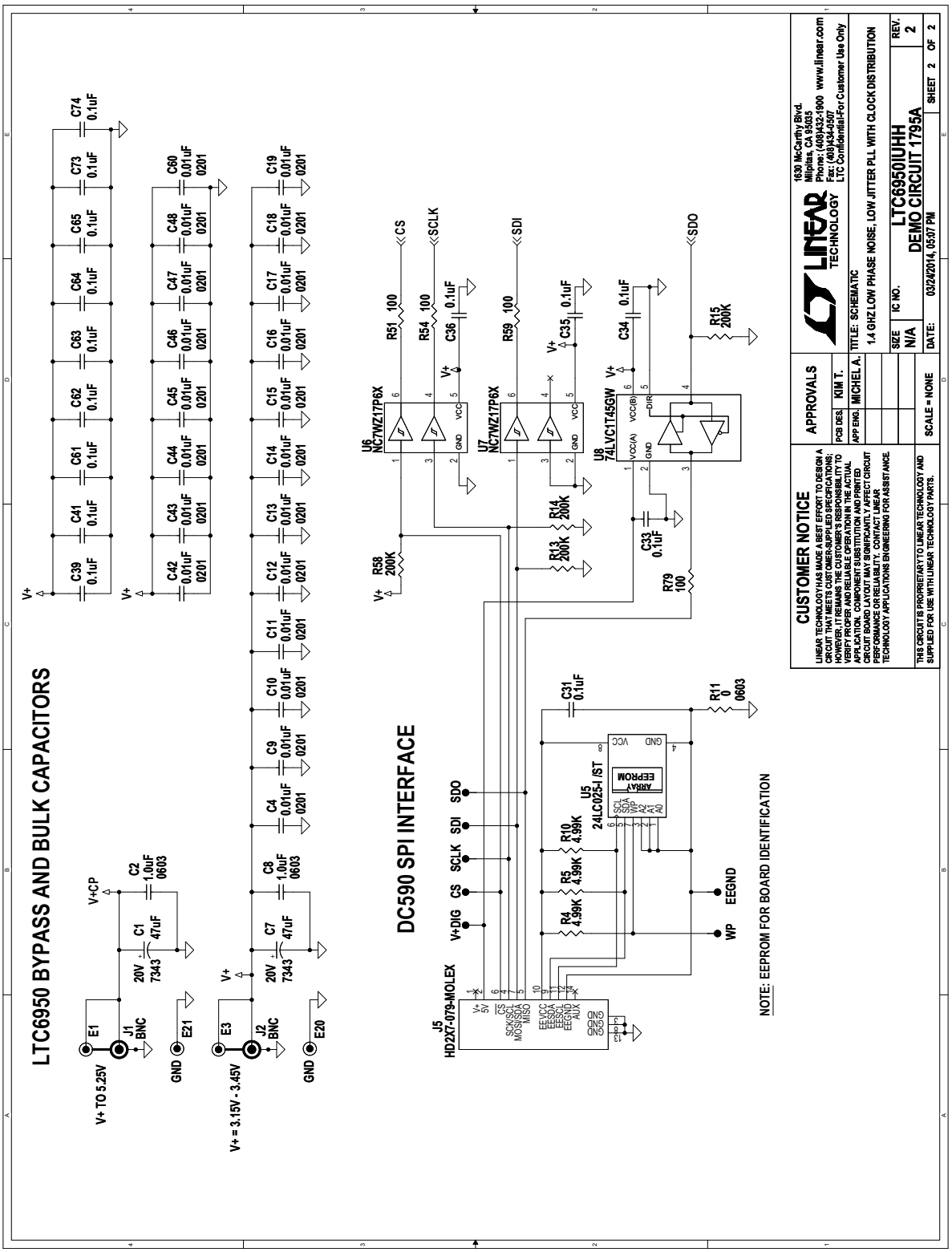
PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	0	CI1_A, C22, C29, CP_A	CAP., 0603	OPT
2	1	CI1_P	CAP., X7R, 0.1µF, 25V, 10%, 0603	AVX, 06033C104KAT2A
3	0	CI2_A	CAP., 1206	OPT
4	1	CI2_P	CAP., X7R, 0.56µF, 25V, 10%, 1206	AVX, 12063C564KAT2A
5	1	CP_P	CAP., X7R, 0.056µF, 16V, 10%, 0603	AVX, 0603YC563KAT2A
6	3	C1, C3, C7	CAP., TANT, 47µF, 20V, 20%, 7343	AVX, TAJD476M020HNJ
7	2	C2, C8	CAP., X7R, 1µF, 10V, 10%, 0603	AVX, 0603ZC105KAT2A
8	20	C4, C9-C19, C42-C48, C60	CAP., X7R, 0.01µF, 6.3V, 10%, 0201	AVX, 02016C103KAT2A
9	3	C5, C24, C32	CAP., X7R, 0.1µF, 50V, 10%, 0805	AVX, 08055C104KAT2A
10	29	C6, C28, C31, C33-C36, C39-C41, C49-C58, C61-C66, C71, C73, C74	CAP., X7R, 0.1µF, 10V, 10%, 0402	AVX, 0402ZC104KAT2A
11	3	C23, C30, C59	CAP., TANT, 47µF, 35V, 10%, 7361	AVX, TAJV476K035RNJ
12	0	C25-C27, C38, C67, C69, C70	CAP., 0402	OPT
13	2	C68, C72	CAP., NPO, 100pF, 25V, 10%, 0402	AVX, 04023A101KAT2A
14	1	D1	LED, GREEN, LED-ROHM-SML-010FT	ROHM, SML-010FTT86L
15	1	D2	LED, RED, LED-ROHM-SML-010VT	ROHM, SML-010VTT86L
16	15	E1-E11, E16, E17, E20, E21	TURRET, TESTPOINT 0.064"	MILL-MAX, 2308-2-00-80-00-00-07-0
17	2	J1, J2	CONN, BNC, 5 PINS	CONNEX, 112404
18	2	J3, J9	CONN., SMA 50Ω STRAIGHT MOUNT	CONNEX, 132134
19	13	J4, J7, J8, J10-J19	CONN., SMA 50Ω EDGE-LAUNCH	EMERSON, 142-0701-851
20	1	J5	CONN., HEADER, 14 PIN, 2mm	MOLEX, 87831-1420
21	1	RZ_P	RES., CHIP, 196Ω, 1/16W, 1%, 0603	VISHAY, CRCW0603196RFKEA
22	5	R1, R2, R4, R5, R10	RES., CHIP, 4.99k, 1/16W, 1% 0402	VISHAY, CRCW04024K99FKED
23	0	R6, R9, R17, R19, R21-R24, R26, R30-R33, R36, R38, R42, R46, R52, R57, R60, R61	RES., 0402	OPT
24	4	R7, R16, R28, R29	RES., CHIP, 49.9, 1/16W, 1% 0402	VISHAY, CRCW040249R9FKED
25	15	R8, R43, R44, R55, R56, R62-R66, R74-R78	RES., CHIP, 0Ω, 0402	VISHAY, CRCW04020000Z0ED
26	5	R11, R12, R70, R72, R73	RES., CHIP, 0Ω, 0603	YAGEO, RC0603JR-070RL
27	5	R13-R15, R35, R58	RES., CHIP, 200K, 1/16W, 1% 0402	VISHAY, CRCW0402200KFKED 2rls
28	0	R18, R67-R69, R71, RZ_A, R53	RES., 0603	OPT
29	5	R20, R51, R54, R59, R79	RES., CHIP, 100, 1/16W, 1% 0402	NIC, NRC04F1000TRF
30	2	R25, R40	RES., CHIP, 150, 1/16W, 1% 0402	VISHAY, CRCW0402150RFKED
31	2	R37, R39	RES., CHIP, 330, 1/16W, 1% 0402	VISHAY, CRCW0402330RFKED
32	1	R41	RES., CHIP, 37.4, 1/16W, 1% 0402	VISHAY, CRCW040237R4FKED
33	1	U1	I.C. LTC6950IUHH, QFN48UHH-5X9	LINEAR TECH., LTC6950IUHH#PBF
34	1	U2	I.C. LT1678IS8, SO8	LINEAR TECH., LT1678IS8#PBF
35	0	U3	VCO, 0.5" × 0.5"	OPT
36	1	U4	VCSO, 1GHz 5V	CRYSTEK, CVCSO-914-1000.000
37	1	U5	I.C., SERIAL EEPROM, TSSOP8	MICROCHIP, 24LC025-I /ST
38	2	U6, U7	I.C., DUAL BUFFER, SC70-6	FAIRCHILD SEMI., NC7WZ17P6X
39	1	U8	I.C., DUAL TRANSCEIVER, SOT363	NXP, 74LVC1T45GW
40	1	U9	CLOCK OSCILLATOR, 100MHz, 3.3V	CRYSTEK, CCHD-575-25-100.000

SCHEMATIC DIAGRAM



SCHEMATIC DIAGRAM



Note: The buffers shown on sheet 2 of 2 of the schematic are used to protect the LTC6950 when connected to the DC590 before the LTC6950 is powered up. There is no need for such circuitry if the SPI bus is not active before powering up the LTC6950. The EEPROM is for identification and is not needed to program the LTC6950.

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Please read the DEMO BOARD manual prior to handling the product. Persons handling this product must have electronics training and observe good laboratory practice standards. **Common sense is encouraged**.

This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

Mailing Address:

Linear Technology
1630 McCarthy Blvd.
Milpitas, CA 95035

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