

Evaluating the **AD7625/AD7626** 16-Bit, 6 MSPS/10 MSPS PulSAR Differential ADC

FEATURES

Full featured evaluation board for the **AD7625/AD7626**
 Versatile analog signal conditioning circuitry
 On-board reference, reference buffers, and ADC drivers
 System demonstration board compatible (**EVAL-SDP-CH1Z**)
 PC software for control and data analysis of time and frequency domain

EVALUATION KIT CONTENTS

EVAL-AD7625FMCZ/EVAL-AD7626FMCZ evaluation board

ADDITIONAL EQUIPMENT AND SOFTWARE

System demonstration platform (**EVAL-SDP-CH1Z**)

Precision source

World-compatible, 12 V dc supply adapter
 (included with **EVAL-SDP-CH1Z**)

Power supply, +7 V/–2.5 V (optional)

USB cable

SMA cable

ONLINE RESOURCES

Documents Needed

AD7625/AD7626 data sheet

EVAL-AD7625FMCZ/EVAL-AD7626FMCZ user guide

Required Software

AD7625/AD7626 evaluation software

GENERAL DESCRIPTION

The **EVAL-AD7625FMCZ/EVAL-AD7626FMCZ** are evaluation boards designed to demonstrate the low power performance of the **AD7625/AD7626** 16-bit, 6 MSPS/10 MSPS PulSAR® differential analog-to-digital converters (ADCs), and to provide an easy to understand interface for a variety of system applications. Full descriptions of the **AD7626** and **AD7625** are available in the respective product data sheets, which should be consulted in conjunction with this user guide when using this evaluation board. The user PC software executable controls the evaluation board over the USB cable through the Analog Devices, Inc., system demonstration platform board (SDP) board, **EVAL-SDP-CH1Z**.

On-board components include: the **ADR3412/ADR4540** high precision, buffered band gap 1.2 V/4.096 V reference options; the **AD8031** reference buffer; the **ADA4899-1/ADA4897-1** signal conditioning circuit with two op amps and an option to use a differential amplifier (**ADA4932-1**); and the **ADP7102**, **ADP7104**, **ADP124**, and **ADP2300** regulators to derive necessary voltage levels on board.

These evaluation boards interface to the SDP board via a 160-pin FMC connector. The SMA connectors (J3/J6 and J5/J8) are provided for the low noise analog signal source.

TYPICAL EVALUATION SETUP

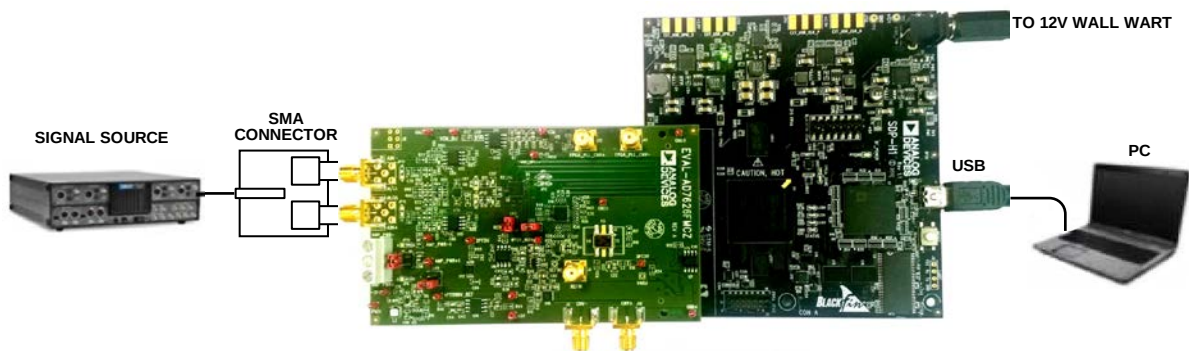


Figure 1.

12552-001

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REVISION HISTORY

8/15—Rev. 0 to Rev. A

Changes to General Description Section	1
Change to Power Supplies Section	4
Change to PLL Enable Section.....	10
Added Evaluation Board Schematics and Artwork Section, and Figure 24; Renumbered Sequentially	17
Added Figure 25.....	18
Added Figure 26.....	19
Added Figure 27.....	20
Added Figure 28.....	21
Added Figure 29 and Figure 30	22
Added Figure 31 and Figure 32	23
Added Figure 33 and Figure 34	24
Added Figure 35.....	25
Added Bill of Materials Section and Table 4	26

11/14—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

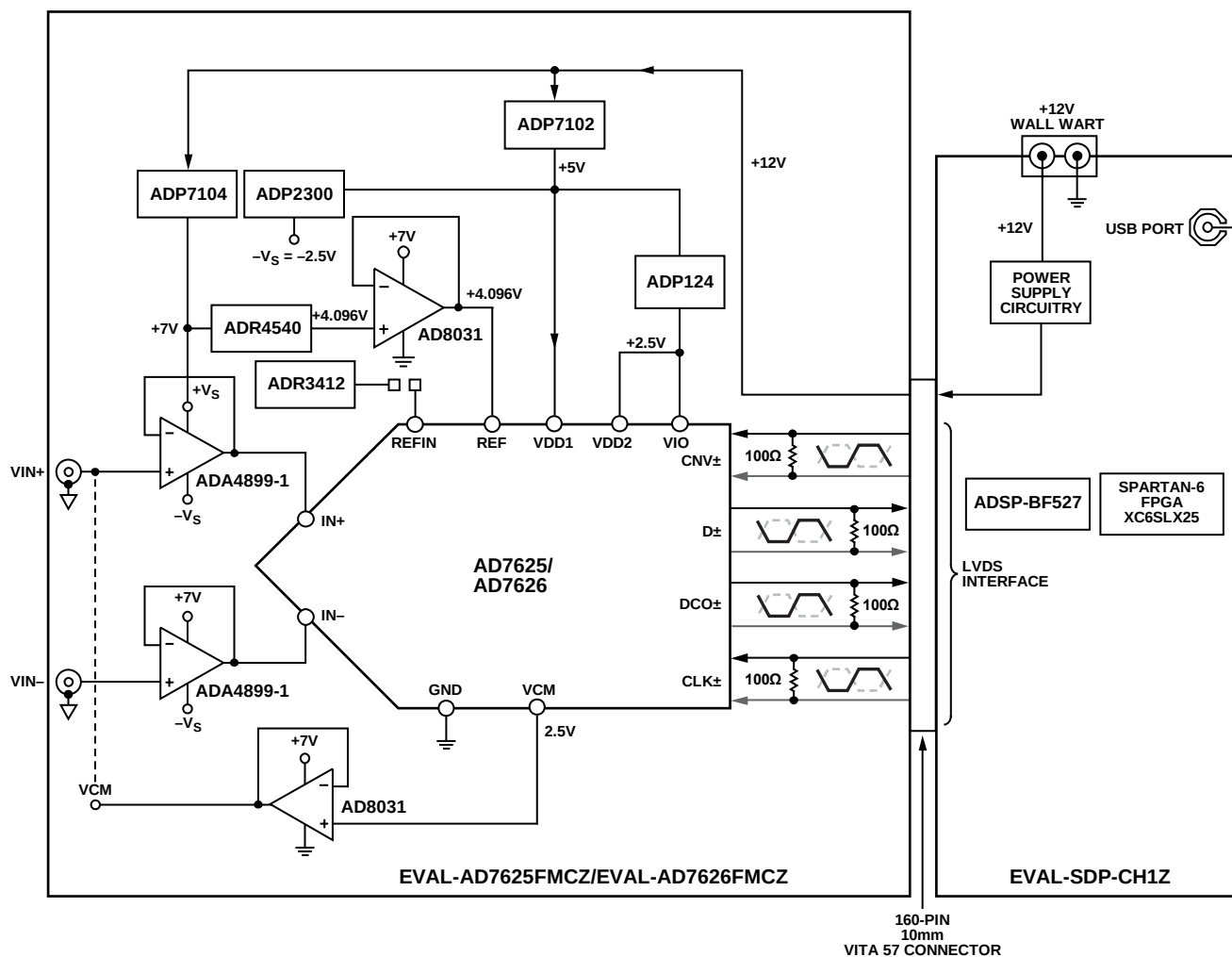


Figure 2.

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EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The [AD7625/AD7626](#) are 6 MSPS/10 MSPS, high precision, power efficient, 16-bit PulSAR ADCs that use SAR based architecture and do not exhibit any pipeline delay or latency. The [AD7625/AD7626](#) are specified for use with 5 V and 2.5 V supplies (VDD1, VDD2). The interfaces from the digital host to the [AD7625/AD7626](#) use 2.5 V logic only.

The [AD7625/AD7626](#) use an LVDS interface to transfer data conversions. Complete specifications for the [AD7625/AD7626](#) are provided in the respective product data sheets, which should be consulted in conjunction with this user guide when using the [EVAL-AD7625FMCZ/EVAL-AD7626FMCZ](#) evaluation boards. Full details on the [EVAL-SDP-CH1Z](#) are available at the SDP product page on the Analog Devices website.

HARDWARE LINK OPTIONS

The default link settings on the board and the function of the link options are described in Table 1.

Table 1. Pin Jumper Descriptions

Link	Default	Description
JP1, JP2	B to center	Connects CNV+ and CNV– from the FPGA. The A to center position connects the CNV signal from the AD9513 .
JP6	B to center	Connects 7 V to amplifier +V _s .
JP10	B to center	Connects –2.5 V to amplifier –V _s .
JP11, JP12	B to center	Connects analog inputs VIN+ and VIN– to the inputs of the ADC driver ADA4899-1 or ADA4897-1 . The A to center position sets the fully differential path through the ADA4932-1 .
JP13, JP14	B to center	Connect outputs from the ADA4899-1 to the inputs of the ADC. The A to center position sets the fully differential path through the ADA4932-1 .
LK2	Inserted	Connects REFIN to the 1.2 V external reference.
LK3	Inserted	Connects the 4.096 V output from the ADR4540 after buffer AD8031 .
LK6	B	Connects the output of the VCM buffer to the VCM of the amplifier.
LK9	A	Connects to the 7 V supply coming from the ADP7102 .
LK10	A	Connects to the –2.5 V coming from the ADP2300 .

Table 2. On-Board Connectors

Connector	Description
J1	SMA low noise, low jitter clock source input.
J2, J10	SMA CNV input. This option is for using the external CNV signal.
J3, J5, J6, J8	SMA analog input. Connects the low noise analog signal source to the inputs of the ADC driver ADA4899-1 , ADA4897-1 , or ADA4932-1 .
J4	3-pin terminal. This option is for using external bench top supplies. Apply external +V _s , –V _s , and GND to power amplifiers on the EVAL-AD7625FMCZ/EVAL-AD7626FMCZ boards.
J9	6-pin (2 × 3) socket. This option is for interfacing with an external ADC driver board.
J7	160-pin FMC 10 mm male VITA 57 connector. This connector mates with the EVAL-SDP-CH1Z board.
J11, J12	SMA low noise, low jitter clock output from the AD9513 .

POWER SUPPLIES

The power (12 V) for the [EVAL-AD7625FMCZ/EVAL-AD7626FMCZ](#) evaluation boards comes through a 160-pin FMC connector (J7) from the [EVAL-SDP-CH1Z](#) SDP board. The user also has the option of using external bench top supplies to power the on-board amplifiers. The on-board regulators generate the required levels from the applied 12 V rail.

The [ADP7102](#) (U18) supplies 7 V for the +V_s of the ADC driver amplifiers ([ADA4899-1](#) or [ADA4932-1](#)) and the external reference [ADR4540](#) (U14). The [ADP7104](#) (U10) delivers 5 V for VDD1 (U1), the external reference [ADR3412](#) (U4), the [ADP2300](#) (U5), and the [ADP124](#) (U12 and U16). The [ADP2300](#) (U5) generates –2.5 V for the amplifier –V_s. The [ADP124](#) (U12 and U16) provides a 2.5 V supply for VDD2 and VIO (U1).

The 3.3 V supply for the EEPROM (U7) comes from the [EVAL-SDP-CH1Z](#) through a 160-pin FMC connector (J7). Each supply is decoupled where it enters the board and again at each device. A single ground plane is used on this board to minimize the effect of high frequency noise interference.

Table 3. On-Board Power Supplies Description

Power Supply	Voltage Range (V)	Description
+V _s	5 to 7	The ADP7104 (U10) and ADP7102 (U18) generate the necessary 5 V and 7 V supplies, respectively, from the 12 V supply coming from the EVAL-SDP-CH1Z . The 7 V supply is recommended for the on-board amplifier +V _s . The 5 V supply is provided to VDD1 (U1), the external reference ADR3412 (U14), the ADP2300 (U5), and the ADP124 (U12 and U16). The user also has an option to use an external bench top supply +V _s through J4.
–V _s	–2 to –5	The ADP2300 generates –2.5 V for amplifier –V _s . The user also has an option to use an external bench top supply –V _s through J4.
+V _s to –V _s	12	Maximum range of supply for correct operation. ¹
VDD1	5	AD7625/AD7626 analog supply rail. ²
VDD2, VIO	2.5	ADC supply rails. ²

¹ Dictated by [ADA4899-1](#) supply operation.² Refer to the [AD7625](#) and [AD7626](#) data sheets.

SERIAL INTERFACE

The [EVAL-AD7625FMCZ/EVAL-AD7626FMCZ](#) evaluation boards use the serial interface connection to the [EVAL-SDP-CH1Z](#) SDP board. The evaluation boards operate only in echo-clocked serial interface mode. This mode requires three LVDS pairs (D $\pm$, CLK $\pm$, and DCO $\pm$) between the [AD7625/AD7626](#) and the digital host. The SDP board features include

- XILINX Spartan®-6 FPGA
- DDR2
 - Micron MT47H32M16Hr-25E:G
8 Mb $\times$ 16 bits $\times$ 4 Banks(512 Mb/64 Mb)
- SRAM
 - ISSI IS61WV25616BLL-10BLI
256 kB $\times$ 16 bits (4 Mb/512 kB)
- 1 $\times$ 160-pin FMC-LPC connector (refer to the VITA 57 specification)
 - Samtec ASP-134603-01
 - Up to 1080 Mbps LVDS
 - Single-ended LVCMOS
 - Power
- Analog Devices [ADSP-BF527](#) Blackfin® processor
 - Core performance up to 600 MHz
 - 208-ball CSP-BGA package
 - 24 MHz CLKIN oscillator
- 32 Mb flash memory
 - Numonyx M29W320EB or Numonyx M25P32
- SDRAM memory
 - Micron MT48LC16M16A2P-6A
16 Mb $\times$ 16 bits (256 Mb/32 MB)
- 2 $\times$ 120-pin small footprint connectors
 - Hirose FX8-120P-SV1(91), 120-pin header
- Blackfin processor peripherals exposed
 - SPI
 - SPORT
 - TWI/I²C
 - GPIO
 - PPI
 - Asynchronous parallel

ANALOG INPUTS

The analog inputs applied to the [EVAL-AD7625FMCZ/EVAL-AD7626FMCZ](#) are the J3 and J5 SMA (push-on) connectors. These inputs are buffered with dedicated discrete driver amplifier circuitry (U13 and U15 or U6), as shown in Figure 1.

The circuit allows different configurations, input range scaling, filtering, the addition of a dc component, the use of a different op amp, and a differential amplifier and supplies. The analog input amplifiers are set as unity-gain buffers at the factory. The driver amplifiers (U6, U13, and U15) positive rails are driven from 7 V (from [ADP7102](#), U18), and the negative rail is driven from –2.5 V. The positive rails of the other reference buffers (U8 and U11) are driven from 7 V, and the negative rails are grounded. Change these values as required.

Table 3 lists the range of possible supplies. The default configuration sets both U13 and U15 at midscale generated from a buffered reference voltage (VCM) of the [AD7625/AD7626](#) (U1). The evaluation board is factory configured to provide either a single-ended path or a fully differential path, as described in Table 1.

For dynamic performance, a fast Fourier transform (FFT) test can be performed by applying a very low distortion source.

For low frequency testing, the audio precision source can be used directly, because the outputs on these are isolated. Set the outputs for balanced and floating. Different sources can be used, though most are single ended and use a fixed output resistance.

Because the evaluation board uses the amplifiers in unity gain, the noninverting input has a common-mode input with a series 1 k Ω resistor, which must be taken into account when directly connecting a source (voltage divider).

REFERENCE OPTIONS

The [AD7625/AD7626](#) have an internal 4.096 V reference along with an internal buffer that can be used with an external reference, or the devices can be used directly with an external 4.096 V reference. The [EVAL-AD7625FMCZ/EVAL-AD7626FMCZ](#) evaluation boards can be configured to use any of these references. To use the internal ADC reference, leave LK2 and LK3 open. To use the [ADR4540](#), insert LK3 and leave LK2 open. (The 4.096V output of the [ADR4540](#) is buffered by an [AD8031](#) in a unity-gain configuration.)

To use the internal reference buffer on the [AD7625/AD7626](#) REFIN pin, insert LK2 and leave LK3 open. The 1.2 V reference voltage is applied to REFIN prior to the internal buffer in the [AD7625/AD7626](#), which creates the required internal 4.096 V reference. (The 1.2 V output of the [ADR3412](#) is buffered by an [AD8031](#) in a unity-gain configuration). The various options for using this reference are controlled by the EN1 and EN0 pins (EN bits on software), as described in the [AD7625/AD7626](#) data sheets.

LAYOUT GUIDELINES

When laying out the printed circuit board (PCB) for the [AD7625/AD7626](#), follow these recommended guidelines to obtain the maximum performance from the converter.

- Solder the [AD7625/AD7626](#) (Pin 33) directly to the PCB and connect the paddle to the ground plane of the board using multiple vias.
- Decouple all the power supply pins (VDD1, VDD2, and VIO) and the REF pin with low ESR and low ESL ceramic capacitors, typically 10 μ F and 100 nF, placed close to the DUT (U1) and connected using short, wide traces. This provides low impedance paths and reduces the effect of glitches on the power supply lines.
- Use a 50 Ω single-ended trace and a 100 Ω differential trace.
- Separate analog and digital sections and keep power supply circuitry away from the [AD7625/AD7626](#).
- Avoid running digital lines under the device as well as crossover of digital and analog signals because these couple noise into the [AD7625/AD7626](#).
- Do not run fast switching signals, such as CNV or clocks, near analog signal paths.
- Remove the ground and power plane beneath the input (including feedback) and output pins of the amplifiers (U6, U13, and U15), because they create an undesired capacitor.

BASIC HARDWARE SETUP

The [EVAL-AD7625FMCZ/EVAL-AD7626FMCZ](#) evaluation boards connect to the [EVAL-SDP-CH1Z](#) SDP board. The SDP board is the controller board, which is the communication link between the PC and the main evaluation board.

1. Figure 1 shows a photograph of the connections made between the [EVAL-AD7625FMCZ/EVAL-AD7626FMCZ](#) daughter board and the [EVAL-SDP-CH1Z](#) SDP controller board.
2. Install the [AD7625/AD7626](#) evaluation software. Ensure that the SDP board is disconnected from the USB port of the PC while installing the software. The PC must be restarted after the installation.
3. Before connecting power, connect the 160-pin FMC connector (J7) on the evaluation board to Connector J4 on the SDP board. Nylon screws are included in the evaluation kit and can be used to ensure that the evaluation board and the SDP board are connected firmly together.
4. Connect the 12 V power supply adapter included in the kit to the SDP board.
5. Connect the SDP board to the PC via the USB cable. Windows® XP users may need to search for the [EVAL-SDP-CH1Z](#) drivers. Choose to automatically search for the drivers for the SDP board if prompted by the operating system.
6. Launch the [AD7625/AD7626](#) evaluation software from the **Analog Devices** subfolder in the **Programs** menu. The full software installation procedure is described in the Evaluation Board Software section.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The evaluation board software is available to download from the [EVAL-AD7625FMCZ/EVAL-AD7626FMCZ](#) evaluation board pages on the Analog Devices website. Double-click the **setup.exe** file to run the install. The default location for the software is **C:\Program Files (x86)\Analog Devices\AD7626_25 Evaluation Software**.

Install the evaluation software before connecting the evaluation board and the [EVAL-SDP-CH1Z](#) board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

There are two parts of the software installation process:

- [AD7625/AD7626](#) evaluation software installation
- [EVAL-SDP-CH1Z](#) board drivers installation

Figure 3 to Figure 9 show the steps to install the [AD7625/AD7626](#) evaluation software, and Figure 10 to Figure 14 show the steps to install the [EVAL-SDP-CH1Z](#) drivers.

Proceed through all of the installation steps to install the software and drivers in the appropriate locations.

Connect the [EVAL-SDP-CH1Z](#) board to the PC only after the software and drivers have been installed.

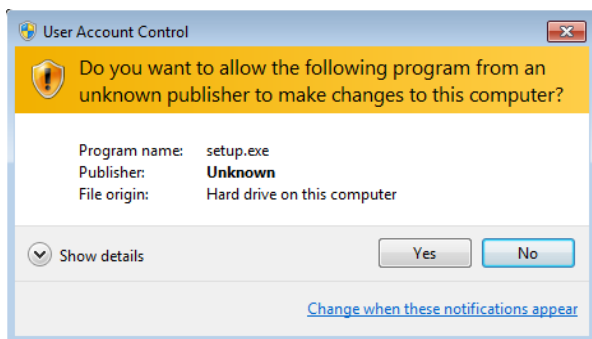


Figure 3. User Account Control

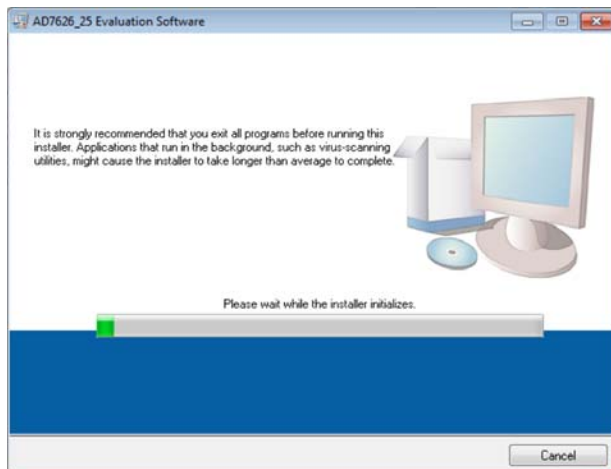


Figure 4. Evaluation Software Installation—Initializing

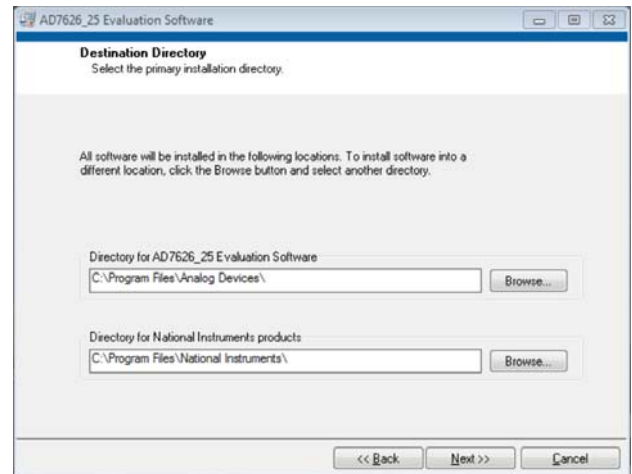


Figure 5. Evaluation Software Installation—Choose Install Location

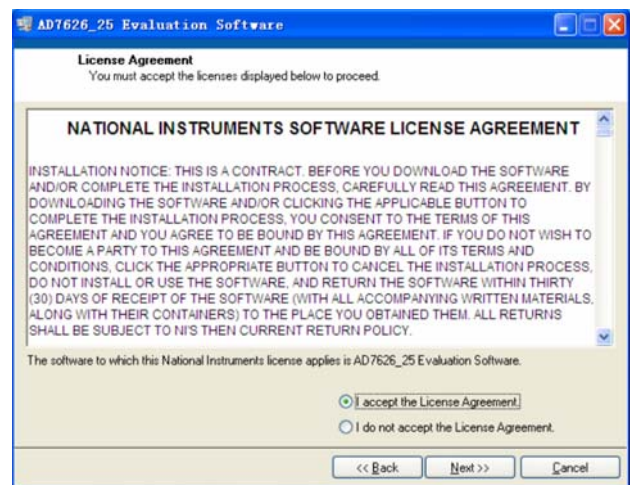


Figure 6. Evaluation Software Installation—License Agreement

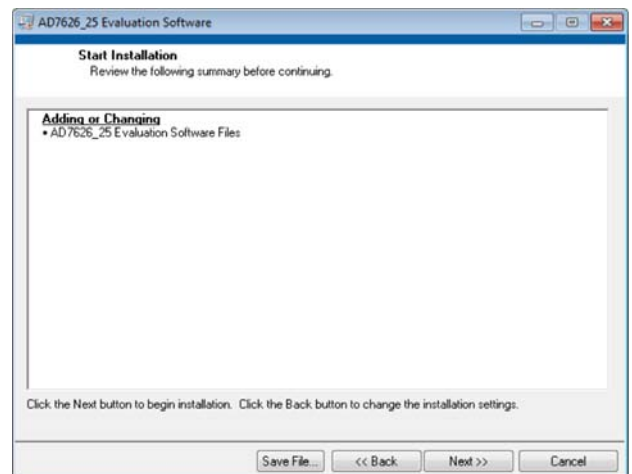


Figure 7. Evaluation Software Installation—Summary

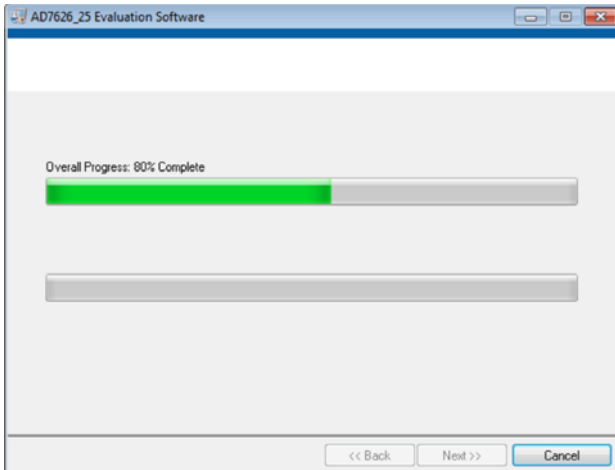


Figure 8. Evaluation Software Installation—In Progress

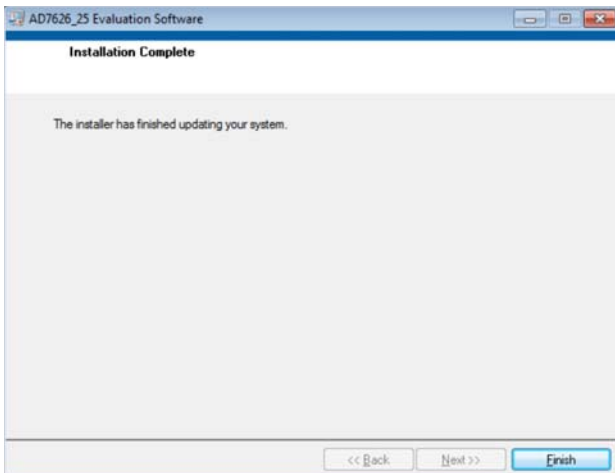


Figure 9. Evaluation Software Installation—Complete

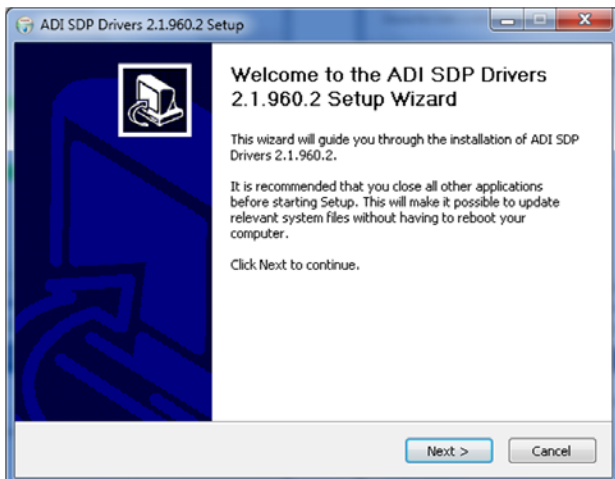


Figure 10. EVAL-SDP-CH1Z Drivers Setup—Welcome

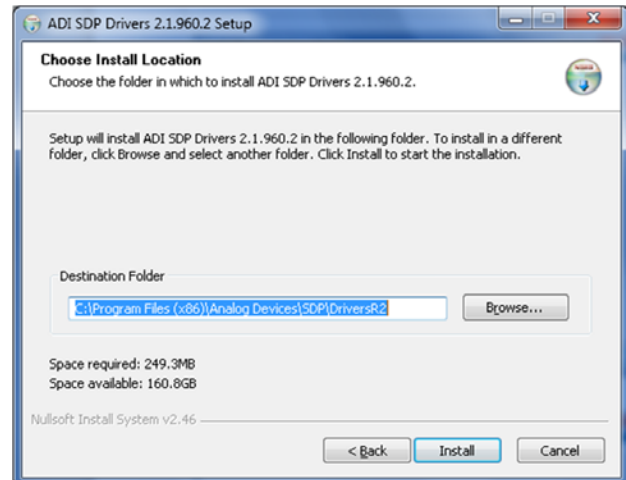


Figure 11. EVAL-SDP-CH1Z Drivers Setup—Choose Install Location

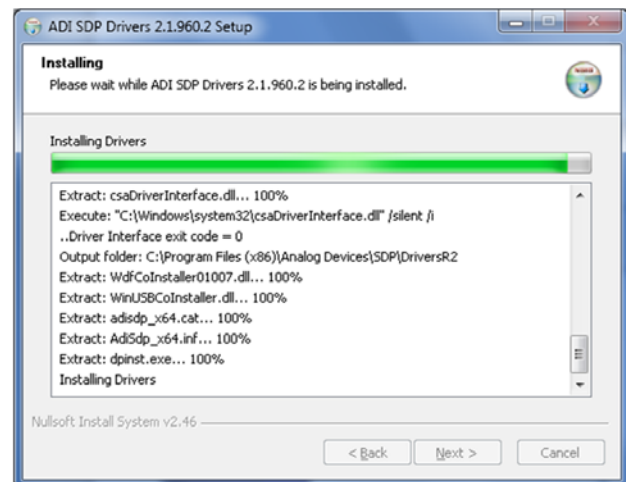


Figure 12. EVAL-SDP-CH1Z Drivers Setup—Installing Drivers

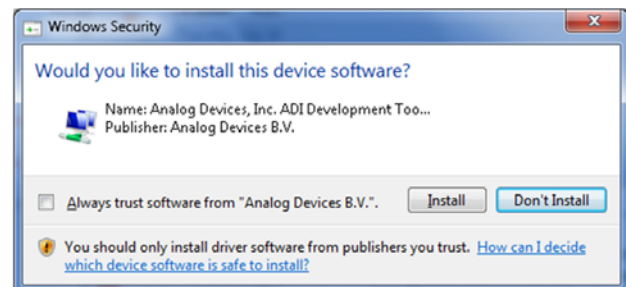


Figure 13. EVAL-SDP-CH1Z Drivers Setup—Windows Security

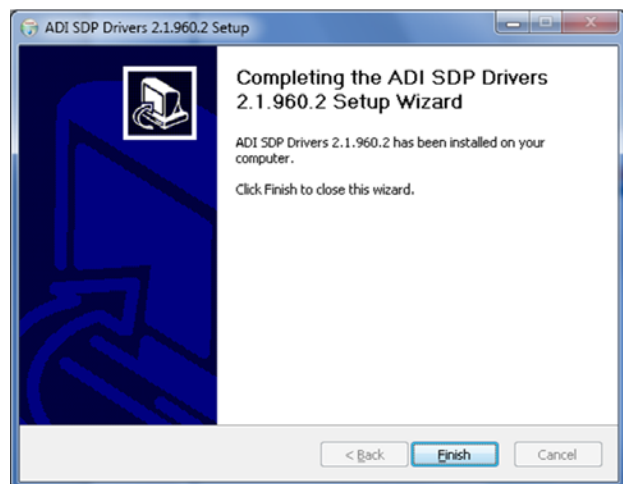


Figure 14. EVAL-SDP-CH1Z Drivers Setup—Installation Complete

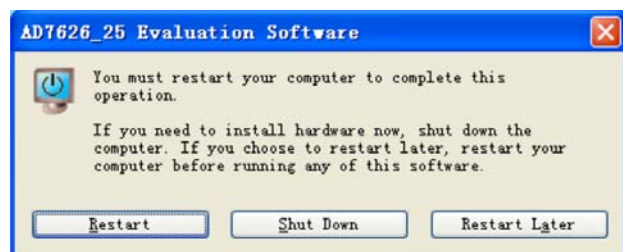


Figure 15. Restart Required

After installation is complete, connect the evaluation board to the SDP board as described in the Evaluation Board Hardware section.

When the SDP board is first plugged in via the USB cable provided, allow the new **Found Hardware Wizard** to run. Once the drivers are installed, check that the board has connected correctly by looking at the **Device Manager** of the PC. The **Device Manager** can be accessed via **My Computer > Manage > Device Manager** from the list of **System Tools**. The **EVAL-SDP-CH1Z** board appears under **ADI Development Tools**, which indicates that the installation is complete.

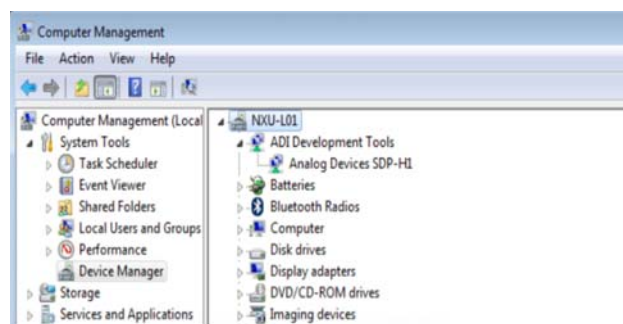


Figure 16. Device Manager

LAUNCHING THE SOFTWARE

When the evaluation board and the SDP board are correctly connected to the PC, the [AD7625/AD7626](#) evaluation software can be launched.

1. From the **Start** menu, click **Programs > Analog Devices > AD7626_25 Evaluation Software**. The main window of the software then displays (see Figure 19).
 - a. If the evaluation system is not connected to the USB port via the [EVAL-SDP-CH1Z](#) when the software is launched, a connectivity error displays (see Figure 17).
 - b. Connect the evaluation board to the USB port of the PC.
 - c. Wait for a few seconds and then click **Rescan** (see Figure 18).

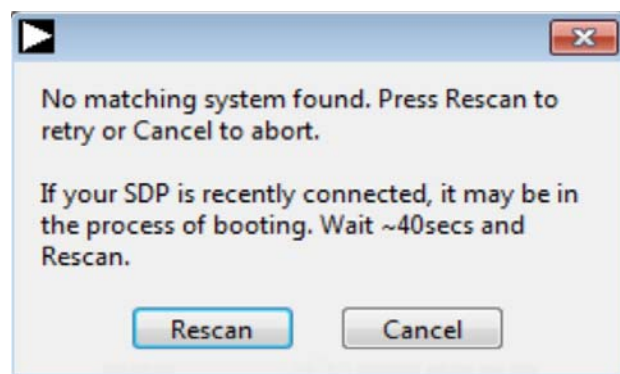


Figure 17. Connectivity Error Alert 1

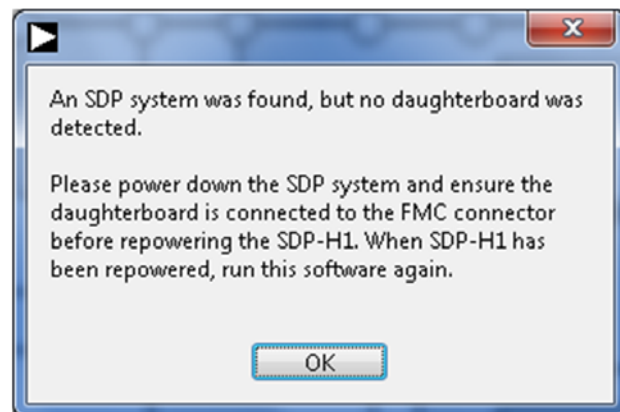


Figure 18. Connectivity Error Alert 2

SOFTWARE OPERATION

This section describes the full software operation and all the windows that appear. When the software is launched, the main software window opens, and the software searches for hardware connected to the PC. The user evaluation software launches as shown in Figure 19. The labels listed in this section correspond to the numbered labels in Figure 19.

File Menu

The **File** menu, Label 1 in Figure 19, has the following options:

- **Save Captured Data:** saves data to a .CSV file
- **Load Captured Data:** loads data for analysis
- **Take Screenshot:** saves the current screen
- **Print:** prints the window to the default printer
- **Exit:** closes the application

Edit Menu

The **Edit** menu, Label 2 in Figure 19, provides the option to **Initialize to Default Values**, which resets the software to its initial state.

Help Menu

The **Help** menu, Label 3 in Figure 19, offers help from the

- **Analog Devices website**
- **User Guide**
- **Context Help**
- **About**

Throughput

The **Throughput** field, Label 4 in Figure 19, controls the throughput. The default throughput (sampling frequency) is 10,000 kSPS for the [AD7626](#), and 6000 kSPS for the [AD7625](#). The user can adjust the sampling frequency; however, there are limitations around the sample frequency related to the SCLK frequency applied. The sample frequency must be at least 500 kSPS. If the user enters a value exceeding the ability of the ADC (the [AD7625/AD7626](#) have a maximum sample frequency of 10M/6M), the software indicates this, and the user must revert to the maximum sample frequency.

Samples

From the **Samples** drop-down menu, Label 5 in Figure 19, select the number of samples to analyze when running the software; this number is limited to 1,048,576 samples.

Single Capture and Continuous Capture

Clicking **Single Capture**, Label 6 in Figure 19, performs a single capture. Clicking **Continuous Capture**, Label 7 in Figure 19, performs a continuous capture from the ADC.

Eval Board Connected

The **Eval Board Connected** indicator, Label 8 in Figure 19, shows that the evaluation board is connected. In Figure 19, the connected evaluation board is the [EVAL-AD7626FMCZ](#).

Voltage Reference

The various options for using the external reference are controlled by the **Control Pins** drop-down menu, Label 9 in Figure 19. The default value is set to 4.096 V (internal reference). The other options are external reference 4.096 V, external 1.2 V, and power down. It is recommended to use an on-board [AD8031](#) device as an external reference buffer.

PLL Enable

The **PLL Enable** check box, Label 10 in Figure 19, is used when the CNV signal is coming from the [AD9513](#). The positions of JP1 and JP2 must also be changed to A connected to center.

Tabs

There are four additional tabs available for displaying the data in different formats.

- Waveform
- Histogram
- FFT
- Summary

To exit the software, go to **File > Exit**.

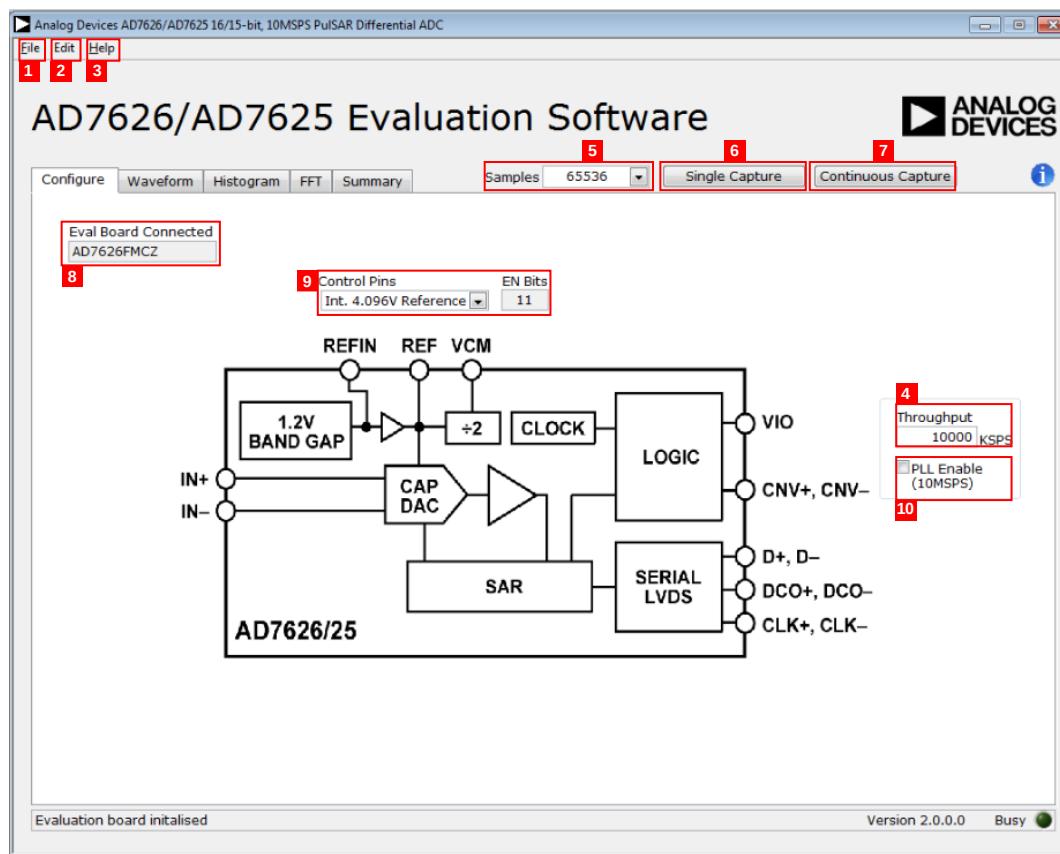


Figure 19. Evaluation Software Window

WAVEFORM CAPTURE

Figure 20 shows the **Waveform** tab. A 20 kHz sine-wave input signal was used along with an on-board 4.096 V external reference.

The **Waveform Analysis** boxes, Label 1 in Figure 20, show the amplitudes recorded from the captured signal in addition to the frequency of the signal tone.

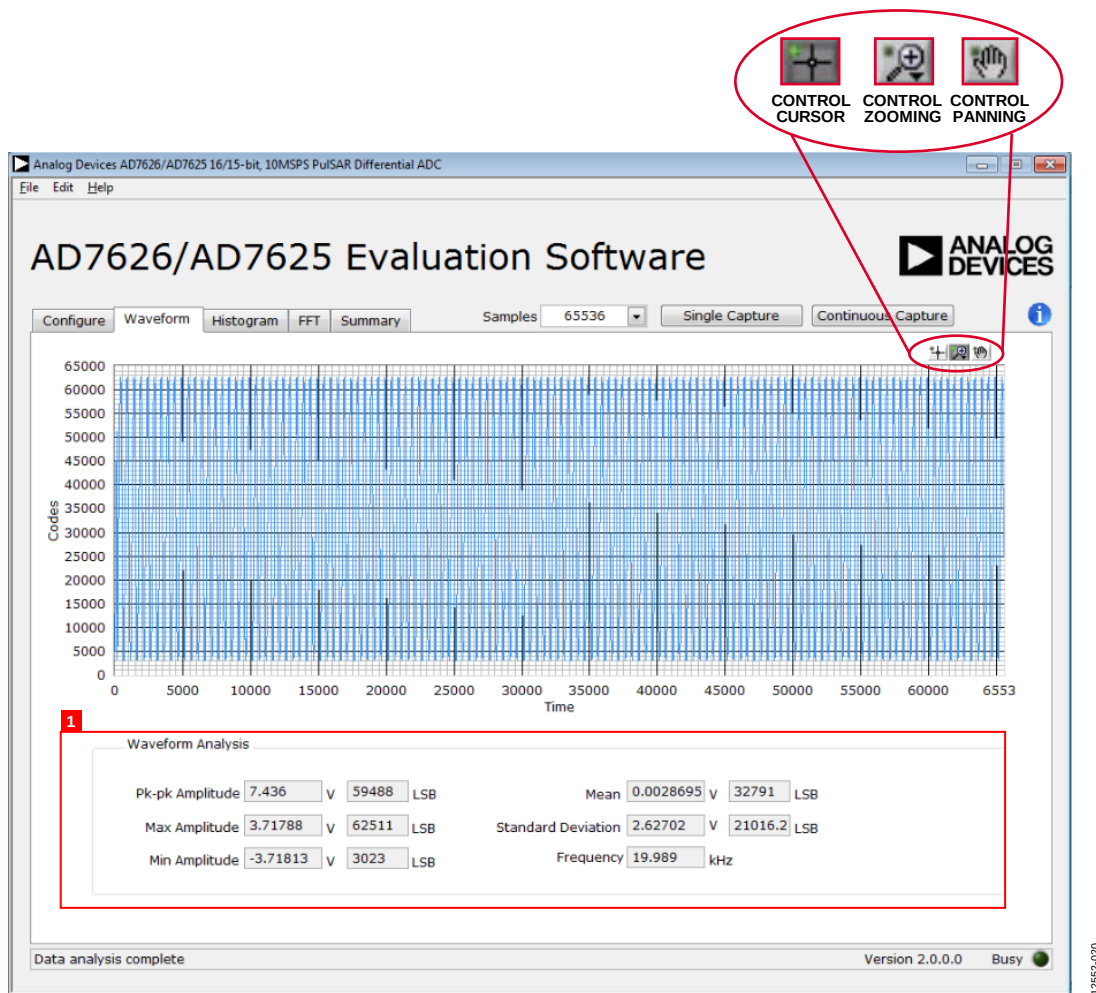


Figure 20. Waveform Capture Tab

DC TESTING—HISTOGRAM

Figure 21 shows the **Histogram** tab. The histogram can be used to test the ADC for the code distribution for dc input, compute the mean and standard deviation or transition noise of the converter, and display the results. Raw data is captured and passed to the PC for statistical computations.

To perform a histogram test, click the **Histogram** tab, then click **Single Capture** or **Continuous Capture**.

A histogram test can be performed without an external source because the evaluation board has a buffered $V_{REF}/2$ source at the ADC input.

To test other dc values, apply a source to the J3 and J5 inputs. The signal may need to be filtered so that the dc source noise is compatible with that of the ADC.

AC TESTING—HISTOGRAM

The histogram can also be used to test the ADC for the code distribution for ac input, compute the mean and standard deviation or transition noise of the converter, and display the results. Raw data is captured and passed to the PC for statistical computations.

To perform a histogram test, click the **Histogram** tab, then click **Single Capture** or **Continuous Capture**.

An AC histogram requires a quality signal source applied to the input J3 and J5 connectors.

Figure 21 shows the histogram for a 20 kHz sine wave applied to the ADC input and the results calculated.

The **Histogram Analysis** boxes, Label 1 in Figure 21, show the various measured values for the data captured.

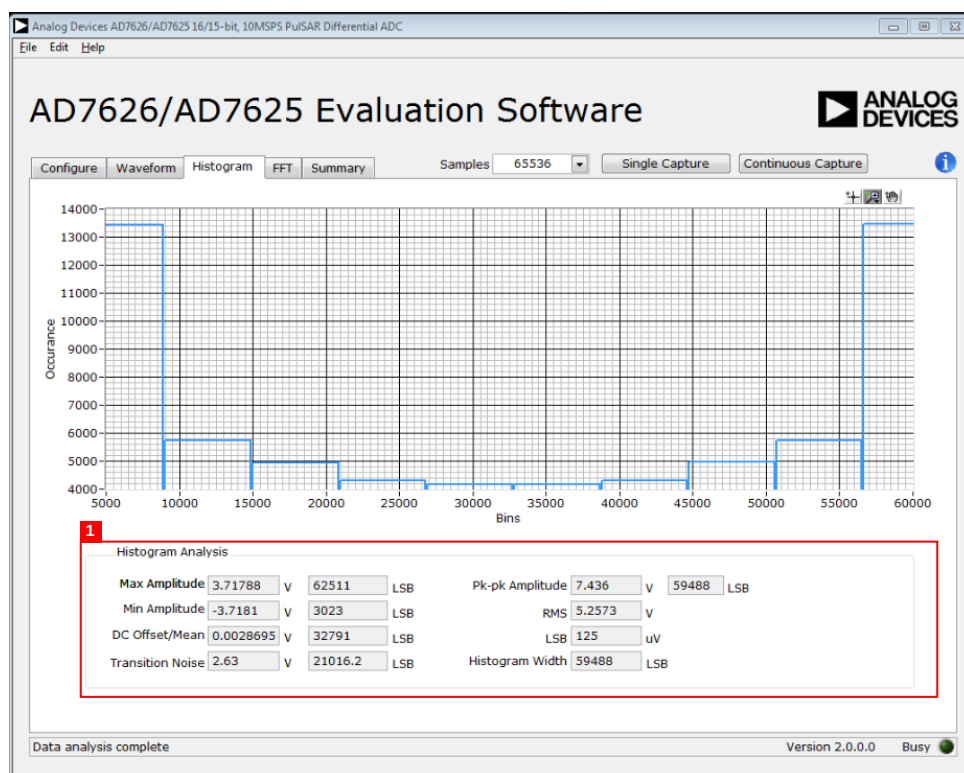


Figure 21. Histogram Capture Tab

AC TESTING—FFT CAPTURE

Figure 22 shows the FFT tab. This tests the traditional ac characteristics of the converter and displays a FFT of the results. As in the histogram test, raw data is captured and passed to the PC where the FFT is performed to display the signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SINAD), total harmonic distortion (THD), and spurious-free dynamic range (SFDR).

To perform an ac test, apply a sinusoidal signal to the evaluation board at the SMA inputs, J1 and J2. A very low distortion, better than 130 dB input signal source (such as audio precision) is required to allow true evaluation of the device. One possibility is to filter the input signal from the ac source. There is no suggested band-pass filter, but carefully consider the choices. Furthermore, if using a low frequency band-pass filter when the

full-scale input range is more than a few volts peak-to-peak, it is recommended to use the on-board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.

Figure 22 displays the results of the captured data.

FFT Analysis shows the input signal information (Label 1 in Figure 22), as well as the performance data, including SNR, dynamic range, THD, SINAD, and noise performance (Label 3 in Figure 22).

Show Harmonic Content displays the fundamental frequency and amplitude in addition to the second to fifth harmonics (Label 2 in Figure 22).

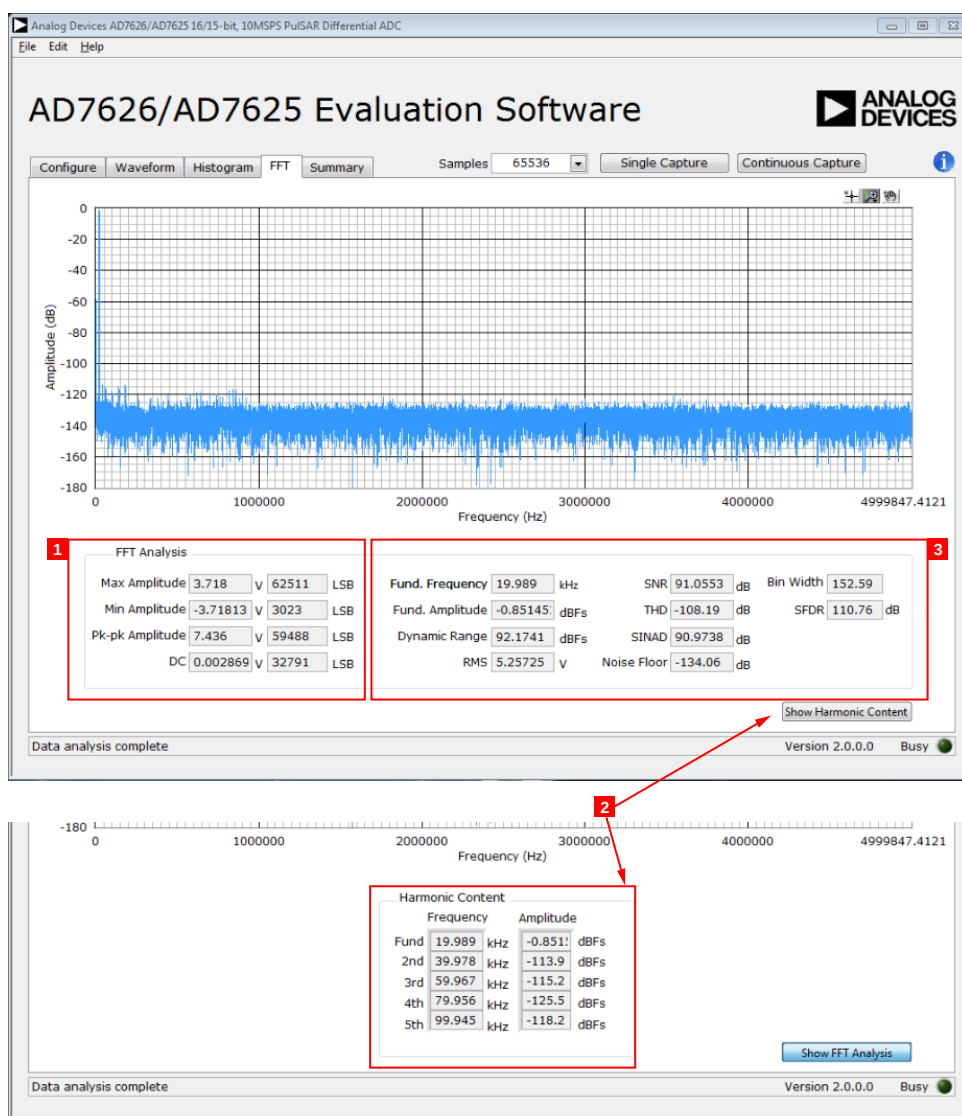


Figure 22. FFT Capture Tab

SUMMARY TAB

Figure 23 shows the **Summary** tab, which captures all the display information and provides it in one tab with a synopsis of the information, including key performance parameters such as SNR and THD.

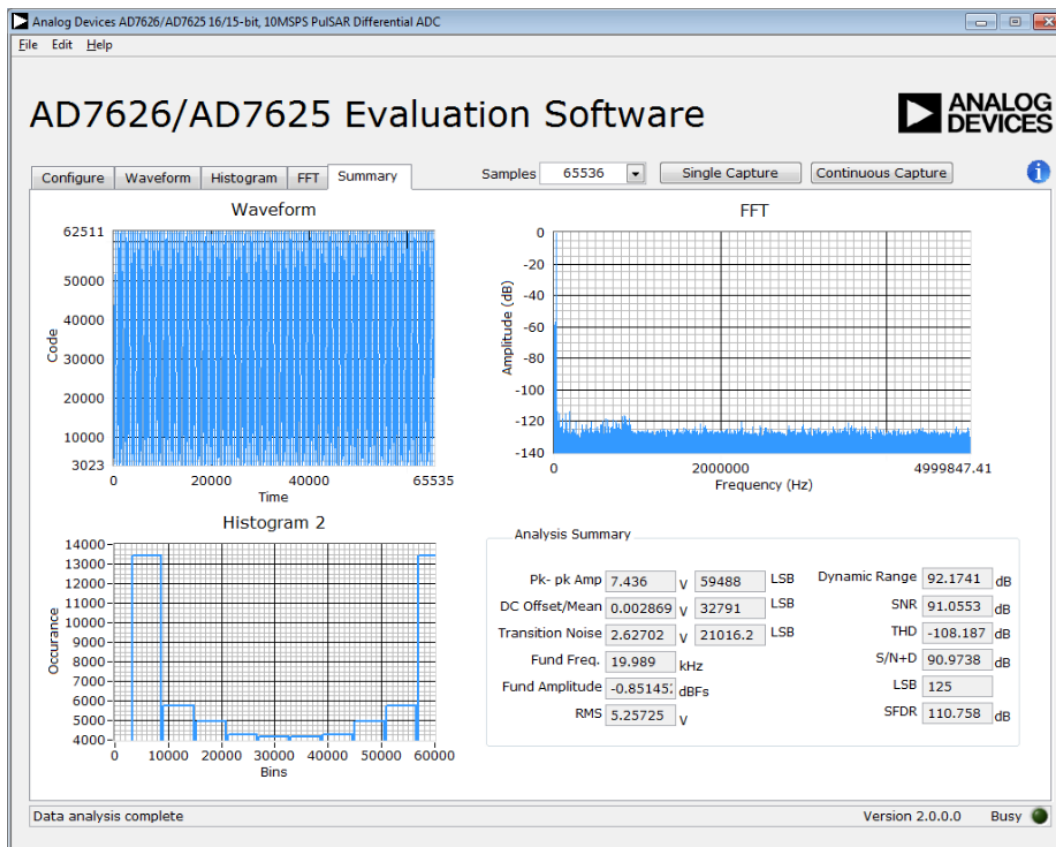


Figure 23. Summary Tab

TROUBLESHOOTING

This section provides recommendations on how to prevent and troubleshoot problems encountered with the software and the hardware.

SOFTWARE

Follow these recommendations for the evaluation software:

- Always install the software prior to connecting the hardware to the PC.
- Always allow the install to fully complete (the software installation is a two-part process: installing the ADC software and the SDP drivers). This may require a restart of the PC.
- When first plugging in the SDP board via the USB cable provided, allow the new **Found Hardware Wizard** to run. Though this may take time, do this prior to starting the software.
- If the board does not appear to be functioning, ensure that the ADC evaluation board is connected to the SDP board and that the SDP board is recognized in the **Device Manager**, as shown in Figure 16.
- If connected to a slower USB port where the SDP board cannot read quickly, a timeout error may occur. In this case, it is advised not to read continuously or, alternatively, to lower the number of samples taken.
- Note that when reading continuously from the ADC, the recommended number of samples is up to 1,048,576.

HARDWARE

If the software does not read any data back, take the following steps:

- With the 12 V wall wart plugged in to the SDP board, check that the voltage applied is within the ranges shown in Table 3.
- Using a digital multimeter (DMM), measure the voltage present at 12 V and the VADJ test points, which should read 12 V and 2.5 V, respectively. The +12V_FMC LED of the evaluation board and the LEDs of the SDP board (FMC_PWR_GO, SYS_PWR, FPGA_DONE, BF_POWER, LED0, and LED2) should all be lit.
- Launch the software and read the data. If nothing happens, exit the software.
- Remove the 12 V wall wart and USB from the SDP board, and then reconnect them and relaunch the software.
- If an error occurs, check that the evaluation board and the SDP board are connected together so that the evaluation board is recognized in the **Device Manager**, as shown in Figure 16.

Note that when working with the software in standalone/offline mode (no hardware connected) and later choose to connect hardware, first close and then relaunch the software.

EVALUATION BOARD SCHEMATICS AND ARTWORK

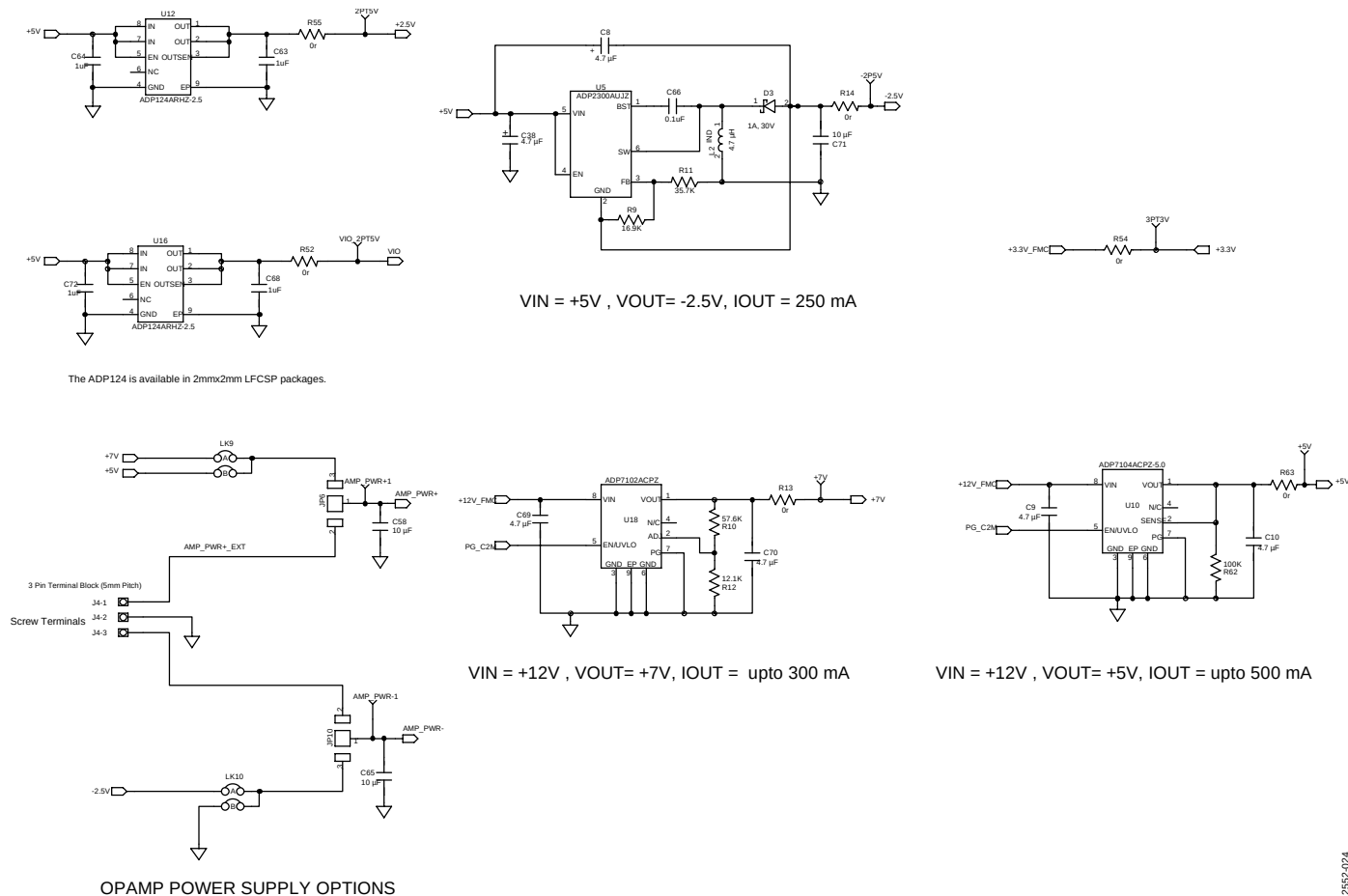


Figure 24. Schematic—System Power Supply Options

External Reference

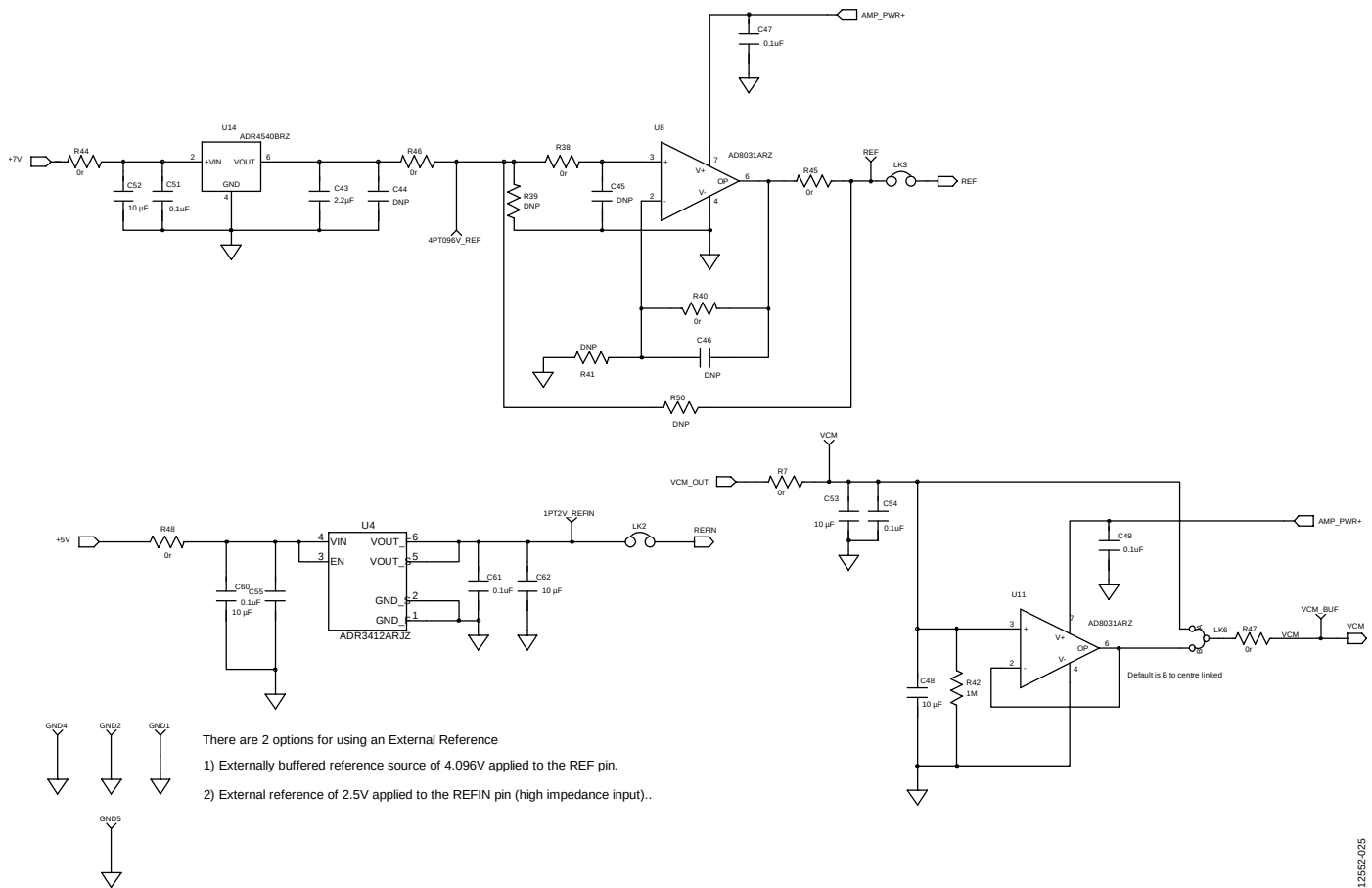


Figure 25. Schematic—External Reference

12852-025



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Figure 27. Schematic—AD7626 Decoupling

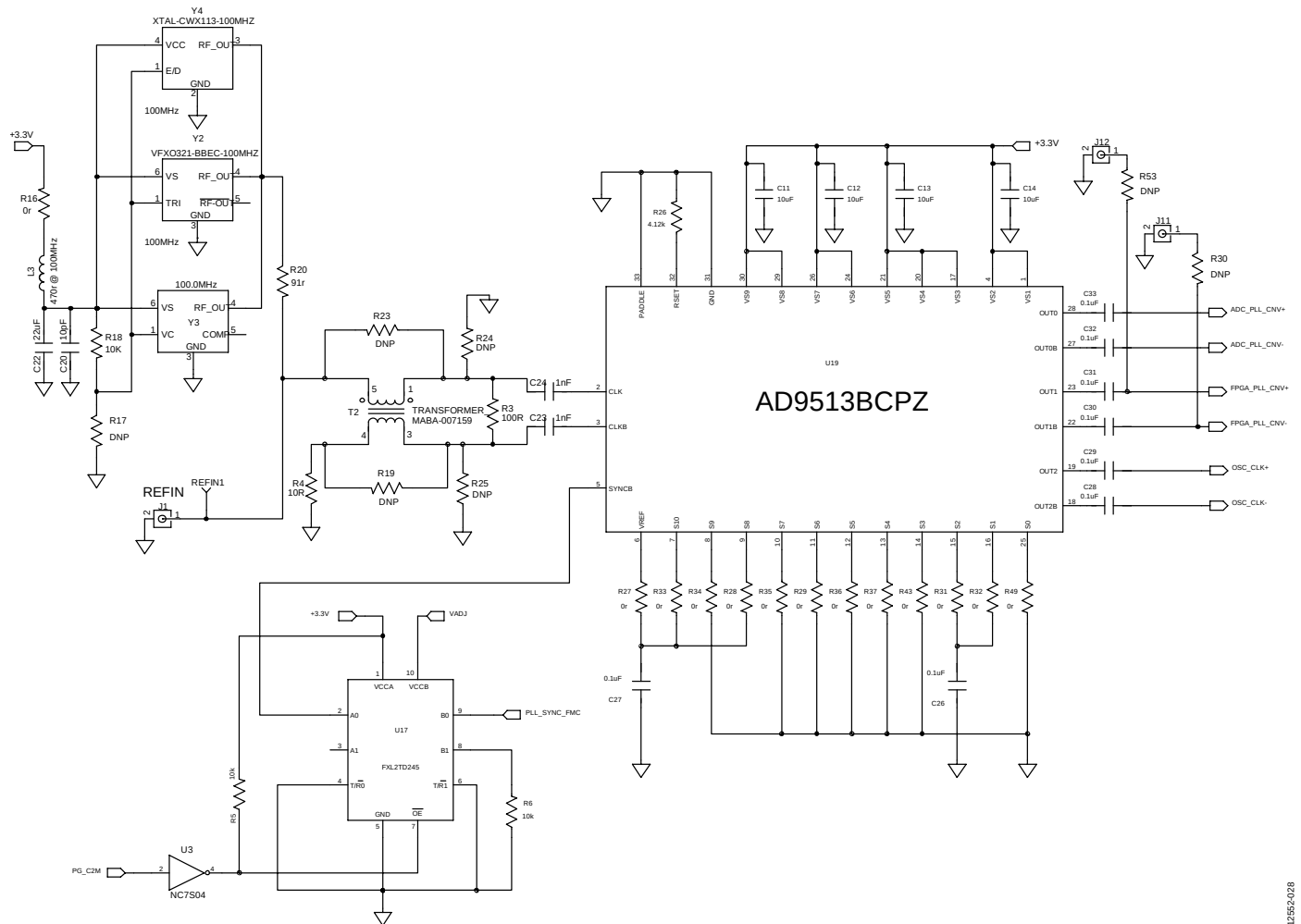


Figure 28. Schematic—Oscillator PLL

12552-028

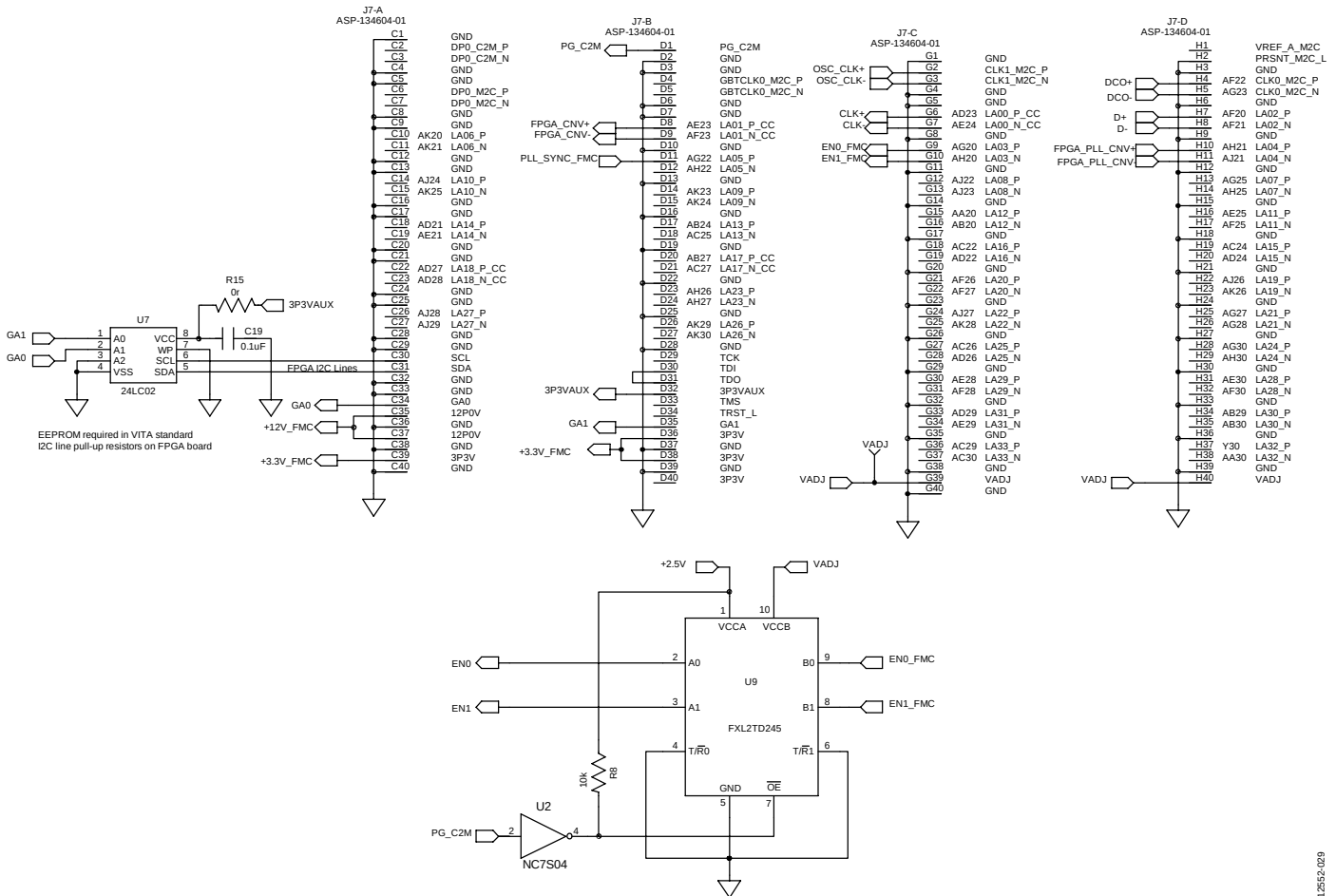


Figure 29. Schematic—FMC-LPC Male Connector

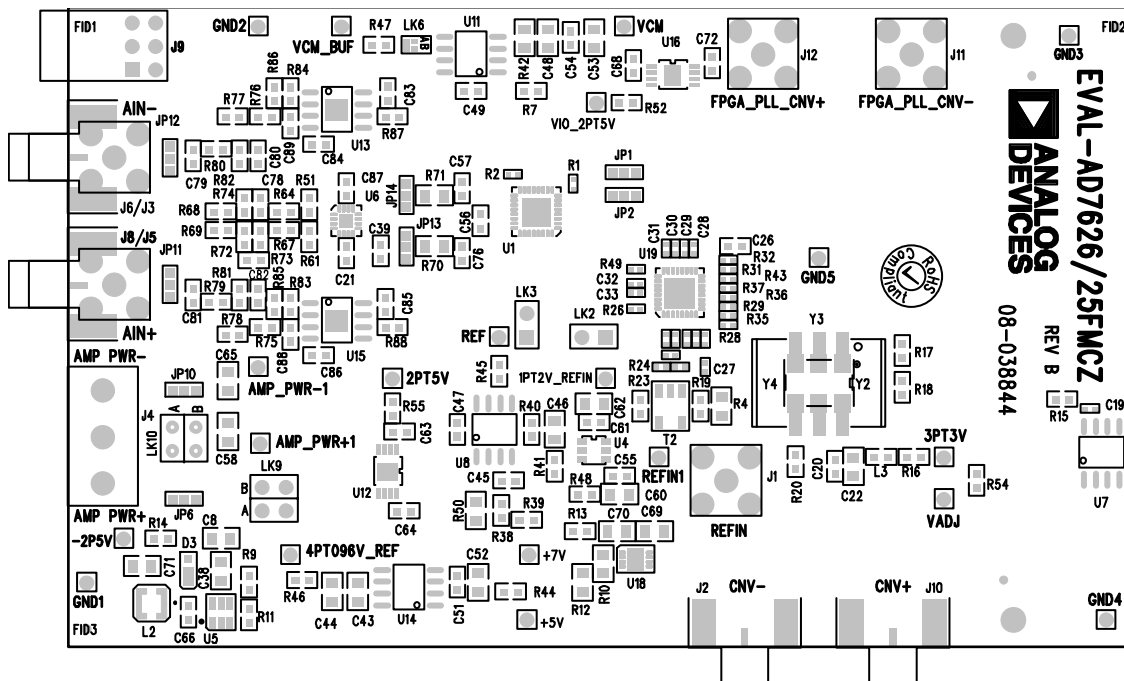


Figure 30. Evaluation Board Silkscreen—Top Assembly

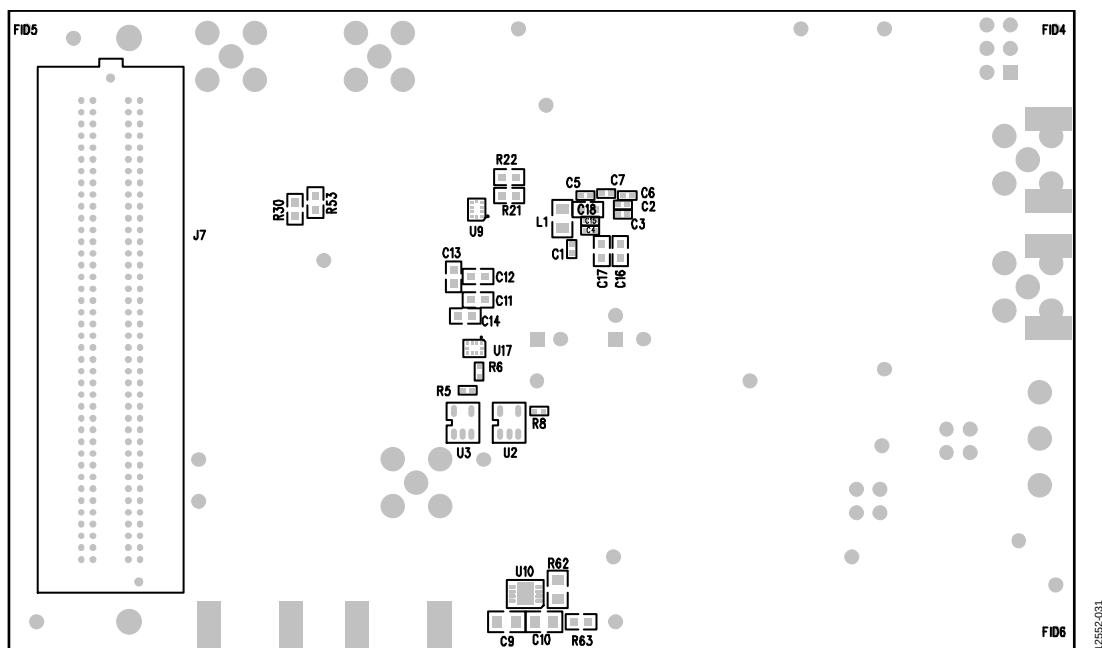


Figure 31. Evaluation Board Silkscreen—Bottom Assembly

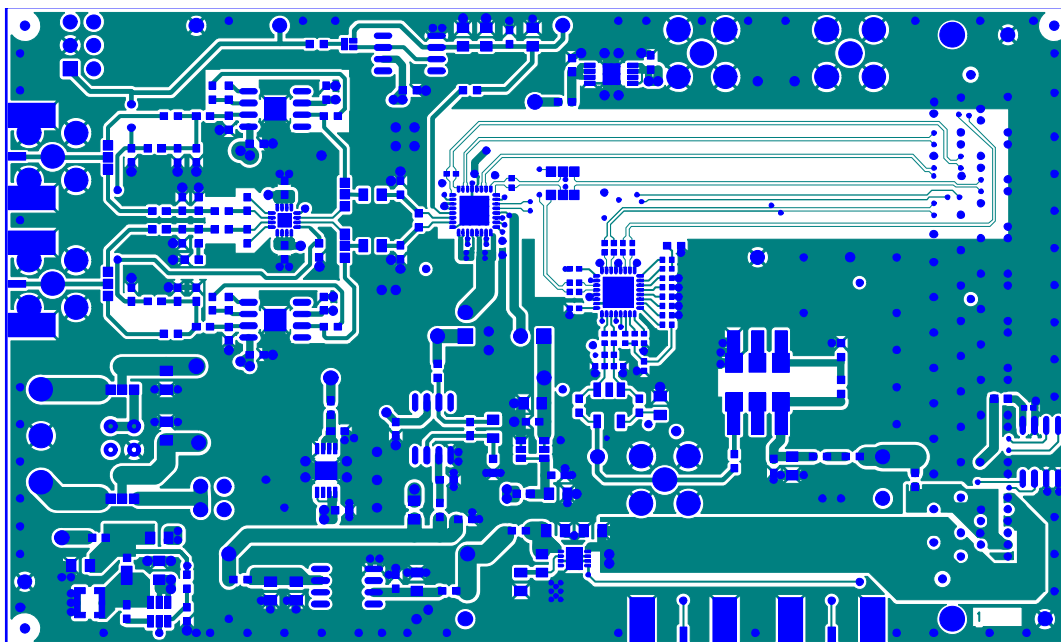
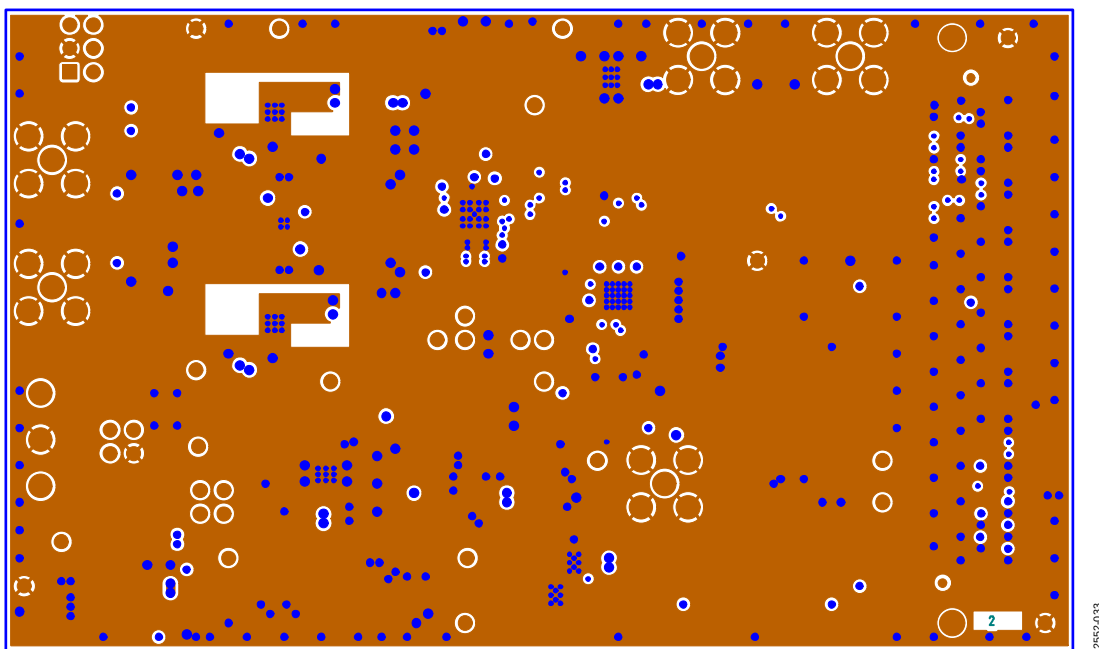
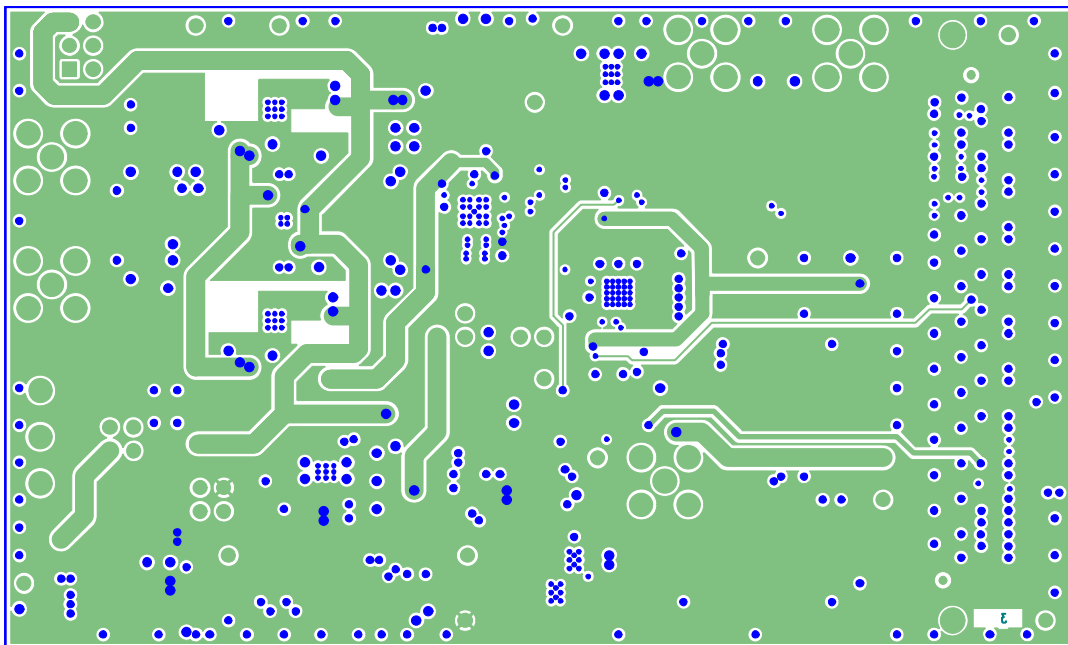


Figure 32. Evaluation Board—Top Layer



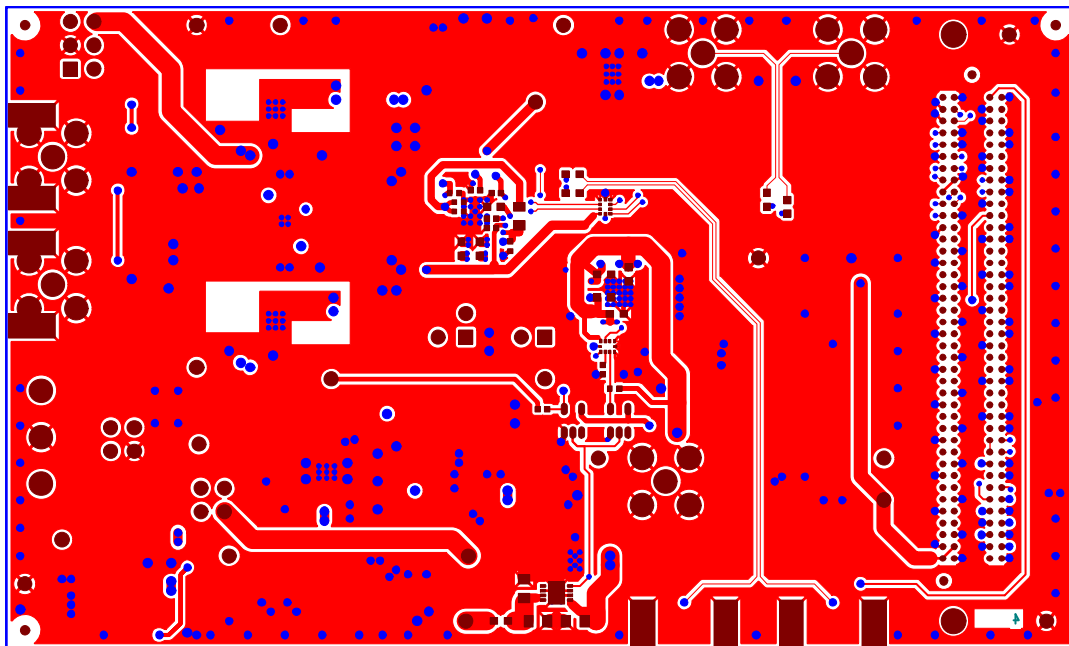
12552-033

Figure 33. Evaluation Board Layer 2—Ground



12552-034

Figure 34. Evaluation Board Layer 3—Power



12552-035

Figure 35. Evaluation Board Bottom Layer

BILL OF MATERIALS

Table 4. Bill of Materials for EVAL-AD7626FMCZ¹

Name	Part Description	Part Number	Stock Code
+5V, +7V, -2P5V, 1PT2V_REFIN, 2PT5V, 3PT3V, 4PT096V_REF, AMP_PWR+1, AMP_PWR-1	Test point	20-313137	FEC 8731144
VADJ	Test point	N/A	Do not insert
VCM, VCM_BUF, VIO_2PT5V	Test point	20-313137	FEC 8731144
REF	Test point	20-313137	FEC 8731144
REFIN1	Test point	20-313137	Not inserted
C1, C2, C3, C4, C5, C6, C7, C19	Capacitor 0603	MCCA000050	FEC 1758896
C8, C9, C10, C38, C69, C70	Capacitor+	EMK212B7475KG-T	FEC 2112841
C11, C12, C13, C14, C16, C17, C18	Capacitor 0603	C1608X5R1A106M	FEC 1962113
C15	Capacitor 0603	MCCA000076	FEC 1758924
C20	Capacitor	06035A100JAT2A	FEC 499110
C21	Capacitor	MCCA000255	FEC 1759122
C22	Capacitor	GRM21BR60J226ME39L	Digi-Key 490-1719-1-ND
C23, C24	Capacitor	GRM1555C1H102JA01D	FEC 8819556
C26, C39, C49, C51, C54, C55, C79, C81, C83 C84, C85, C86, C87, C47, C61, C66	Capacitor	MCCA000255	FEC 1759122
C27, C28, C29, C30, C31, C32, C33	Capacitor	MCCA000050	FEC 1758896
C43	Capacitor	EMK212B7225KG-T	FEC 1683654
C44, C45, C46	Capacitor	TBA	Do not place
C48, C42, C53, C58, C60, C62, C65, C71	Capacitor	GRM219R61C106KA73D	FEC 1845747
C56	Capacitor 0603	N/A	Do not place
C57, C76	Capacitor 0603	06035A560JAT2A	FEC 2280650
C63, C64, C68, C72	Capacitor	LMK107B7105KA-T	FEC 2112849
C77, C78, C80, C82	Capacitor 0603	N/A	Do not place
C88, C89	Capacitor 0603	C1608C0G1H101J080AA	FEC 1907297
D3	Diode Schottky, 30 V, 1 A, PD3S130L	PD3S130L	Digi-Key PD3S130LDICT-ND
GND1, GND2, GND3, GND4, GND5	Test point	20-313137	FEC 8731144
J1	Switching mode amplifier (SMA)	5-1814832-1	FEC 1248990
J2, J10	SMA	142-0701-851	Not inserted
J3, J5	SMA	5-1814400-1	Not inserted
J4	Connector\Power3	CTB5000/3	FEC 151790
J6, J8	SMA	142-0701-851	Digi-Key J658-ND
J7	ASP-134604-01	ASP-134604-01	Samtec ASP-134604-01
J9	Header 06-SKT-RA	SSW-103-02-T-D-RA	Not inserted
J11, J12	SMA	5-1814832-1	Not inserted
JP1, JP2, JP6, JP10, JP11, JP12, JP13, JP14	3W, solder link, 0603	N/A	N/A
L1	Bead, 0805	HZ0805E601R	Digi-Key 240-1018-1-ND
L2	Inductor	LPS3015-472MLB	Coilcraft LPS3015-472MLB
L3	Bead	7427-92642	FEC 1635690
LK2, LK3	Jumper	M20-9990246	FEC 1022247 and FEC 150-411
LK6	Jumper2\solder bridge	N/A	N/A
LK9	Jumper-2	M20-9980445	FEC 1022232 and FEC 150-411
LK10	Jumper-2	M20-9980446	FEC 1022232 and FEC 150-412
R1, R2	Resistor	RC0402FR-07100RL	FEC 9239111
R3	Resistor	ERJ-2RKF1000X	FEC 2304034
R4	Resistor	MC01W0805110R	FEC 9332421
R5, R6, R8	Resistor	MC 0.0625W 0402 1% 10K	FEC 1358069

Name	Part Description	Part Number	Stock Code
R7, R13, R14, R15, R16, R38, R40, R44, R45, R46, R47, R48, R52, R54, R55, R63, R68, R69, R77, R78	Resistor	MC 0.063W 0603 0R	FEC 9331662
R9	Resistor	MC 0.063W 0603 1% 16K9	FEC 1170908
R10	Resistor	MCTC0525B5762T5E	FEC 1575988
R11	Resistor	MC 0.063W 0603 1% 35K7	FEC 1170942
R12	Resistor	ERJ6ENF1212V	FEC 2057636
R17, R19, R21, R22, R23	Resistor	MC 0.063W 0603 10K	Do not place
R18	Resistor	MC 0.063W 0603 10K	FEC 9330399
R20	Resistor	MC 0.063W 0603 1% 91R	FEC 9331646
R24, R25	Resistor	N/A	Do not place
R26	Resistor	MC 0.0625W 0402 1% 4K12	FEC 1803097
R27, R28, R29, R31, R32, R33, R34, R35, R36, R37	Resistor	CRCW04020000Z0ED	FEC 1469661
R30, R53	Resistor	MC 0.063W 0603 10K	Do not place
R39, R41, R50	Resistor	N/A	Do not place
R42	Resistor	ERJP06F1004V	FEC 1750796
R43, R49	Resistor	CRCW04020000Z0ED	FEC 1469661
R51, R61, R64, R67	Resistor	ERA3AEB4990V	FEC 1810089
R62	Resistor	MC 0.1W 0805 1% 100K	FEC 9332405
R70, R71	Resistor	RP73PF2A20RBTDF	FEC 2116980
R72, R73, R74, R81, R82	Resistor, 0 Ω	N/A	Do not place
R75, R76	82 Ω , 0603, 1%, 0.063 W	MC0063W0603182R	FEC 9331590
R79, R80	Resistor, 0 Ω	MC 0.063W 0603 1% 1K	FEC 9330380
R83, R84, R85, R86, R87, R88	Resistor	MC 0.063W 0603 0R	FEC 9331662
T2	Transformer	MABA-007159-000000	MACOM MABA-007159-000000
U1	AD7626BCPZ	AD7626BCPZ	AD7626BCPZ
U2, U3	NC7S04	NC7SZ04M5	FEC 1013809
U4	ADR3412ARJZ	ADR3412ARJZ	ADR3412ARJZ-R2
U5	ADP2300AUJZ	ADP2300AUJZ	ADP2300AUJZ-R7
U6	ADA4932-1	ADA4932-1YCPZ	ADA4932-1YCPZ-R2
U7	24LC02B-I/SN	M24C02-WMN6P	FEC 9882804
U8	AD8031ARZ	AD8031ARZ	AD8031ARZ
U9	FXL2TD245	FXL2TD245L10X	Digi-Key FXL2TD245L10XCT-ND
U10	ADP7104ACPZ-5.0	ADP7104ACPZ-5.0	ADP7104ACPZ-5.0-R7
U11	AD8031ARZ	AD8031ARZ	AD8031ARZ
U12	ADP124ARHZ-2.5	ADP124ARHZ-2.5	ADP124ARHZ-2.5-R7
U13	ADA4899-1	ADA4899-1YRDZ	ADA4899-1YRDZ
U14	ADR4540BRZ	ADR4540BRZ	ADR4540BRZ
U15	ADA4899-1	ADA4899-1YRDZ	ADA4899-1YRDZ
U16	ADP124ARHZ-2.5	ADP124ARHZ-2.5	ADP124ARHZ-2.5-R7
U17	FXL2TD245	FXL2TD245L10X	Digi-Key FXL2TD245L10XCT-ND
U18	ADP7102ACPZ	ADP7102ACPZ	ADP7102ACPZ-R7
U19	AD9513BCPZ	AD9513BCPZ	AD9513BCPZ
Y2	VFXO321-BBEC-100MHZ	VFXO 321-BBEC-100MHZ	Do not place
Y3	TCXO-TX500	TX-500	Do not place
Y4	XTAL-CWX113-100MHZ	CWX113-100.0M	Do not place

¹ N/A means not applicable.

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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