4.5-V TO 20-V INPUT, 3-A OUTPUT SYNCHRONOUS PWM SWITCHER WITH INTEGRATED FET (SWIFT™)

FEATURES

- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of -55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **100 mW, 4.5-A Peak MOSFET Switch for High Efficiency at 3-A Continuous Output Current**
- **Uses External Lowside MOSFET or Diode**
- **Output Voltage Adjustable Down to 0.891 V With 2% Accuracy**
- **Synchronizes to External Clock**
- **180° Out of Phase Synchronization**
- **Wide PWM Frequency – Fixed 250 kHz, 500 kHz or Adjustable 250 kHz to 700 kHz**
- **Internal Slow Start**
- **Load Protected by Peak Current Limit and Thermal Shutdown**
- **Adjustable Undervoltage Lockout**
- **16-Pin TSSOP PowerPAD™ Package**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

APPLICATIONS

- **Industrial & Commercial Low Power Systems**
- **LCD Monitors and TVs**
- **Computer Peripherals**
- **Point of Load Regulation for High Performance DSPs, FPGAs, ASICs, and Microprocessors**

DESCRIPTION

The TPS54350 is a medium output current synchronous buck PWM converter with an integrated high side MOSFET and a gate driver for an optional low side external MOSFET. Features include a high performance voltage error amplifier that enables maximum performance under transient conditions and flexibility in choosing the output filter inductors and capacitors. The TPS54350 has an under-voltage-lockout circuit to prevent start-up until the input voltage reaches 4.5 V; an internal slow-start circuit to limit in-rush currents; and a power good output to indicate valid output conditions. The synchronization feature is configurable as either an input or an output for easy 180° out of phase synchronization.

The TPS54350 device is available in a thermally enhanced 16-pin TSSOP (PWP) PowerPAD™ package. Texas Instruments provides evaluation modules and the SWIFT™ designer software tool to aid in quickly achieving high-performance power supply designs to meet aggressive equipment development cycles.

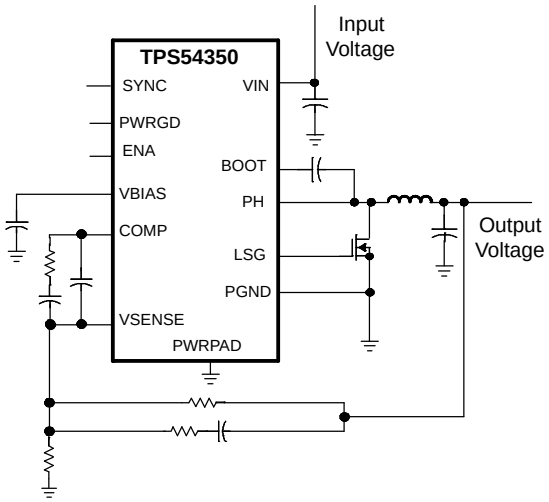
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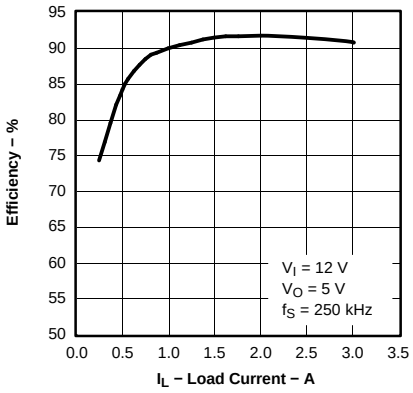
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SIMPLIFIED SCHEMATIC



EFFICIENCY vs LOAD CURRENT



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	OUTPUT VOLTAGE	PACKAGE	PART NUMBER
–55°C to 125°C	Adjustable to 0.891 V	Plastic HTSSOP (PWP)(1)	TPS54350MPWPREP

(1) The PWP package is also available taped and reeled. Add an R suffix to the device type (i.e., TPS54350PWPR).

PACKAGE DISSIPATION RATINGS(1)(2)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A = 25°C POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
16-Pin PWP with solder(3)	42.1°C/W	2.36	1.31	0.95
16-Pin PWP without solder	151.9°C/W	0.66	0.36	0.26

(1) See Figure 46 for power dissipation curves.
(2) For more information, see the Texas Instruments technical brief SLMA002.
(3) Test Board Conditions
a. Thickness: 0.062 inch
b. 3 inch x 3 inch
c. 2 oz. Copper traces located on the top and bottom of the PCB for soldering
d. Copper areas located on the top and bottom of the PCB for soldering
e. Power and Ground planes, 1 oz. Copper (0.036 mm thick)
f. Thermal vias, 0,33 mm diameter, 1,5 mm pitch
g. Thermal isolation of power plane

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE / UNIT
V_I	Input voltage range	VIN	–0.3 V to 21.5 V
		VSENSE	–0.3 V to 8 V
		UVLO	–0.3 V to 8 V
		SYNC	–0.3 V to 4 V
		ENA	–0.3 V to 4 V
		BOOT	VI(PH) + 8.V
V_O	Output voltage range	VBIAS	–0.3 to 8.5 V
		LSG	–0.3 to 8.5 V
		SYNC	–0.3 to 4 V
		RT	–0.3 to 4 V
		PWRGD	–0.3 to 6 V
		COMP	–0.3 to 4 V
		PH	–1.5 V to 22 V
I_O	Source current	PH	Internally Limited (A)
		LSG (Steady State Current)	10 mA
		COMP, VBIAS	3 mA
I_S	Sink current	SYNC	5 mA
		LSG (Steady State Current)	100 mA
		PH (Steady State Current)	500 mA
		COMP	3 mA
		ENA, PWRGD	10 mA
	Voltage differential	AGND to PGND	±0.3 V
TJ	Operating virtual junction temperature range		–55°C to +150°C
Tstg	Storage temperature		–65°C to +150°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	4.5		20	V
T_J	Operating junction temperature	–55		125	°C

ELECTRICAL CHARACTERISTICS

T_J = –55°C to 125°C, V_{IN} = 4.5 V to 20 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Quiescent current	Operating current, PH pin open, no external low side MOSFET, RT = Hi-Z		5		mA
		Shutdown, ENA = 0 V		1		
VIN	Start threshold voltage			4.32	4.52	V
	Stop threshold voltage		3.63	3.97		V
	Hysteresis			350		mV
UNDER VOLTAGE LOCK OUT (UVLO PIN)						
UVLO	Start threshold voltage			1.2	1.28	V
	Stop threshold voltage		1.02	1.1		V
	Hysteresis			100		mV
BIAS VOLTAGE (VBIAS PIN)						
VBIAS	Output voltage	I_{VBIAS} = 1 mA, VIN ≥ 12 V	7.5	7.8	8.035	V
		I_{VBIAS} = 1 mA, VIN = 4.5 V	4.4	4.47	4.5	
REFERENCE SYSTEM ACCURACY						
	Reference voltage	T_J = 25°C	0.888	0.891	0.896	V
			0.88	0.891	0.899	
OSCILLATOR (RT PIN)						
	Internally set PWM switching frequency	RT grounded	183	250	300	kHz
		RT open	396	500	600	
	Externally set PWM switching frequency	RT = 100 kΩ (1% resistor to AGND)	400	500	595	kHz
FALLING EDGE TRIGGERED BIDIRECTIONAL SYNC SYSTEM (SYNC PIN)						
	SYNC out low-to-high rise time (10%/90%) (1)	25 pF to ground		200	500	ns
	SYNC out high-to-low fall time (90%/10%) (1)	25 pF to ground		5	10	ns
	Falling edge delay time (1)	Delay from rising edge to rising edge of PH pins, See Figure 19		180		deg
	Minimum input pulsewidth (1)	RT = 100 kΩ		100		ns
	Delay (falling edge SYNC to rising edge PH) (1)	RT = 100 kΩ		360		ns
	SYNC out high level voltage	50-kΩ resistor to ground, no pullup resistor	2.5			
	SYNC out low level voltage				0.6	V
	SYNC in low level threshold		0.8			V
	SYNC in high level threshold				2.3	V
	SYNC in frequency range (1)	Percentage of programmed frequency	–10%		10%	
			225		770	kHz
FEED-FORWARD MODULATOR (INTERNAL SIGNAL)						
	Modulator gain	VIN = 12 V, T_J = 25°C		8		V/V
	Modulator gain variation		–25%		25%	
	Minimum controllable ON time (1)			180		ns
	Maximum duty factor (1)	VIN = 4.5 V	80%	86%		
ERROR AMPLIFIER (VSENSE AND COMP PINS)						
	Error amplifier open loop voltage gain (1)		60	80		dB
	Error amplifier unity gain bandwidth (1)		1	2.8		MHz
	Input bias current, VSENSE pin (1)				500	nA
COMP	Output voltage slew rate (symmetric) (1)			1.5		V/µs

(1) Ensured by design, not production tested.

ELECTRICAL CHARACTERISTICS (continued)

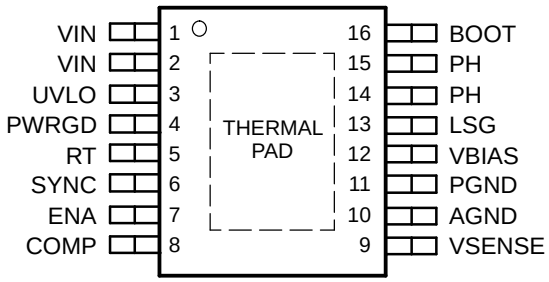
T_J = –55°C to 125°C, V_{IN} = 4.5 V to 20 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE (ENA PIN)						
	Disable low level input voltage				0.5	V
	Internal slow-start time (10% to 90%)	f_s = 250 kHz, RT = ground(1)		4.6		ms
		f_s = 500 kHz, RT = Hi-Z(1)		2.3		
	Pullup current source		1.8	5	10	µA
	Pulldown MOSFET	II(ENA) = 1 mA		0.1		V
POWER GOOD (PWRGD PIN)						
	Power good threshold	Rising voltage		97%		
	Rising edge delay(1)	f_s = 250 kHz		4		ms
		f_s = 500 kHz		2		
PWRGD	Output saturation voltage	I_{sink} = 1 mA, VIN > 4.5 V		0.05		V
		I_{sink} = 100 µA, VIN = 0 V		0.76		V
	Open drain leakage current	Voltage on PWRGD = 6 V			3	µA
CURRENT LIMIT						
	Current limit	VIN = 12 V, T_A = 25°C	3	4.5	7.2	A
	Current limit Hiccup Time(2)	f_s = 500 kHz		4.5		ms
THERMAL SHUTDOWN						
	Thermal shutdown trip point(2)			165		°C
	Thermal shutdown hysteresis(2)			7		°C
LOW SIDE MOSFET DRIVER (LSG PIN)						
	Turn on rise time, (10% / 90%(2))	VIN = 4.5 V, Capacitive load = 1000 pF		15		ns
	Deadtime(2)	VIN = 12 V		60		ns
	Driver ON resistance	VIN = 4.5 V sink/source		7.5		Ω
		VIN = 12 V sink/source		5		
OUTPUT POWER MOSFETS (PH PIN)						
	Phase node voltage when disabled	DC conditions and no load, ENA = 0 V		0.5		V
	Voltage drop, low side FET and diode	VIN = 4.5 V, Idc = 100 mA		1.13	1.42	V
		VIN = 12 V, Idc = 100 mA		1.08	1.38	
$r_{DS(ON)}$	High side power MOSFET switch(3)	VIN = 4.5 V, BOOT-PH = 4.5 V, I_O = 0.5 A		150	300	mΩ
		VIN = 12 V, BOOT-PH = 8 V, I_O = 0.5 A		100	220	

(2) Ensured by design, not production tested.
(3) Resistance from VIN to PH pins.

PIN ASSIGNMENTS

PWP PACKAGE
(TOP VIEW)

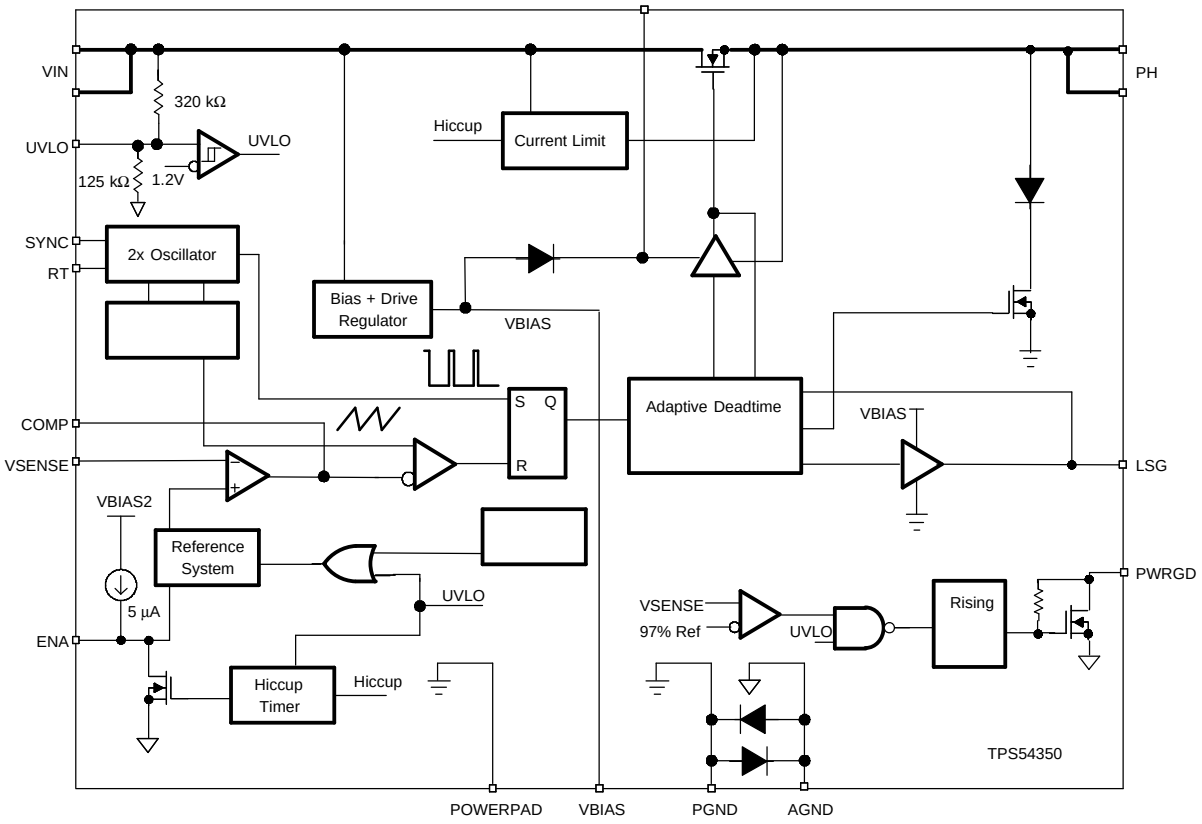


NOTE: If there is not a Pin 1 indicator, turn device to enable reading the symbol from left to right. Pin 1 is at the lower left corner of the device.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NO.	NAME	
1, 2	VIN	Input supply voltage, 4.5 V to 20 V. Must bypass with a low ESR 10-µF ceramic capacitor.
3	UVLO	Undervoltage lockout pin. Connecting an external resistive voltage divider from VIN to the pin overrides the internal default VIN start and stop thresholds.
4	PWRGD	Power good output. Open drain output. A low on the pin indicates that the output is less than the desired output voltage. There is an internal rising edge filter on the output of the PWRGD comparator.
5	RT	Frequency setting pin. Connect a resistor from RT to AGND to set the switching frequency. Connecting the RT pin to ground or floating will set the frequency to an internally preselected frequency.
6	SYNC	Bidirectional synchronization I/O pin. SYNC pin is an output when the RT pin is floating or connected low. The output is a falling edge signal out of phase with the rising edge of PH. SYNC may be used as an input to synchronize to a system clock by connecting to a falling edge signal when an RT resistor is used. See the *180° Out of Phase Synchronization* operation in the Application Information section.
7	ENA	Enable. Below 0.5 V, the device stops switching. Float pin to enable.
8	COMP	Error amplifier output. Connect frequency compensation network from COMP to VSENSE pins.
9	VSENSE	Inverting node error amplifier
10	AGND	Analog ground – internally connected to the sensitive analog ground circuitry. Connect to PGND and PowerPAD.
11	PGND	Power ground – noisy internal ground–return currents from the LSG driver output return through the PGND pin. Connect to AGND and PowerPAD.
12	VBIAS	Internal 8-V bias voltage. A 1-µF ceramic bypass capacitance is required on the VBIAS pin.
13	LSG	Gate drive for optional low side MOSFET. Connect gate of n-channel MOSFET for a higher efficiency synchronous buck converter configuration. Otherwise, leave open and connect schottky diode from ground to PH pins.
14, 15	PH	Phase node – Connect to external L-C filter.
16	BOOT	Bootstrap capacitor for high side gate driver. Connect 0.1-µF ceramic capacitor from BOOT to PH pins.
PowerPAD		PGND and AGND pins must be connected to the exposed pad for proper operation. See Figure 21 for an example PCB layout.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) system has an internal voltage divider from VIN to AGND. The defaults for the start/stop values are labeled VIN and given in Table 1. The internal UVLO threshold can be overridden by placing an external resistor divider from VIN to ground. The internal divider values are approximately 320 kΩ for the high side resistor and 125 kΩ for the low side resistor. The divider ratio (and therefore the default start/stop values) is quite accurate, but the absolute values of the internal resistors may vary as much as 15%. If high accuracy is required for an externally adjusted UVLO threshold, select lower value external resistors to set the UVLO threshold. Using a 1-kΩ resistor for the low side resistor (R2 see Figure 1) is recommended. Under no circumstances should the UVLO pin be connected directly to VIN.

Table 1. Start/Stop Voltage Threshold

	START VOLTAGE THRESHOLD	STOP VOLTAGE THRESHOLD
VIN (Default)	4.49	3.69
UVLO	1.24	1.02

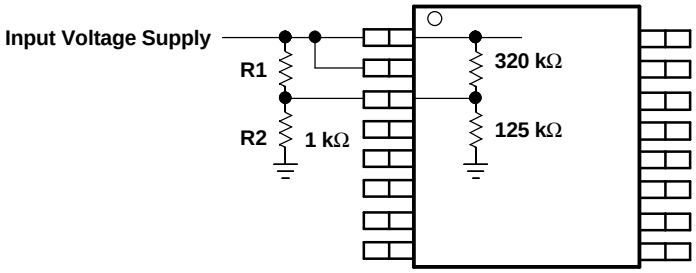


Figure 1. Circuit Using External UVLO Function

The equations for selecting the UVLO resistors are:

$$R1 = \frac{VIN(start) \times 1\ k\Omega}{1.24\ V} - 1k\Omega \quad (1)$$

$$VIN(stop) = \frac{(R1 + 1\ k\Omega) \times 1.02\ V}{1\ k\Omega} \quad (2)$$

For applications which require an undervoltage lock out (UVLO) threshold greater than 4.49 V, external resistors may be implemented, see Figure 1, to adjust the start voltage threshold. For example, an application needing an UVLO start voltage of approximately 7.8 V using the Equation 1, R1 is calculated to the nearest standard resistor value of 5.36 kΩ. Using Equation 2, the input voltage stop threshold is calculated as 6.48 V.

Enable (ENA) and Internal Slow Start

Once the ENA pin voltage exceeds 0.5 V, the TPS54350 starts operation. The TPS54350 has an internal digital slow start that ramps the reference voltage to its final value in 1150 switching cycles. The internal slow start time (10%–90%) is approximated by the following expression:

$$T_{SS_INTERNAL(ms)} = \frac{1.15k}{f_{s(kHz)}} \quad (3)$$

Once the TPS54350 device is in normal regulation, the ENA pin is high. If the ENA pin is pulled below the stop threshold of 0.5 V, switching stops and the internal slow start resets. If an application requires the TPS54350 to be disabled, use open drain or open collector output logic to interface to the ENA pin (see Figure 2). The ENA pin has an internal pullup current source. Do not use external pullup resistors.

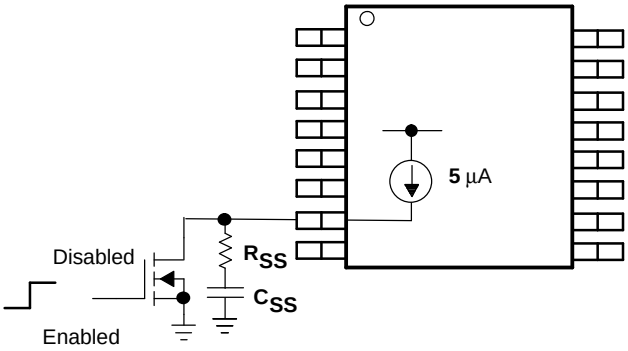


Figure 2. Interfacing to the ENA Pin

Extending Slow Start Time

In applications that use large values of output capacitance, there may be a need to extend the slow start time to prevent the startup current from tripping the current limit. The current limit circuit is designed to disable the high side MOSFET and reset the internal voltage reference for a short amount of time when the high side MOSFET current exceeds the current limit threshold. If the output capacitance and load current cause the startup current to exceed the current limit threshold, the power supply output will not reach the desied output voltage. To extend the slow start time and to reduce the startup current, an external resistor and capcitor can be added to the ENA pin. The slow start capacitance is calculated using the following equation:

$C_{SS}(\mu F) = 5.55e\text{-}3\ T_{ss}(ms)$

The R_{SS} resistor must be 2 kΩ and the slow start capacitor must be less than 0.47 µF.

Switching Frequency (RT)

The TPS54350 has an internal oscillator that operates at twice the PWM switching frequency. The internal oscillator frequency is controlled by the RT pin. Grounding the RT pin sets the PWM switching frequency to a default frequency of 250 kHz. Floating the RT pin sets the PWM switching frequency to 500 kHz.

Connecting a resistor from RT to AGND sets the frequency according to the following equation (also see Figure 30).

$$RT(k\Omega) = \frac{46000}{f_{s(kHz)} - 35.9} \quad (4)$$

The RT pin controls the SYNC pin functions. If the RT pin is floating or grounded, SYNC is an output. If the switching frequency has been programmed using a resistor from RT to AGND, then SYNC functions as an input.

The internal voltage ramp charging current increases linearly with the set frequency and keeps the feed forward modulator constant (Km = 8) regardless of the frequency set point.

SWITCHING FREQUENCY	SYNC PIN	RT PIN
250 kHz, internally set	Generates SYNC output signal	AGND
500 kHz, internally set	Generates SYNC output signal	Float
Externally set to 250 kHz to 700 kHz	Terminate to quiet ground with 10-kΩ resistor.	R = 215 kΩ to 69 kΩ
Externally synchronized frequency	Synchronization signal	Use 110 kΩ when RT floats and 237 kΩ when RT is grounded and using the sync out signal of another TPS54350. Set RT resistor equal to 90% to 110% of external synchronization frequency.

180° Out of Phase Synchronization (SYNC)

The SYNC pin is configurable as an input or as an output, per the description in the previous section. When operating as an input, the SYNC pin is a falling-edge triggered signal (see Figure 3, Figure 4, and Figure 19). When operating as an output, the signal's falling edge is approximately 180° out of phase with the rising edge of the PH pins. Thus, two TPS54350 devices operating in a system can share an input capacitor and draw ripple current at twice the frequency of a single unit.

When operating the two TPS54350 devices 180° out of phase, the total RMS input current is reduced. Thus reducing the amount of input capacitance needed and increasing efficiency.

When synchronizing a TPS54350 to an external signal, the timing resistor on the RT pin must be set so that the oscillator is programmed to run at 90% to 110% of the synchronization frequency.

NOTE:

Do not use synchronization input for designs with output voltages >10 V.

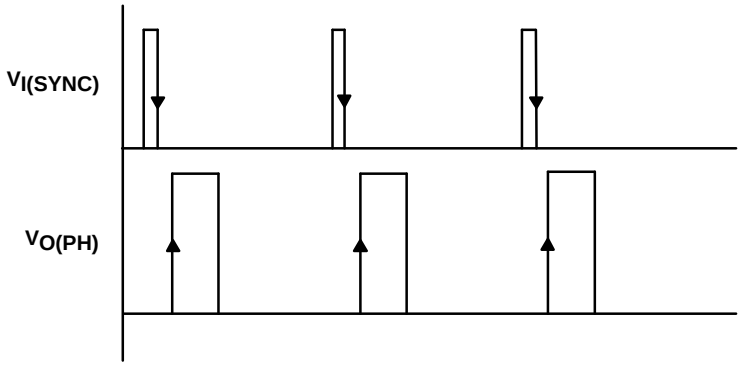


Figure 3. SYNC Input Waveform

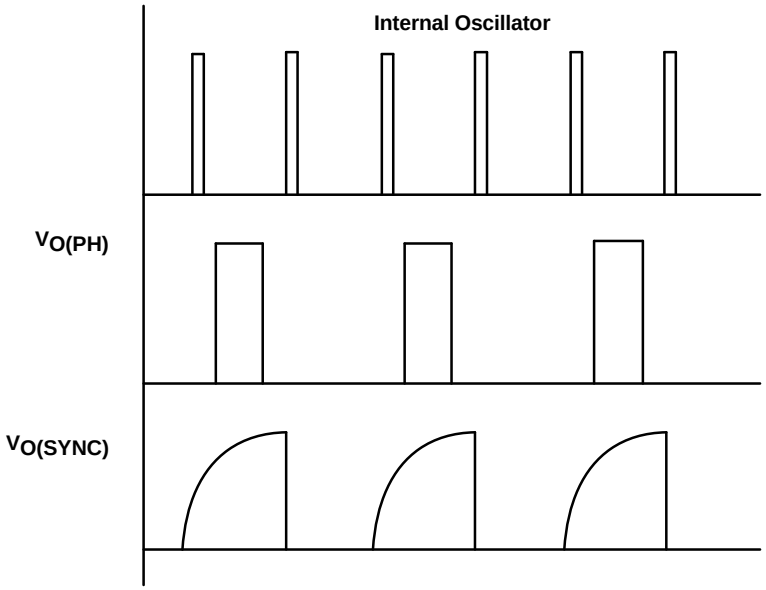


Figure 4. SYNC Output Waveform

Power Good (PWRGD)

The VSENSE pin is compared to an internal reference signal, if the VSENSE is greater than 97% and no other faults are present, the PWRGD pin presents a high impedance. A low on the PWRGD pin indicates a fault. The PWRGD pin has been designed to provide a weak pulldown and indicates a fault even when the device is unpowered. If the TPS54350 has power and has any fault flag set, the TPS54350 indicates the power is not good by driving the PWRGD pin low. The following events, singly or in combination, indicate power is not good:

- VSENSE pin out of bounds
- Overcurrent
- Thermal shutdown
- UVLO undervoltage
- Input voltage not present (weak pull down)
- Slow starting
- VBIAS voltage is low

Once the PWRGD pin presents a high impedance (i.e., power is good), a VSENSE pin out of bounds condition forces PWRGD pin low (i.e., power is bad) after a time delay. This time delay is a function of the switching frequency and is calculated using Equation 5:

$$T_{delay} = \frac{1000}{f_{s(kHz)}} \text{ ms} \quad (5)$$

Bias Voltage (VBIAS)

The VBIAS regulator provides a stable supply for the internal analog circuits and the low side gate driver. Up to 1 mA of current can be drawn for use in an external application circuit. The VBIAS pin must have a bypass capacitor value of 1 µF. X7R or X5R grade dielectric ceramic capacitors are recommended because of their stable characteristics over temperature.

Bootstrap Voltage (BOOT)

The BOOT capacitor obtains its charge cycle by cycle from the VBIAS capacitor. A capacitor from the BOOT pin to the PH pins is required for operation. The bootstrap connection for the high side driver must have a bypass capacitor of 0.1 µF.

Error Amplifier

The VSENSE pin is the error amplifier inverting input. The error amplifier is a true voltage amplifier with 1.5 mA of drive capability with a minimum of 60 dB of open loop voltage gain and a unity gain bandwidth of 2 MHz.

Voltage Reference

The voltage reference system produces a precision reference signal by scaling the output of a temperature stable bandgap circuit. During production testing, the bandgap and scaling circuits are trimmed to produce 0.891 V at the output of the error amplifier, with the amplifier connected as a voltage follower. The trim procedure improves the regulation, since it cancels offset errors in the scaling and error amplifier circuits.

PWM Control and Feed Forward

Signals from the error amplifier output, oscillator, and current limit circuit are processed by the PWM control logic. Referring to the internal block diagram, the control logic includes the PWM comparator, PWM latch, and the adaptive dead-time control logic. During steady-state operation below the current limit threshold, the PWM comparator output and oscillator pulse train alternately reset and set the PWM latch.

Once the PWM latch is reset, the low-side driver and integrated pulldown MOSFET remain on for a minimum duration set by the oscillator pulse width. During this period, the PWM ramp discharges rapidly to the valley voltage. When the ramp begins to charge back up, the low-side driver turns off and the high-side FET turns on. The peak PWM ramp voltage varies inversely with input voltage to maintain a constant modulator and power stage gain of 8 V/V.

As the PWM ramp voltage exceeds the error amplifier output voltage, the PWM comparator resets the latch, thus turning off the high-side FET and turning on the low-side FET. The low-side driver remains on until the next oscillator pulse discharges the PWM ramp.

During transient conditions, the error amplifier output can be below the PWM ramp valley voltage or above the PWM peak voltage. If the error amplifier is high, the PWM latch is never reset and the high-side FET remains on until the oscillator pulse signals the control logic to turn the high-side FET off and the internal low-side FET and driver on. The device operates at its maximum duty cycle until the output voltage rises to the regulation set point, setting VSENSE to approximately the same voltage as the internal voltage reference. If the error amplifier output is low, the PWM latch is continually reset and the high-side FET does not turn on. The internal low-side FET and low side driver remain on until the VSENSE voltage decreases to a range that allows the PWM comparator to change states. The TPS54350 is capable of sinking current through the external low side FET until the output voltage reaches the regulation set point.

The minimum on time is designed to be 180 ns. During the internal slow-start interval, the internal reference ramps from 0 V to 0.891 V. During the initial slow-start interval, the internal reference voltage is small resulting in a couple of skipped pulses because the minimum on time causes the actual output voltage to be slightly greater than the preset output voltage until the internal reference ramps up.

Deadtime Control

Adaptive dead time control prevents shoot through current from flowing in the integrated high-side MOSFET and the external low-side MOSFET during the switching transitions by actively controlling the turn on times of the drivers. The high-side driver does not turn on until the voltage at the gate of the low-side MOSFET is below 1 V. The low-side driver does not turn on until the voltage at the gate of the high-side MOSFET is below 1 V.

Low Side Gate Driver (LSG)

LSG is the output of the low-side gate driver. The 100-mA MOSFET driver is capable of providing gate drive for most popular MOSFETs suitable for this application. Use the SWIFT Designer Software Tool to find the most appropriate MOSFET for the application. Connect the LSG pin directly to the gate of the low-side MOSFET. Do not use a gate resistor as the resulting turn-on time may be too slow.

Integrated Pulldown MOSFET

The TPS54350 has a diode-MOSFET pair from PH to PGND. The integrated MOSFET is designed for light-load continuous-conduction mode operation when only an external Schottky diode is used. The combination of devices keeps the inductor current continuous under conditions where the load current drops below the inductor's critical current. Care should be taken in the selection of inductor in applications using only a low-side Schottky diode. Since the inductor ripple current flows through the integrated low-side MOSFET at light loads, the inductance value should be selected to limit the peak current to less than 0.3 A during the high-side FET turn off time. The minimum value of inductance is calculated using Equation 6:

$$L(H) = \frac{VO \times \left(1 - \frac{VO}{VI}\right)}{f_S \times 0.6} \quad (6)$$

Thermal Shutdown

The device uses the thermal shutdown to turn off the MOSFET drivers and controller if the junction temperature exceeds 165°C. The device is restarted automatically when the junction temperature decreases to 7°C below the thermal shutdown trip point and starts up under control of the slow-start circuit.

Overcurrent Protection

Overcurrent protection is implemented by sensing the drain-to-source voltage across the high-side MOSFET and compared to a voltage level which represents the overcurrent threshold limit. If the drain-to-source voltage exceeds the overcurrent threshold limit for more than 100 ns, the ENA pin is pulled low, the high-side MOSFET is disabled, and the internal digital slow-start is reset to 0 V. ENA is held low for approximately the time that is calculated by the following equation:

$$T_{HICCUP(ms)} = \frac{2250}{f_{s(kHz)}} \quad (7)$$

Once the hiccup time is complete, the ENA pin is released and the converter initiates the internal slow-start.

Setting the Output Voltage

The output voltage of the TPS54350 can be set by feeding back a portion of the output to the VSENSE pin using a resistor divider network. In the application circuit of Figure 24, this divider network is comprised of resistors R1 and R2. To calculate the resistor values to generate the required output voltage use the following equation:

$$R2 = \frac{R1 \times 0.891}{V_O - 0.891} \quad (8)$$

Start with a fixed value of R1 and calculate the required R2 value. Assuming a fixed value of 10 kΩ for R1, the following table gives the appropriate R2 value for several common output voltages:

OUTPUT VOLTAGE (V)	R2 VALUE (kΩ)
1.2	28.7
1.5	14.7
1.8	9.76
2.5	5.49
3.3	3.74

Output Voltage Limitations

Due to the internal design of the TPS54350 there are both upper and lower output voltage limits for any given input voltage. Additionally, the lower boundary of the output voltage set point range is also dependent on operating frequency. The upper limit of the output voltage set point is constrained by the maximum duty cycle of the device and is shown in Figure 48. The lower limit is constrained by the minimum controllable on time which may be as high as 220 ns. The approximate minimum output voltage for a given input voltage and range of operating frequencies is shown in Figure 29 while the maximum operating frequency versus input voltage for some common output voltages is shown in Figure 29.

The curves shown in these two figures are valid for output currents greater than 0.5 A. As output currents decrease towards no load (0 A), the minimum output voltage decreases. For applications where the load current is less than 100 mA, the curves shown in Figure 31 and Figure 32 are applicable. All of the data plotted in these curves are approximate and take into account a possible 20 percent deviation in actual operating frequency relative to the intended set point.

TYPICAL CHARACTERISTICS

LOOP RESPONSE

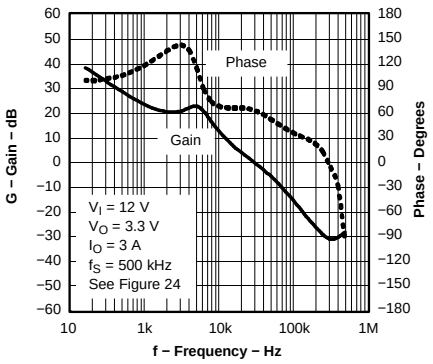


Figure 5.

LOAD REGULATION

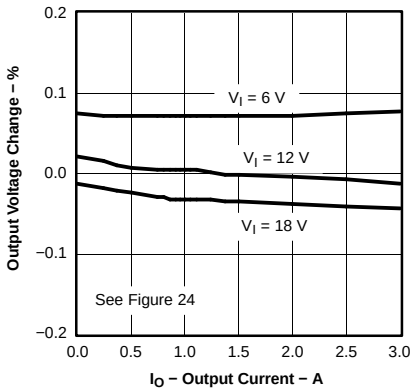


Figure 6.

LINE REGULATION

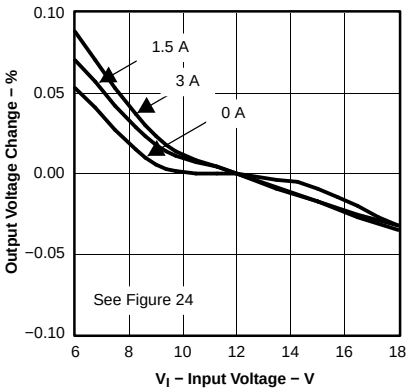


Figure 7.

EFFICIENCY vs OUTPUT CURRENT

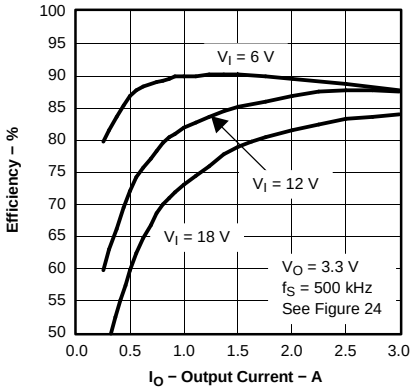


Figure 8.

INPUT RIPPLE VOLTAGE

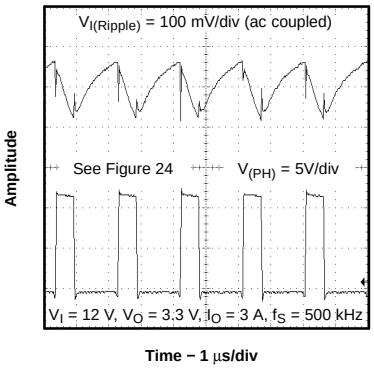


Figure 9.

OUTPUT RIPPLE VOLTAGE

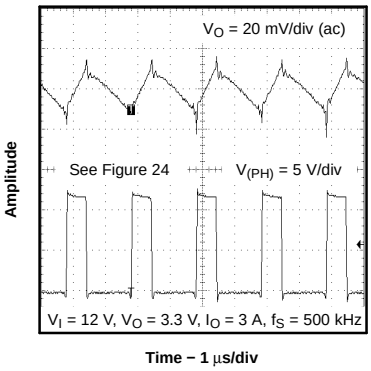


Figure 10.

PH PIN VOLTAGE

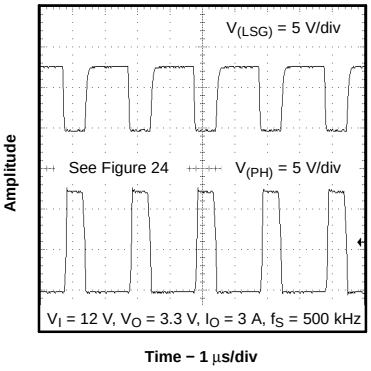


Figure 11.

LOAD TRANSIENT RESPONSE

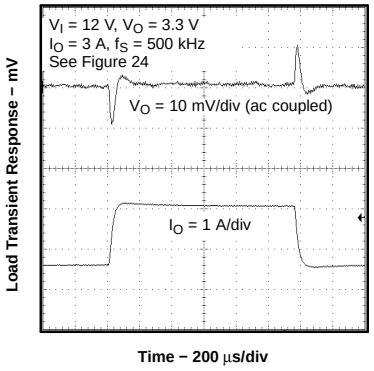


Figure 12.

POWER UP

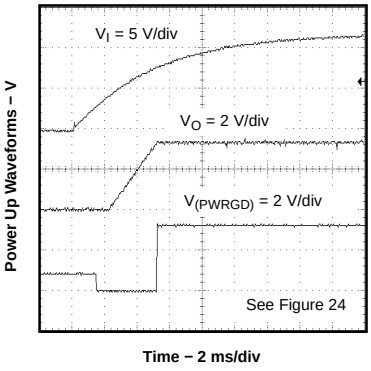


Figure 13.

TYPICAL CHARACTERISTICS (continued)

POWER DOWN

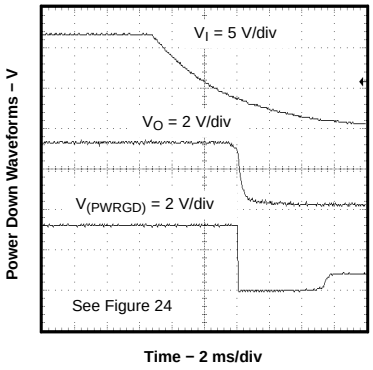


Figure 14.

EFFICIENCY vs OUTPUT CURRENT

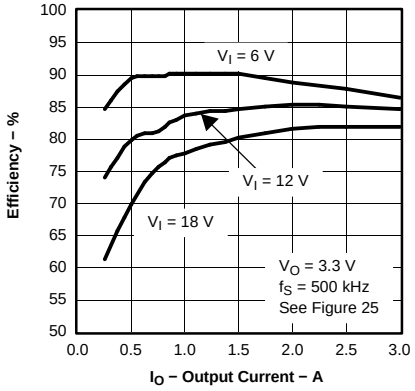


Figure 15.

CONTINUOUS CONDUCTION MODE

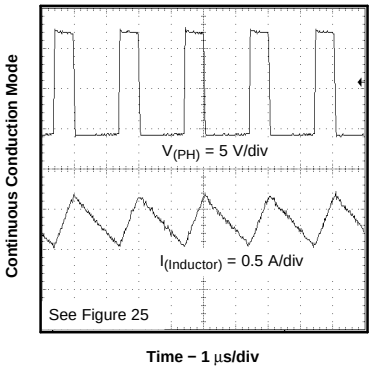


Figure 16.

DISCONTINUOUS CONDUCTION MODE

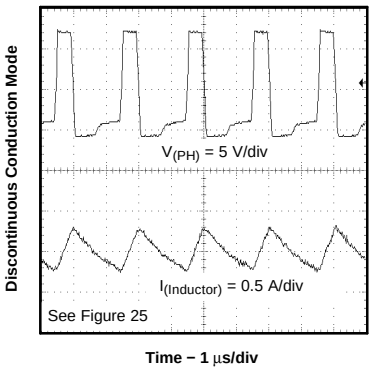


Figure 17.

SEQUENCING WAVEFORMS

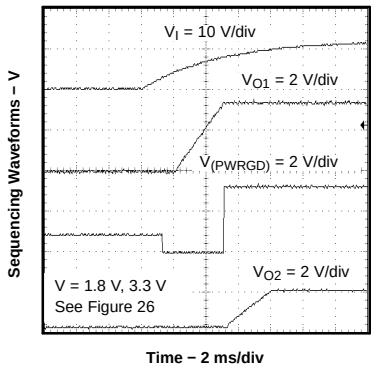


Figure 18.

INPUT RIPLE CANCELLATION

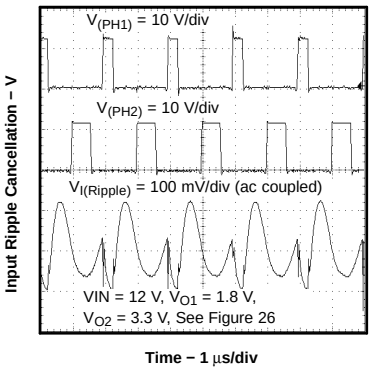


Figure 19.

EFFICIENCY vs OUTPUT CURRENT

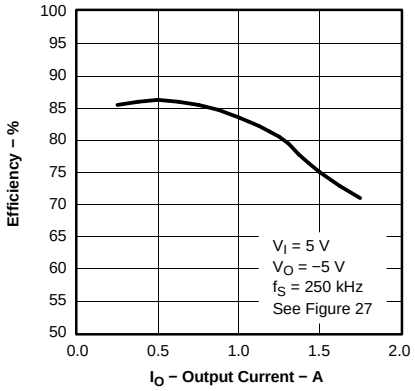


Figure 20.

APPLICATION INFORMATION

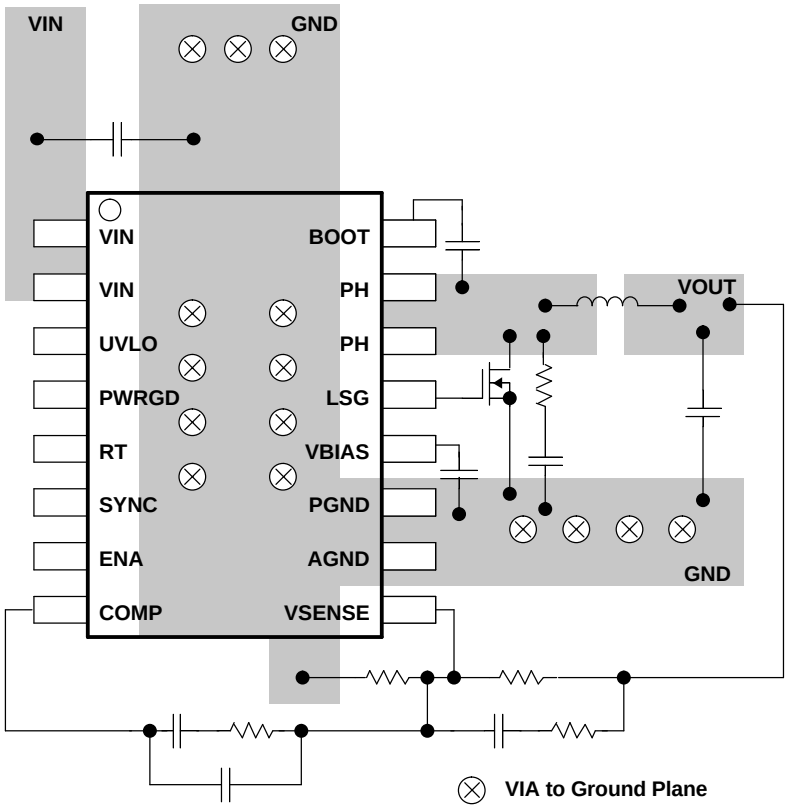


Figure 21. TPS54350 PCB Layout

PCB LAYOUT

The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54350 ground pins. The minimum recommended bypass capacitance is 10-µF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the AGND and PGND pins. See Figure 21 for an example of a board layout. The AGND and PGND pins should be tied to the PCB ground plane at the pins of the IC. The source of the low-side MOSFET and the anode of the Schottky diode should be connected directly to the PCB ground plane. The PH pins should be tied together and routed to the drain of the low-side MOSFET or to the cathode of the external Schottky diode. Since the PH connection is the switching node, the MOSFET (or diode) should be located close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The recommended conductor width from pins 14 and 15 is 0.05 inch to 0.075 inch of 1-ounce copper. The length of the copper land pattern should be no more than 0.2 inch.

For operation at full rated load, the analog ground plane must provide adequate heat dissipating area. A 3-inch by 3-inch plane of copper is recommended, though not mandatory, dependent on ambient temperature and airflow. Most applications have larger areas of internal ground plane available and the PowerPAD should be connected to the largest area available. Additional areas on the bottom or top layers also help dissipate heat, and any area available should be used when 3 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013-inch diameter vias to avoid solder wicking through the vias. Four vias should be in the PowerPAD area with four additional vias outside the pad area and underneath the package. Additional vias beyond those recommended to enhance thermal performance should be included in areas not under the device package.

APPLICATION INFORMATION (continued)

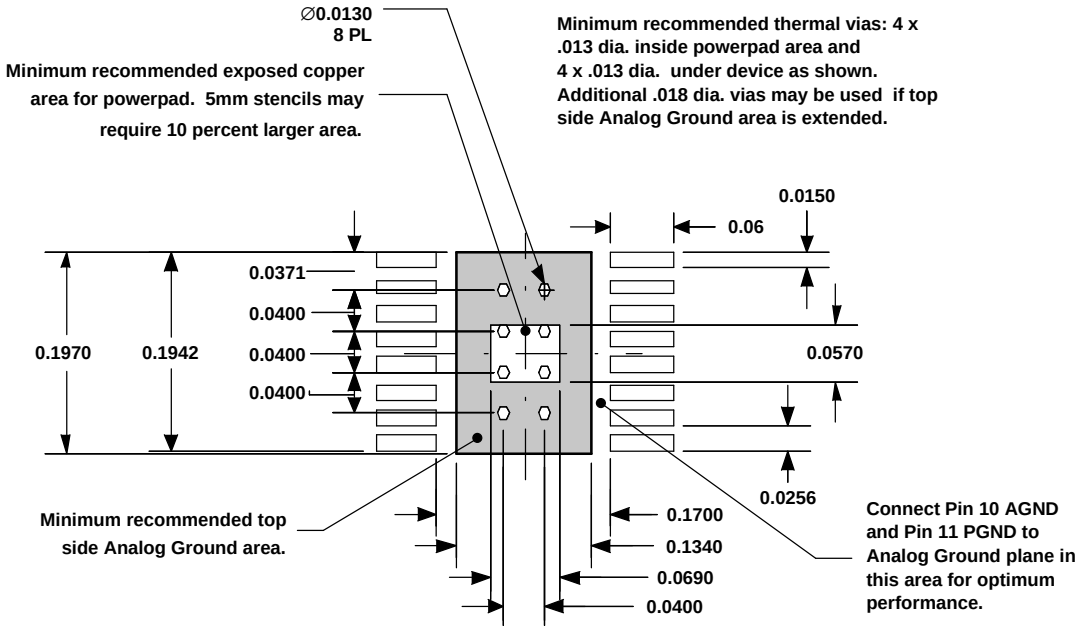


Figure 22. Thermal Considerations for PowerPAD Layout

MODEL FOR LOOP RESPONSE

The Figure 23 shows an equivalent model for the TPS54350 control loop which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier in the TPS54350 is a voltage amplifier with 80 dB (10000 V/V) of open loop gain. The error amplifier can be modeled using an ideal voltage-controlled current source as shown in Figure 23 with a resistor and capacitor on the output. The TPS54350 device has an integrated feed forward compensation circuit which eliminates the impact of the input voltage changes to the overall loop transfer function.

The feed forward gain is modeled as an ideal voltage-controlled voltage source with a gain of 8 V/V. The 1-mV ac voltage between nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting b/c shows the small-signal response of the power stage. Plotting c/a shows the small-signal response of the frequency compensation. Plotting a/b shows the small- signal response of the overall loop. The dynamic load response can be checked by replacing the R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

APPLICATION INFORMATION (continued)

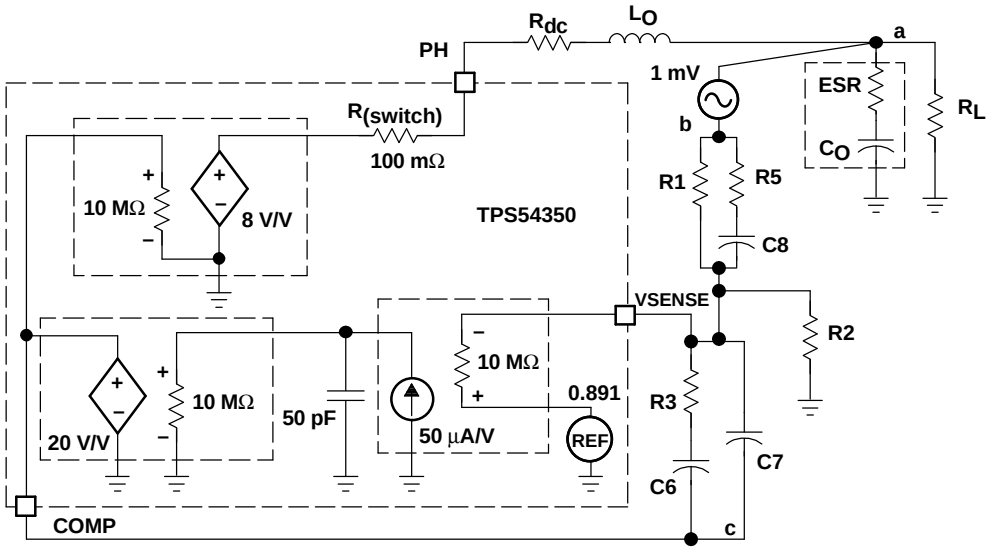


Figure 23. Model of Control Loop

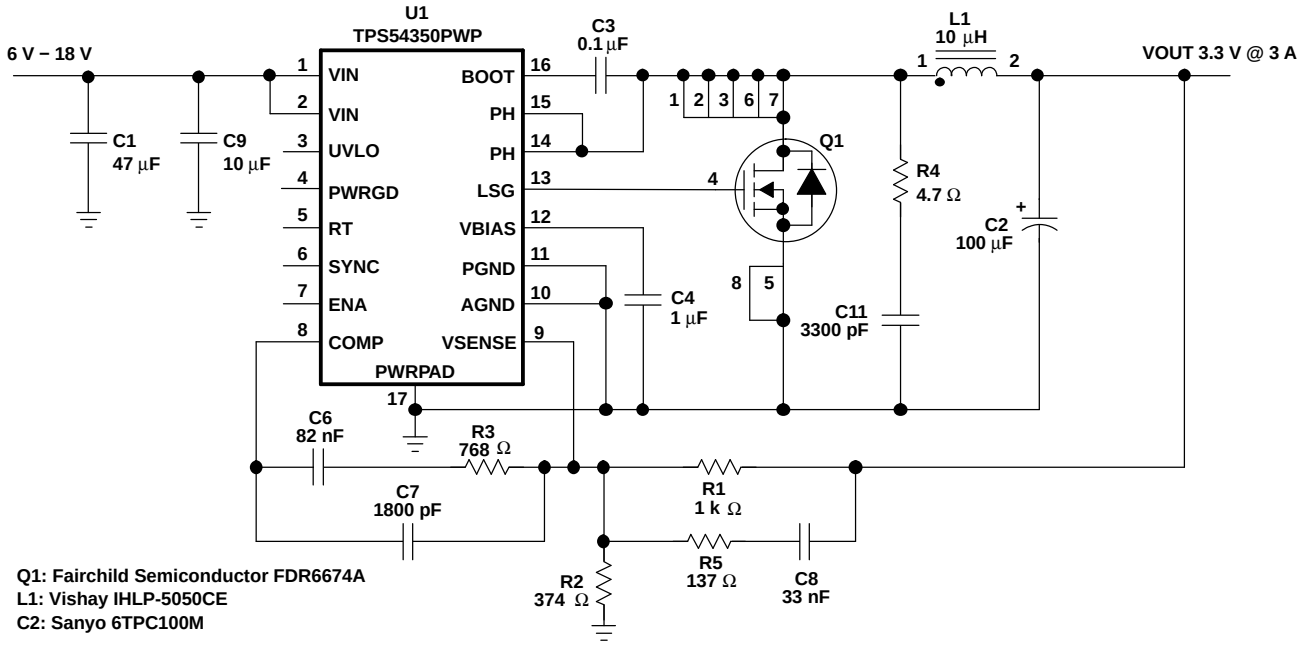


Figure 24. Application Circuit, 12 V to 3.3 V

Figure 24 shows the schematic for a typical TPS54350 application. The TPS54350 can provide up to 3-A output current at a nominal output voltage of 3.3 V. For proper thermal performance, the exposed PowerPAD underneath the device must be soldered down to the printed circuit board.

DESIGN PROCEDURE

The following design procedure can be used to select component values for the TPS54350. Alternately, the SWIFT Designer Software may be used to generate a complete design. The SWIFT Designer Software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

APPLICATION INFORMATION (continued)

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Input voltage range
- Output voltage
- Input ripple voltage
- Output ripple voltage
- Output current rating
- Operating frequency

For this design example, use the following as the input parameters:

DESIGN PARAMETER(1)	EXAMPLE VALUE
Input voltage range	6 V to 18 V
Output voltage	3.3 V
Input ripple voltage	300 mV
Output ripple voltage	30 mV
Output current rating	3 A
Operating frequency	500 kHz

(1) As an additional constraint, the design is set up to be small size and low component height.

SWITCHING FREQUENCY

The switching frequency is set using the RT pin. Grounding the RT pin sets the PWM switching frequency to a default frequency of 250 kHz. Floating the RT pin sets the PWM switching frequency to 500 kHz. By connecting a resistor from RT to AGND, any frequency in the range of 250 to 700 kHz can be set. Use Equation 9 to determine the proper value of RT.

$$RT(k\Omega) = \frac{46000}{f_S(kHz) - 35.9} \quad (9)$$

In this example circuit, RT is not connected and the switching frequency is set at 500 kHz.

INPUT CAPACITORS

The TPS54350 requires an input decoupling capacitor and, depending on the application, a bulk input capacitor. The minimum value for the decoupling capacitor (C9) is 10 µF. A high quality ceramic type X5R or X7R is recommended. The voltage rating should be greater than the maximum input voltage. Additionally some bulk capacitance may be needed, especially if the TPS54350 circuit is not located within about two inches from the input voltage source. The value for this capacitor is not critical but it also should be rated to handle the maximum input voltage including ripple voltage and should filter the output so that input ripple voltage is acceptable.

This input ripple voltage can be approximated by Equation 10:

$$\Delta V_{IN} = \frac{I_{OUT(MAX)} \times 0.25}{C_{BULK} \times f_{sw}} + \left(I_{OUT(MAX)} \times ESR_{MAX}\right) \quad (10)$$

Where $I_{OUT(MAX)}$ is the maximum load current, f_{SW} is the switching frequency, C_{BULK} is the bulk capacitor value and ESR_{MAX} is the maximum series resistance of the bulk capacitor.

The maximum RMS ripple current also needs to be checked. For worst case conditions, this can be approximated by Equation 11:

$$I_{CIN} = \frac{I_{OUT(MAX)}}{2} \quad (11)$$

In this case the input ripple voltage would be 140 mV and the RMS ripple current would be 1.5 A. The maximum voltage across the input capacitors would be VIN max plus delta VIN/2. The chosen bulk and bypass capacitors are each rated for 25 V and the combined ripple current capacity is greater than 3 A, both providing ample margin. It is important that the maximum ratings for voltage and current are not exceeded under any circumstance.

OUTPUT FILTER COMPONENTS

Two components need to be selected for the output filter, L1 and C2. Since the TPS54350 is an externally compensated device, a wide range of filter component types and values can be supported.

Inductor Selection

To calculate the minimum value of the output inductor, use Equation 12:

$$L_{MIN} = \frac{V_{OUT(MAX)} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(max)} \times K_{IND} \times I_{OUT} \times F_{SW}} \quad (12)$$

K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. For designs using low ESR output capacitors such as ceramics, use K_{IND} = 0.3. When using higher ESR output capacitors, K_{IND} = 0.2 yields better results.

For this design example, use K_{IND} = 0.2 and the minimum inductor value is calculated to be 8.98 µH. The next highest standard value is 10 µH, which is used in this design.

For the output filter inductor it is important that the RMS current and saturation current ratings not be exceeded. The RMS inductor current can be found from Equation 13:

$$I_{L(RMS)} = \sqrt{I^2_{OUT(MAX)} + \frac{1}{12} \times \left[\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}\right]^2} \quad (13)$$

and the peak inductor current can be determined with Equation 14:

$$I_{L(PK)} = I_{OUT(MAX)} + \frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{1.6 \times V_{IN(MAX)} \times L_{OUT} \times F_{SW}} \quad (14)$$

For this design, the RMS inductor current is 3.01 A and the peak inductor current is 3.34 A. The chosen inductor is a Vishay IHLP5050CE-01 10 µH. It has a saturation current rating of 14 A and a RMS current rating of 7 A, easily meeting these requirements. A lesser rated inductor could be used, however this device was chosen because of its low profile component height. In general, inductor values for use with the TPS54350 are in the range of 6.8 µH to 47mH.

Capacitor Selection

The important design factors for the output capacitor are dc voltage rating, ripple current rating, and equivalent series resistance (ESR). The dc voltage and ripple current ratings cannot be exceeded. The ESR is important because along with the inductor current it determines the amount of output ripple voltage. The actual value of the output capacitor is not critical, but some practical limits do exist. Consider the relationship between the desired closed loop crossover frequency of the design and LC corner frequency of the output filter. In general, it is desirable to keep the closed loop crossover frequency at less than 1/5 of the switching frequency. With high switching frequencies such as the 500-kHz frequency of this design, internal circuit limitations of the TPS54350 limit the practical maximum crossover frequency to about 50 kHz. Additionally, to allow for adequate phase gain in the compensation network, the LC corner frequency should be about one decade or so below the closed loop crossover frequency. This limits the minimum capacitor value for the output filter to:

$$C_{OUT} = \frac{1}{L_{OUT}} \times \left(\frac{K}{2\pi f_{CO}}\right)^2 \quad (15)$$

Where K is the frequency multiplier for the spread between f_{LC} and f_{CO}. K should be between 5 and 15, typically 10 for one decade difference. For a desired crossover of 50 kHz and a 10-µH inductor, the minimum value for the output capacitor is 100 µF. The selected output capacitor must be rated for a voltage greater than the desired output voltage plus one half the ripple voltage. Any derating amount must also be included. The maximum RMS ripple current in the output capacitor is given by Equation 16:

$$I_{COUT(RMS)} = \frac{1}{\sqrt{12}} \times \left[\frac{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times N_C}\right] \quad (16)$$

where N_C is the number of output capacitors in parallel.

The maximum ESR of the output capacitor is determined by the amount of allowable output ripple as specified in the initial design parameters. The output ripple voltage is the inductor ripple current times the ESR of the output filter so the maximum specified ESR as listed in the capacitor data sheet is given by Equation 17:

$$ESR_{MAX} = N_C \times \left[\frac{V_{IN(MAX)} \times L_{OUT} \times F_{SW} \times 0.8}{V_{OUT} \times \left(V_{IN(MAX)} - V_{OUT}\right)}\right] \times \Delta V_{p-p(MAX)} \quad (17)$$

Where ΔV_{p-p} is the desired peak-to-peak output ripple. For this design example, a single 100-µF output capacitor is chosen for C2 since the design goal is small size. The calculated RMS ripple current is 156 mV and the maximum ESR required is 59 mΩ. A capacitor that meets these requirements is a Sanyo Poscap 6TPC100M, rated at 6.3 V with a maximum ESR of 45 mΩ and a ripple current rating of 1.7 A. An additional small 0.1-µF ceramic bypass capacitor is also used.

Other capacitor types work well with the TPS54350, depending on the needs of the application.

COMPENSATION COMPONENTS

The external compensation used with the TPS54350 allows for a wide range of output filter configurations. A large range of capacitor values and types of dielectric are supported. The design example uses type 3 compensation consisting of R1, R3, R5, C6, C7, and C8. Additionally, R2 along with R1 forms a voltage divider network that sets the output voltage. These component reference designators are the same as those used in the SWIFT Designer Software. There are a number of different ways to design a compensation network. This procedure outlines a relatively simple procedure that produces good results with most output filter combinations. Use of the SWIFT Designer Software for designs with unusually high closed loop crossover frequencies, low value, low ESR output capacitors such as ceramics or if the designer is unsure about the design procedure is recommended.

When designing compensation networks for the TPS54350, a number of factors need to be considered. The gain of the compensated error amplifier should not be limited by the open loop amplifier gain characteristics and should not produce excessive gain at the switching frequency. Also, the closed loop crossover frequency should be set less than one fifth of the switching frequency, and the phase margin at crossover must be greater than 45 degrees. The general procedure outlined here produces results consistent with these requirements without going into great detail about the theory of loop compensation.

First calculate the output filter LC corner frequency using Equation 18:

$$f_{LC} = \frac{1}{2\pi\sqrt{L_{OUT}C_{OUT}}} \quad (18)$$

For the design example, f_{LC} = 5033 Hz.

The closed loop crossover frequency should be greater than f_{LC} and less than one fifth of the switching frequency. Also, the crossover frequency should not exceed 50 kHz, as the error amplifier may not provide the desired gain. For this design, a crossover frequency of 30 kHz was chosen. This value is chosen for comparatively wide loop bandwidth while still allowing for adequate phase boost to insure stability.

Next calculate the R2 resistor value for the output voltage of 3.3 V using Equation 19:

$$R2 = \frac{R1 \times 0.891}{V_{OUT} - 0.891} \tag{19}$$

For any TPS54350 design, start with an R1 value of 1 kΩ. R2 is then 374 Ω.

Now the values for the compensation components that set the poles and zeros of the compensation network can be calculated. Assuming that R1 > R5 and C6 > C7, the pole and zero locations are given by Equation 20 through Equation 23:

$$f_{Z1} = \frac{1}{2\pi R3C6} \tag{20}$$

$$f_{INT} = \frac{1}{2\pi R1C6} \tag{21}$$

$$f_{Z2} = \frac{1}{2\pi R1C8} \tag{22}$$

$$f_{P1} = \frac{1}{2\pi R5C8} \tag{23}$$

Additionally there is a pole at the origin, which has unity gain with the following frequency:

$$f_{P2} = \frac{1}{2\pi R3C7} \tag{24}$$

This pole is used to set the overall gain of the compensated error amplifier and determines the closed loop crossover frequency. Since R1 is given as 1 kΩ and the crossover frequency is selected as 30 kHz, the desired f_{INT} can be calculated with Equation 25:

$$f_{INT} = \frac{10^{-0.9} \times f_{CO}}{2} \tag{25}$$

And the value for C6 is given by Equation 26:

$$C6 = \frac{1}{2\pi R1 f_{INT}} \tag{26}$$

The first zero, fZ1, is located at one half the output filter LC corner frequency, so R3 can be calculated from:

$$R3 = \frac{1}{\pi C6 f_{LC}} \tag{27}$$

The second zero, f_{Z2}, is located at the output filter LC corner frequency, so C8 can be calculated from:

$$C8 = \frac{1}{2\pi R1 f_{LC}} \tag{28}$$

The first pole, f_{P1}, is located to coincide with the output filter ESR zero frequency. This frequency is given by:

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}} \tag{29}$$

where R_{ESR} is the equivalent series resistance of the output capacitor.

In this case, the ESR zero frequency is 35.4 kHz and R5 can be calculated from:

$$R5 = \frac{1}{2\pi C8 f_{ESR}} \quad (30)$$

The final pole is placed at a frequency above the closed loop crossover frequency high enough to not cause the phase to decrease too much at the crossover frequency while still providing enough attenuation so that there is little or no gain at the switching frequency. The f_{P2} pole location for this circuit is set to four times the closed loop crossover frequency and the last compensation component value C7 can be derived as follows:

$$C7 = \frac{1}{8\pi R3 f_{CO}} \quad (31)$$

Note that capacitors are only available in a limited range of standard values, so the nearest standard value has been chosen for each capacitor. The measured closed loop response for this design is shown in Figure 5.

BIA AND BOOTSTRAP CAPACITORS

Every TPS54350 design requires a bootstrap capacitor, C3 and a bias capacitor, C4. The bootstrap capacitor must be 0.1 µF. The bootstrap capacitor is located between the PH pins and BOOT pin. The bias capacitor is connected between the VBIAS pin and AGND. The value should be 1 µF. Both capacitors should be high quality ceramic types with X7R or X5R grade dielectric for temperature stability. They should be placed as close to the device connection pins as possible.

LOW-SIDE FET

The TPS54350 is designed to operate using an external low-side FET and the LSG pin provides the gate drive output. Connect the drain to the PH pin, the source to PGND, and the gate to LSG. The TPS54350 gate drive circuitry is designed to accommodate most common n-channel FETs that are suitable for this application. The SWIFT Designer Software can be used to calculate all the design parameters for low-side FET selection. There are some simplified guidelines that can be applied that produce an acceptable solution in most designs.

The selected FET must meet the absolute maximum ratings for the application:

Drain-source voltage (V_{DS}) must be higher than the maximum voltage at the PH pin, which is V_{INMAX} + 0.5 V.

Gate-source voltage (V_{GS}) must be greater than 8 V.

Drain current (ID) must be greater than 1.1 x I_{OUTMAX}.

Drain-source on resistance (r_{DSON}) should be as small as possible, less than 30 mΩ is desirable. Lower values for r_{DSON} result in designs with higher efficiencies. It is important to note that the low-side FET on time is typically longer than the high-side FET on time, so attention paid to low-side FET parameters can make a marked improvement in overall efficiency.

Total gate charge (Q_g) must be less than 50 nC. Again, lower Q_g characteristics result in higher efficiencies.

Additionally, check that the device chosen is capable of dissipating the power losses.

For this design, a Fairchild FDR6674A 30-V n-channel MOSFET is used as the low-side FET. This particular FET is specifically designed to be used as a low-side synchronous rectifier.

POWER GOOD

The TPS54350 is provided with a power good output pin PWRGD. This output is an open drain output and is intended to be pulled up to a 3.3-V or 5-V logic supply. A 10-kΩ, pullup resistor works well in this application. The absolute maximum voltage is 6 V, so care must be taken not to connect this pullup resistor to VIN if the maximum input voltage exceeds 6 V.

SNUBBER CIRCUIT

R4 and C11 of the application schematic in Figure 24 comprise a snubber circuit. The snubber is included to reduce over-shoot and ringing on the phase node when the internal high-side FET turns on. Since the frequency and amplitude of the ringing depends to a large degree on parasitic effects, it is best to choose these component values based on actual measurements of any design layout. See literature number SLUP100 for more detailed information on snubber design.

Figure 25 shows an application where a clamp diode is used in place of the low-side FET. The TPS54350 incorporates an integrated pull-down FET so that the circuit remains operating in continuous mode during light load operation. A 3-A, 40-V Schottky diode such as the Motorola MBRS340T3 or equivalent is recommended.

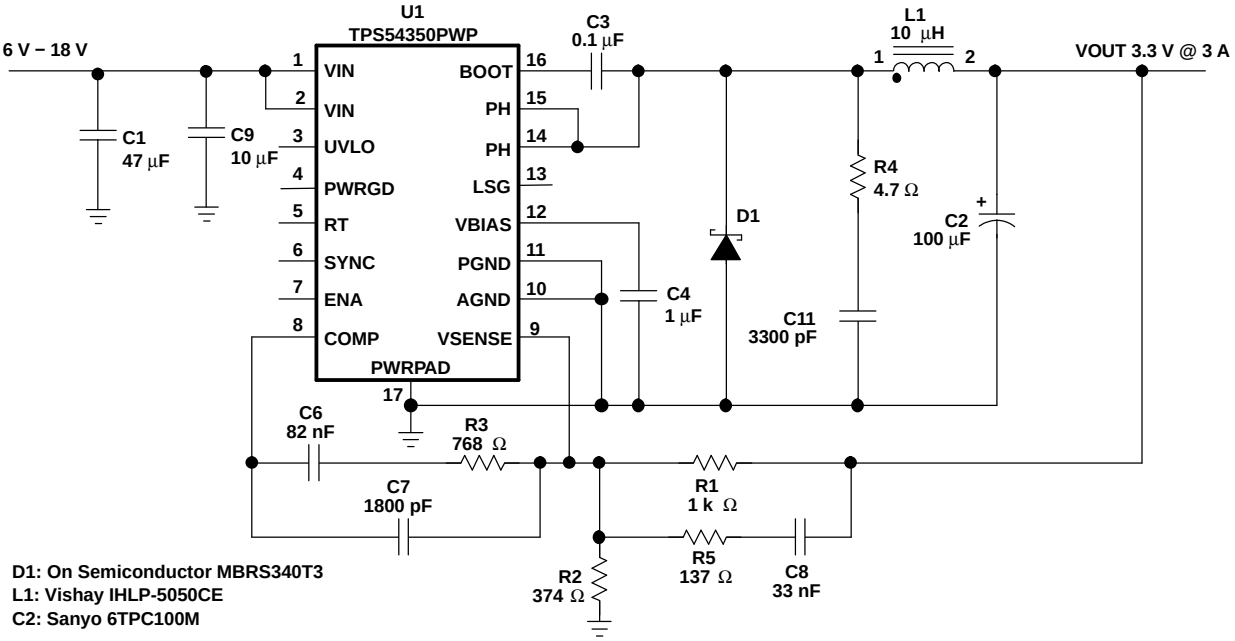


Figure 25. 3.3-V Power Supply With Schottky Diode

Figure 25 is an example of power supply sequencing using two TPS54350s. U1 is used to generate an output of 3.3 V, while the voltage output of U2 is set at 1.8 V, typical I/O and core voltages for microprocessors and FPGAs. In the circuit, the 3.3-V supply is designed to power up first. The PWRGD pin of U1 is tied to the ENA pin of U2 so that the 1.8-V supply starts to ramp up after the 3.3-V supply is within regulation. Since the RT pin of U1 is floating, the SYNC pin is an output. This synchronization signal is fed to the SYNC pin of U2. The RT pin of U2 has a 110-kΩ resistor to ground, and the SYNC pin for this device acts as an input. The 1.8-V supply operates synchronously with the 3.3-V supply and their switching node rising edges are approximately 1805 out of phase allowing for a reduction in the input voltage ripple. See Figure 19 for this waveform.

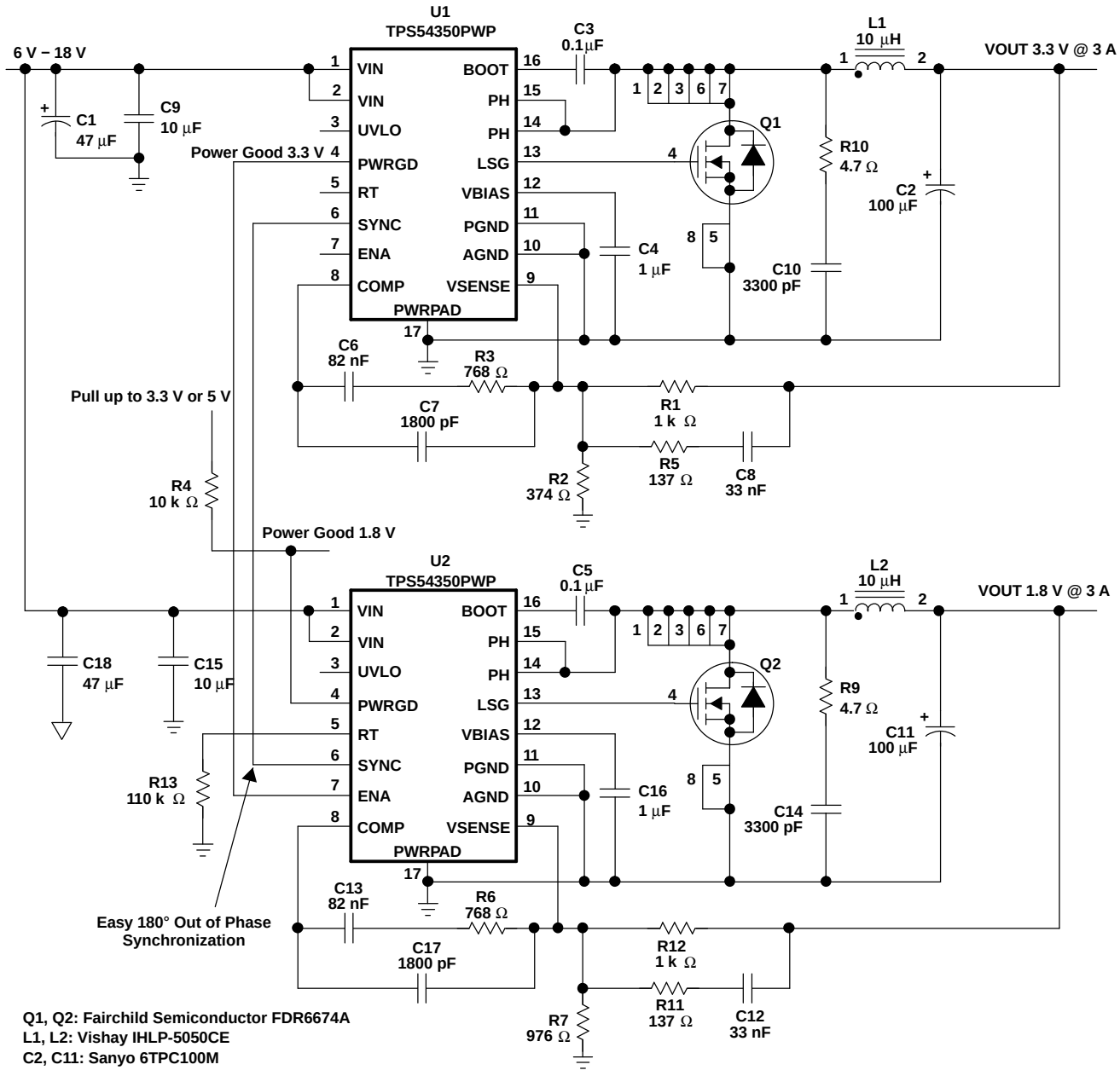


Figure 26. 3.3-V/1.8-V Power Supply With Sequencing

In Figure 27 the TPS54350 is configured as an inverting supply. The -5-V output is at the pins which would normally be connected to ground. The output junction of the LC output filter, which is normally the output in a buck converter, is tied to ground. An additional 10-µF capacitor, C7, is required from the output to VIN.

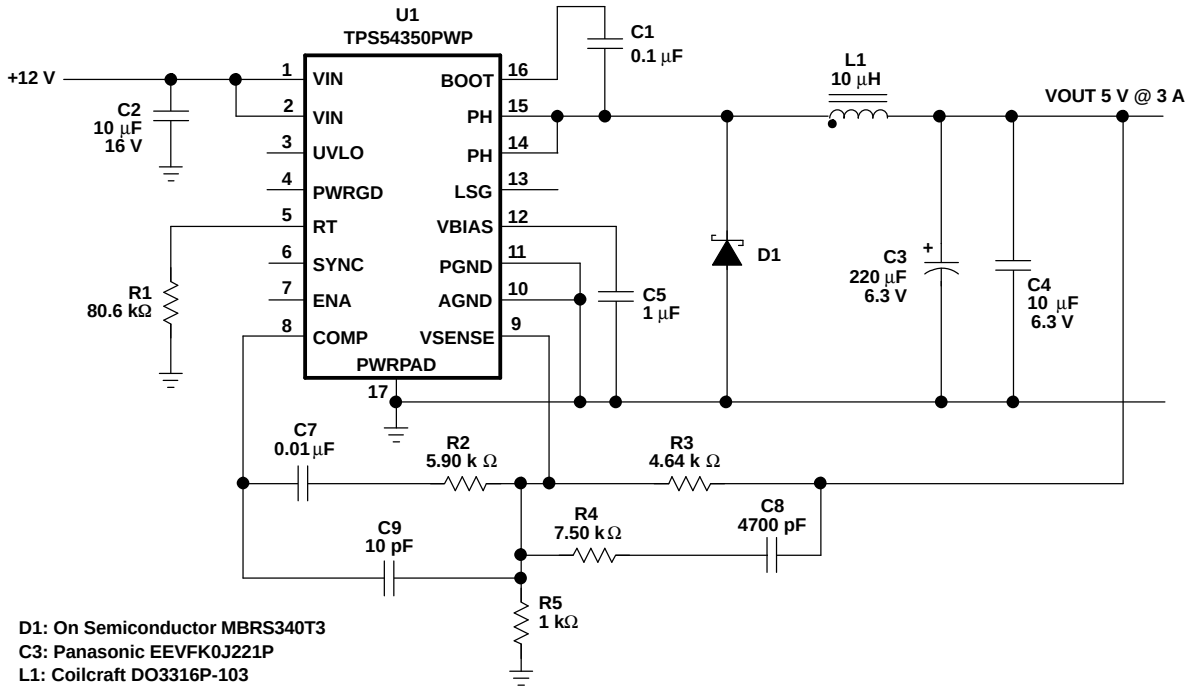


Figure 27. Inverting Power Supply, 5 V to –5 V at 1.5 A

Figure 28 is an example of a 12-V to 5-V converter using economical output filter components.

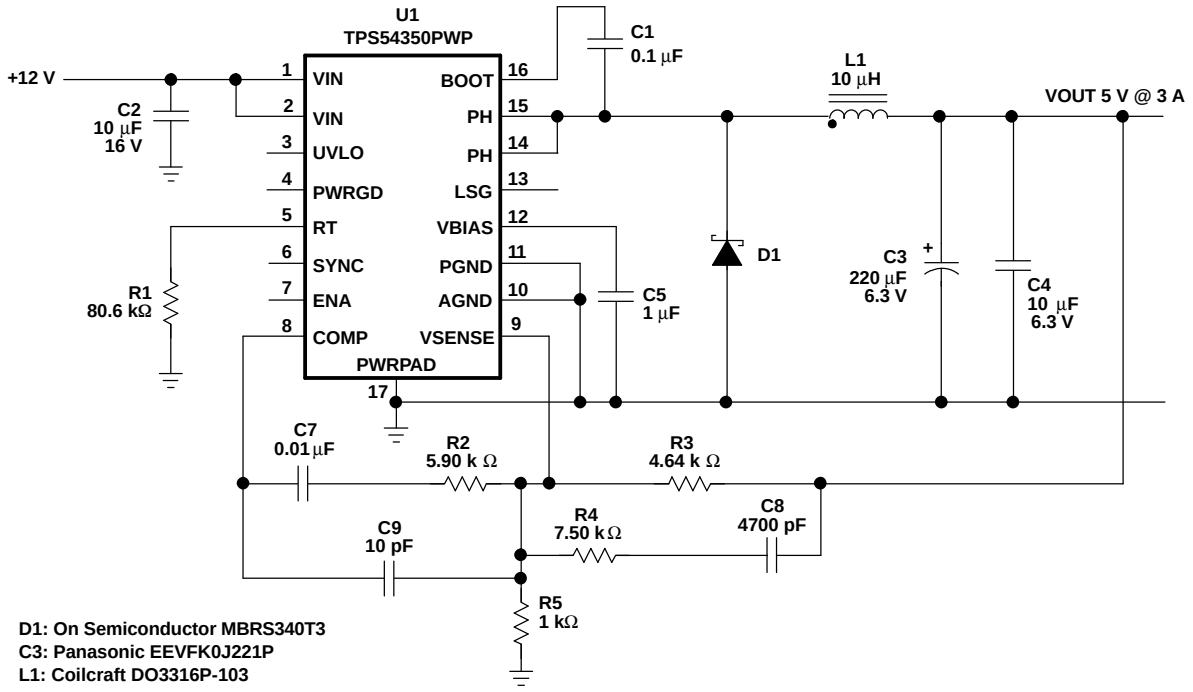


Figure 28. 12-V to 5-V Using Aluminum Electrolytic for LCD TV

MINIMUM OUTPUT VOLTAGE vs INPUT VOLTAGE

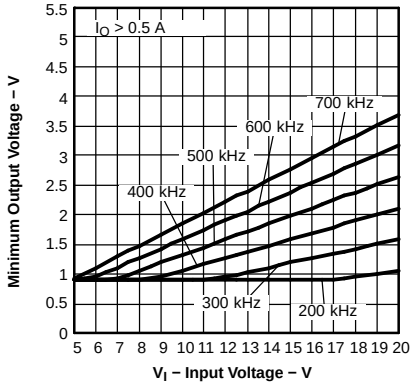


Figure 29.

MAXIMUM SWITCHING FREQUENCY vs INPUT VOLTAGE

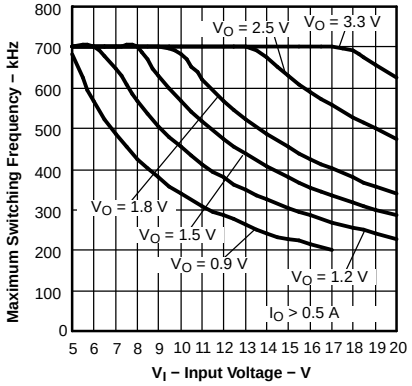


Figure 30.

MINIMUM OUTPUT VOLTAGE vs INPUT VOLTAGE

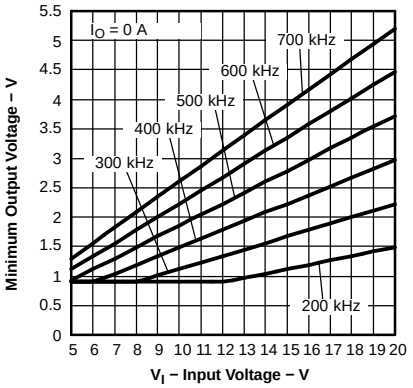


Figure 31.

MAXIMUM SWITCHING FREQUENCY vs INPUT VOLTAGE

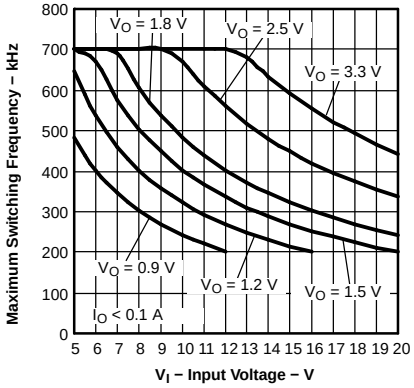


Figure 32.

RT RESISTANCE vs SWITCHING FREQUENCY

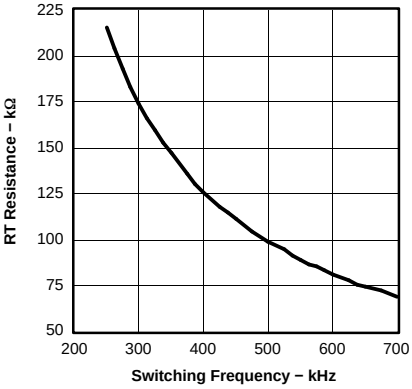


Figure 33.

VIN(UVLO) START AND STOP vs FREE-AIR TEMPERATURE

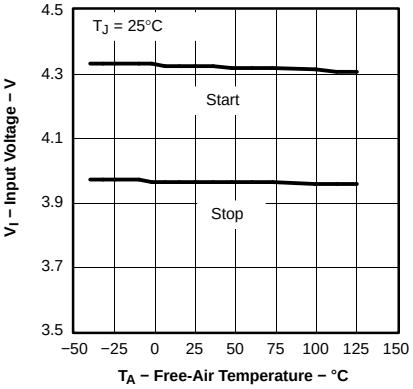


Figure 34.

ENABLED SUPPLY CURRENT vs INPUT VOLTAGE

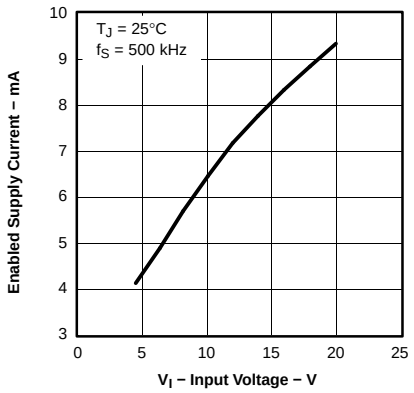


Figure 35.

DISABLED SUPPLY CURRENT vs INPUT VOLTAGE

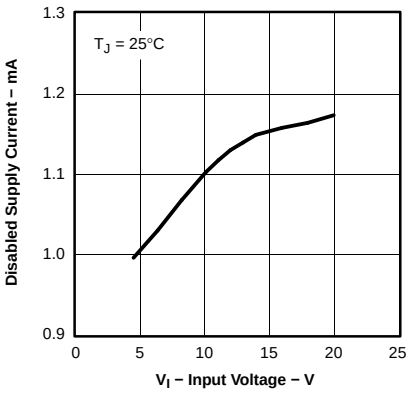


Figure 36.

BIAS VOLTAGE vs INPUT VOLTAGE

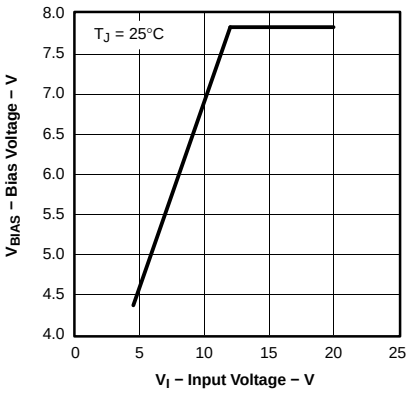


Figure 37.

POWER GOOD THRESHOLD VS JUNCTION TEMPERATURE

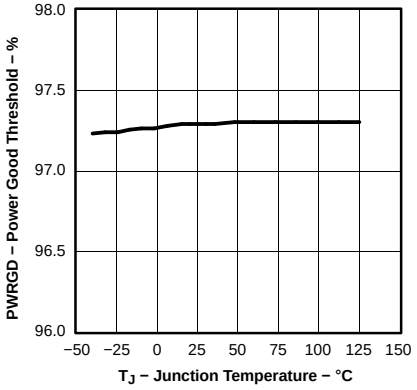


Figure 38.

INTERNAL VOLTAGE REFERENCE VS JUNCTION TEMPERATURE

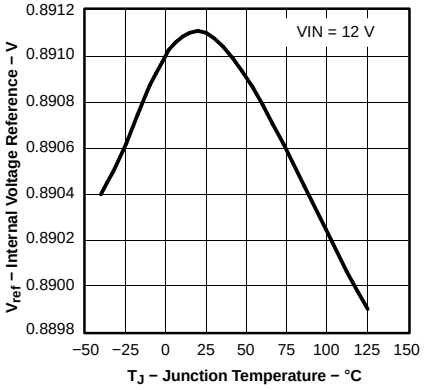


Figure 39.

CURRENT LIMIT VS INPUT VOLTAGE

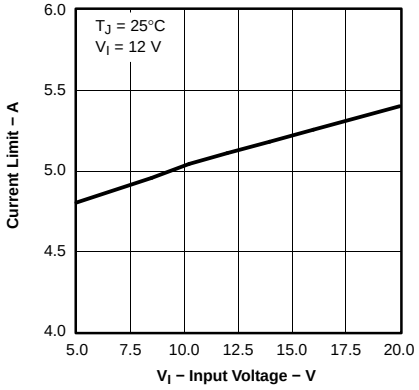


Figure 40.

ON RESISTANCE VS JUNCTION TEMPERATURE

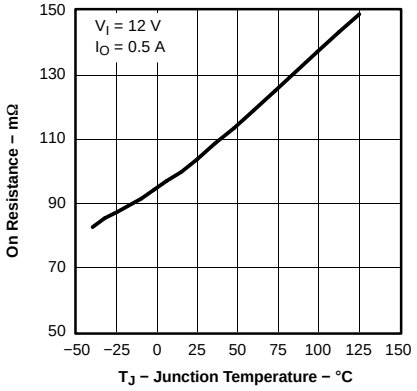


Figure 41.

PH VOLTAGE VS SUPPLY CURRENT

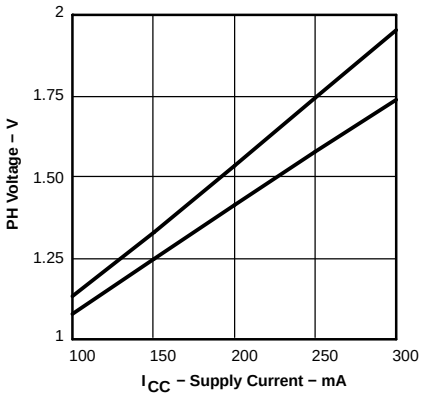


Figure 42.

SLOW START CAPACITANCE VS TIME

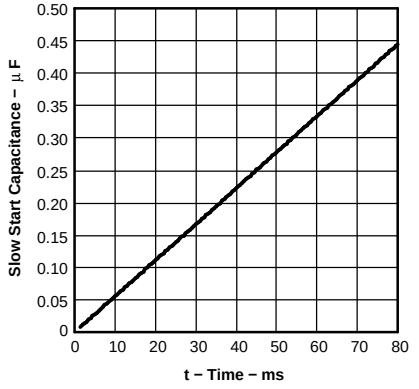


Figure 43.

POWER GOOD DELAY VS SWITCHING FREQUENCY

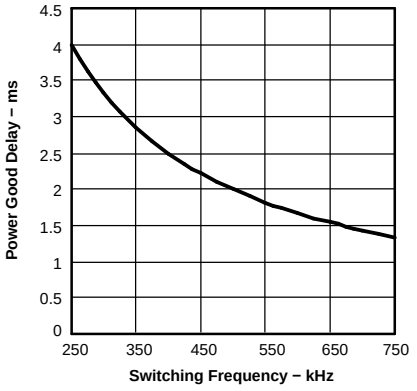


Figure 44.

HHICCUP TIME VS SWITCHING FREQUENCY

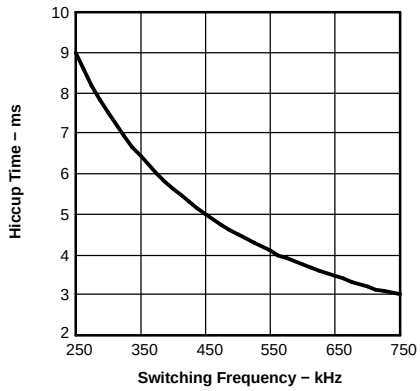


Figure 45.

INTERNAL SLOW START TIME VS SWITCHING FREQUENCY

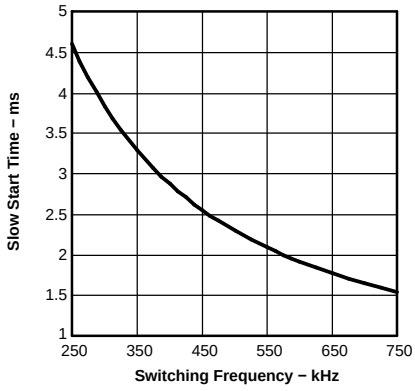


Figure 46.

FREE-AIR TEMPERATURE vs MAXIMUM OUTPUT CURRENT

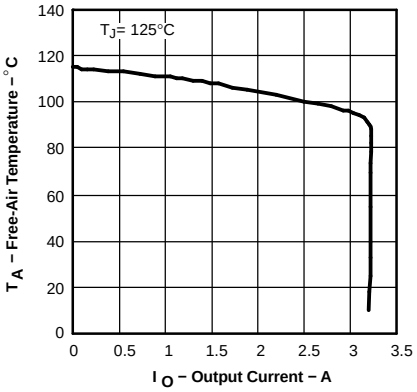


Figure 47.

MAXIMUM OUTPUT VOLTAGE vs INPUT VOLTAGE

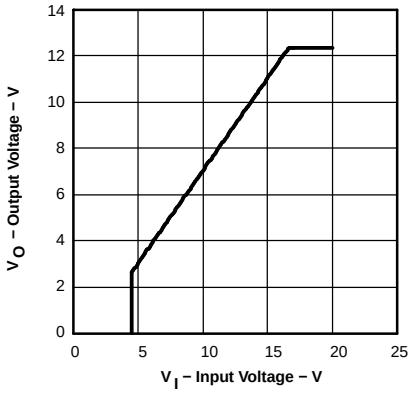


Figure 48.

POWER DISSIPATION vs FREE-AIR TEMPERATURE

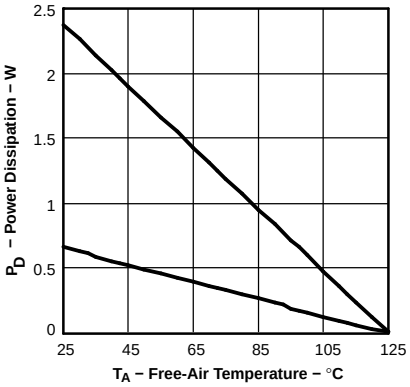


Figure 49.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54350MPWPREP	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	54350EP	Samples
TPS54350MPWPREPG4	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	54350EP	Samples
V62/06610-01XE	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	54350EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS54350-EP :

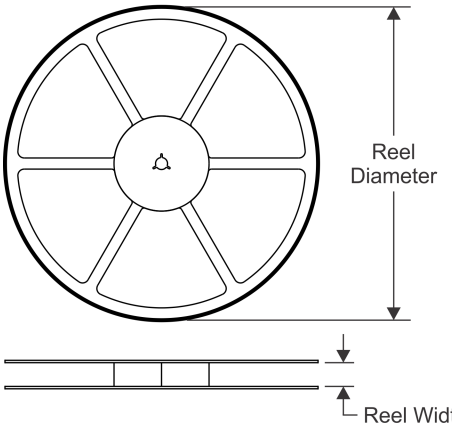
- Catalog: TPS54350

NOTE: Qualified Version Definitions:

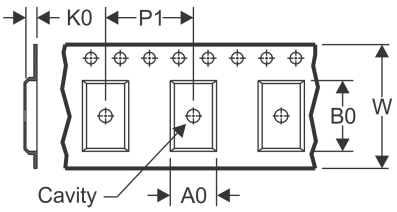
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

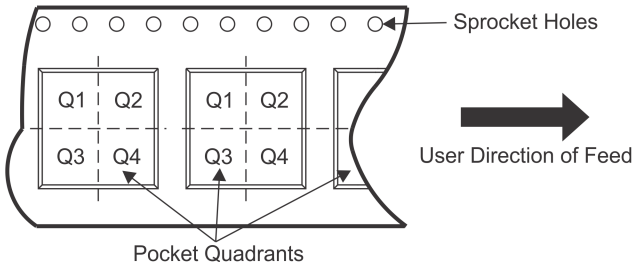


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

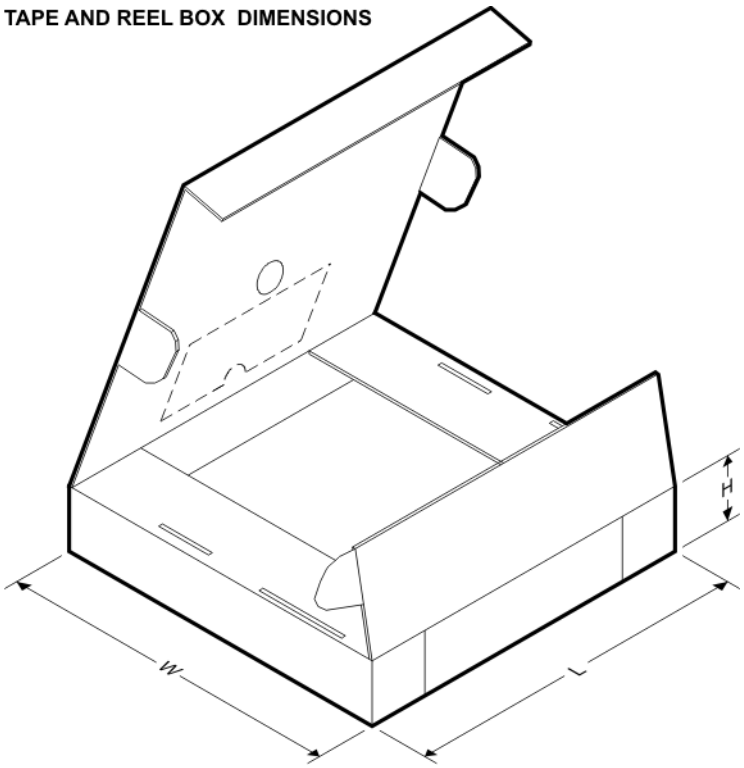
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54350MPWPREP	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

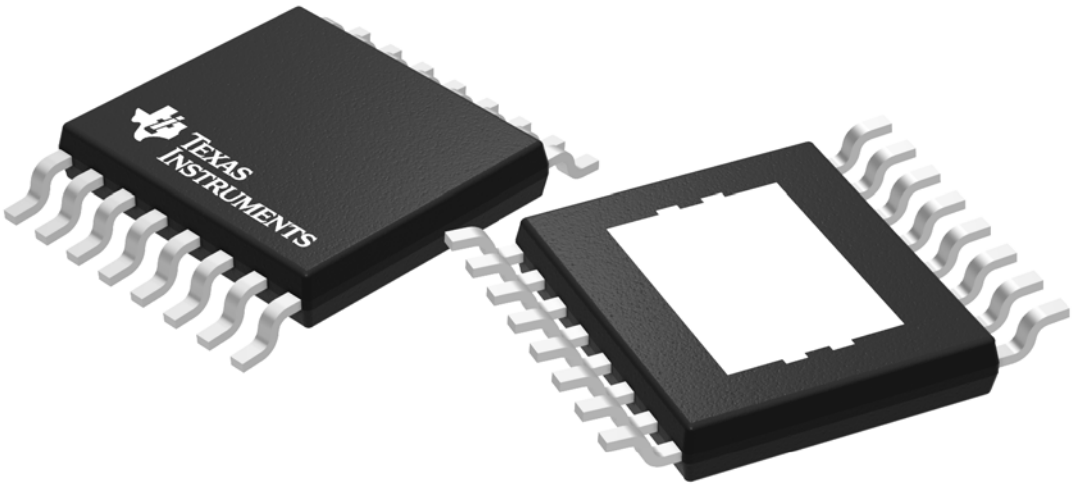


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54350MPWPREP	HTSSOP	PWP	16	2000	350.0	350.0	43.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

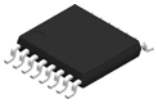
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

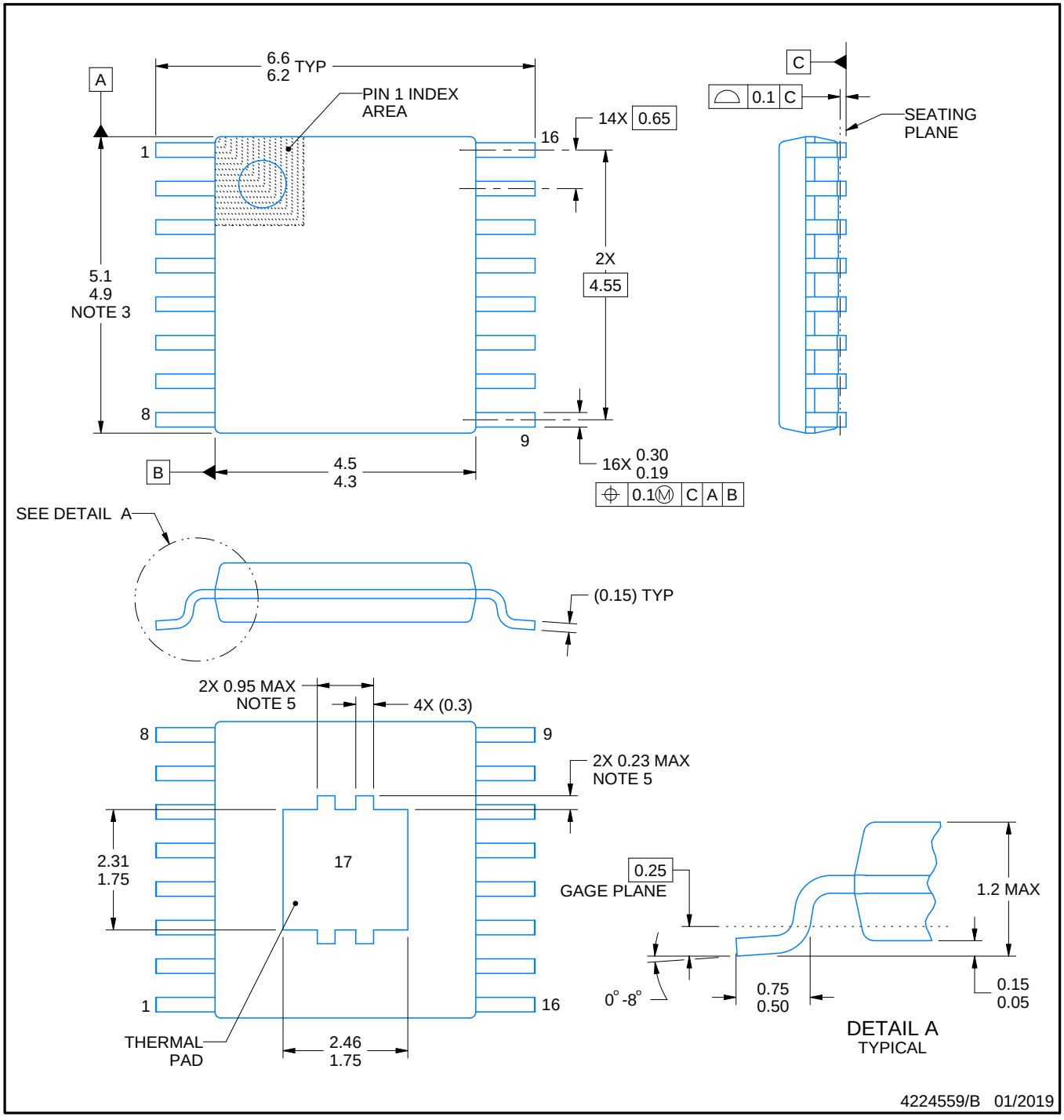
PACKAGE OUTLINE

PWP0016C



PowerPAD™ TSSOP - 1.2 mm max height

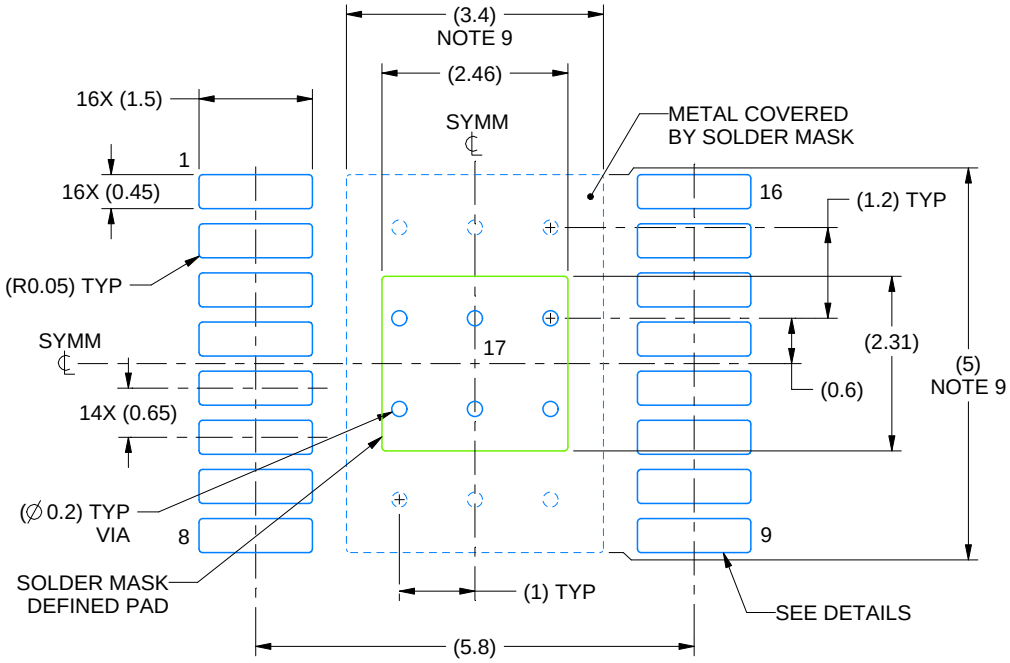
SMALL OUTLINE PACKAGE



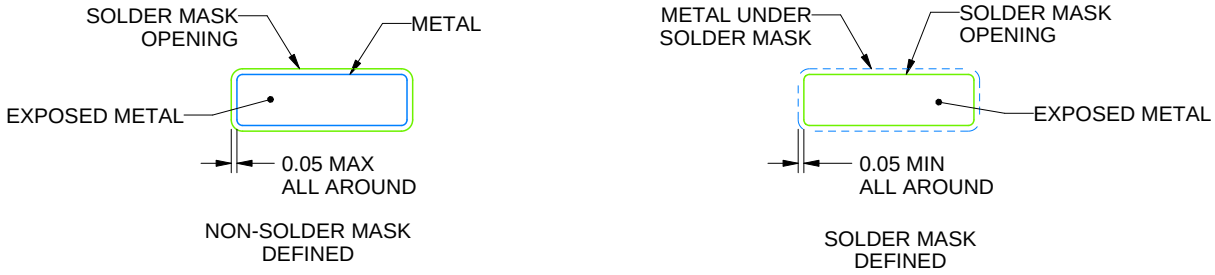
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

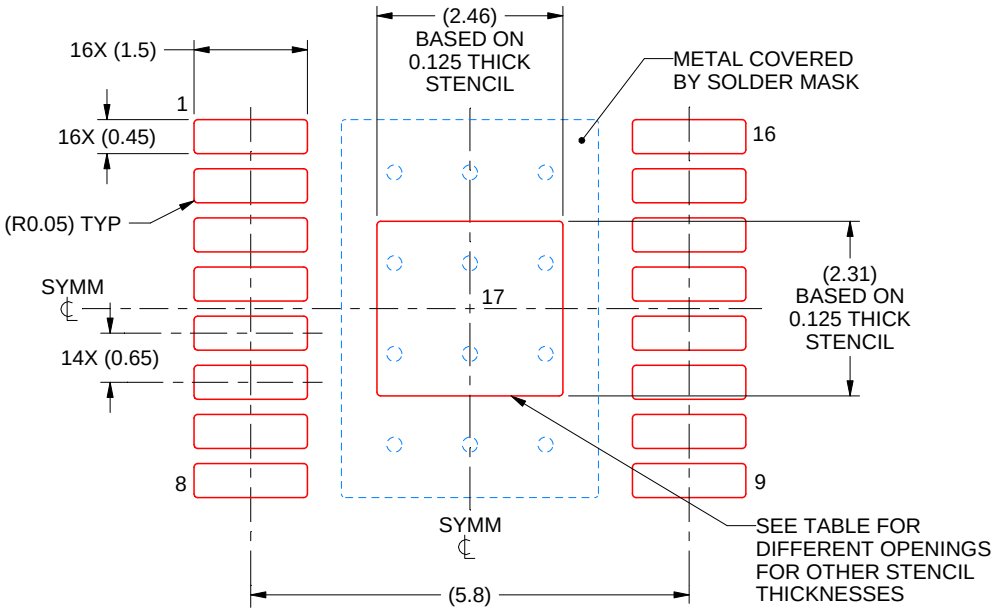


SOLDER MASK DETAILS

4224559/B 01/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.58
0.125	2.46 X 2.31 (SHOWN)
0.15	2.25 X 2.11
0.175	2.08 X 1.95

4224559/B 01/2019

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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