ATA663431/54

LIN SBC including LIN Transceiver, Voltage Regulator, Window Watchdog and High-Side Switch

Features

- Supply Voltage up to 40V
- Operating Voltage V_{VS} = 5V to 28V
- Supply Current
  - Sleep mode: typically 10 µA
  - Silent mode: typically 47 µA
  - Very low current consumption at low supply voltages (2V < V_{VS} < 5.5V): typically 150 µA
- Linear Low-Drop Voltage Regulator, 85 mA Current Capability:
  - MLC (multilayer ceramic) capacitor with 0Ω ESR
  - Normal, Fail-Safe, and Silent mode

    ATA663454: V_{VCC} = 5.0V, ±2%

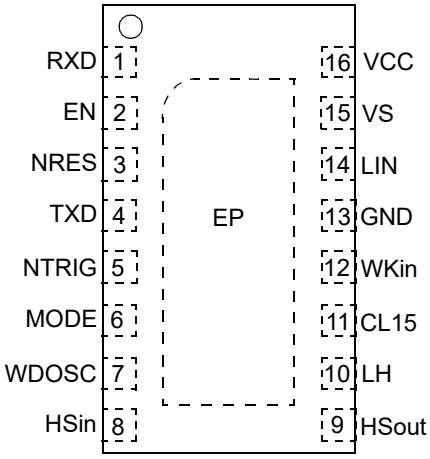
    ATA663431: V_{VCC} = 3.3V, ±2%
  - Sleep mode: VCC is switched off
- VCC Undervoltage Detection with Open Drain Reset Output (NRES, 4 ms reset time)
- Voltage Regulator is Short Circuit and Overtemperature Protected
- Adjustable Watchdog Time via External Resistor
- Negative Trigger Input for Watchdog
- Limp Home Watchdog Failure Output
- LIN Physical Layer according to LIN 2.0, 2.1, 2.2, 2.2A, ISO 17987-4 and SAEJ2602-2
- Bus Pin is Overtemperature and Short Circuit Protected versus GND and Battery
- High-Side Switch
- Wake-Up Capability via LIN Bus (100 µs dominant), WKin pin and CL15 pin
- Wake-up Source Recognition
- TXD Time-out Timer
- Advanced EMC and ESD Performance
- Fulfills the OEM “Hardware Requirements for LIN in Automotive Applications Rev.1.3”
- Interference and Damage Protection According to ISO 7637
- Qualified According to AEC-Q100
- Package: 16-lead 3 x 5.5 mm VDFN with Wettable Flanks (Moisture Sensitivity Level 1)

General Description

The ATA663431/54 is a new generation of system basis chip (SBC) with a fully integrated LIN transceiver, designed in compliance with LIN specifications 2.0, 2.1, 2.2, 2.2A, ISO 17987-4 and SAEJ2602-2, with a low-drop voltage regulator (3.3V/5V/85 mA), a window watchdog and a high-side switch. This combination makes it possible to develop simple, but powerful, slave nodes in LIN-bus systems. ATA663431/54 is designed to handle low-speed data communication in vehicles (such as in convenience electronics). Improved slope control at the LIN driver ensures secure data communication up to 20 Kbaud. The bus output is designed to withstand high voltage. Sleep mode and Silent mode guarantee minimized current consumption even in the case of a floating or short-circuited LIN bus.

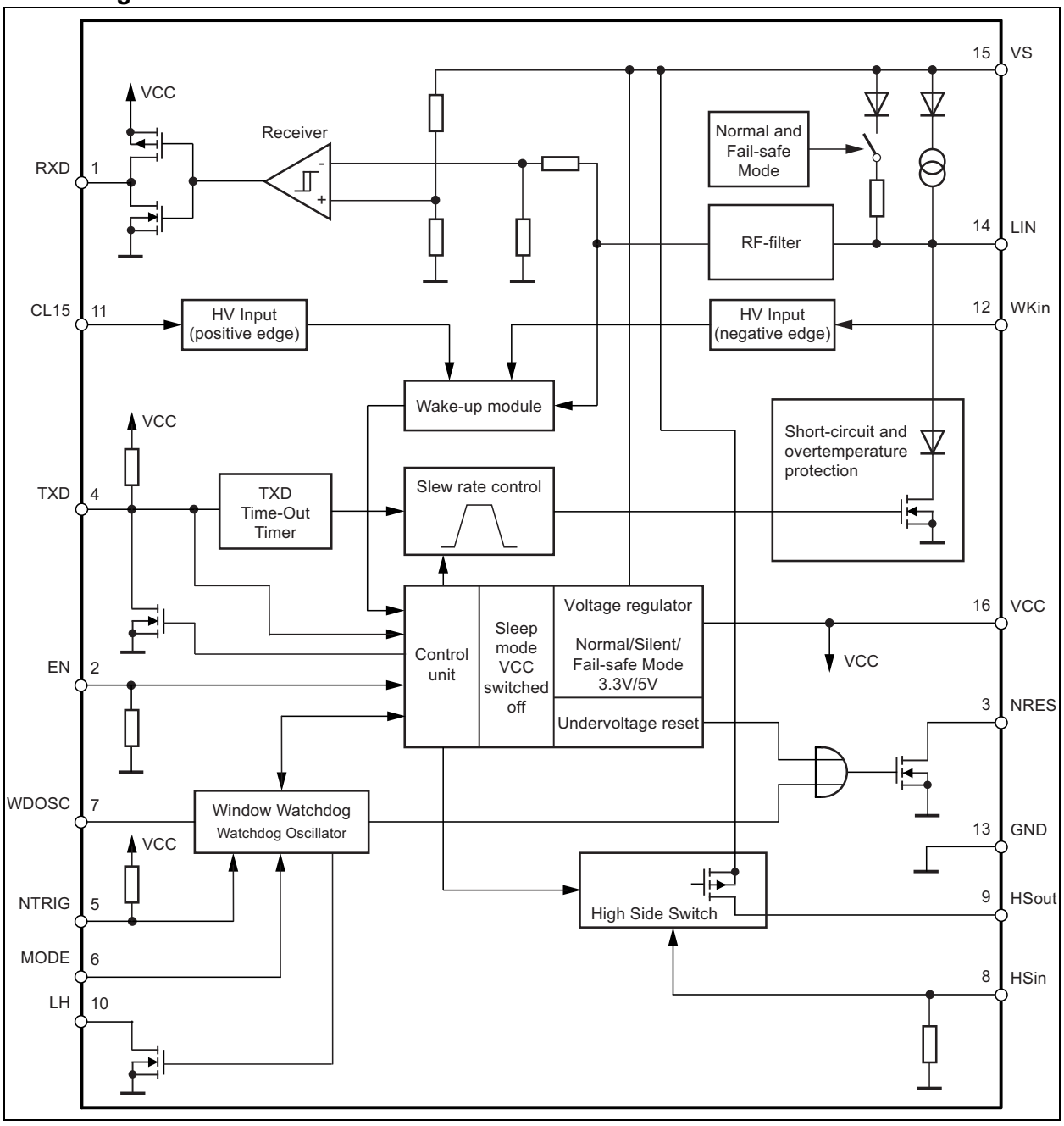
Package Types

ATA663431/ATA663454
3 x 5.5 mm VDFN16*



* Includes Exposed Thermal Pad (EP).

Block Diagram



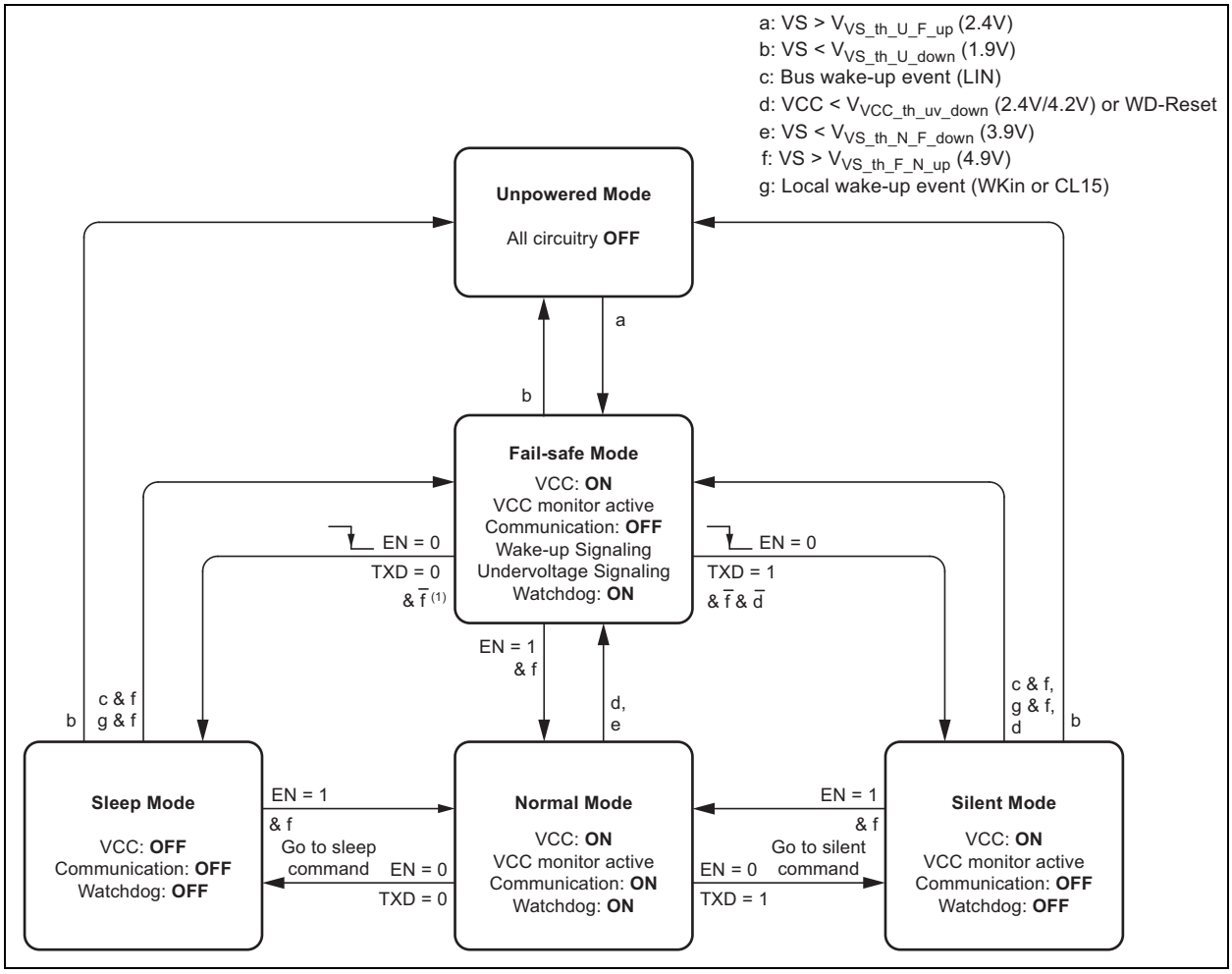
1.0 FUNCTIONAL DESCRIPTION

1.1 Physical Layer Compatibility

Because the LIN physical layer is independent of higher LIN layers (such as the LIN protocol layer), all nodes with a LIN physical layer according to revision 2.x can be mixed with LIN physical layer nodes found in older versions (for example, LIN 1.0, LIN, 1.1, LIN 1.2, LIN 1.3) without any restrictions.

1.2 Operating Modes

FIGURE 1-1: OPERATING MODES



Note 1: Condition $\bar{f}$ is valid for the VS ramp up; for the VS ramp down condition e is valid instead of the condition $\bar{f}$.

TABLE 1-1: OPERATING MODES (MODE PIN IS ALWAYS LOW)

Operating Modes	Transceiver	Voltage Regulator	Watchdog	LH	High-Side Output	LIN	TXD	RXD
Fail-Safe	OFF	ON	ON	WD dependent	HSin-dependent	Recessive	Signaling fail-safe sources (see Table 1-2)	
Normal	ON	ON	ON	WD dependent	HSin-dependent	TXD dependent	Follows data transmission	
Silent	OFF	ON	OFF	Remains in previ-ous state	HSin-dependent	Recessive	High	High
Sleep/ Unpowered	OFF	OFF	OFF	OFF	OFF	Recessive	Low	Low

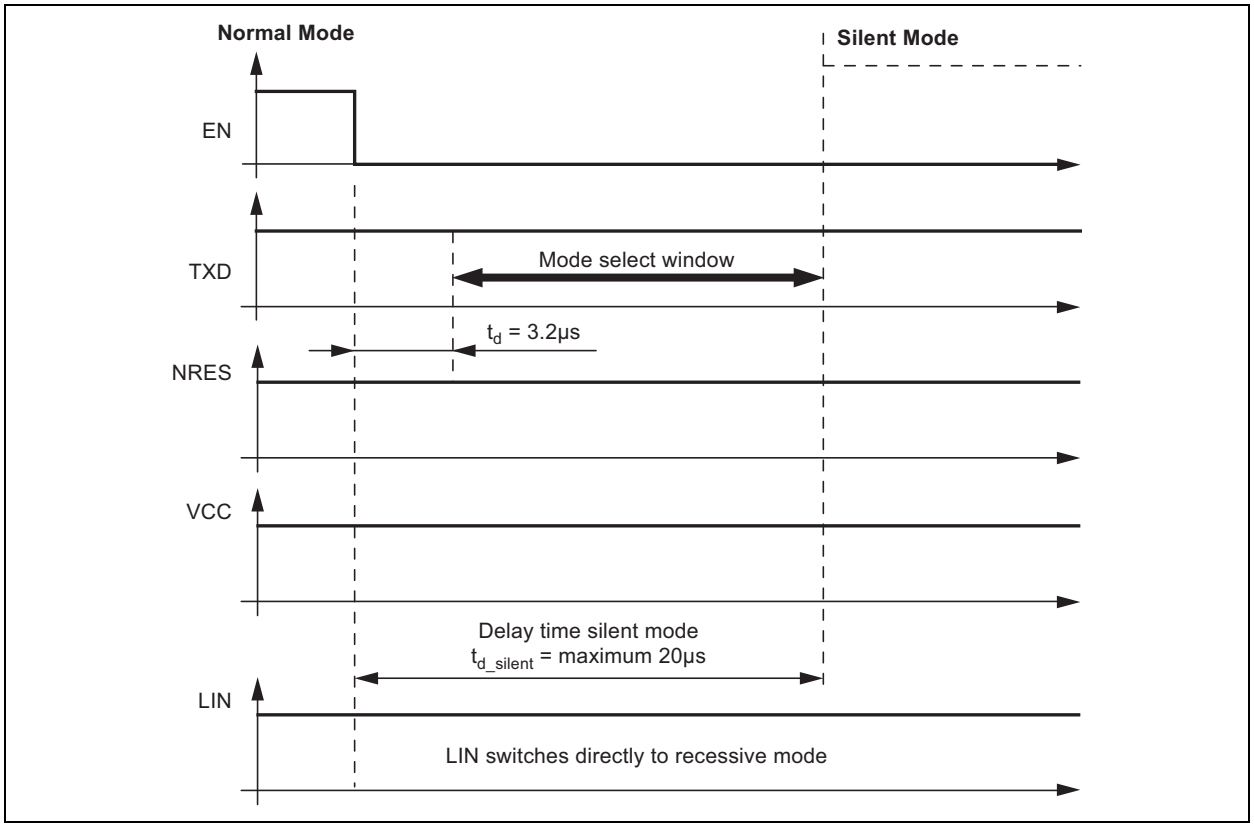
1.2.1 NORMAL MODE

This is the normal transmission and receiving mode of the LIN interface. The VCC voltage regulator works with 3.3V/5V output voltage. The watchdog needs a trigger signal from NTRIG to avoid resets at NRES. If NRES switches to low, the IC changes its state to Fail-Safe mode.

1.2.2 SILENT MODE

A falling edge at EN while TXD is high switches the IC into Silent mode. The TXD signal has to be logic high during the mode select window. The transmission path is disabled in Silent mode. The voltage regulator is active. The overall supply current from V_{Bat} is a combination of the $I_{VSsilent}$ of typically 47 µA plus the VCC regulator output current I_{VCC}.

FIGURE 1-2: SWITCHING TO SILENT MODE



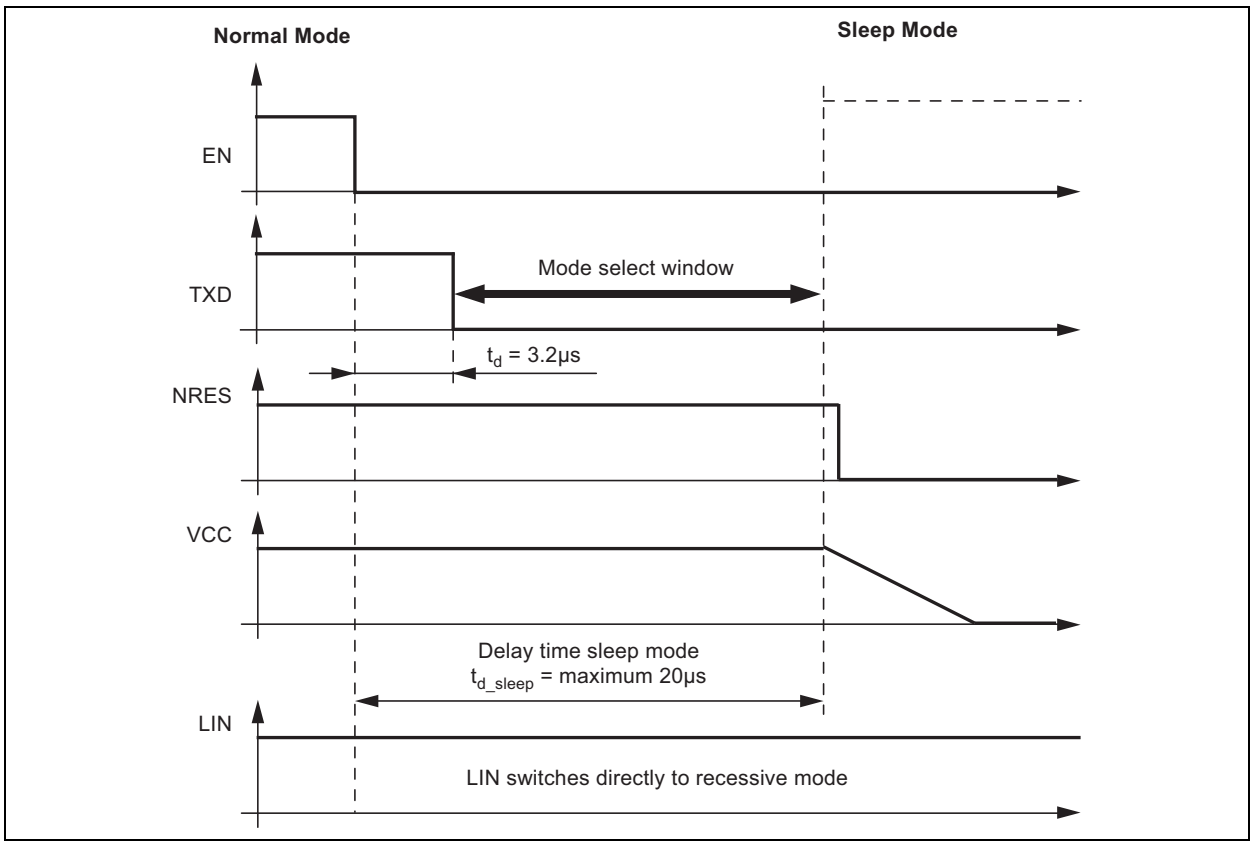
In Silent mode, the internal slave termination between the LIN pin and VS pin is disabled to minimize current consumption in case the LIN pin is short-circuited to GND. Only a weak pull-up current (typically 10 µA) is present between the LIN pin and the VS pin. Silent mode can be activated regardless of the current level on the LIN pin or WKin pin.

If an undervoltage condition or a watchdog failure occur, NRES is switched to low and the ATA663431/54 changes its state to Fail-Safe mode.

1.2.3 SLEEP MODE

A falling edge at EN while TXD is low switches the IC to Sleep mode. The TXD signal has to be logic low during the mode select window.

FIGURE 1-3: SWITCHING TO SLEEP MODE



In order to avoid any influence to the LIN pin while switching into Sleep mode, it is possible to switch the EN to low up to 3.2 µs earlier than the TXD. The best and easiest way is to generate two simultaneous falling edges at TXD and EN.

The transmission path is disabled in Sleep mode. Supply current from VBAT is typically $I_{VSsleep}$ = 10 µA. The VCC regulator is switched off; NRES and RXD are low. The internal slave termination between the LIN and VS pins is disabled to minimize current consumption in case the LIN pin is short-circuited to GND. Only a weak pull-up current (typically 10 µA) between the LIN pin and VS pin is present. Sleep mode can be activated independently from the current level on the LIN pin. A voltage of less than the LIN pre-wake detection V_{LINL} at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer.

If TXD is short-circuited to GND, it is possible to switch to Sleep mode via EN after $t > t_{dom}$.

1.2.4 FAIL-SAFE MODE

The device automatically switches to Fail-Safe mode at system power-up. The voltage regulator and the watchdog are switched on. The NRES output remains low for t_{res} = 4 ms and resets the microcontroller. LIN communication is switched off.

The IC stays in Fail-Safe mode until EN is switched to high. The IC then changes to Normal mode. A low at NRES switches the IC directly into Fail-Safe mode. During Fail-Safe mode the TXD pin is an output and together with the RXD output pin signals the fail-safe source.

If the device enters Fail-Safe mode coming from Normal mode (EN = 1) due to a VS undervoltage condition ($V_{VS} < V_{VS\_th\_N\_F\_down}$), it is possible to switch to Sleep mode or Silent mode through a falling edge at the EN input. The current consumption can be reduced further with this feature.

A wake-up event from either Silent mode or Sleep mode is indicated to the microcontroller using the two pins RXD and TXD.

A VS undervoltage condition is also signaled at these two pins. The coding is shown in **Table 1-2**.

A wake-up event switches the IC to Fail-Safe mode.

TABLE 1-2: SIGNALING IN FAIL-SAFE MODE

Fail-Safe sources	TXD	RXD
LIN wake-up (LIN pin)	Low	Low
Local wake-up (WKin pin or CL15 pin)	Low	High
$V_{VS\_th\_N\_F\_down}$ (battery) undervoltage detection (V_{VS} < 3.9V)	High	Low

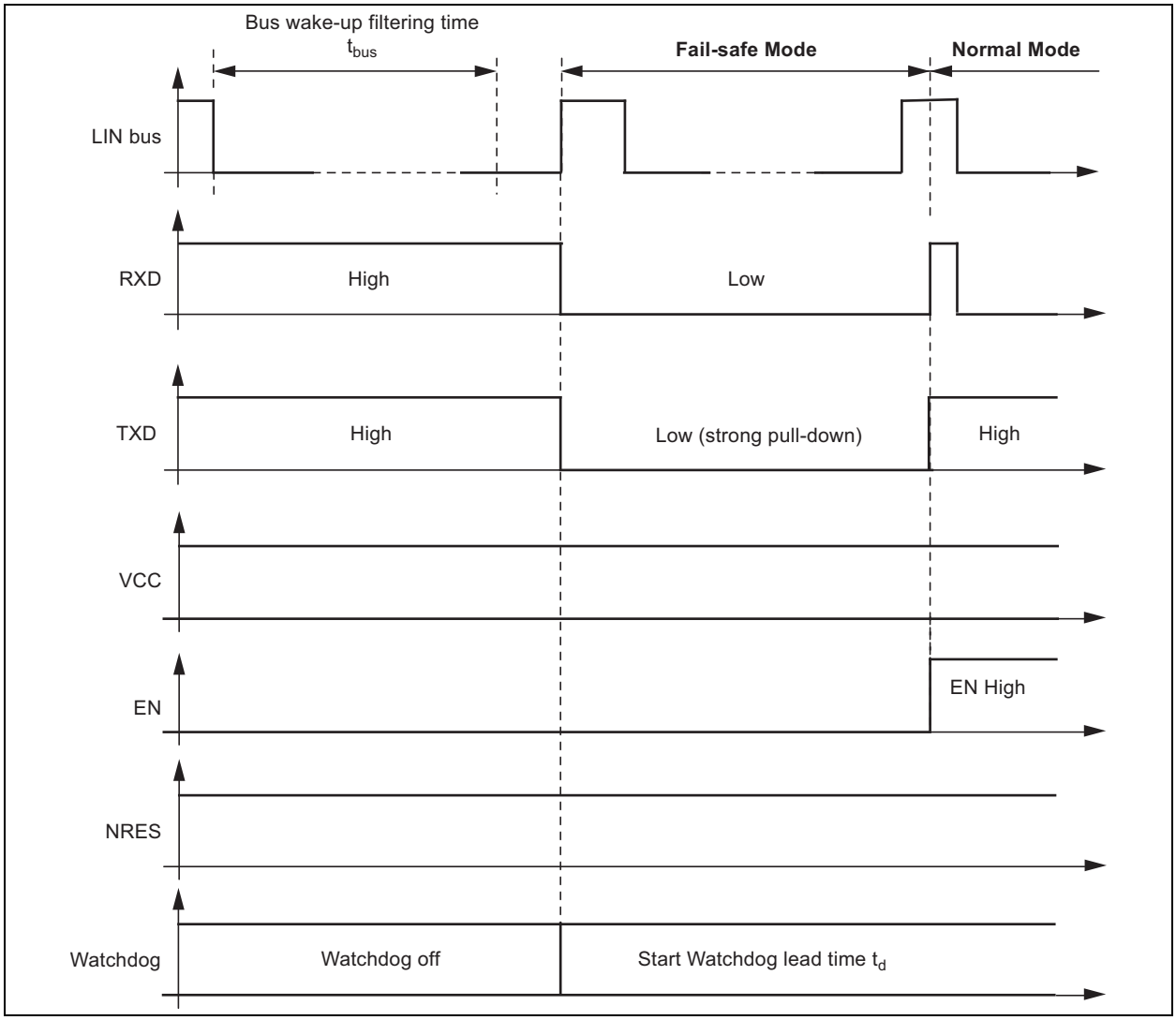
1.3 Wake-up Scenarios from Silent Mode or Sleep Mode

1.3.1 REMOTE WAKE-UP VIA LIN BUS

1.3.1.1 Remote Wake-up from Silent Mode

A remote wake-up from Silent mode is only possible if TXD is high. A voltage less than the LIN pre-wake detection V_{LINL} at the LIN pin activates the internal LIN receiver and starts the wake-up detection timer. A falling edge at the LIN pin followed by a dominant bus level maintained for a given time period (> t_{bus}) and the following rising edge at the LIN pin (see **Figure 1-4**) result in a remote wake-up request. The device switches from Silent mode to Fail-Safe mode, the VCC voltage regulator remains activated and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at the RXD and TXD pins (strong pull-down at TXD). EN high can be used to switch directly to Normal mode.

FIGURE 1-4: LIN WAKE-UP FROM SILENT MODE



1.3.1.2 Remote Wake-up from Sleep Mode

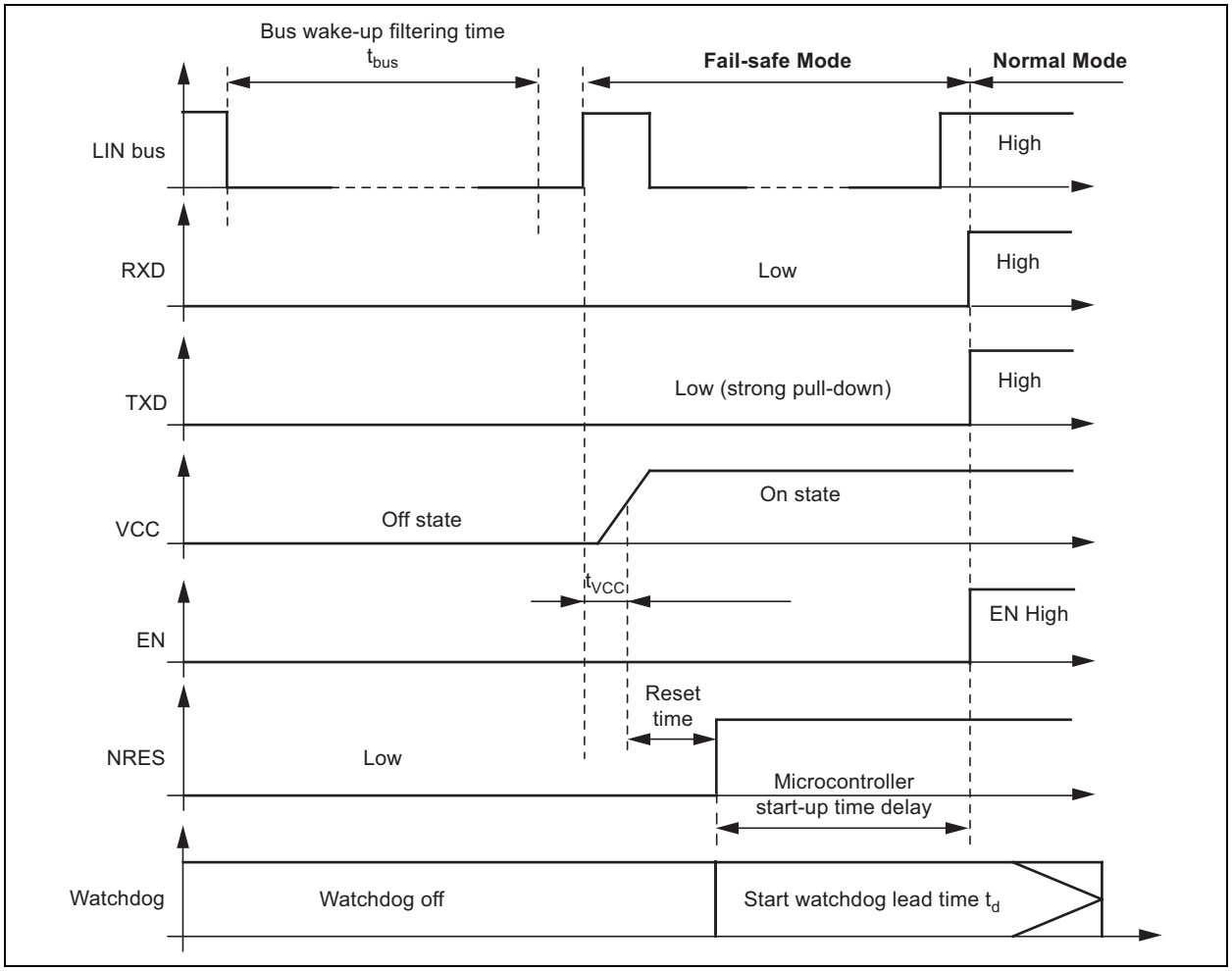
A voltage less than the LIN pre-wake detection V_{LINL}, at the LIN pin, activates the internal LIN receiver and starts the wake-up detection timer.

A falling edge at the LIN pin followed by a dominant bus level maintained for a given time period (> t_{bus}) and a subsequent rising edge at the LIN pin result in a remote wake-up request. The device switches from Sleep mode to Fail-Safe mode.

The VCC regulator is activated and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at RXD and TXD (strong pull-down at TXD).

EN high can be used to switch directly from Sleep/Silent mode to Fail-Safe mode. If EN is still high after VCC ramp-up and the undervoltage reset time, the IC switches to Normal mode.

FIGURE 1-5: LIN WAKE-UP FROM SLEEP MODE



1.3.2 LOCAL WAKE-UP VIA WKIN PIN

A falling edge at the WKin pin, followed by a low level maintained for a given time period (> t_{WKin}) results in a local wake-up request. The device switches to Fail-Safe mode. The internal slave termination resistor is switched on. The local wake-up request is indicated by a low level at the TXD pin to generate an interrupt for the microcontroller. When the WKin pin is low, it is possible to switch to Silent mode or Sleep mode via the EN pin. In this case, the wake-up signal has to be switched to high > 10 µs before the negative edge at WKin starts a new local wake-up request.

FIGURE 1-6: LOCAL WAKE-UP VIA WKIN PIN FROM SLEEP MODE

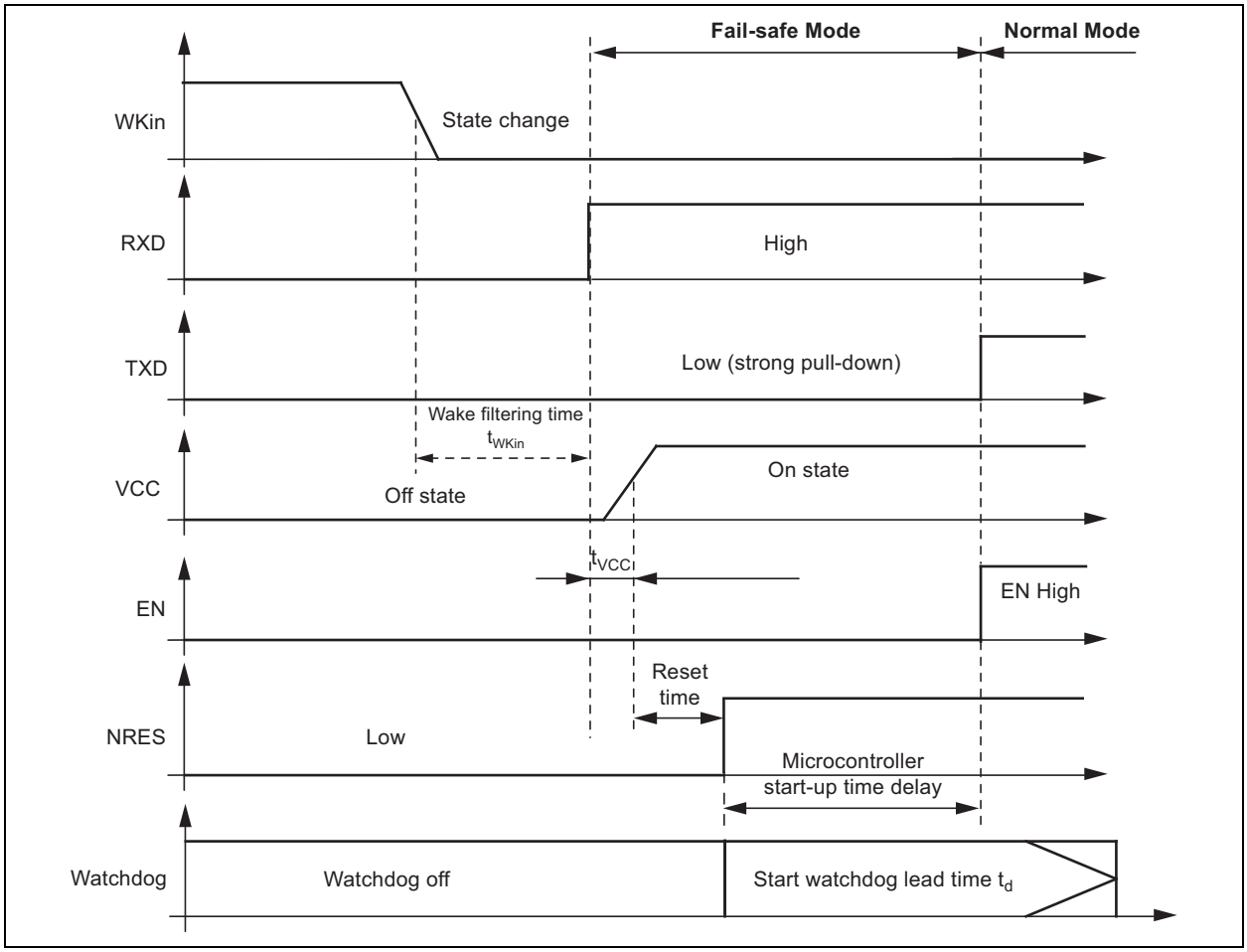
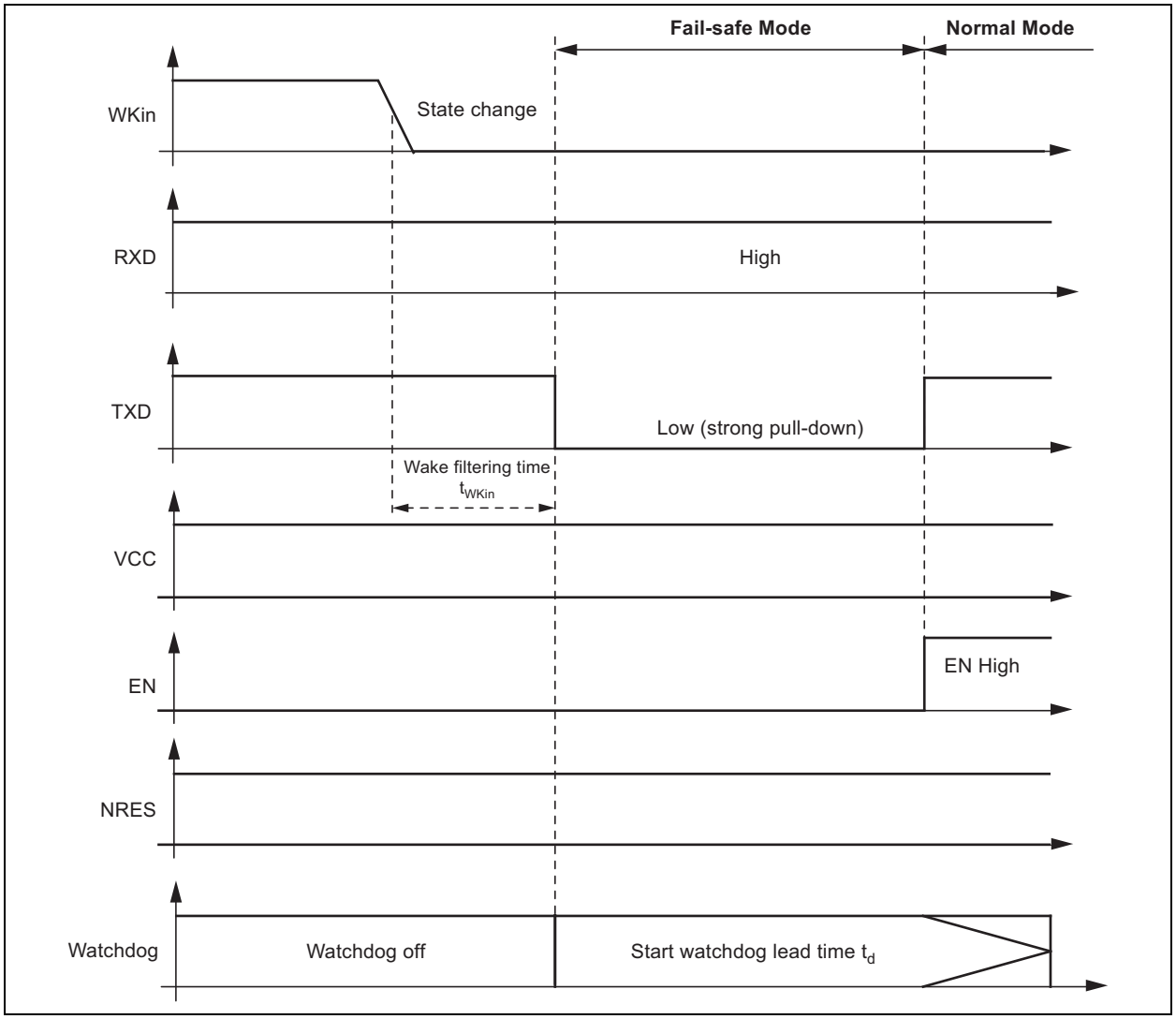


FIGURE 1-7: LOCAL WAKE-UP VIA WKIN PIN FROM SILENT MODE



1.3.3 LOCAL WAKE-UP VIA CL15

A voltage on pin CL15 above V_{CL15H} for at least t_{dbCL15} results in a local wake-up request. The device switches to Fail-Safe mode. The internal slave termination resistor is switched on. The local wake-up request is indicated by a low level at the TXD pin to generate an interrupt for the microcontroller. Even when the CL15 pin is high, it is possible to switch to Silent mode or Sleep mode via the EN pin. In this case, the wake-up signal at CL15 has to be switched to low > 10 µs before the rising edge at CL15 starts a new local wake-up request.

1.3.4 WAKE-UP SOURCE RECOGNITION

The device can distinguish between different wake-up sources (see **Table 1-3**). The wake-up source can be read on the TXD and RXD pin in Fail-Safe mode. These flags are immediately reset if the microcontroller sets the EN pin to high and the IC is in Normal mode.

TABLE 1-3: SIGNALING IN FAIL-SAFE MODE

Fail-Safe Sources	TXD	RXD
LIN wake-up (LIN pin)	Low	Low
Local wake-up (WKin pin or CL15 pin)	Low	High
$V_{VS\_th\_N\_F\_down}$ (battery) undervoltage detection (V_{VS} < 3.9V)	High	Low

1.4 Behavior under Low Supply Voltage Conditions

After the battery voltage has been connected to the application circuit, the voltage at the VS pin increases according to the block capacitor (see **Figure 1-12**). If V_{VS} is higher than the minimum VS operation threshold $V_{VS\_th\_U\_up}$ (typically 2.25V) the IC mode changes from Unpowered mode to Fail-Safe mode. As soon as V_{VS} exceeds the undervoltage threshold $V_{VS\_th\_F\_N\_up}$ (typically 4.6V) the LIN transceiver can be activated. The VCC output voltage reaches its nominal value after t_{VCC}. This parameter depends on the externally applied VCC capacitor and the load. The NRES output is low for the reset time delay t_{reset}. No mode change is possible during t_{reset}.

The behavior of VCC, NRES and VS is shown in the following graphs.

FIGURE 1-8: VCC AND NRES VERSUS VS (RAMP-UP) FOR ATA663431

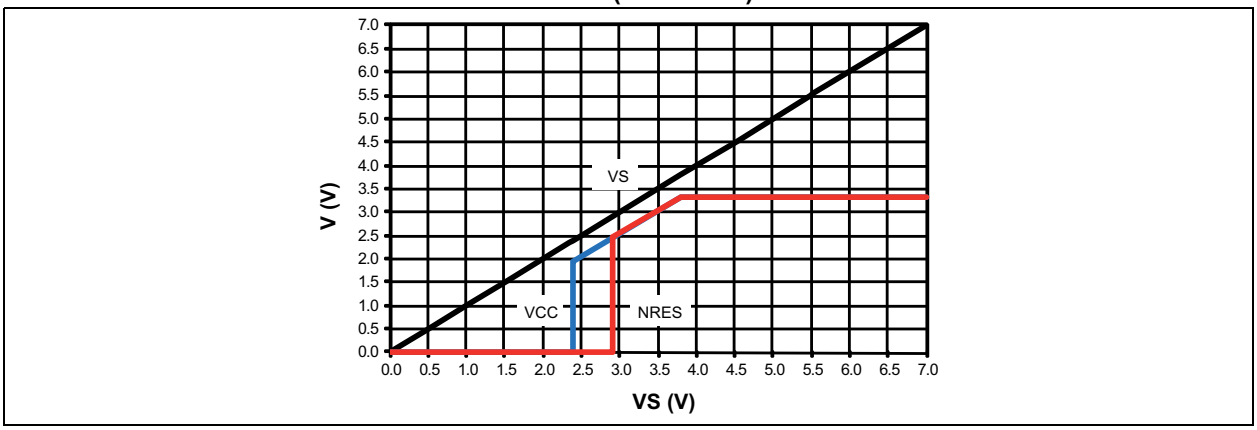


FIGURE 1-9: VCC AND NRES VERSUS VS (RAMP-DOWN) FOR ATA663431

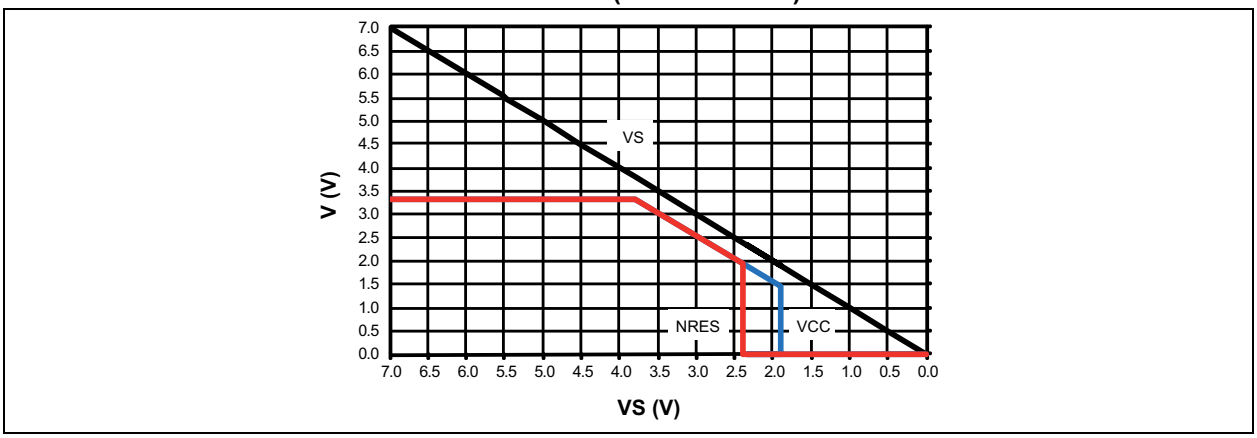


FIGURE 1-10: VCC AND NRES VERSUS VS (RAMP-UP) FOR ATA663454

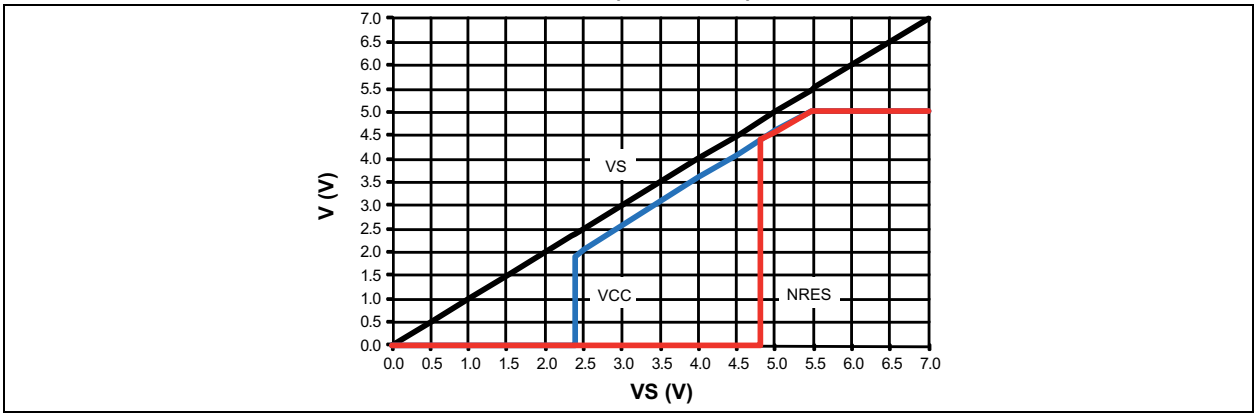
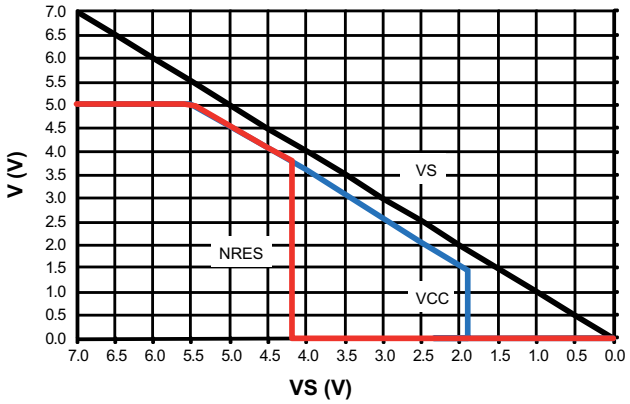


FIGURE 1-11: VCC AND NRES VERSUS VS (RAMP-DOWN) FOR ATA663454



Please note that the upper graphs are only valid if the V_{VS} ramp-up and ramp-down time is much slower than the VCC ramp-up time t_{VCC} and the NRES delay time t_{reset}.

If during Sleep mode the voltage level of V_{VS} drops below the undervoltage detection threshold $V_{VS\_th\_N\_F\_down}$ (typically 4.3V), the operating mode is not changed and no wake-up is possible. The IC switches to Unpowered mode only if the supply voltage on pin VS drops below the V_{VS} operation threshold $V_{VS\_th\_U\_down}$ (typically 2.05V).

If during Silent mode the VCC voltage drops below the VCC undervoltage threshold $V_{VCC\_th\_uv\_down}$, the IC switches into Fail-Safe mode. If the supply voltage on pin VS drops below the V_{VS} operation threshold $V_{VS\_th\_U\_down}$ (typically 2.05V), the IC switches to Unpowered mode.

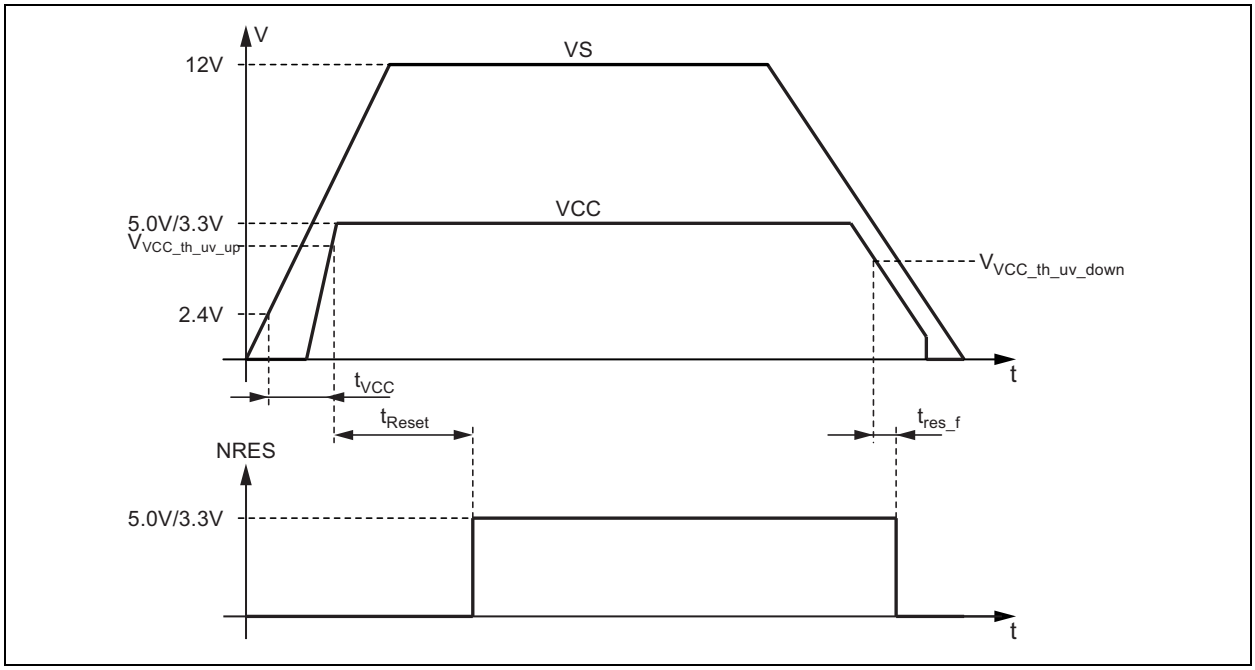
If during Normal mode the voltage level on pin VS drops below the V_{VS} undervoltage detection threshold $V_{VS\_th\_N\_F\_down}$ (typically 4.3V), the IC switches to Fail-Safe mode. This means the LIN transceiver is disabled in order to avoid malfunctions or false bus messages. The voltage regulator remains active.

- **For ATA663431**: In this undervoltage situation, it is possible to switch the device into Sleep mode or Silent mode through a falling edge at the EN input pin. This feature ensures that it is always possible to switch to these two current saving modes so that current consumption can be reduced even further.
  When the VCC voltage drops below the VCC undervoltage threshold $V_{VCC\_th\_uv\_down}$ (typically 2.6V) the IC switches into Fail-Safe mode.
- **For ATA663454**: Because of the VCC undervoltage condition in this situation, the IC is in Fail-Safe mode and can be switched into Sleep mode only.
  The IC switches into Unpowered mode only when the supply voltage V_{VS} drops below the operation threshold $V_{VS\_th\_U\_down}$ (typically 2.05V).

The current consumption of ATA663431/54 in Silent mode is always below 200 µA, even when the supply voltage V_{VS} is lower than the regulator's nominal output voltage V_{VCC}.

1.5 Voltage Regulator

FIGURE 1-12: VCC VOLTAGE REGULATOR: SUPPLY VOLTAGE RAMP-UP AND RAMP-DOWN



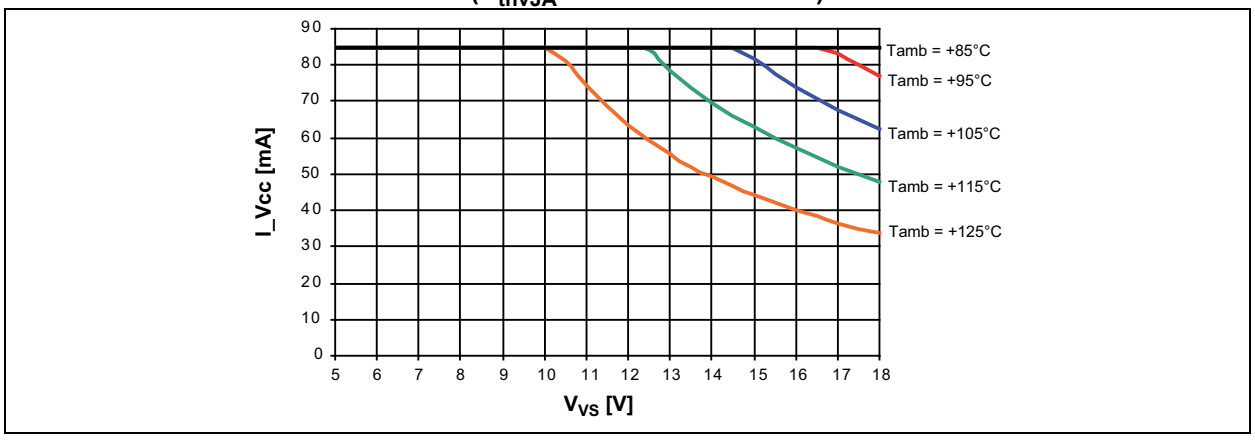
The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommended to use a MLC capacitor with a minimum capacitance of 1.8 µF together with a 100 nF ceramic capacitor. Depending on the application, the values of these capacitors can be modified by the customer.

During a short circuit at VCC, the output limits the output current to I_{VCClim}. Because of undervoltage, NRES switches to low and sends a reset to the microcontroller. If the chip temperature exceeds the value T_{VCCoff}, the VCC output switches off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again.

When the ATA663431/54 is being soldered onto the PCB, it is mandatory to connect the thermal pad with a wide GND plate on the printed board to achieve a good heat sink.

The main power dissipation of the IC is created from the VCC regulator output current I_{VCC}, which is needed for the application. **Figure 1-13** shows the safe operating area of the ATA663431/54 without considering any output current of the high-side output HSOUT.

FIGURE 1-13: POWER DISSIPATION: SAFE OPERATING AREA: REGULATOR'S OUTPUT CURRENT I_{VCC} VERSUS SUPPLY VOLTAGE V_{VS} AT DIFFERENT AMBIENT TEMPERATURES (R_{thvJA} = 45 K/W ASSUMED)



1.6 Watchdog

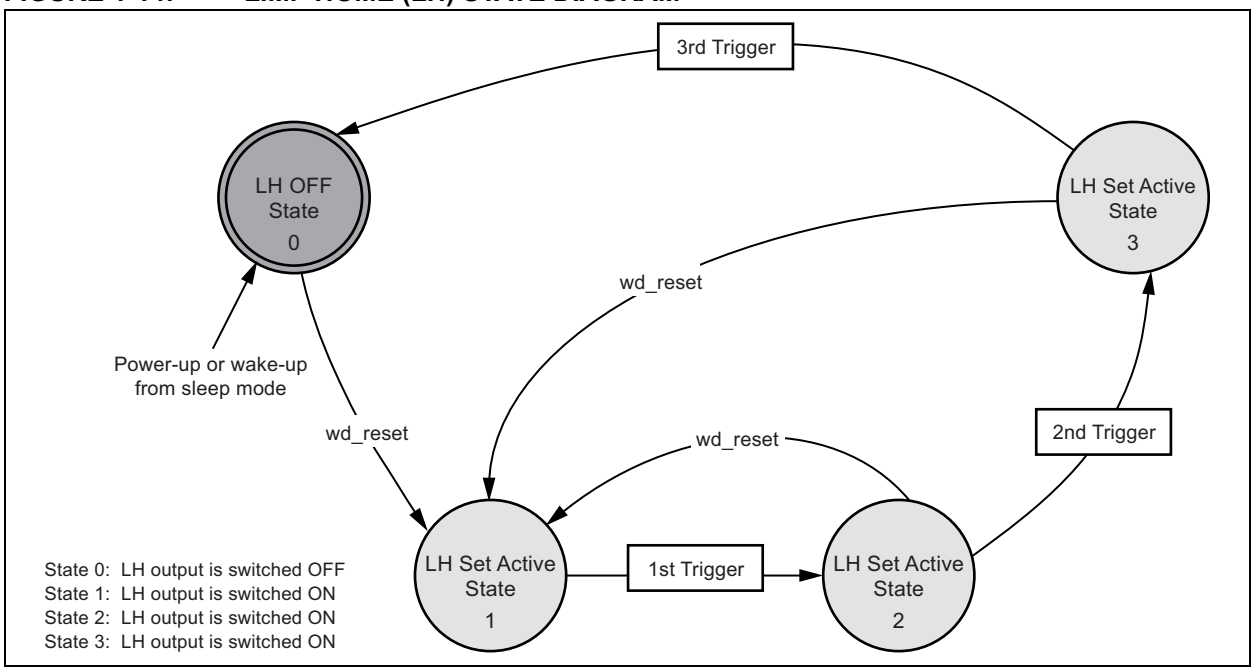
The watchdog anticipates a trigger signal from the microcontroller at the NTRIG (negative edge) input within a time window of t_{wd}. The trigger signal must exceed a minimum time of $t_{trigmin}$ > 200 ns. If a trigger signal is not received, a reset signal is generated at output NRES and the LH output transistor switches on. The timing basis of the watchdog is provided by the internal oscillator. Its time period t_{osc} is adjustable via the external resistor R_{WDOSC} (34 kΩ to 120 kΩ). During Silent mode or Sleep mode the watchdog is switched off to reduce current consumption. The minimum time for the first watchdog pulse is required after the undervoltage reset at NRES disappears. It is defined as lead time t_d. After wake-up from Sleep mode, the lead time t_d starts with the rising edge at the NRES output. After a wake-up from Silent mode, the lead time t_d starts with the falling edge at the TXD pin.

The Limp Home output LH is a high voltage NMOS open drain structure which is signaling watchdog failures. It works independently of the VCC voltage. So it is possible to switch on some external devices in the case of a watchdog failure independent from the microcontroller and the VCC voltage. During power up or after a wake-up from Sleep mode the LH output is switched off. If a watchdog reset occurs, the LH output transistor switches on immediately, and it switches off only after three correct consecutive watchdog trigger pulses have been occurred at the NTRIG pin.

As the watchdog is only working in Normal mode and Fail-Safe mode, the state of the LH output transistor can change only in these two modes. In Silent mode, the LH output remains in the same state as it was before switching into Silent mode. When the watchdog is disabled via a high level at the mode pin or during Sleep or Unpowered mode, the LH output is also disabled.

The behavior of the LH output when the watchdog is active during Fail-Safe mode and Normal mode is depicted in **Figure 1-14**.

FIGURE 1-14: LIMP HOME (LH) STATE DIAGRAM



In Sleep mode and Unpowered mode, the watchdog and therefore the LH output are deactivated. In Silent mode the LH output remains in the same state as it was before switching into Silent mode.

1.6.1 TYPICAL TIMING SEQUENCE WITH R_{WDOSC} = 51 KΩ

The trigger signal t_{wd} is adjustable between 20 ms and 64 ms using the external resistor R_{WDOSC}.

For example, with an external resistor of R_{WDOSC} = 51 kΩ ± 1%, the typical parameters of the watchdog are shown in **Equation 1-1**.

EQUATION 1-1:

$$t_{osc} = (0.405 \times R_{WDOSC} - 0.0004 \times (R_{WDOSC})^2) \times 2$$

$$t_{osc} = 39.3\ \mu s \ \ due\ to\ 51\ k\Omega$$

$$t_d = 3984 \times 39.2\ \mu s = 154.8\ ms$$

$$t_1 = 527 \times 39.2\ \mu s = 20.6\ ms$$

$$t_2 = 553 \times 39.3\ \mu s = 21.6\ ms$$

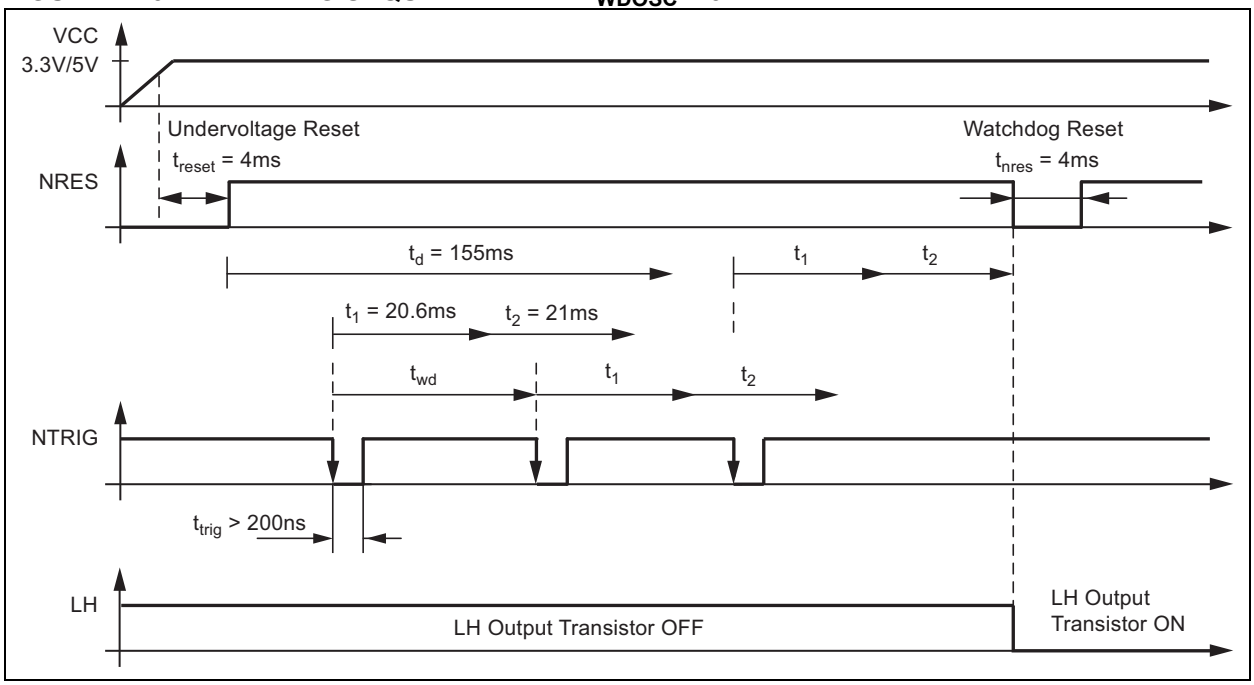
Where:

R_{WDOSC} in kΩ; t_{osc} in µs

t_{nres} = constant = 4 ms

After ramping up the battery voltage, the VCC regulator is switched on. The reset output NRES stays low for the time t_{reset} (typically 4 ms), then it switches to high and the watchdog waits for the trigger sequence from the microcontroller. During power up or after a wake-up from Sleep mode, the LH output is switched off. If a watchdog reset occurs, the LH output transistor switches on immediately and switches off only after three correct consecutive watchdog trigger pulses have occurred at the NTRIG pin. The lead time, t_d follows the reset and is t_d = 155 ms. In this time, the first watchdog pulse from the microcontroller is required. If the trigger pulse NTRIG occurs during this time, the time t_1 starts immediately. If no trigger signal occurs during the time t_d, a watchdog reset with t_{NRES} = 4 ms will reset the microcontroller after t_d = 155 ms and the LH output transistor switches on. The times t_1 and t_2 have a fixed relationship. A trigger signal from the microcontroller is anticipated within the time frame of t_2 = 21.6 ms. To avoid false triggering from glitches, the trigger pulse must be longer than $t_{trigmin}$ > 200 ns. This slope serves to restart the watchdog sequence. If the triggering signal fails in this open window t_2, the NRES output is drawn to ground as well as the LH output. A trigger signal during the closed window t_1 immediately switches NRES and LH to low.

FIGURE 1-15: TIMING SEQUENCE WITH R_{WDOSC} = 51 kΩ



1.6.2 WORST-CASE CALCULATION WITH R_{WDOSC} = 51 KΩ

The internal oscillator has a tolerance of 20%. This means that t_1 and t_2 can also vary by 20%. The worst-case calculation for the watchdog period t_{wd} is calculated in **Equation 1-2**. The ideal watchdog time t_{wd} is between the maximum t_1 and the minimum t_1 plus the minimum t_2.

EQUATION 1-2:

$$t_{1,min} = 0.8 \times t_1 = 16.5\ ms$$
$$t_{1,max} = 1.2 \times t_1 = 24.8\ ms$$
$$t_{2,min} = 0.8 \times t_2 = 17.3\ ms$$
$$t_{2,max} = 1.2 \times t_2 = 26\ ms$$
$$t_{wdmax} = t_{1,min} + t_{2,min} = 16.5\ ms + 17.3\ ms = 33.8\ ms$$
$$t_{wdmin} = t_{1,max} = 24.8\ ms$$

Where:

t_{wd} = 29.3 ms ± 4.5 ms (± 15%)

A microcontroller with an oscillator tolerance of ± 15% is sufficient to supply the trigger inputs correctly.

TABLE 1-4: TYPICAL WATCHDOG TIMINGS

R_{WDOSC} kΩ	Oscillator Period t_{osc}/µs	Lead Time t_d/ms	Closed Window t_1/ms	Open Window t_2/ms	Trigger Period from Microcontroller t_{wd}/ms	Reset Time t_{nres}/ms
34	13.3 x 2	105	14.0	14.7	19.9	4
51	19.61 x 2	154.8	20.64	21.67	29.32	4
91	3.54 x 2	264.80	37.06	37.06	50.14	4
120	42,84 x 2	338.22	45.11	47.34	64.05	4

If the WDOSC pin has a short circuit to GND or the external resistor at the WDOSC pin is disconnected, the watchdog runs with an internal oscillator and guarantees a reset and activation of the LH output.

1.7 Pin Descriptions

The descriptions of the pins are listed in **Table 1-5**.

TABLE 1-5: PIN DESCRIPTION

Pin Number	Symbol	Function
1	RXD	Receive Data Output
2	EN	Enable Normal Mode if the Input is High
3	NRES	VCC Undervoltage Output, Open-Drain, Low at Reset
4	TXD	Transmit Data Input
5	NTRIG	Low-Level Watchdog Trigger Input from Microcontroller; if not needed, connect to VCC
6	MODE	Control Input from Watchdog. Low: Watchdog is On. High: Watchdog is Off
7	WDOSC	Connection for External Resistor to set the Watchdog Frequency
8	HSin	High-Side Input Control
9	HSout	High-Side Switch Output
10	LH	Failure Output of the Watchdog (Limp Home), Open-Drain
11	CL15	Ignition Detection (Edge Sensitive); if not needed, connect to GND
12	WKin	High Voltage Input for Local Wake-Up Request; if not needed, connect directly to VS
13	GND	Ground
14	LIN	LIN Bus Line Input/Output
15	VS	Supply Voltage
16	VCC	Output Voltage Regulator 3.3V/5V/85 mA
EP	EP	Exposed Thermal Pad, internally connected to GND

1.7.1 BUS DATA OUTPUT PIN (RXD)

In Normal mode this pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is indicated by a high level at RXD; LIN low (dominant state) is indicated by a low level at RXD. The output is a push-pull stage switching between VCC and GND. The AC characteristics are measured with an external load capacitor of 20 pF.

In Silent mode the RXD output switches to high.

1.7.2 ENABLE INPUT PIN (EN)

The enable input pin controls the operating mode of the device. If EN is high, the circuit is in Normal mode, with the TXD to LIN and the LIN to RXD transmission paths both active. The VCC voltage regulator operates with 3.3V/5V/85 mA output capability.

If EN is switched to low while TXD is still high, the device is forced to Silent mode. No data transmission is possible and the current consumption is reduced to $I_{VSsilent}$ typ. 47 µA. The VCC regulator maintains full functionality.

If EN is switched to low while TXD is low, the device is forced into Sleep mode. This disables data transmission and the voltage regulator is switched off.

Pin EN provides a pull-down resistor to force the transceiver into Recessive mode if EN is disconnected.

1.7.3 UNDERVOLTAGE RESET OUTPUT PIN (NRES)

If the VCC voltage falls below the undervoltage detection threshold $V_{VCC\_th\_uv\_down}$, NRES switches to low after t_{res_f}. The NRES stays low even if V_{VCC} = 0V because it is internally driven from the VS voltage. If VS voltage ramps down, NRES stays low until V_{VS} < 1.5V and then becomes high-impedant.

The undervoltage delay implemented keeps NRES low for t_{Reset} = 4 ms after V_{VCC} reaches its nominal value.

1.7.4 BUS DATA INPUT/OUTPUT (TXD)

In Normal mode the TXD pin is the microcontroller interface for controlling the state of the LIN output. TXD must be pulled to ground in order to drive the LIN bus low. If TXD is high or unconnected (internal pull-up resistor), the LIN output transistor is turned off and the bus is in recessive state. If the TXD pin stays at GND level while switching into Normal mode, it must be pulled to high longer than 10 µs before the LIN driver can be activated. This feature prevents the bus line from being driven unintentionally to the dominant state after Normal mode has been activated (also in the case of a short circuit at TXD to GND). If TXD is short-circuited to GND, it is possible to switch to Sleep mode via the EN pin after t > t_{dom}.

In Fail-Safe mode this pin is used as an output and signals the fail-safe source.

An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{dom} > 20 ms the LIN bus driver is switched to the recessive state. Nevertheless, when switching to Sleep mode, the actual level at the TXD pin is relevant.

To reactivate the LIN bus driver, TXD needs to be set high for at least t_{DTOrel} (min 10 µs).

1.7.5 NTRIG INPUT PIN

The NTRIG input pin is the trigger input for the window watchdog. A pull-up resistor is implemented. A falling edge triggers the watchdog. The trigger signal (low) must exceed a minimum time of $t_{trigmin}$ to generate a watchdog trigger and avoid false triggers caused by transients.

1.7.6 MODE INPUT PIN (MODE)

Connect the MODE pin directly or via an external resistor to GND for normal watchdog operation. To debug the software of the connected microcontroller, connect the MODE pin to VCC and the watchdog is switched off. For fail-safe reasons, the MODE pin has a self-holding function, pulling the input to ground (i.e., watchdog enabled) in case of an open connection.

Note:	If you do not use the watchdog, connect the MODE pin directly to VCC.

1.7.7 WDOSC OUTPUT PIN

The WDOSC output pin provides a typical voltage of 1.23V intended to supply an external resistor with values between 34 kΩ and 120 kΩ. The value of the resistor adjusts the watchdog oscillator frequency to provide a certain range of time windows.

If the watchdog is disabled, the WDOSC output voltage is switched off and the pin can either be tied to VCC or left open.

1.7.8 HIGH-SIDE SWITCH PINS (HSOUT, HSIN)

This high-side switch is designed for low-power loads such as LEDs, sensors or a voltage divider for measuring the supply voltage. It is functional in all operating modes of the chip except for Sleep mode. Its structure is connected to the VS supply pin. This pin is short-circuit protected and also protected against overheating, whereas the protective shutdown is debounced and latched. In other words, after a protective shutdown of the output switch, the control line HSin has to go to low level first before the output can be restarted again.

The high-side switch is controlled via the low-voltage input pin HSin. If the input is high, the output is switched on. For fail-safe reasons, the HSin input is equipped with a pull-down resistor to GND. This keeps the high-side switch off in case of a missing connection from the controller.

Please note that in case of a disconnected system ground, the module can be supplied via the connected load on the high-side output and an internal ESD structure. This is the case if the load has a different ground connection than the PCB. See also **Section 2.1 "Absolute Maximum Ratings†"** for current limits in such cases.

1.7.9 LIMP HOME WATCHDOG FAILURE OUTPUT (LH)

The LH output pin indicates a failure of the watchdog. It is realized as a high-voltage open drain NMOS structure. During power up or after a wake-up from Sleep mode the LH output is switched off. As the watchdog is only working in Normal and Fail-Safe mode, the state of the LH output transistor can change only in these two modes. In Silent mode the LH output remains in the same state as it was before switching into Silent mode.

If a watchdog reset occurs, the LH output transistor switches on immediately, and it switches off only after three correct consecutive watchdog trigger pulses have been occurred at the NTRIG pin.

1.7.10 CL15 PIN

The CL15 pin is a high-voltage input that can be used to wake up the device from Sleep mode or Silent mode. It is an edge sensitive pin (low to-high transition). Thus, even if the CL15 pin is at high voltage ($V_{CL15} > V_{CL15H}$), it is possible to switch the IC into Sleep mode or Silent mode. It is usually connected to the ignition for generating a local wake-up in the application if the ignition is switched on. The CL15 pin should be tied directly to ground if not needed. A debounce timer with a value t_{dbCL15} of typically 100 µs is implemented. To protect this pin against transients, a serial resistor with 10 kΩ and a ceramic capacitor with 47 nF are recommended. With this RC combination you can increase the CL15 wake-up time.

1.7.11 WAKE INPUT PIN (WKIN)

The WKin pin is a high-voltage input used for waking up the device from Sleep mode or Silent mode. It is usually connected to an external switch in the application to generate a local wake-up. A pull-up current source with typically 10 µA is implemented. The voltage threshold for a wake-up signal is typically 2V below V_{VS}. If the WKin pin is not needed in the application, it can be connected directly to the VS pin.

1.7.12 GROUND PIN (GND)

The IC does not affect the LIN bus in the event of GND disconnection. It can handle ground shifts of up to 11.5% with respect to V_{VS}.

1.7.13 BUS PIN (LIN)

A low-side driver is implemented with internal current limitation and thermal shutdown as well as an internal pull-up resistor in compliance with LIN specification 2.x. The voltage range is from -27V to +40V. This pin exhibits no reverse current from the LIN bus to VS, even in the event of a GND shift or supply disconnection. The LIN receiver thresholds comply with the LIN protocol specification.

The fall time (transition from recessive to dominant state) and the rise time (transition from dominant to recessive state) are slope-controlled.

During a short-circuit at the LIN pin to VBAT the output limits the output current to I_{BUS_LIM}. Due to the power dissipation, the chip temperature exceeds T_{LINoff} and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys} switches the output on again. RXD stays on high because LIN is high. During LIN overtemperature switch-off, the VCC regulator works independently.

During a short circuit from LIN to GND the IC can be switched into Sleep or Silent mode and even in this case the current consumption is lower than 100 µA in Sleep mode and lower than 120 µA in Silent mode. If the short circuit disappears, the IC starts with a remote wake-up.

The reverse current is < 2 µA at the LIN pin during loss of V_{Bat}. This is optimal behavior for bus systems where some slave nodes are supplied from battery or ignition.

1.7.14 SUPPLY PIN (VS)

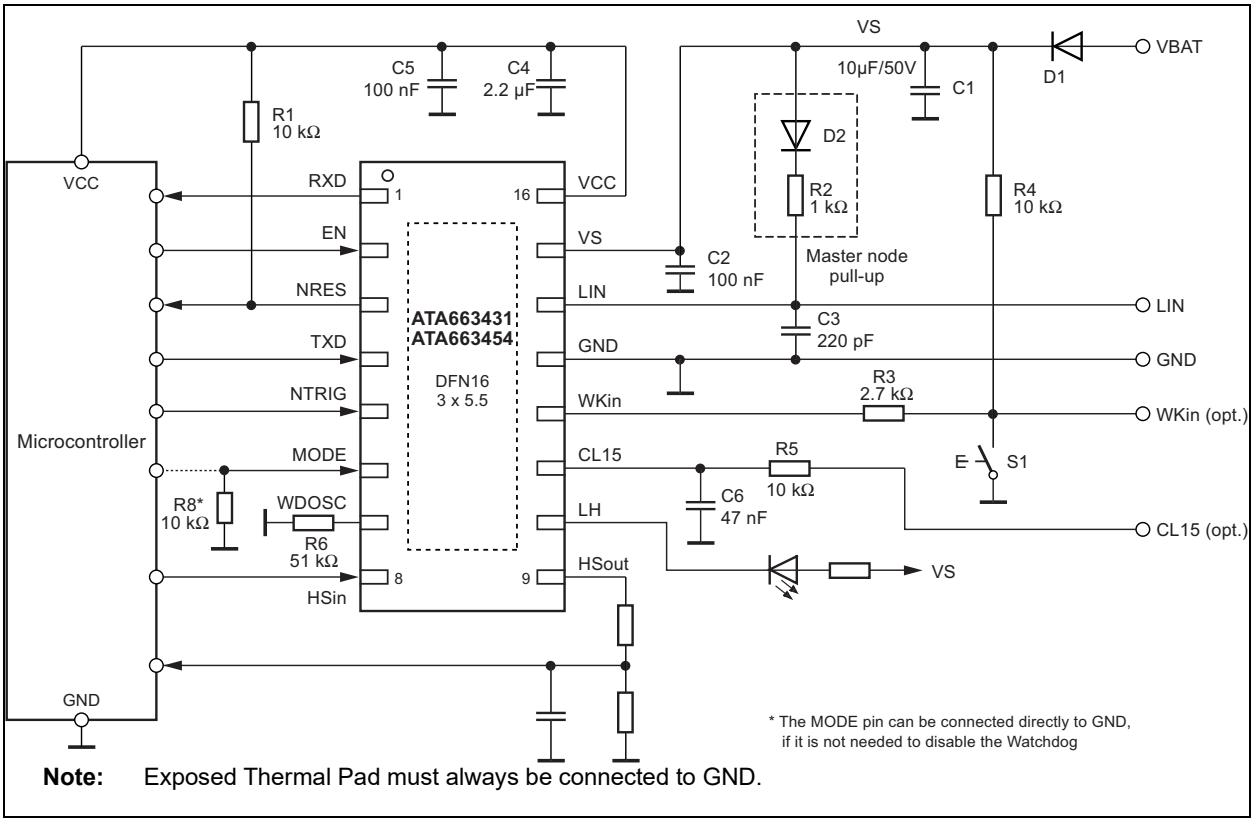
LIN operating voltage is V_{VS} = 5V to 28V. In order to avoid false bus messages an undervoltage detection is implemented to disable transmission if V_{VS} falls below $V_{VS\_th\_N\_F\_down}$. After switching on V_{VS}, the IC starts in Fail-Safe mode and the voltage regulator is switched on.

The supply current in Sleep mode is typically 10 µA and 47 µA in Silent mode.

1.7.15 VOLTAGE REGULATOR OUTPUT PIN (VCC)

The internal 3.3V/5V voltage regulator is capable of driving loads up to 85 mA, supplying the microcontroller and other ICs on the PCB, and is protected against overload by means of current limitation and overtemperature shutdown. Furthermore, the output voltage is monitored and causes a reset signal at the NRES output pin if it drops below a defined threshold $V_{VCC\_th\_uv\_down}$.

TYPICAL APPLICATION CIRCUIT



Note: Exposed Thermal Pad must always be connected to GND.

2.0 ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings†

Supply Voltage VS Pin

DC Voltage, V_{VS} ..... -0.3V to +40V

T_a = 25°C, Pulse Time ≤ 500 ms, I_{VCC} ≤ 85 mA, V_{VS} ..... +40V

T_a = 25°C, Pulse Time ≤ 2 min, I_{VCC} ≤ 85 mA, V_{VS} ..... +28V

Logic Pins

Logic Pin Voltage Levels (TXD, RXD, EN, HSin, MODE, WDOSC, NRES, NTRIG), V_{LOGIC} ..... -0.3V to +5.5V

Logic Pin Output DC Currents, I_{LOGIC} ..... -5 mA to +5 mA

LIN Pin

DC Voltage, V_{LIN} ..... -27V to +40V

Pulse Time ≤ 500 ms, V_{LIN} ..... +43.5V

VCC Pin

DC Voltage, V_{VCC} ..... -0.3V to +5.5V

DC Input Current, I_{VCC} ..... +200 mA

Logic Level Pins Injection Currents

DC Currents, I_{LOGIC} ..... -5 mA to 0.1 mA

Pulse Time ≤ 2 min, I_{LOGIC} ..... -5 mA to +5 mA

LH Pin

DC Voltage, V_{LH} ..... -0.3V to V_{VS} + 0.3V

HSout Pin

DC Voltage, V_{HSout} ..... -0.3V to V_{VS} + 0.3V

DC Output Current, I_{HSout} ..... -50 mA

DC Current Injection Levels, V_{HSout} < 0V and V_{HSout} > V_{VS}, I_{HSout} ..... -20 mA to +10 mA

CL15 Pin

DC Voltage, V_{CL15} ..... -0.3V to +40V

WKin Pin

DC Voltage, V_{WKin} ..... -0.3V to +40V

Transient Voltage According to ISO 7637 (coupling 1 nF), (with 2.7K Serial Resistor), V_{WKin} ..... -150V to +100V

ESD According to IBEE LIN EMC; Test Specification 1.0 Following IEC 61000-4-2

Pins VS, WKin, CL15 and LIN to GND (CL15 and WKin with External Circuitry acc. to Applications Diagram) ..... ±6 KV

ESD According to ISO 10605, with 330 pF/330Ω

Pin HSout (100Ω Series Resistor, 22 nF to GND) to GND ..... ±6 KV

ESD (HBM following STM 5.1 with 1.5 kΩ/100 pF)

Pin VS, LIN, WKin, HSout, CL15 to GND ..... ±6 KV

Component Level ESD (HBM according to ANSI/ESD STM5.1) JESD22-A114 AEC-Q100 (002) ..... ±3 KV

CDM ESD STM 5.3.1 ..... ±750V

ESD Machine Model AEC-Q100-RevF(003) ..... ±100V

Virtual Junction Temperature, T_{vJ} ..... -40°C to +150°C

Storage Temperature, T_{stg} ..... -55°C to +150°C

† NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise specified all values are specified for 5V < V_{VS} < 28V, -40°C < T_{vJ} < +150°C and refer to the GND pin.

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
1	**VS Pin**						
1.1	Nominal DC Voltage Range	V_{VS}	5	13.5	28	V	
1.2	Supply Current in Sleep Mode	$I_{VSsleep}$	5	10	15	µA	Sleep mode V_{LIN} > V_{VS} - 0.5V V_{VS} < 14V, T = +27°C (**Note 1**)
		$I_{VSsleep}$	3	11	18	µA	Sleep mode V_{LIN} > V_{VS} - 0.5V V_{VS} < 14V
		$I_{VSsleep\_short}$	20	50	100	µA	Sleep mode, V_{LIN} = 0V Bus shorted to GND V_{VS} < 14V
1.3	Supply Current in Silent Mode	$I_{VSsilent}$	30	47	58	µA	Bus recessive 5.5V < V_{VS} < 14V, HS-driver off without load at VCC T = +27°C (**Note 1**)
		$I_{VSsilent}$	30	50	64	µA	Bus recessive 5.5V < V_{VS} < 14V, HS-driver off without load at VCC
		$I_{VSsilent}$	30	150	190	µA	Bus recessive V_{VS} < 5.5V, V_{VCC} > $V_{VCC\_th\_uv}$ HS-driver off without load at VCC
		$I_{VSsilent\_short}$	50	90	130	µA	Silent mode 5.5V < V_{VS} < 14V, HS-driver off without load at VCC Bus shorted to GND
1.4	Supply Current in Normal Mode	I_{VSrec}	300	400	500	µA	Bus recessive V_{VS} < 14V, HS-driver off without load at VCC, watchdog on, 51 kΩ at WDOSC
		I_{VSrec}	150	250	350	µA	Bus recessive V_{VS} < 14V, HS-driver off without load at VCC, watchdog off (V_{MODE} = V_{VCC})
1.5	Supply Current in Normal Mode	I_{VSdom}	600	900	1150	µA	Bus dominant (internal LIN pull-up resistor active) V_{VS} < 14V, HS-driver off without load at VCC, watchdog on, 51 kΩ at WDOSC
		I_{VSdom}	500	750	1000	µA	Bus dominant (internal LIN pull-up resistor active) V_{VS} < 14V, HS-driver off without load at VCC, watchdog off (V_{MODE} = V_{VCC})

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified all values are specified for 5V < V_{VS} < 28V, -40°C < T_{VJ} < +150°C and refer to the GND pin.

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
1.6	Supply Current in Fail-Safe Mode	I_{VSfail}	100	200	300	µA	Bus recessive 5.5V < V_{VS} < 14V, HS-driver off without load at VCC, watchdog on, 51 kΩ at WDOSC
		I_{VSfail}	40	70	100	µA	Bus recessive 5.5V < V_{VS} < 14V, HS-driver off without load at VCC, watchdog off (V_{MODE} = V_{VCC})
		I_{VSfail}	150	280	320	µA	Bus recessive 2V < V_{VS} < 5.5V, HS-driver off without load at VCC, watchdog on, 51 kΩ at WDOSC
		I_{VSfail}	50	150	200	µA	Bus recessive 2V < V_{VS} < 5.5V, HS-driver off without load at VCC watchdog off (V_{MODE} = V_{VCC})
1.7	VS Undervoltage Threshold (switching from Normal mode to Fail-Safe mode)	$V_{VS\_th\_N\_F\_down}$	3.9	4.3	4.7	V	Decreasing supply voltage
		$V_{VS\_th\_F\_N\_up}$	4.1	4.6	4.9	V	Increasing supply voltage
1.8	VS Undervoltage Hysteresis	$V_{VS\_hys\_F\_N}$	0.1	0.25	0.4	V	
1.9	VS Operation Threshold (switching to Unpowered mode)	$V_{VS\_th\_U\_down}$	1.9	2.05	2.3	V	Switch to Unpowered mode
		$V_{VS\_th\_U\_up}$	2.0	2.25	2.4	V	Switch from Unpowered mode to Fail-Safe mode
1.10	VS Undervoltage Hysteresis	$V_{VS\_hys\_U}$	0.1	0.2	0.3	V	
2	**RXD Output Pin**						
2.1	Low-Level Output Sink Capability	V_{RXDL}	—	0.2	0.4	V	Normal mode, V_{LIN} = 0V, I_{RXD} = 2 mA
2.2	High-Level Output Source Capability	V_{RXDH}	V_{VCC} - 0.4V	V_{VCC} - 0.2V	—	V	Normal mode V_{LIN} = V_{VS}, I_{RXD} = -2 mA
3	**TXD Input/Output Pin**						
3.1	Low-Level Voltage Input	V_{TXDL}	-0.3	—	+0.8	V	
3.2	High-Level Voltage Input	V_{TXDH}	2	—	V_{VCC} + 0.3V	V	
3.3	Pull-Up Resistor	R_{TXD}	40	70	100	kΩ	V_{TXD} = 0V
3.4	High-Level Leakage Current	I_{TXD}	-3	—	+3	µA	V_{TXD} = V_{VCC}
3.5	Low-Level Output Sink Current at Wake-Up Request	I_{TXD}	2	2.5	8	mA	Fail-Safe mode V_{LIN} = V_{VS} V_{WKin} = 0V V_{TXD} = 0.4V

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified all values are specified for 5V < V_{VS} < 28V, -40°C < T_{vJ} < +150°C and refer to the GND pin.

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
4	**EN Input Pin**						
4.1	Low-Level Voltage Input	V_{ENL}	-0.3	—	+0.8	V	
4.2	High-Level Voltage Input	V_{ENH}	2	—	V_{VCC} + 0.3V	V	
4.3	Pull-Down Resistor	R_{EN}	50	125	200	kΩ	$V_{EN} = V_{VCC}$
4.4	Low-Level Input Current	I_{EN}	-3	—	+3	µA	V_{EN} = 0V
5	**NRES Open Drain Output Pin**						
5.1	Low-Level Output Voltage	V_{NRESL}	—	0.2	0.4	V	$V_{VS} \geq 5.5V$ I_{NRES} = 2 mA
5.2	Undervoltage Reset Time	t_{Reset}	2	4	6	ms	$V_{VS} \geq 5.5V$ C_{NRES} = 20 pF
5.3	Reset Debounce Time for Falling Edge	t_{res_f}	0.5	—	10	µs	$V_{VS} \geq 5.5V$ C_{NRES} = 20 pF
5.4	Switch-Off Leakage Current	I_{NRES_L}	-3	—	+3	µA	V_{NRES} = 5.5V
6	**VCC Voltage Regulator ATA663431**						
6.1	Output Voltage V_{VCC}	V_{VCCnor}	3.234	—	3.366	V	4V < V_{VS} < 18V (0 mA to 50 mA)
		V_{VCCnor}	3.234	—	3.366	V	4.5V < V_{VS} < 18V (0 mA to 85 mA) (**Note 2**)
6.2	Output Voltage V_{VCC} at Low V_{VS}	V_{VCClow}	V_{VS} - V_D	—	3.366	V	3V < V_{VS} < 4V
6.3	Regulator Drop Voltage	V_{D1}	—	200	250	mV	V_{VS} > 3V, I_{VCC} = -15 mA
6.4	Regulator Drop Voltage	V_{D2}	—	300	500	mV	V_{VS} > 3V, I_{VCC} = -50 mA
6.5	Line Regulation Maximum	VCC_{line}	—	0.1	0.2	%	4V < V_{VS} < 18V
6.6	Load Regulation Maximum	VCC_{load}	—	0.1	0.5	%	5mA < I_{VCC} < 50 mA
6.7	Output Current Limitation	I_{VCClim}	—	-180	-120	mA	V_{VS} > 4V
6.8	Load Capacity	C_{load}	1.8	2.2	—	µF	MLC capacitor (**Note 3**)
6.9	VCC Undervoltage Threshold (NRES ON)	$V_{VCC\_th\_uv\_down}$	2.4	2.6	2.8	V	Referred to VCC V_{VS} > 4V
	VCC Undervoltage Threshold (NRES OFF)	$V_{VCC\_th\_uv\_up}$	2.5	2.7	2.9	V	Referred to VCC V_{VS} > 4V
6.10	Hysteresis of VCC Undervoltage Threshold	$V_{VCC\_hys\_uv}$	100	200	300	mV	Referred to VCC V_{VS} > 4V
6.11	Ramp-Up Time V_{VS} > 4V to VCC = 3.3V	t_{VCC}	—	1	1.5	ms	C_{VCC} = 2.2 µF I_{load} = -5 mA at VCC

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified all values are specified for 5V < V_{VS} < 28V, -40°C < T_{VJ} < +150°C and refer to the GND pin.

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
7	**VCC Voltage Regulator ATA663454**						
7.1	Output Voltage V_{VCC}	V_{VCCnor}	4.9	—	5.1	V	5.5V < V_{VS} < 18V (0 mA to 50 mA)
		V_{VCCnor}	4.9	—	5.1	V	6V < V_{VS} < 18V (0 mA to 85 mA) (**Note 2**)
7.2	Output Voltage V_{VCC} at Low V_{VS}	V_{VCClow}	V_{VS} - V_D	—	5.1	V	4V < V_{VS} < 5.5V
7.3	Regulator Drop Voltage	V_{D1}	—	100	200	mV	V_{VS} > 4V, I_{VCC} = -20 mA
7.4	Regulator Drop Voltage	V_{D2}	—	300	500	mV	V_{VS} > 4V, I_{VCC} = -50 mA
7.5	Regulator Drop Voltage	V_{D3}	—	—	150	mV	V_{VS} > 3.3V, I_{VCC} = -15 mA
7.6	Line regulation maximum	VCC_{line}	—	0.1	0.2	%	5.5V < V_{VS} < 18V
7.7	Load Regulation Maximum	VCC_{load}	—	0.1	0.5	%	5 mA < I_{VCC} < 50 mA
7.8	Output Current Limitation	I_{VCClim}	—	-180	-120	mA	V_{VS} > 5.5V
7.9	Load Capacity	C_{load}	1.8	2.2	—	µF	MLC capacitor (**Note 3**)
7.10	VCC Undervoltage Threshold (NRES ON)	$V_{VCC\_th\_uv\_down}$	4.2	4.4	4.6	V	Referred to VCC V_{VS} > 4V
	VCC Undervoltage Threshold (NRES OFF)	$V_{VCC\_th\_uv\_up}$	4.3	4.6	4.8	V	Referred to VCC V_{VS} > 4V
7.11	Hysteresis of Undervoltage Threshold	$V_{VCC\_hys\_uv}$	100	200	300	mV	Referred to VCC V_{VS} > 5.5V
7.12	Ramp-Up Time V_{VS} > 5.5V to VCC = 5V	t_{VCC}	—	1	1.5	ms	C_{VCC} = 2.2 µF I_{load} = -5 mA at VCC
8	**LIN Bus Driver: Bus Load Conditions: Load 1 (Small): 1 nF, 1 kΩ; Load 2 (Large): 10 nF, 500Ω; C_{RXD} = 20 pF, Load 3 (Medium): 6.8 nF, 660Ω characterized on samples; 10.7 and 10.8 specifies the timing parameters for proper operation at 20 kb/s and 10.9 and 10.10 at 10.4 kb/s**						
8.1	Driver Recessive Output Voltage	V_{BUSrec}	0.9 × V_{VS}	—	V_{VS}	V	Load1/Load2
8.2	Driver-Dominant Voltage	$V_{\_LoSUP}$	—	—	1.2	V	V_{VS} = 7V R_{load} = 500Ω
8.3	Driver-Dominant Voltage	$V_{\_HiSUP}$	—	—	2	V	V_{VS} = 18V R_{load} = 500Ω
8.4	Driver-Dominant Voltage	$V_{\_LoSUP\_1k}$	0.6	—	—	V	V_{VS} = 7V R_{load} = 1000Ω
8.5	Driver-Dominant Voltage	$V_{\_HiSUP\_1k}$	0.8	—	—	V	V_{VS} = 18V R_{load} = 1000Ω
8.6	Pull-Up Resistor to VS	R_{LIN}	20	30	47	kΩ	The serial diode is mandatory

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified all values are specified for 5V < V_{VS} < 28V, -40°C < T_{vJ} < +150°C and refer to the GND pin.

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
8.7	Voltage Drop at the Serial Diodes	$V_{SerDiode}$	0.4	—	1.0	V	In pull-up path with R_{slave} $I_{SerDiode}$ = 10 mA (**Note 3**)
8.8	LIN Current Limitation V_{BUS} = V_{Bat_max}	I_{BUS_LIM}	40	120	200	mA	
8.9	Input Leakage Current at the Receiver Including Pull-Up Resistor as Specified	$I_{BUS\_PAS\_dom}$	-1	-0.35	—	mA	Input leakage current Driver off V_{BUS} = 0V V_{VS} = 12V
8.10	Leakage Current LIN Recessive	$I_{BUS\_PAS\_rec}$	—	10	20	µA	Driver off 8V < V_{VS} < 18V 8V < V_{BUS} < 18V V_{BUS} ≥ V_{Bat}
8.11	Leakage Current when Control Unit Disconnected from Ground. Loss of local ground must not affect communication in the residual network	$I_{BUS\_NO\_gnd}$	-10	+0.5	+10	µA	GND_{Device} = V_{VS} V_{VS} = 12V 0V < V_{BUS} < 18V
8.12	Leakage Current at Disconnected Battery. Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition.	$I_{BUS\_NO\_bat}$	–	0.1	2	µA	V_{Bat} disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V
8.13	Capacitance on the LIN Pin to GND	C_{LIN}	—	—	20	pF	**Note 3**
9	**LIN Bus Receiver**						
9.1	Center of Receiver Threshold	V_{BUS_CNT}	0.475 × V_{VS}	0.5 × V_{VS}	0.525 × V_{VS}	V	V_{BUS_CNT} = (V_{th_dom} + V_{th_rec})/2
9.2	Receiver Dominant State	V_{BUSdom}	-27	—	0.4 × V_{VS}	V	V_{EN} = 5V/3.3V
9.3	Receiver Recessive State	V_{BUSrec}	0.6 × V_{VS}	—	40	V	V_{EN} = 5V/3.3V
9.4	Receiver Input Hysteresis	V_{BUShys}	0.028 × V_{VS}	0.1 × V_{VS}	0.175 × V_{VS}	V	V_{hys} = V_{th_rec} – V_{th_dom}
9.5	Pre-Wake Detection LIN High-Level Input Voltage	V_{LINH}	V_{VS} - 2V	—	V_{VS} + 0.3V	V	

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified all values are specified for 5V < V_{VS} < 28V, -40°C < T_{VJ} < +150°C and refer to the GND pin.

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
9.6	Pre-Wake Detection LIN Low-Level Input Voltage	V_{LINL}	-27	—	V_{VS} - 3.3V	V	Activates the LIN receiver
10	**Internal Timers**						
10.1	Dominant Time for Wake-Up via LIN Bus	t_{bus}	50	100	150	µs	V_{LIN} = 0V
10.2	Time delay for Mode Change from Fail-Safe Mode to Normal Mode via the EN Pin	t_{norm}	5	15	20	µs	V_{EN} = 5V/3.3V
10.3	Time Delay for Mode Change from Normal Mode to Sleep Mode via the EN Pin	t_{sleep}	5	15	20	µs	V_{EN} = 0V
10.4	TXD-Dominant Time-Out Time	t_{dom}	20	40	60	ms	V_{TXD} = 0V
10.6	Time Delay for Mode Change from Silent Mode to Normal Mode via the EN Pin	t_{s_n}	5	15	40	µs	V_{EN} = 5V/3.3V
10.7	Duty Cycle 1	D1	0.396	—	—	—	$TH_{Rec(max)} = 0.744 \times V_{VS}$ $TH_{Dom(max)} = 0.581 \times V_{VS}$ V_{VS} = 7.0V to 18V t_{Bit} = 50 µs $D1 = t_{bus\_rec(min)}/(2 \times t_{Bit})$
10.8	Duty Cycle 2	D2	—	—	0.581	—	$TH_{Rec(min)} = 0.422 \times V_{VS}$ $TH_{Dom(min)} = 0.284 \times V_{VS}$ V_{VS} = 7.6V to 18V t_{Bit} = 50 µs $D2 = t_{bus\_rec(max)}/(2 \times t_{Bit})$
10.9	Duty Cycle 3	D3	0.417	—	—	—	$TH_{Rec(max)} = 0.778 \times V_{VS}$ $TH_{Dom(max)} = 0.616 \times V_{VS}$ V_{VS} = 7.0V to 18V t_{Bit} = 96 µs $D3 = t_{bus\_rec(min)}/(2 \times t_{Bit})$
10.10	Duty Cycle 4	D4	—	—	0.590	—	$TH_{Rec(min)} = 0.389 \times V_{VS}$ $TH_{Dom(min)} = 0.251 \times V_{VS}$ V_{VS} = 7.6V to 18V t_{Bit} = 96 µs $D4 = t_{bus\_rec(max)}/(2 \times t_{Bit})$
10.11	Slope Time Falling and Rising Edge at LIN	t_{SLOPE_fall} t_{SLOPE_rise}	3.5	—	22.5	µs	V_{VS} = 7.0V to 18V
10.12	TXD Release Time after Dominant Time-Out Detection	t_{DTOrel}	10	—	20	µs	**Note 2**

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified all values are specified for 5V < V_{VS} < 28V, -40°C < T_{vJ} < +150°C and refer to the GND pin.

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
11	**Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions: C_{RXD} = 20 pF**						
11.1	Propagation Delay of Receiver	t_{rx_pd}	—	—	6	µs	V_{VS} = 7.0V to 18V t_{rx_pd} = max(t_{rx_pdr} , t_{rx_pdf})
11.2	Symmetry of Receiver Propagation Delay Rising Edge Minus Falling Edge	t_{rx_sym}	-2	—	+2	µs	V_{VS} = 7.0V to 18V t_{rx_sym} = t_{rx_pdr} - t_{rx_pdf}
12	**WKin Pin**						
12.1	High-Level Input Voltage	V_{WKinH}	V_{VS} - 1V	—	V_{VS} + 0.3V	V	
12.2	Low-Level Input Voltage	V_{WKinL}	-1	—	V_{VS} - 3.3V	V	Initializes a wake-up signal
12.3	WKin Pull-Up Current	I_{WKin}	-30	-10	—	µA	V_{VS} < 28V, V_{WKin} = 0V
12.4	High-Level Leakage Current	I_{WKinL}	-5	—	+5	µA	V_{VS} = 28V, V_{WKin} = 28V
12.5	Debounce Time of Low Pulse for Wake-Up via WKin Pin	t_{WKin}	50	100	150	µs	V_{WKin} = 0V
13	**Watchdog Oscillator**						
13.1	Voltage at WDOSC in Normal or Fail-Safe Mode	V_{WDOSC}	1.13	1.23	1.33	V	I_{WD_OSC} = -200 µA V_{VS} ≥ 4V
13.2	Possible Values of Resistor	R_{WDOSC}	34	—	120	kΩ	Resistor ±1% (**Note 3**)
13.3	Oscillator Period	t_{OSC}	21.3	26.6	31.94	µs	R_{WDOSC} = 34 kΩ
13.6	Oscillator Period	t_{OSC}	68.4	85.6	102.8	µs	R_{WDOSC} = 120 kΩ
13.7	Watchdog Lead Time After Reset	t_d	—	3948	—	cycles	**Note 1**
13.8	Watchdog Closed Window	t_1	—	527	—	cycles	**Note 1**
13.9	Watchdog Open Window	t_2	—	553	—	cycles	**Note 1**
13.10	Watchdog Reset Time NRES	t_{nres}	2	4	6	ms	**Note 1**
14	**Watchdog Trigger Input Pin NTRIG**						
14.1	Low-Level Voltage Input	V_{NTRIG_L}	-0.3	—	0.3V_{VCC}	V	
14.2	High-Level Voltage Input	V_{NTRIG_H}	0.7 x V_{VCC}	—	V_{VCC} + 0.3	V	
14.3	Pull-Up Resistor	R_{NTRIG}	125	250	400	K	V_{NTRIG} = 0V
14.4	Input Leakage Current	$I_{NTRIGleakH}$	—	—	1	µA	V_{NTRIG} = V_{VCC}
14.5	Minimum Trigger Width	t_{trig}	200	—	—	ns	V_{NTRIG} = V_{VCC} (**Note 3**)

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified all values are specified for 5V < V_{VS} < 28V, -40°C < T_{VJ} < +150°C and refer to the GND pin.

No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
15	**MODE Pin**						
15.1	Low-Level Input Voltage	V_{MODE_L}	-0.3	—	0.3 x V_{VCC}	V	
15.2	High-Level Input Voltage	V_{MODE_H}	0.7 x V_{VCC}	—	V_{VCC} + 0.3	V	
15.4	Leakage Current	I_{MODE}	-3	—	+3	µA	V_{MODE} = 0V or V_{MODE} = V_{VCC}
15.5	MODE Pin Pull-Up Current	I_{MODE_PU}	-75	—	-5	µA	V_{MODE} = 0.7 x V_{VCC}
15.6	MODE Pin Pull-Down Current	I_{MODE_PD}	5	—	75	µA	V_{MODE} = 0.3 x V_{VCC}
16	**Limp Home Open Drain Failure Output Pin LH**						
16.1	Output Drain-to-Source on Resistance	$R_{DSon,LH}$	—	—	50	Ω	Tj = +125°C
16.2	Leakage Current	$I_{leak,LH}$	—	—	2	µA	V_{LH} < 40V
17	**HSout Pin**						
17.1	Output Drain-to-Source on Resistance	$R_{DSon,HS}$	—	—	20	Ω	I_{HSout} = -20 mA
17.2	Leakage Current	$I_{leak,HS}$	—	—	2	µA	–0.2V < V_{HSout} < V_{VS}+ 0.2V
17.5	Switch-Off Slope (Fall Time)	$t_{HSslope,fall}$	0.75	—	5	µs	V_{VS} = 16V R_{load} = 560Ω C_{load} = 1 nF transition from 80% down to 20% of V_{VS}
17.6	Switch-On Slope (Rise Time)	$t_{HSslope,rise}$	0.75	—	5	µs	V_{VS} = 16V R_{load} = 560Ω C_{load} = 1 nF transition from 20% to 80% of V_{VS}
17.7	Switch-On Delay	t_{HSdel}	3	—	20	µs	V_{VS} = 16V R_{load} = 560Ω C_{load} = 1 nF time from HSin = HIGH to V_{HSout} = 50% of V_{VS}
17.8	Switch-Off Delay	t_{HSdel}	3	—	20	µs	V_{VS} = 16V R_{load} = 560Ω C_{load} = 1 nF time from HSin = LOW to V_{HSout} = 50% of V_{VS}
17.9	Short-Circuit Detection Threshold	V_{SCth_HS}	V_{VS} - 6V	—	V_{VS} - 2V	V	
17.10	Short-Circuit Debounce Time	t_{HS_deb}	2	—	10	µs	
18	**HSin Pin**						
18.1	Low-Level Voltage Input	V_{HSin_L}	-0.3	—	0.3 x V_{VCC}	V	

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: Unless otherwise specified all values are specified for 5V < V_{VS} < 28V, -40°C < T_{vJ} < +150°C and refer to the GND pin.

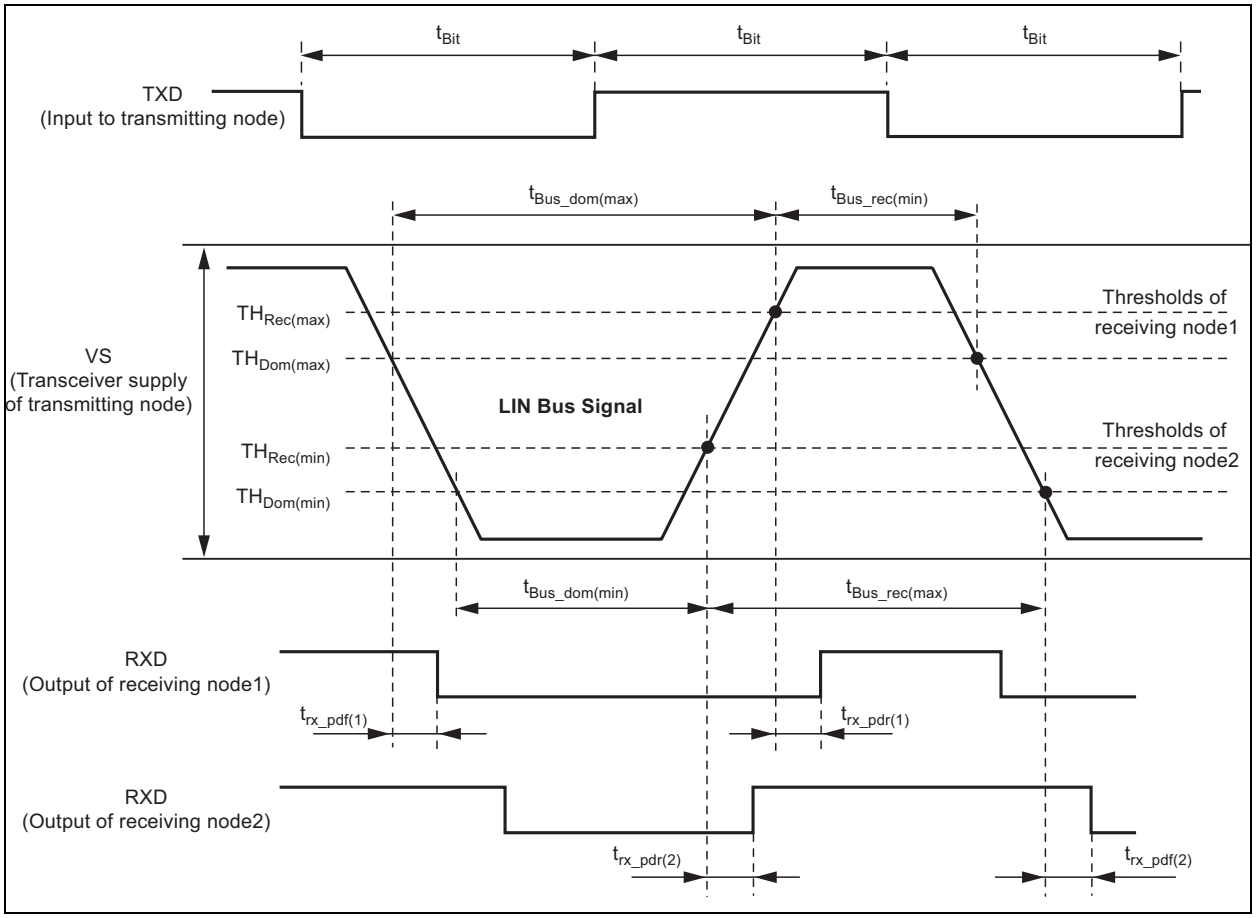
No.	Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
18.2	High-Level Voltage Input	V_{HSin_H}	0.7 x V_{VCC}	—	V_{VCC} + 0.3	V	
18.3	Pull-Down Resistor	R_{HSin}	50	100	150	kΩ	V_{HSin} = V_{VCC}
18.4	Low-Level Input Current	I_{HSin}	-1	—	+1	µA	V_{HSin} = 0V
18.5	Maximum Switching Frequency	$f_{HSin,max}$	5	—	—	kHz	R_{load} = 560Ω (**Note 3**)
19	**CL15 HV Input Pin**						
19.1	High Level Input Voltage	V_{CL15H}	4	—	—	V	Positive edge initiates a local wake-up
19.2	Low Level Input Voltage	V_{CL15L}	-1	—	+2	V	
19.3	Pull-Down Current	I_{CL15}	—	50	60	µA	V_{VS} < 28V, V_{CL15} = 28V
19.4	Internal Debounce Time	t_{dbCL15}	50	100	150	µs	Without external capacitor

Note 1: 100% correlation tested.

2: Characterized on samples.

3: Design parameter.

FIGURE 2-1: DEFINITION OF BUS TIMING CHARACTERISTICS



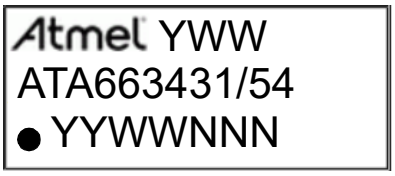
TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Unit
Thermal Resistance Virtual Junction to Thermal Pad	R_{thvJC}	—	8	—	K/W
Thermal Resistance Virtual Junction to Ambient, where Thermal Pad is Soldered to PCB according to JEDEC	R_{thvJA}	—	45	—	K/W
Thermal Shutdown of VCC Regulator	T_{VCCoff}	+150	+165	+180	°C
Thermal Shutdown of LIN Output	T_{LINoff}	+150	+165	+180	°C
Thermal Shutdown of High-Side Driver	T_{DSoff}	+150	+165	+180	°C
Thermal Shutdown Hysteresis	T_{hys}	—	+10	—	°C

3.0 PACKAGING INFORMATION

3.1 Package Marking Information

16-Lead 3 x 5.5 mm VDFN



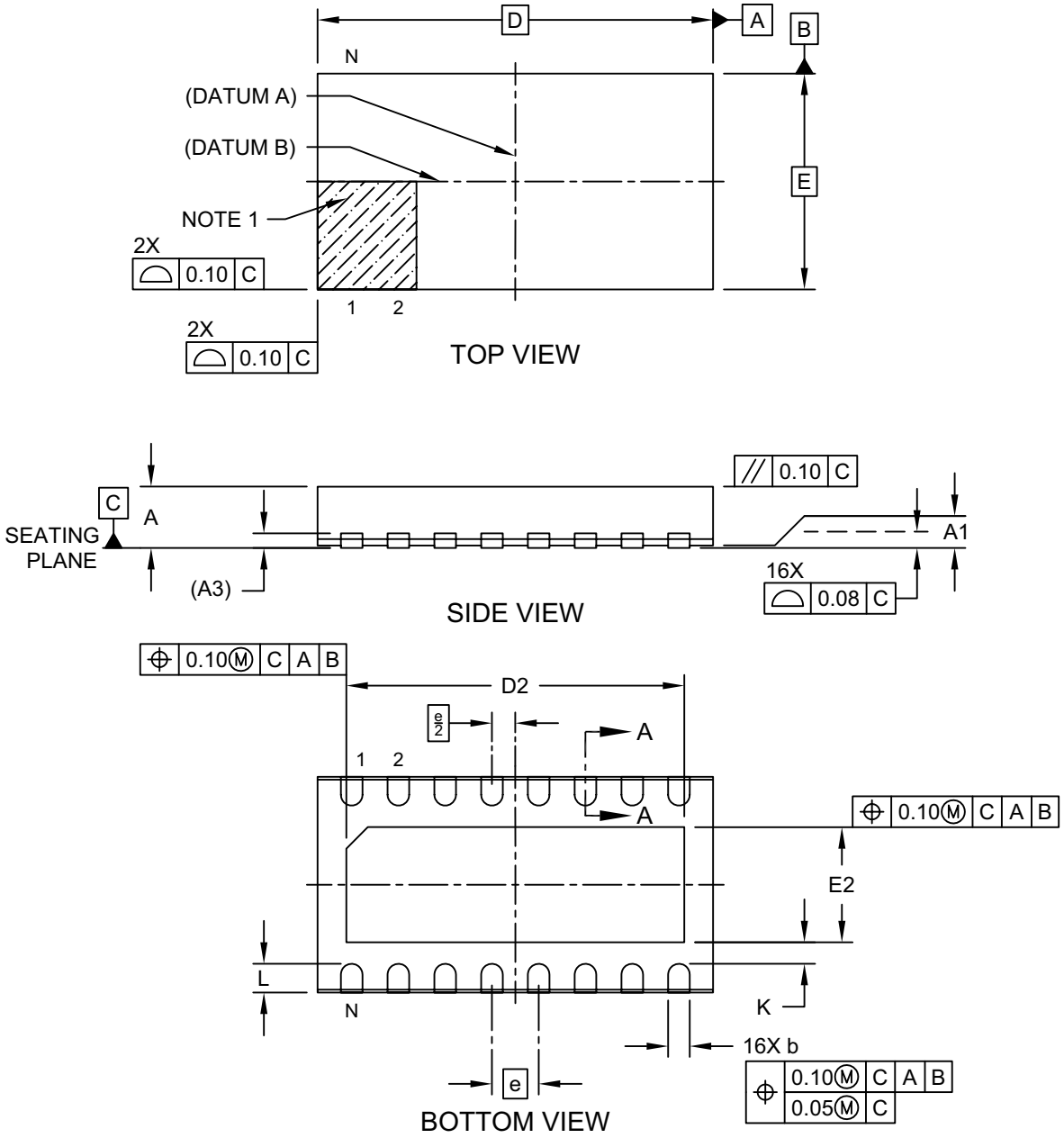
Examples:

Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

16-Lead Very Thin Plastic Dual Flat, No Lead Package (QDB) - 5.5x3 mm Body [VDFN] With Stepped Wettable Flanks and 4.7x1.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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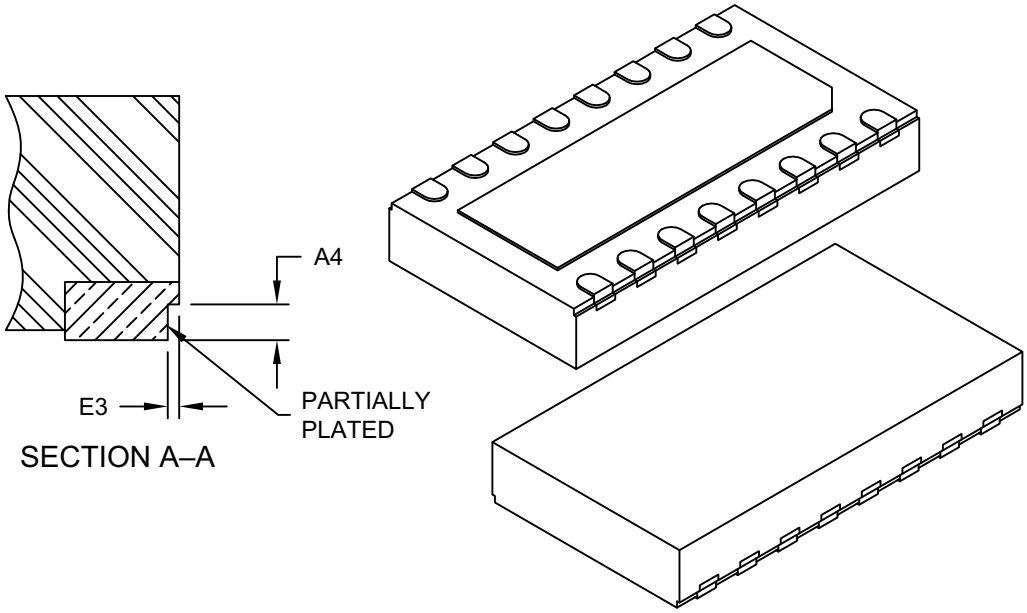
16-Lead Very Thin Plastic Dual Flat, No Lead Package (QDB) - 5.5x3 mm Body [VDFN] With Stepped Wettable Flanks and 4.7x1.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Wettable Flank Step Cut Depth	A4	0.10	0.13	0.15
Overall Length	D		5.50 BSC	
Exposed Pad Length	D2	4.60	4.70	4.80
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.50	1.60	1.70
Wettable Flank Step Cut Width	E3	-	-	0.04
Terminal Width	b	0.25	0.30	0.35
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

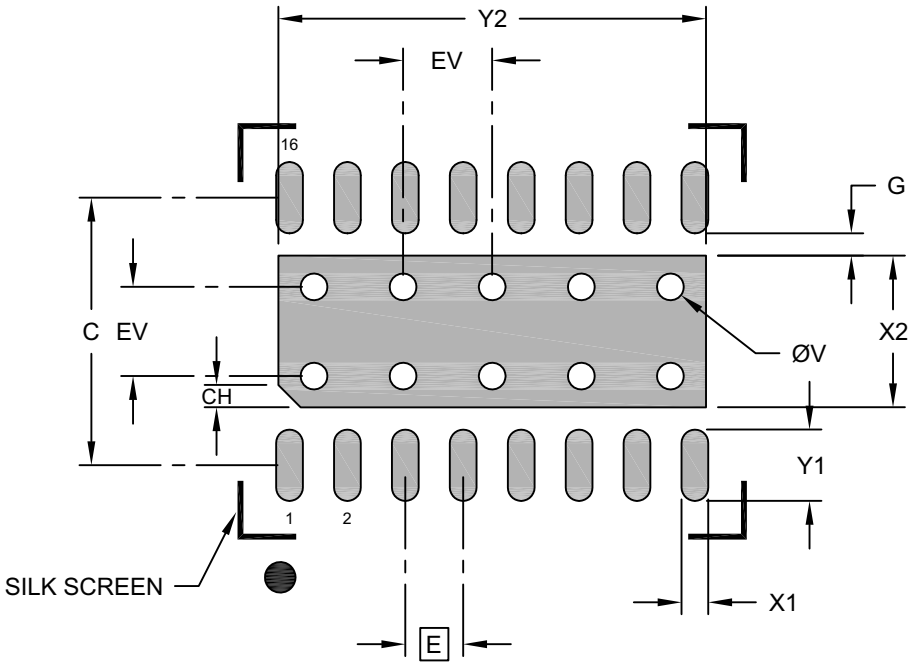
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21363 Rev A Sheet 2 of 2

16-Lead Very Thin Plastic Dual Flat, No Lead Package (QDB) - 5.5x3 mm Body [VDFN] With Stepped Wettable Flanks and 4.7x1.6 mm Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Optional Center Pad Width	X2			1.70
Optional Center Pad Length	Y2			4.80
Contact Pad Spacing	CH		0.25	
Exposed Pad 45° Corner Chamfer	C		3.00	
Contact Pad Width (X16)	X1			0.30
Contact Pad Length (X16)	Y1			0.80
Contact Pad to Center Pad (X16)	G	0.25		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23363 Rev A

APPENDIX A: REVISION HISTORY

Revision A (November 2018)

- Original Release of this Document.
- This document replaces *Atmel - 9232H-AUTO-09/14*.
- Minor text updates.

Revision B (November 2018)

- Minor text updates.

Revision C (May 2020)

- Updated Maximum rating of pin VS in chapter 2.1.
- Minor text updates.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	—	XX	[X](1)	X
Device		Package	Tape and Reel Option	Package Directives Classification

Device:	ATA663431/54:	LIN SBC including LIN Transceiver, Voltage Regulator, Window Watchdog and High-Side Switch
Package:	GD =	16-Lead VDFN
Tape and Reel Option:	Q =	330 mm diameter Tape and Reel(1)
Package Directives Classification:	W =	Package according to RoHS(2)

Examples:

a) ATA663431-GDQW: 16-Lead VDFN, Tape and Reel, Package according to RoHS

b) ATA663454-GDQW: 16-Lead VDFN, Tape and Reel, Package according to RoHS

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: RoHS compliant; maximum concentration value of 0.09% (900 ppm) for Bromine (Br) and Chlorine (Cl) and less than 0.15% (1500 ppm) total Bromine (Br) and Chlorine (Cl) in any homogeneous material. Maximum concentration value of 0.09% (900 ppm) for Antimony (Sb) in any homogeneous material.

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