



CSD13381F4 12 V N-Channel FemtoFET™ MOSFET

1 Features

- Low On-Resistance
- Low Q_g and Q_{gd}
- Low Threshold Voltage
- Ultra-Small Footprint (0402 Case Size)
 - 1.0 mm × 0.6 mm
- Ultra-Low Profile
 - 0.35 mm Height
- Integrated ESD Protection Diode
 - Rated >4 kV HBM
 - Rated >2 kV CDM
- Lead and Halogen Free
- RoHS Compliant

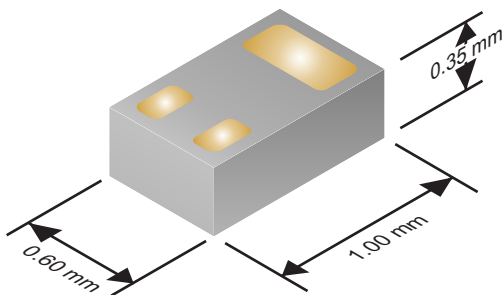
2 Applications

- Optimized for Load Switch Applications
- Optimized for General Purpose Switching Applications
- Single-Cell Battery Applications
- Handheld and Mobile Applications

3 Description

This 140 mΩ, 12 V N-channel FemtoFET™ MOSFET technology is designed and optimized to minimize the footprint in many handheld and mobile applications. This technology is capable of replacing standard small signal MOSFETs while providing at least a 60% reduction in footprint size.

Typical Part Dimensions



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	12		V
Q_g	Gate Charge Total (4.5 V)	1060		pC
Q_{gd}	Gate Charge Gate-to-Drain	140		pC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 1.8\text{ V}$	310	mΩ
		$V_{GS} = 2.5\text{ V}$	170	mΩ
		$V_{GS} = 4.5\text{ V}$	140	mΩ
$V_{GS(th)}$	Threshold Voltage	0.85		V

Ordering Information⁽¹⁾

Device	Qty	Media	Package	Ship
CSD13381F4	3000	7-Inch Reel	Femto (0402) 1.0 mm x 0.6 mm SMD Lead Less	Tape and Reel
CSD13381F4T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	12	V
V_{GS}	Gate-to-Source Voltage	8	V
I_D	Continuous Drain Current, $T_A = 25^\circ\text{C}^{(1)}$	2.1	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}^{(2)}$	7	A
I_G	Continuous Gate Clamp Current	35	mA
	Pulsed Gate Clamp Current ⁽²⁾	350	
P_D	Power Dissipation ⁽¹⁾	500	mW
ESD Rating	Human Body Model (HBM)	4	kV
	Charged Device Model (CDM)	2	kV
T_J, T_{stg}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 7.4\text{ A}$, $L = 0.1\text{ mH}$, $R_G = 25\text{ }\Omega$	2.7	mJ

(1) Typical $R_{\theta JA} = 90^\circ\text{C/W}$ on 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 0.06 inch (1.52 mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

Top View

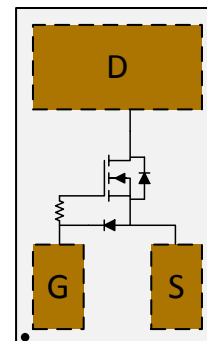


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2014) to Revision D Page

- Corrected typo for I_{GSS} Test Condition **3**

Changes from Revision B (February 2014) to Revision C Page

- Corrected timing V_{DS} to read 6 V **3**

Changes from Revision A (November 2013) to Revision B Page

- Added I_G parameter **1**
- Lowered I_{DSS} limit..... **3**
- Lowered I_{GSS} limit **3**

Changes from Original (July 2013) to Revision A Page

- Updated device ordering information..... **1**
- Changed test voltage conditions **3**
- Changed [Figure 4](#) Gate Charge graph..... **5**

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV _{DSS}	Drain-to-Source Voltage	V _{GS} = 0 V, I _{DS} = 250 μA	12			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 9.6 V	100			nA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = 8 V	50			nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _{DS} = 250 μA	0.65	0.85	1.10	V
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 1.8 V, I _{DS} =0.5 A	310		400	mΩ
		V _{GS} = 2.5 V, I _{DS} =0.5 A	170		225	mΩ
		V _{GS} = 4.5 V, I _{DS} = 0.5 A	140		180	mΩ
g _{fs}	Transconductance	V _{DS} = 6 V, I _{DS} = 0.5 A	3.2			S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 6 V, f = 1 MHz	155		200	pF
C _{oss}	Output Capacitance		47		62	pF
C _{rss}	Reverse Transfer Capacitance		2.5		3.3	pF
R _G	Series Gate Resistance	V _{DS} = 6 V, I _{DS} = 0.5 A	23			Ω
Q _g	Gate Charge Total (4.5 V)		1060		1400	pC
Q _{gd}	Gate Charge Gate-to-Drain		140			pC
Q _{gs}	Gate Charge Gate-to-Source		230			pC
Q _{g(th)}	Gate Charge at V _{th}		155			pC
Q _{oss}	Output Charge		1120			pC
t _{d(on)}	Turn On Delay Time	V _{DS} = 6 V, V _{GS} = 4.5 V, I _{DS} = 0.5 A, R _G = 2 Ω	3.7			ns
t _r	Rise Time		1.5			ns
t _{d(off)}	Turn Off Delay Time		11.0			ns
t _f	Fall Time		3.8			ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{SD} = 0.5 A, V _{GS} = 0 V	0.73		0.9	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 6 V, I _F = 0.5 A, di/dt = 300 A/μs	1550			pC
t _{rr}	Reverse Recovery Time		6			ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

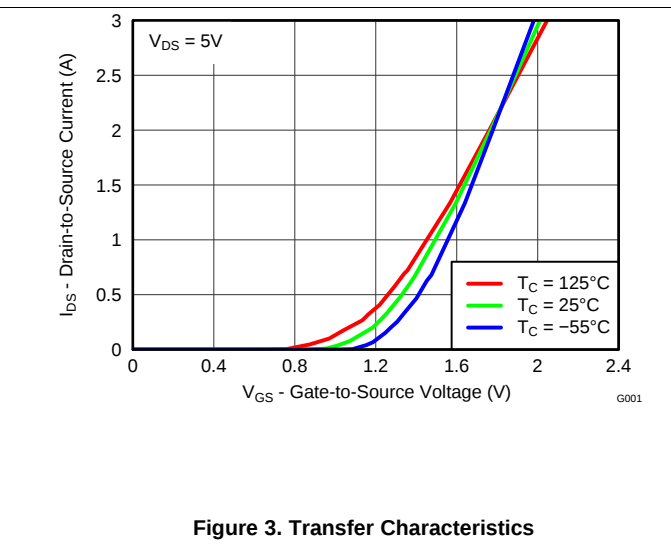
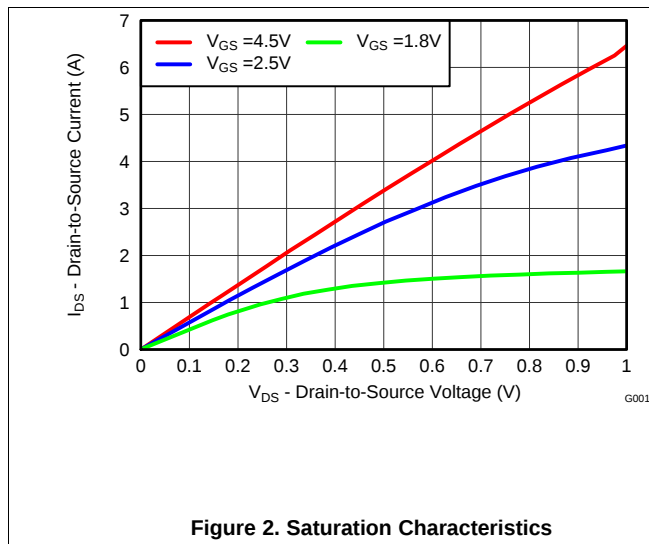
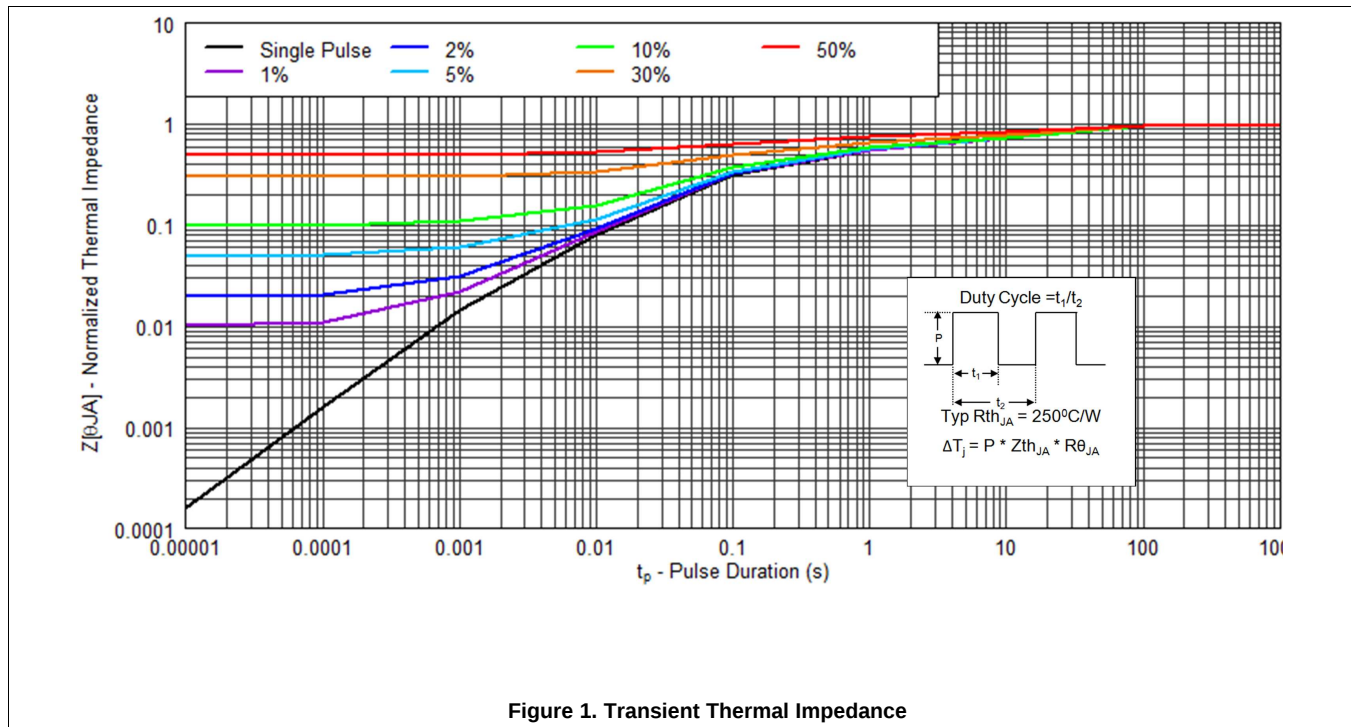
THERMAL METRIC		TYPICAL VALUES	UNIT
R _{θJA}	Junction-to-Ambient Thermal Resistance ⁽¹⁾	90	°C/W
	Junction-to-Ambient Thermal Resistance ⁽²⁾	250	

(1) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

(2) Device mounted on FR4 material with minimum Cu mounting area.

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

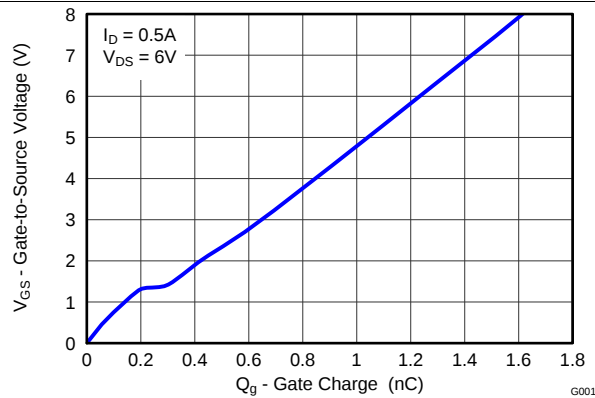


Figure 4. Gate Charge

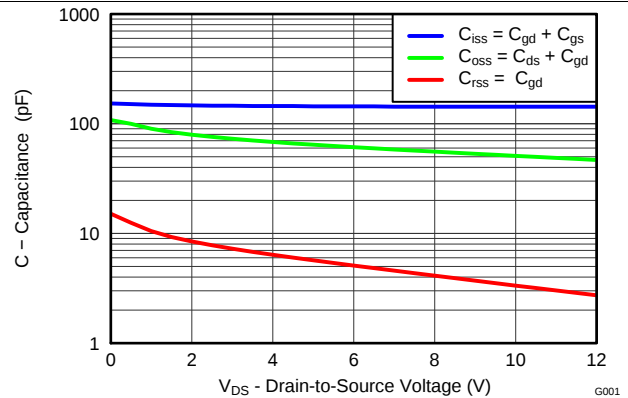


Figure 5. Capacitance

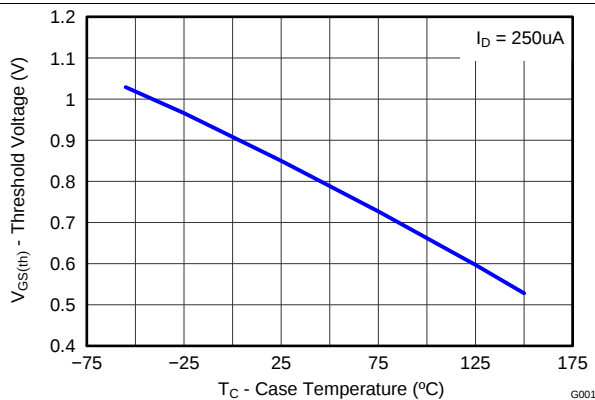


Figure 6. Threshold Voltage vs Temperature

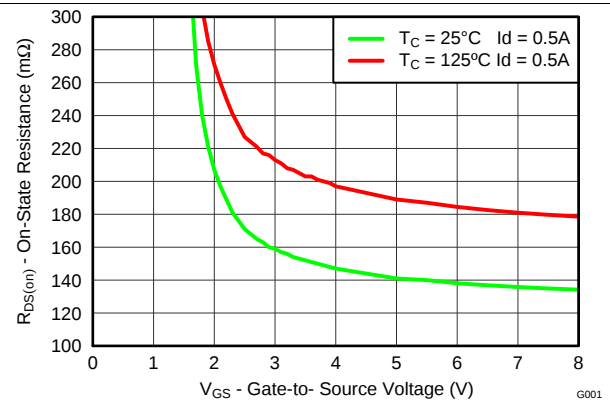


Figure 7. On-State Resistance vs Gate-to-Source Voltage

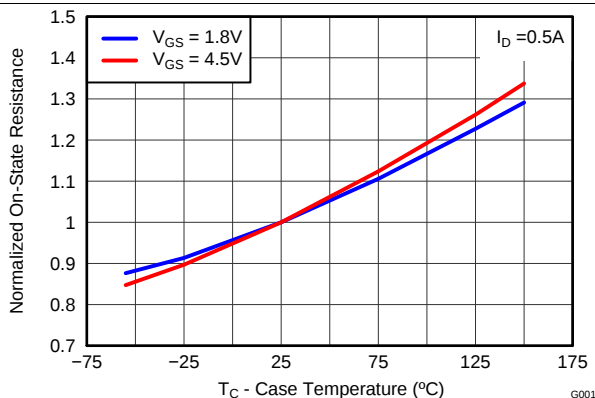


Figure 8. Normalized On-State Resistance vs Temperature

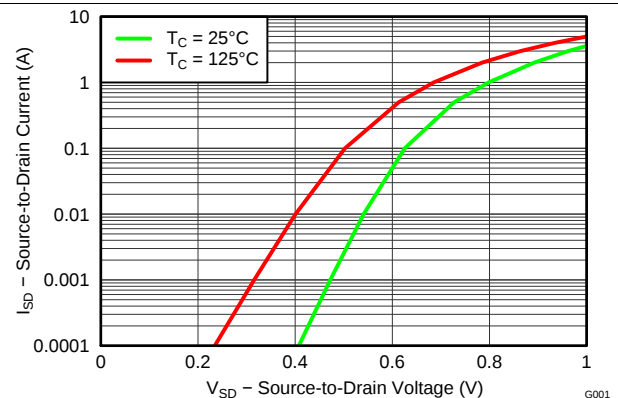


Figure 9. Typical Diode Forward Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

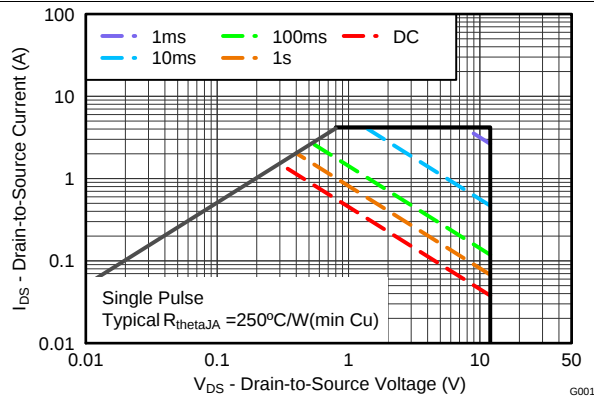


Figure 10. Maximum Safe Operating Area (SOA)

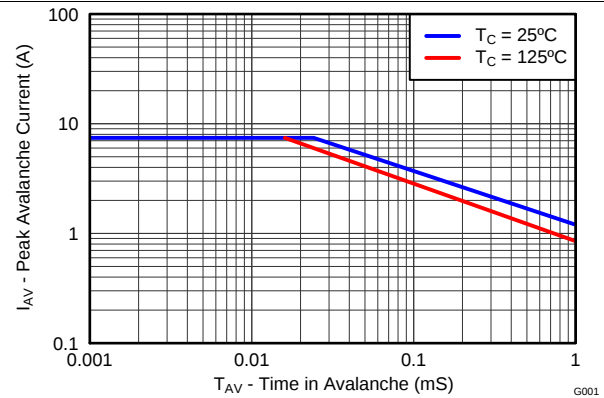


Figure 11. Single Pulse Unclamped Inductive Switching

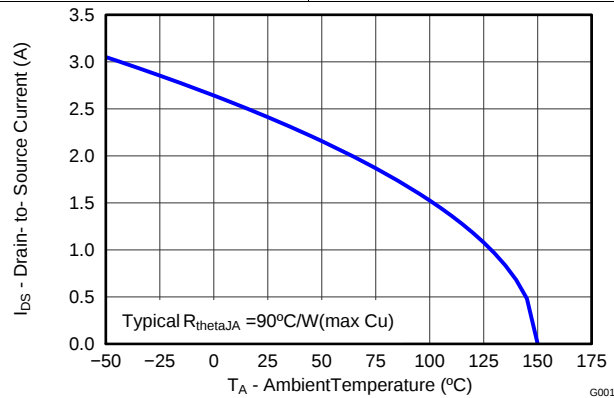


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

FemtoFET is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

6.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

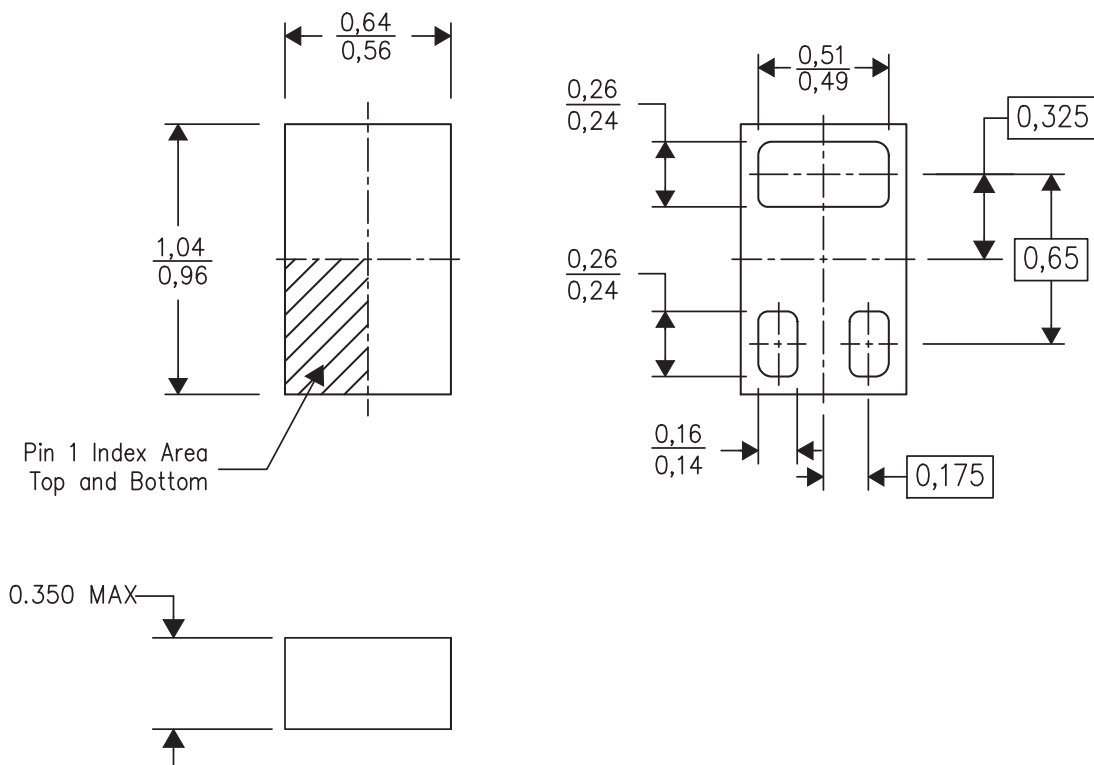
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 Mechanical Data

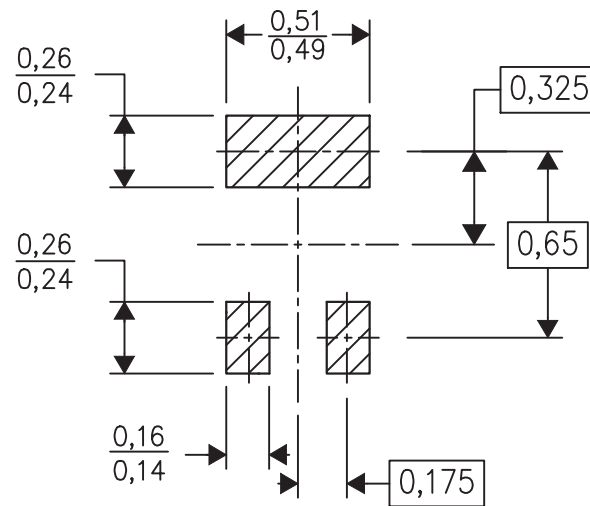
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions



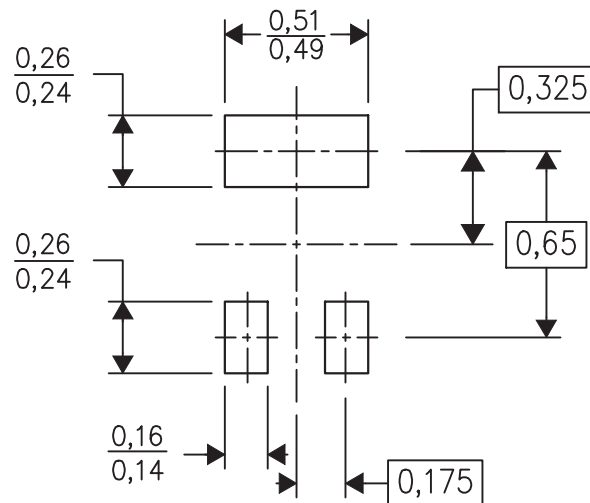
- (1) All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
- (2) This drawing is subject to change without notice.
- (3) This package is a PB-free solder land design.

7.2 Recommended Minimum PCB Layout



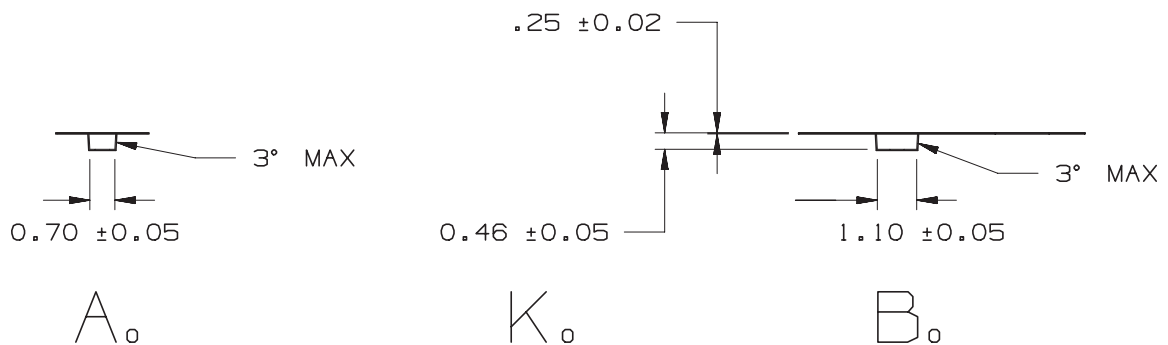
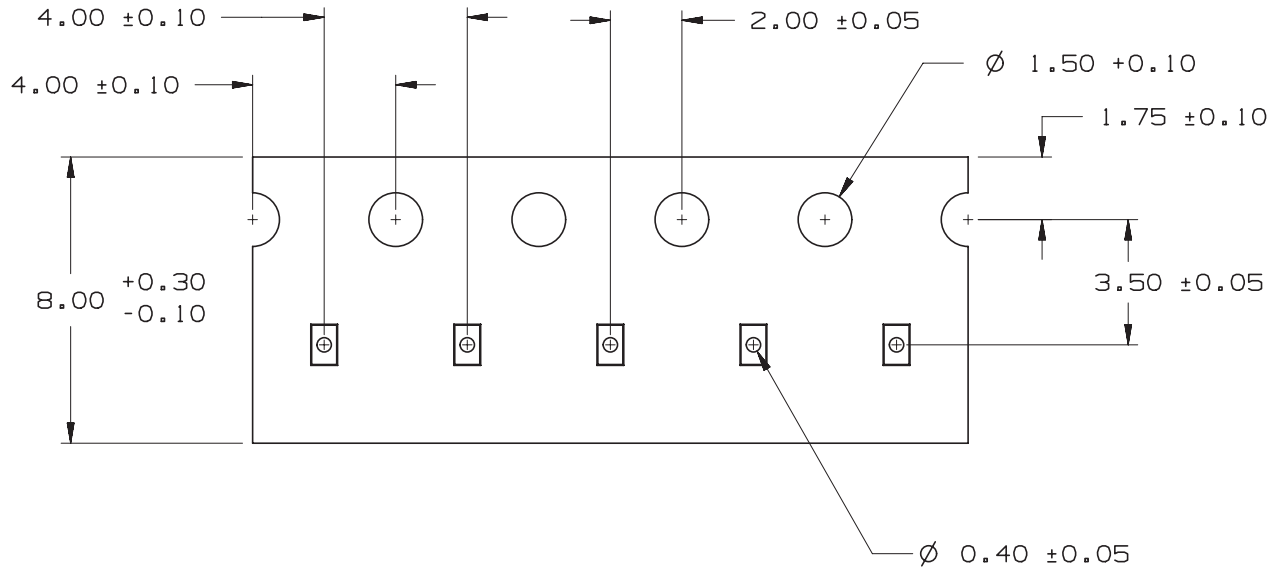
(1) All dimensions are in millimeters.

7.3 Recommended Stencil Pattern



(1) All dimensions are in millimeters.

7.4 CSD13381F4 Embossed Carrier Tape Dimensions



- (1) Pin 1 is oriented in the top-right quadrant of the tape enclosure (quadrant 2), closest to the carrier tape sprocket holes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD13381F4	ACTIVE	PICOSTAR	YJC	3	3000	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	DQ	Samples
CSD13381F4T	ACTIVE	PICOSTAR	YJC	3	250	Green (RoHS & no Sb/Br)	Call TI	Level-1-260C-UNLIM	-55 to 150	DQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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