MPM3682

18V 10A Step-Down Power Module in 12x12x4mm QFN

DESCRIPTION

The MPM3682 is an easy-to-use fully integrated 10A step-down DC/DC power module. It integrates the DC/DC converter, power inductor, input/output capacitors and the necessary resistors/capacitors in a compact QFN 12mmX12mmX4mm package. This total power solution needs as few as two external components (one resistor and one capacitor) to work. MPM3682 can deliver 10A output current over a wide input supply voltage range with excellent load and line regulation.

The MPM3682 uses Constant-On-Time (COT) control to provide fast transient response and ease the loop stabilization.

The default under voltage lockout threshold is internally set around 4.1V, but a resistor network on the enable pin can increase this threshold. The MPM3682 has an internal LDO to power the control circuits and the integrated power devices. This LDO can be disabled by an external 5V to boost the efficiency.

The MPM3682 has an internal about 3ms soft start (SS) timer. It can be increased with an extra SS capacitor. An open drain power good signal indicates that the output voltage is within nominal voltage range.

The MPM3682 has fully integrated protection features that include over-current protection, over-voltage protection and thermal shutdown.

FEATURES

- Complete 10A DC-to-DC Solution
- Wide Input Voltage Range from 2.5V:
  -- 2.5V to 18V with External 5V Bias
  -- 4.5V to 18V with Internal Bias
- 1% Reference Voltage Over 0˚C to 70˚C Junction Temperature Range
- Adaptive COT Control for Ultrafast Transient Response
- Programmable Switching Frequency from 200KHz to 1MHz
- Support Pre-Bias Start Up
- Programmable Soft-Start Time with Default 3ms
- Non-latch OCP, OVP and Thermal Shutdown
- Output Adjustable from 0.65V to 5V
- QFN-57 (12mm x 12mm x 4mm) package

APPLICATIONS

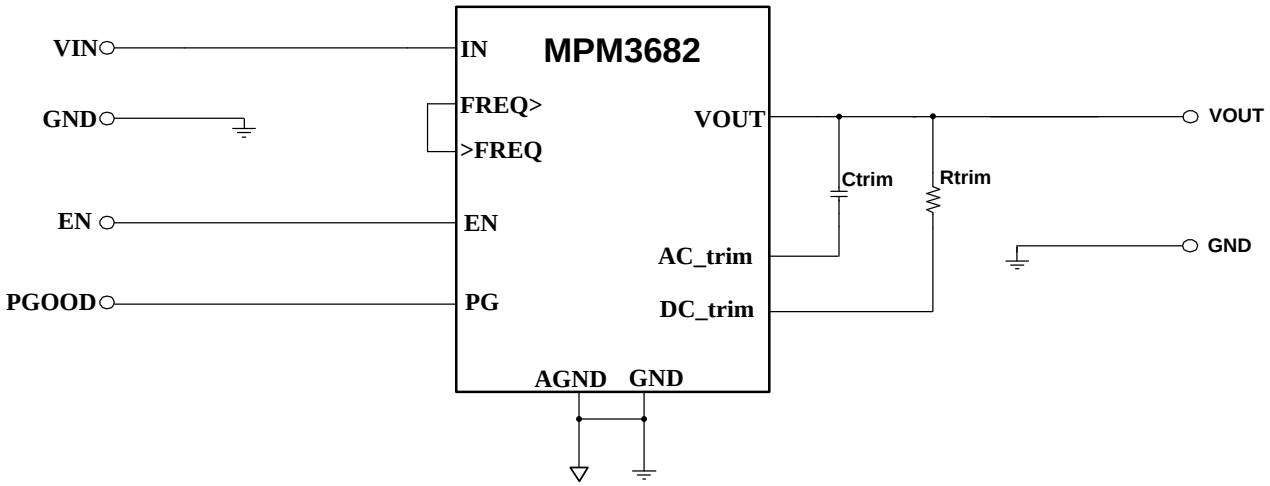
- Telecom and Networking Systems
- Base Stations
- Servers
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

"MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

TYPICAL APPLICATION



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking
MPM3682GRE	QFN-57 (12mmx12mmx4mm)	*See Below*

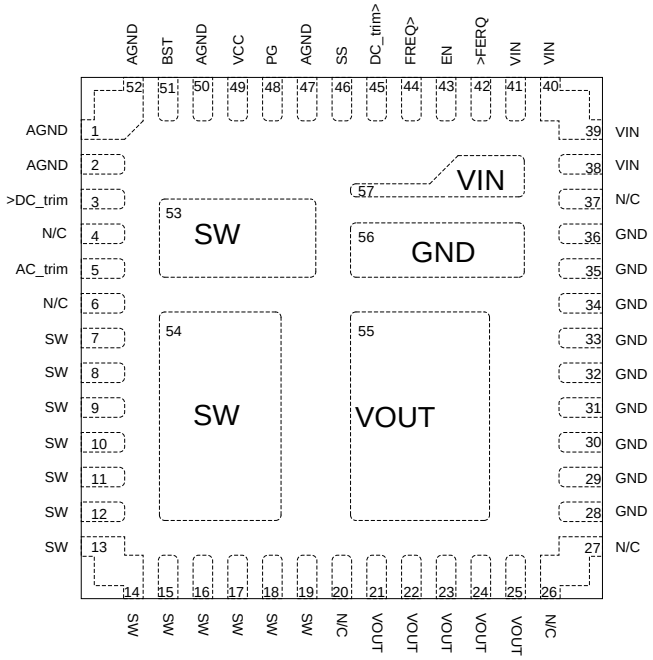
TOP MARKING

MPSYYWW
MP3682
LLLLLLLLL
M

MPS: MPS prefix:
YY: year code;
WW: week code:
MP3682: product code;
LLLLLLLLL: lot number;
M: module

PACKAGE REFERENCE

TOP VIEW



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} to GND..... -0.3V to 21V
$V_{SW(DC)}$ to GND .....–1V to V_{IN}+0.3V
$V_{SW5\ (30ns)}$ to GND..... –3 V to V_{IN}+3V or 24V
V_{BST} .....–0.3 V to V_{IN}+6V
All Other Pins to AGND..... –0.3V to +6V
Continuous Power Dissipation (T_A=+25°) (2)
QFN-65 (12mmx12mmx4mm) 50W
Continuous Output Current 12A
Junction Temperature .....150°C
Lead Temperature .....260°C
Storage Temperature..... –55°C to +150°C
MSL .....Level 3 (5)
ESD (HBM)..... 2kV
ESD (CDM)..... 500V

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....4.5V to 18V
Output Voltage V_{OUT} .....0.65V to 5V
Enable Current I_{EN}……..…....1mA
Ambient Temperature.....–40°C to +85°C
Junction Temperature .....–40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

QFN-57 (12mmx12mmx4mm)..16.2.....6.3 .. °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.
5) Need to get some test data from 1st sample for calibration and evaluation for MSL Level 2.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, R_{trim} =10kΩ, C_{trim} =560pF, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Voltage Range						
Input Voltage Range	V_{IN}	5V External VCC	2.5		18	V
			4.5		18	V
Output Voltage						
Output Voltage Range (6)	V_{OUT_RANGE}		0.65		5	V
Output Voltage Accuracy (Load Regulation) (6)	$V_{OUT_DC_Load}$	C_{OUT} =5X47μF Ceramic, I_{OUT} =0A to 10A		±0.5		%Vout
Output Voltage Accuracy (Line Regulation) (6)	$V_{OUT_DC_Line}$	C_{OUT} =5X47μF Ceramic, V_{IN} =4.5V to 18V, I_{OUT} =5A		±0.4		%Vout
Quiescent Current						
Quiescent Current	I_{IN}	V_{EN} =2V, V_{FB}=0.65V	700	860	1000	uA
Current Limit						
Output Current Limit	I_{LIM}		12	15	19	A
Switching Frequency (6)						
Switching Frequency	f_{SW}	I_{OUT}=5A	400	500	600	kHz
Over-voltage and Under-voltage Protection						
OVP Non-latch Threshold (7)	$V_{OVP_NON-LATCH}$	With negative current limit	117%	120%	123%	V_{FB}
OVP Threshold (6)	V_{OVP_TH}	No negative current limit	127%	130%	133%	V_{FB}
UVP Threshold (6)	V_{UVP}		47%	50%	53%	V_{FB}
Reference And Soft Start						
Reference Voltage (8)	V_{REF}	T_J = 0°C to +70°C	608	611	614	mV
		T_J = 0°C to +120°C	605	611	617	mV
		T_J = -40°C to +125°C	602	611	620	mV
Soft Start Time	t_{SS}		2	2.8	3.6	ms
Timer (6)						
Minimum ON Time	T_{ON_MIN}		20	30	40	ns
Minimum OFF Time	T_{OFF_MIN}		200	360	420	ns

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1.2V, R_{trim} =10kΩ, C_{trim} =560pF, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Power Good						
Power Good Rising Threshold (7)	PG_{Vth-Hi}		87%	91%	94%	V_{FB}
Power Good Falling Threshold (7)	PG_{Vth-Lo}			80%		V_{FB}
Power Good Low to High Delay (7)	PG_{Td}			2.5		ms
Power Good Sink Current Capability (7)	I_{OL}	V_{OL}=600mV			12	mA
Power Good Leakage Current (7)	I_{PG_LEAK}	V_{PG}=3.3V		0.01		uA
PG Low-Level Output Voltage	V_{OL_100}	V_{IN}=0V, Pull PGood up to 3.3V through a 100KΩ resistor.	500	550	600	mV
	V_{OL_10}	V_{IN}=0V, Pull PGood up to 3.3V through a 10KΩ resistor.	600	650	700	mV
Enable (7)						
Enable Input Low Voltage	VIL_{EN}		1.1	1.3	1.5	V
Enable Hysteresis	V_{EN-HYS}			250		mV
Enable Input Current	I_{EN}	V_{EN} = 2V		0		µA
VCC Regulator (7)						
VCC Under Voltage Lockout Threshold Rising	VCC_{Vth}			3.8		V
VCC Under Voltage Lockout Threshold Hysteresis	VCC_{HYS}			500		mV
VCC Regulator	V_{CC}			4.8		V
VCC Load Regulation		I_{CC}=5mA		0.5		%
Thermal Protection (6)						
Thermal Shutdown	T_{SD}		150			°C
Thermal Shutdown Hysteresis				25		°C

Notes:

6) Guaranteed by design
7) 100% tested for internal IC prior to module assembly
8) Guaranteed by production test and/or characterization for internal IC prior to module assembly

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1, 2, 47, 50, 52	AGND	Analog/Signal Ground. It needs to be connected to GND on PCB layout.
3	>DC_trim	Output Voltage DC Trimming. Connect this pin to pin DC_trim> first, and then to the output voltage sense point through a resistor. The resistor value can be chosen based on equation 1.
4, 6, 20, 26, 27, 37	N/C	Not connected. Keep these pins floating.
5	AC_trim	Output Voltage AC Trimming. Connect these pins to the output through a capacitor. The capacitor value can be chosen based on equation 2.
7 - 19, 53, 54	SW	Switch Output. Keep them floating.
21 - 25, 55	VOUT	Module voltage output node.
28 - 36, 56	GND	System Power Ground. Reference ground of the regulated output voltage. PCB layout requires extra care. Connect using wide PCB traces.
38 - 41, 57	VIN	Supply Voltage. Supply power to the internal MOSFET and regulator. The MPM3682 operates from a +2.5V to +18V input rail with 5V external bias and from a +4.5V to +18V input rail with internal bias. It requires input decoupling capacitors. Connect using wide PCB traces and multiple vias.
42	>FREQ	Frequency Set In. An internal 430K frequency set resistor is used if connecting this pin to Pin FREQ<. Keep this pin floating if values other than 300K are needed.
43	EN	Enable. Digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Connect EN to IN through a pull-up resistor or a resistive voltage divider for automatic startup. Do not float this pin.
44	FREQ>	Frequency Set Out. An internal 430K frequency set resistor is used if connecting this pin to Pin FREQ>. If values other than 430K are needed, connect the resistor between this pin and pin VIN.
45	DC_trim>	Output Voltage DC Trimming. Connect this pin to pin >DC_trim first, and then to the output voltage sense point through a resistor. The resistor value can be chosen based on equation 1.
46	SS	Soft Start. Floating this pin has the default 3ms SS time. The SS time can be extended by connecting an external capacitor between SS and AGND pins.
48	PG	Power Good. The output is an open drain signal. Require a pull-up resistor to a DC voltage to indicate high if the output voltage exceeds 91% of the nominal voltage. There is a 2.5ms delay from FB ≥ 91% to PG goes high.
49	VCC	Internal 4.8V LDO Output. Power the driver and control circuits. Keep this pin floating. Applying a 5V external bias can disable the internal LDO to boost the efficiency.
51	BST	Bootstrap. Keep this pin floating.

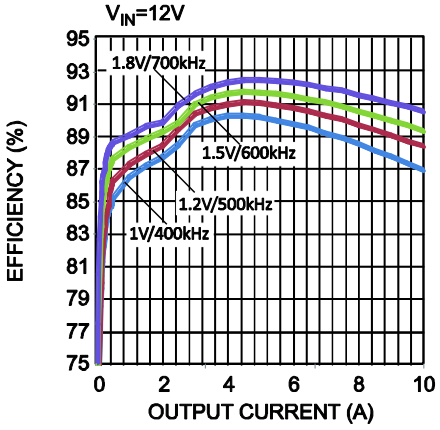
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

V_{IN}=12V, V_{OUT}=1.2V, T_A=25˚C, unless otherwise noted.

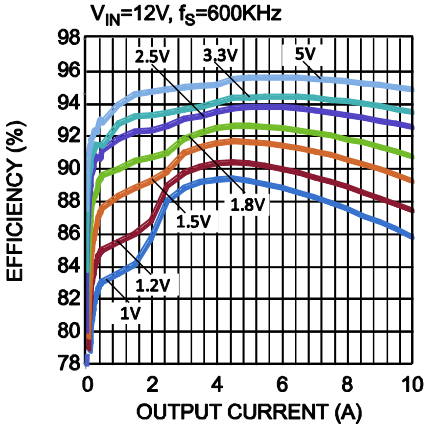
Efficiency vs. Output Current

V_{IN}=12V



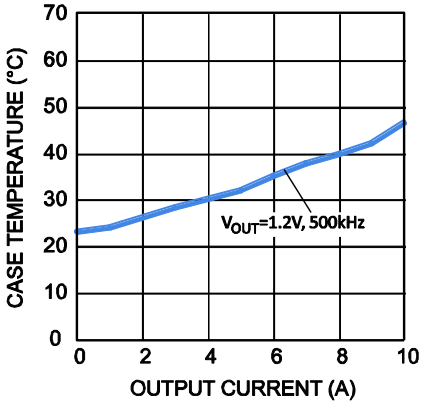
Efficiency vs. Output Current

V_{IN}=12V, f_S=600KHz



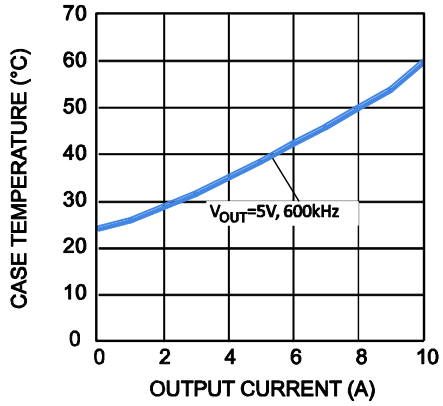
Thermal Results

$T_{AMBIENT}$=22˚C, No Airflow



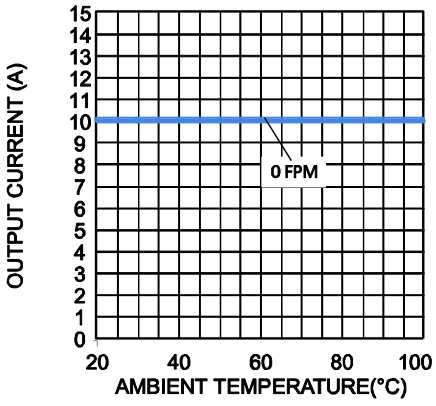
Thermal Results

$T_{AMBIENT}$=22˚C, No Airflow



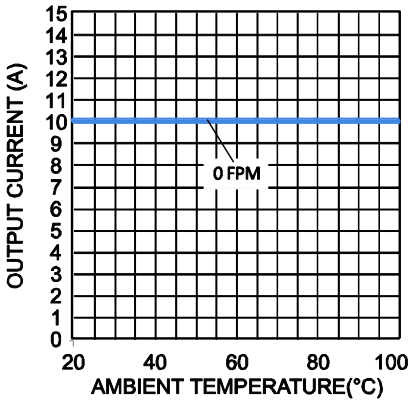
Output Current De-Rating

12V to 1.2V, 600kHz



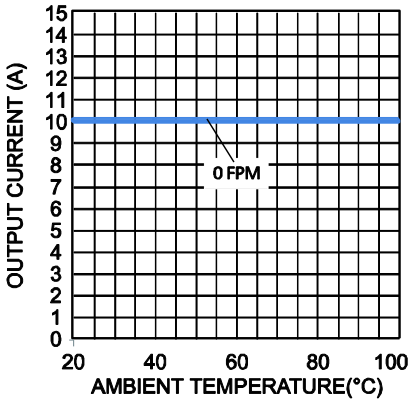
Output Current De-Rating

12V to 2.5V, 600kHz



Output Current De-Rating

12V to 5V, 600kHz



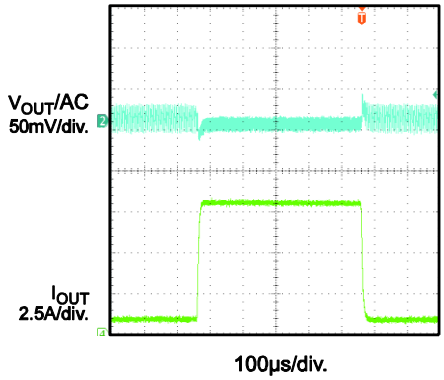
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

TYPICAL CHARACTERISTICS

V_{IN}=12V, V_{OUT}=1.2V, T_A=25˚C, unless otherwise noted.

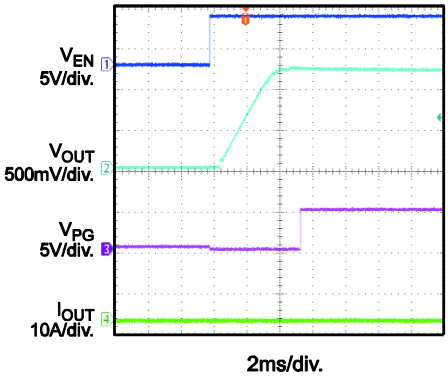
Load Transient response

I_{OUT}=1~8A @ 2.5A/μs



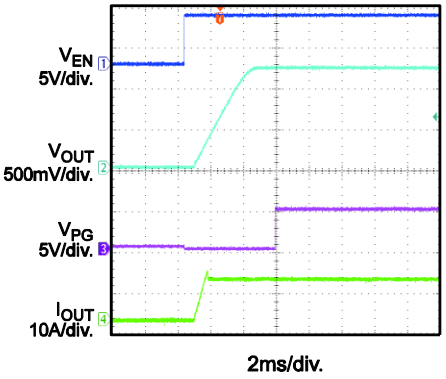
Power Up Through EN

0A



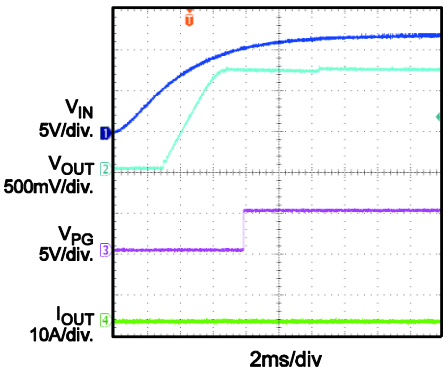
Power Up Through EN

10A



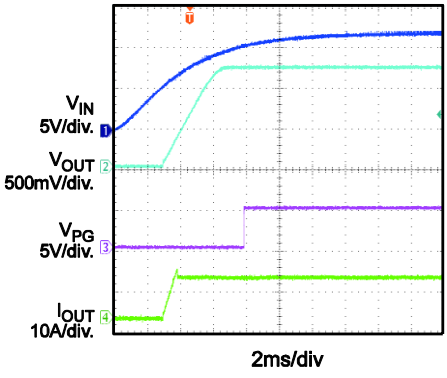
Power Up Through Input

0A



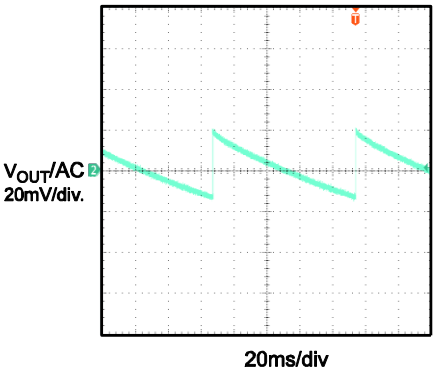
Power Up Through Input

10A



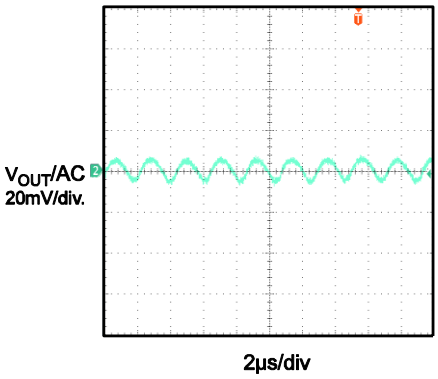
Output Ripple

0A



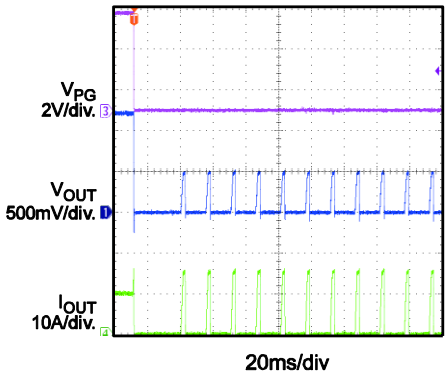
Output Ripple

10A

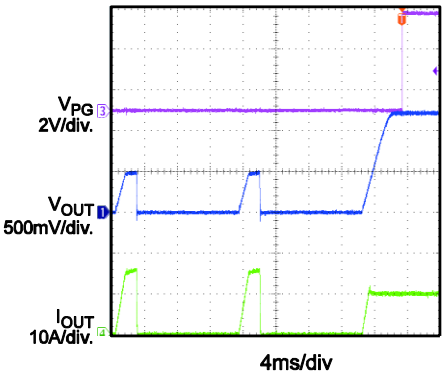


Over Current Protection

OCP

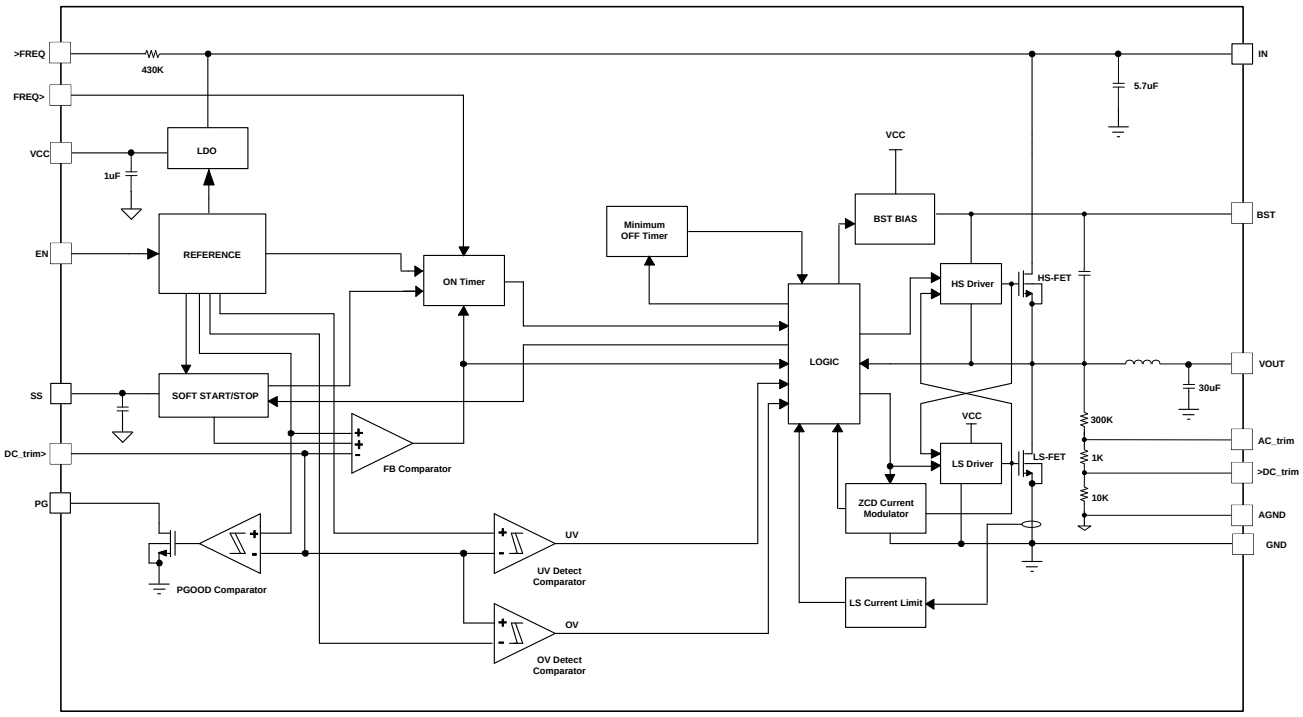


Over Current Protection Recovery



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

BLOCK DIAGRAM



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

OPERATION

Power Module Operation

The MPM3682 is a high performance single output synchronous switching mode DC-to-DC power supply. It can deliver 10A continuous output current. The MPM3682 can provide an output voltage from 0.65V to 5V over a 4.5V to 18V (or 2.5V to 18V with 5V external VCC bias) wide input voltage range.

The MPM3682 is a complete power solution. It integrates a constant-on-time (COT) control DC-to-DC regulator, power devices, an inductor, input/output capacitors and some other supporting resistors and small capacitors. It only needs as few as one external resistor and one external small capacitor to operate.

The MPM3682 is controlled by both the VCC voltage and the EN signal. It can only be turned on when both voltages are higher than the thresholds.

The switching frequency is determined by a frequency set resistor. The default switching frequency with the integrated resistor is shown in table 1. The default switching frequency increases with the output voltage. The switching frequency can also be programmed externally in the range of 200KHz to 1000KHz. The details can be found in the section of "SWITCHING FREQUENCY SETTING" on Page 12.

The MPM3682 utilizes constant-on-time control. It has sufficient stability margin with simple loop compensation. And it provides very good transient response with a wide range of output capacitors, even with all ceramic output capacitors.

The MPM3682 has a variable soft start timer to smooth-out the output voltage during start-up. The default (with SS pin floating) soft start timer is about 3ms. The soft-start time can be extended by adding a capacitor between SS pin and AGND pin.

PWM Operation

The MPM3682 uses Constant-on-time (COT) control to provide a fast transient response and ease loop stabilization.

At the beginning of each cycle, the high-side MOSFET (HS-FET) turns ON when the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}), which indicates an insufficient output voltage. The input voltage and the frequency-set resistor determine the ON period as follows:

$$T_{ON}(ns) = \frac{6.1 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \quad (1)$$

After the ON period elapses, the HS-FET turns off. It turns ON again when V_{FB} drops below V_{REF}. By repeating this operation, the converter regulates the output voltage to the desired level. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET is OFF to minimize the conduction loss. There is a dead short (or shoot-through) between input and GND if both HS-FET and LS-FET turn on at the same time. A dead-time (DT) internally generated between HS-FET OFF and LS-FETON, or LS-FET OFF and HS-FET ON avoids shoot-through.

Heavy-Load Operation

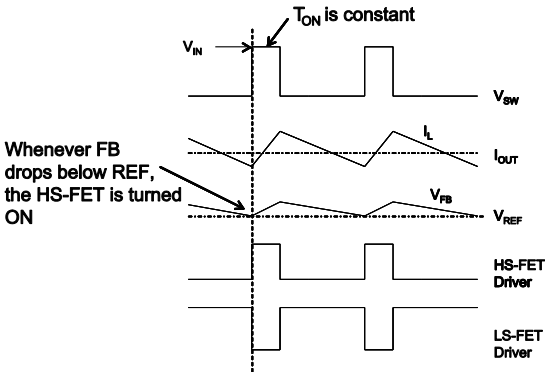


Figure 2—Heavy Load Operation

When the output current is high and the inductor current is always above zero amps, it is called continuous-conduction-mode (CCM). Figure 2 shows the CCM operation. When V_{FB} is below V_{REF}, HS-FET turns on for a fixed interval determined by the one-shot on-timer as per equation 1. When the HS-FET turns off, the LS-FET turns on until the next period.

In CCM operation, the switching frequency is fairly constant and is also called PWM mode.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

Light-Load Operation

As the load decreases, the inductor current decreases too. When the inductor current touches zero, the operation is transited from continuous-conduction-mode (CCM) to discontinuous-conduction-mode (DCM).

Figure 3 shows the light load operation. When V_{FB} drops below V_{REF}, HS-FET turns on for a fixed interval determined by the one- shot on-timer as per equation 1. When the HS-FET turns off, the LS-FET turns on until the inductor current reaches zero. In DCM operation, the V_{FB} does not reach V_{REF} when the inductor current is approaching zero. The LS-FET driver turns into tri-state (high Z) whenever the inductor current reaches zero. A current modulator takes over the control of LS-FET and limits the inductor current less than -1mA. Hence, the output capacitors discharge slowly to GND through LS-FET. As a result, this mode improves the efficiency greatly at light load condition. At this condition, the HS-FET does not turns ON as frequently as at heavy load condition. This is called pulse skip mode.

At light load or no load condition, the output drops very slowly and the MPM3682 reduces the switching frequency naturally and then achieves high efficiency at light load.

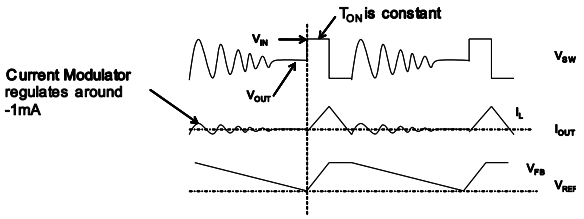


Figure 3—Light Load Operation

As the output current increases from the light load condition, the current modulator regulates the operating period that becomes shorter. The HS-FET turns ON more frequently. Hence, the switching frequency increases correspondingly. The output current reaches the critical level when the current modulator time decreases to zero. The critical output current level can be determined as follows:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_{SW} \times V_{IN}} \quad (2)$$

Where F_{SW} is the switching frequency.

The IC turns into PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Switching Frequency

Selecting the switching frequency requires trading off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductor and capacitor values to minimize the output voltage ripple.

The MPM3682 uses adaptive constant-on-time (COT) control to generate a fairly constant frequency at CCM condition, though the IC lacks a dedicated oscillator. The ON time of HSFET can be set by connecting a resistor between IN pin and FREQ pin. It's input voltage adaptive. So for a fixed output voltage, the switching frequency stays fairly constant. The switching frequency can be set internally and externally.

Figure 4 shows that the switching frequency is determined by the internal 430K resistor. The 430K resistor is connected to IN pin so that the input voltage is feed-forwarded to the one-shot ON-time timer. When operating in steady state at CCM, the duty ratio stays at V_{OUT}/V_{IN}, so the switching frequency is fairly constant over the input voltage range. The switching frequency can be determined by equation 3:

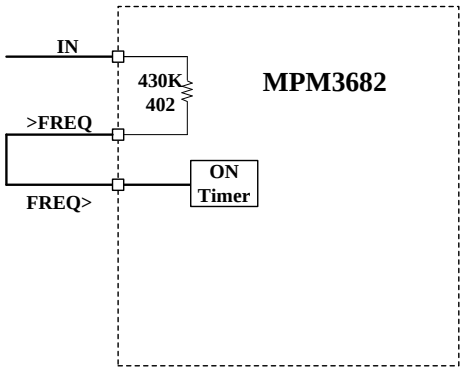


Figure 4

$$F_{SW}(kHz) = \frac{10^6}{\frac{6.1 \times 430(k\Omega)}{V_{IN}(V) - 0.4} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + T_{DELAY}(ns)} \quad (3)$$

Where T_{DELAY} is the comparator delay of about 5ns.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

Table 1 shows the switching frequency with different common output voltages:

Vo (V)	fs(KHz)
1	400
1.2	500
1.5	600
1.8	700

Table 1

If a switching frequency other than those listed in Table 1 is desired, an external frequency set resistor can be connected as shown in figure 5:

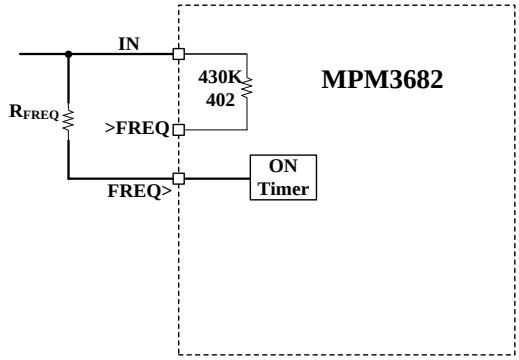


Figure 5

The switching frequency can be estimated through equation (4) as follows:

$$F_{SW}(kHz) = \frac{10^6}{\frac{6.1 \times R_{FREQ}(k\Omega)}{V_{IN}(V) - 0.4} \times \frac{V_{IN}(V)}{V_{OUT}(V)} + T_{DELAY}(ns)} \quad (4)$$

Where T_{DELAY} is the comparator delay of about 5ns.

Typically, the MPM3682 is set to 200kHz to 1MHz applications. Thanks to its monolithic structure, the MPM3682 is optimized to operate at high switching frequencies at high efficiency. High switching frequencies allow for physically smaller LC filter components to reduce the PCB footprint.

Configuring the EN Control

The power module turns on when EN goes high; conversely it turns off when EN goes low. Do not float the pin.

For automatic start-up, pull the EN pin up to input voltage through a resistive voltage divider. Choose the values of the pull-up resistor (R_{UP} from the IN pin to the EN pin) and the pull-down resistor (R_{DOWN} from the EN pin to GND) to determine the automatic start-up voltage:

$$V_{IN-START} = 1.5 \times \frac{(R_{UP} + R_{DOWN})}{R_{DOWN}}(V) \quad (5)$$

For example, for R_{UP}=100kΩ and R_{DOWN}=51kΩ, the $V_{IN-START}$ is set at 4.44V.

To reduce noise, add a 10nF ceramic capacitor from EN to GND.

An internal zener diode on the EN pin clamps the EN pin voltage to prevent running away. The maximum pull up current (assuming the worst case 6V for the internal zener clamp) should be limited to 1mA or less.

Therefore, when driving EN with an external logic signal, the driving voltage should be less than 6V. When connecting EN to IN through a pull-up resistor or a resistive voltage divider, select a resistance that ensures a maximum pull-up current of 1mA.

If using a resistive voltage divider and V_{IN} exceeds 6V, then the minimum resistance for the pull-up resistor R_{UP} should meet:

$$\frac{V_{IN} - 6V}{R_{UP}} - \frac{6V}{R_{DOWN}} \le 1mA \quad (6)$$

With only R_{UP} (the pull-down resistor, R_{DOWN}, is not connected), then the VCC UVLO threshold determines $V_{IN-START}$, so the minimum resistor value is:

$$R_{UP} \ge \frac{V_{IN} - 6V}{1mA}(\Omega) \quad (7)$$

A typical pull-up resistor is 100kΩ.

VCC Power Supply

The MPM3682 has an internal VCC LDO to supply the power to the internal circuits and drives the power devices. This VCC LDO is derived from the input supply. To ensure proper operation, the minimum input voltage should be 4.5V.

An external 5V VCC bias can disable the internal LDO. In this case, Vin can be as low as 2.5V. The efficiency can be higher with external 5V VCC bias. Figure 6 shows the comparison.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

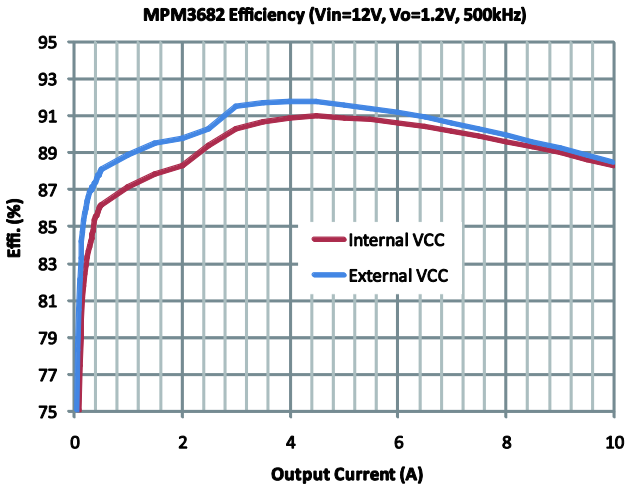


Figure 6

Soft Start

The MPM3682 employs a soft start (SS) mechanism to ensure a smooth output during power-up. When the EN pin goes high, an internal current source (20μA) charges the SS capacitor. The SS capacitor voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches the REF voltage, it continues ramping up while V_{REF} takes over the PWM comparator. At this point, soft start finishes and the device enters steady state operation.

An internal 100nF SS capacitor is used. So the default (with SS pin floating) SS time can be estimated as:

$$T_{SS}(ms) = \frac{100(nF) \times V_{REF}(V)}{I_{SS}(uA)} \quad (8)$$

So the default SS time is about 3ms.

If longer SS time is needed, an external SS capacitor can be added between SS pin and AGND pin. The external capacitor value can be determined as follows:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(uA)}{V_{REF}(V)} - 100(nF) \quad (9)$$

Pre-Bias Startup

The MPM3682 has been designed for monotonic startup into pre-biased loads. If the output is pre-biased to a certain voltage during startup, the IC will disable switching for both high-side and low-side switches until the voltage on the soft-start capacitor exceeds the sensed output voltage at the FB pin.

Power Good (PG)

The MPM3682 has a power-good (PG) output. The PG pin is the open drain of a MOSFET. Connect it to VCC or some other voltage source that measures less than 5.5V through a pull-up resistor (typically 100kΩ). After applying the input voltage, the MOSFET turns on so that the PG pin is pulled to GND before the SS is ready. After the FB voltage reaches 91% of the REF voltage, the PG pin is pulled high after a 2.5ms delay.

When the FB voltage drops to 80% of the REF voltage or exceeds 120% of the nominal REF voltage, the PG pin is pulled low.

If the input supply fails to power the MPM3682, the PG pin is also pulled low even though this pin is tied to an external DC source through a pull-up resistor.

Over-Current Protection (OCP)

The MPM3682 features two current limit levels for over-current conditions: low-side valley current limit and low-side negative current limit.

Low-Side Valley Current Limit: The device monitors the inductor current during the LS-FET ON state. If the LS-FET sourcing current is higher than the internal positive-valley-current limit, the HS-FET remains OFF and the LS-FET remains ON for the next ON time. When the LS-FET sourcing current drops below the valley current limit, then the LS-FET turns off and the HS-FET turns on again.

The MPM3682 enters OCP non-latch protection mode if the LS-FET sourcing valley current keeps exceeding the valley current limit for a certain period of time. During OCP, the device tries to recover from the over-current fault with hiccup mode: the chip disables the output power stage, discharges the soft-start capacitor and then automatically retries soft-start. The device repeats this operation cycle as long as the over-current condition still exists. When the over-current condition disappears, the MPM3682 initiates a new SS to rise back to regulation level.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

Low-Side Negative Current Limit: If the sensed LS-FET negative current exceeds the negative current limit, the LS-FET turns off immediately and stays OFF for the remainder of the OFF period. In this situation, both MOSFETs are OFF until the end of a fixed interval. The HS-FET body diode conducts the inductor current for the fixed time.

Over -Voltage Protection (OVP)

The MPM3682 monitors the output voltage using the FB pin connected to the tap of a resistor divider to detect over-voltage. It provides non-latch OVP mode.

If the FB voltage exceeds the nominal REF voltage but remains lower than 120% of the REF voltage (0.611V), both MOSFETs are off.

If the FB voltage exceeds 120% of the REF voltage but remains below 130%, the LS-FET turns on while the HS-FET remains off. The LS-FET remains on until the FB voltage drops below 110% of the REF voltage or the low-side negative current limit is hit.

If the FB voltage exceeds 130% of the REF voltage, it enters a non-latch mode. The LS-FET remains on until the FB voltage drops below 110% of the REF voltage, and the MPM3682 initiates a new SS to rise back to regulation level and operates normally again.

UVLO protection

The MPM3682 has under-voltage lock-out protection (UVLO). When the VCC voltage exceeds the UVLO rising threshold, the MPM3682 powers up. It shuts off when the VCC voltage falls below the UVLO falling threshold voltage. This is non-latch protection. The MPM3682 is disabled when the VCC voltage falls below 3.3 V. If an application requires a higher UVLO threshold, use the two external resistors connected to the EN pin as shown in Figure 9 to adjust the startup input voltage. For best results, use the enable resistors to set the input voltage falling threshold (V_{STOP}) above 3.6 V. Set the rising threshold (V_{START}) to provide enough hysteresis to account for any input supply variations.

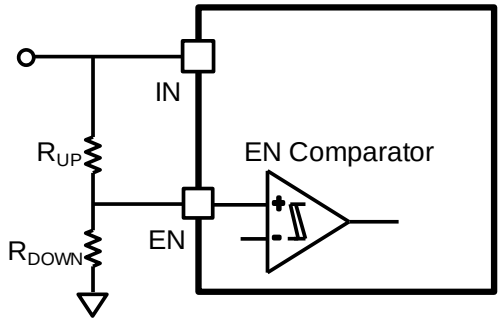


Figure 7—Adjustable UVLO Threshold

Thermal Shutdown

The MPM3682 has thermal shutdown. The IC internally monitors the junction temperature. If the junction temperature exceeds the threshold value (minimum 150ºC), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 125ºC, it initiates a soft startup.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage-Small ESR Capacitors

When the output capacitors are all ceramic capacitors or capacitors with small ESR, external RAMP is injected through the R/C network across the inductor. The circuit connection is as follows:

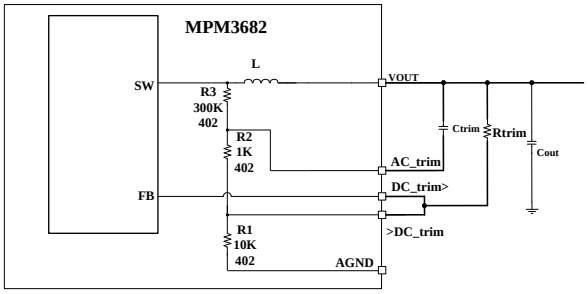


Figure 8

Here is the procedure to find the values for Ctrim and Rtrim:

a) Determine the Ton

$$T_{ON}(ns) = \frac{5.3 \times R_{FREQ}(K\Omega)}{V_{IN}(V) - 0.4} \quad (10)$$

b) Determine Ctrim. Choose a V_{RAMP} around 10mV-30mV for most of the applications.

$$C_{TRIM}(pF) = \frac{V_{IN}(V) - V_{OUT}(V)}{R_3(K\Omega) \times V_{RAMP}(V)} \times T_{ON}(ns) \quad (11)$$

c) Find the average feedback voltage V_{FB}

$$V_{FB_AVG}(V) = V_{REF}(V) + \frac{V_{RAMP}(V)}{2} \quad (12)$$

d) Calculate Rtrim to get the desired output voltage:

$$R_o(K\Omega) = (\frac{V_{OUT}(V)}{V_{FB_AVG}(V)} - 1) \times 10(K\Omega) \quad (13)$$

$$R_{TRIM}(K\Omega) = \frac{R_O(K\Omega) \times 300(K\Omega)}{300(K\Omega) - R_O(K\Omega)} \quad (14)$$

Setting the Output Voltage-Large ESR Capacitors

If one or more piece of the output capacitors have large ESR, then there is no need of external RAMP. Otherwise, it'll generate group pulses atlight load conditions. The Ctrim is still recommended to boost the phase margin of the system. A value between 100pF and 2.2nF is recommended. The circuit connection can be made as the following:

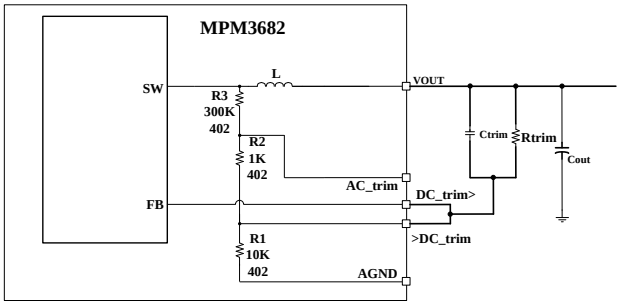


Figure 9

The Rtrim can be determined as follows to obtain the desired output voltage:

$$R_{TRIM}(K\Omega) = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times 10 \quad (15)$$

Input Capacitor

The input current to the step-down power module is discontinuous, and therefore, it requires a capacitor to supply the AC current to the step-down power module while maintaining the DC input voltage. Use ceramic capacitors for best performance. During layout, Place the input capacitors as close to the IN and GND pins as possible.

The capacitance can vary significantly with temperature. Use capacitors with X5R or X7R ceramic dielectrics because they are fairly stable over a wide temperature range.

The capacitors must also have a ripple current rating that exceeds the converter's maximum input ripple current. Estimate the input ripple current as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (16)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (17)$$

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

For simplification, choose an input capacitor with an RMS current rating that exceeds half the maximum load current.

The input capacitance value determines the converter input voltage ripple. Select a capacitor value that meets any input voltage ripple requirements.

Estimate the input voltage ripple as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (18)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (19)$$

PCB Layout Recommendations

1. Place the input/output capacitors on the same side of the MPM3682, and as close to the MPM3682 package as possible.

2. A solid system ground layer is required to be placed immediately below the surface layer with the MPM3682.

3. Thermal VIAs (18 mil diameter and 8 mil hole size) are required to be placed underneath the GND, IN and VOUT pads, as well as the edges of the MPM3682 and the input/output capacitors.

4. Keep the DC_trim traces as short as possible.

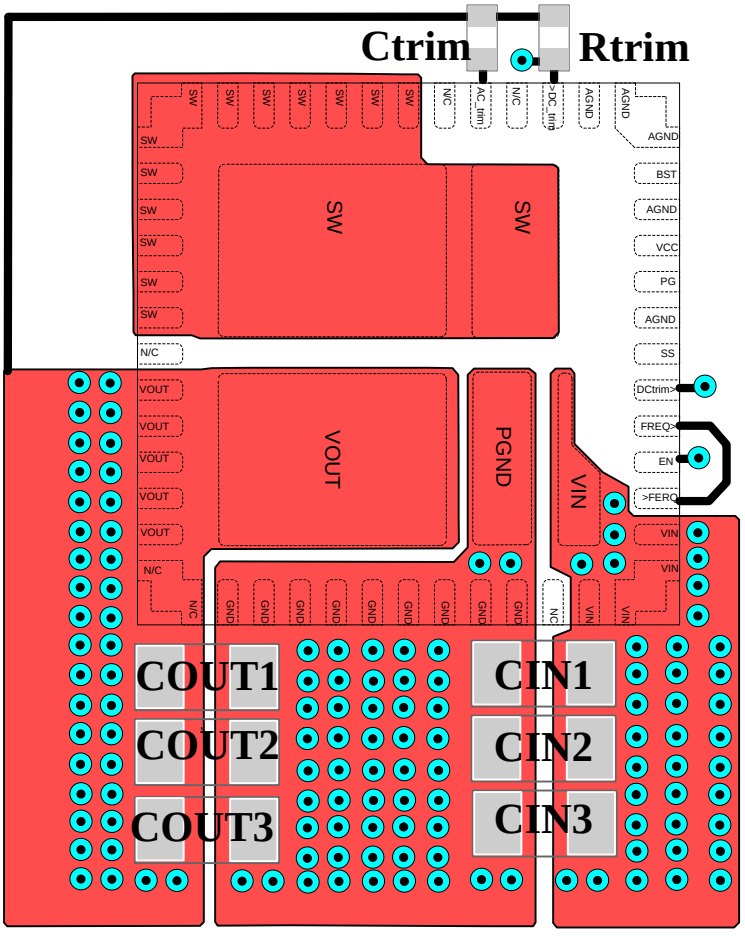


Figure 10

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

Typical Design Parameter Table

The following table (Table 2) includes the recommended component values for typical designs.

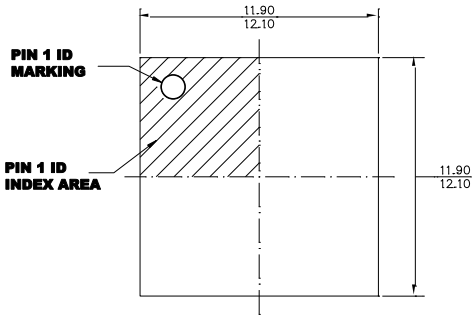
Ref	Vin (V)	Vout (V)	Rtrim (KΩ)	Ctrim (pF)	Rfreq (KΩ)	fs (KHz)	Cout (uF)	Ripple (mV)
1	12	1	6.49	560	NS	400	5X47	11.6
2	12	1	6.49	560	NS	400	3X47	16.4
3	12	1	6.49	560	300	600	5X47	5.0
4	12	1	6.49	560	300	600	3X47	7.6
5	12	1	6.49	220	178	1000	3X47	3.8
6	12	1	6.49	330	178	1000	5X47	2.2
7	12	1.2	10	560	649	300	5X47	24.0
8	12	1.2	10	560	649	300	3X47	38.4
9	12	1.2	10	560	NS	500	5X47	11.2
10	12	1.2	10	560	NS	500	3X47	14.8
11	12	1.2	10	270	200	1000	5X47	3.2
12	12	1.2	10	270	200	1000	3X47	4.6
13	12	1.5	15	680	806	300	5X47	32.8
14	12	1.5	15	680	806	300	3X47	46.0
15	12	1.5	15	560	NS	600	5X47	8.4
16	12	1.5	15	560	NS	600	3X47	11.6
17	12	1.5	15.8	330	243	1000	5X47	5.8
18	12	1.5	15.8	330	243	1000	3X47	7.0
19	12	1.8	21	560	750	400	5X47	25.4
20	12	1.8	21	560	750	400	3X47	49.6
21	12	1.8	21	560	NS	750	5X47	7.6
22	12	1.8	21	560	NS	750	3X47	9.4
23	12	1.8	21	470	301	1000	5X47	8.8
24	12	1.8	21	330	301	1000	3X47	12.4
25	12	2.5	34	680	1000	400	5X47	34.2
26	12	2.5	34	680	1000	400	3X47	46.4
27	12	2.5	35.7	680	698	600	5X47	18.8
28	12	2.5	35.7	680	715	600	3X47	25.2
29	12	2.5	34	330	432	1000	5X47	9.8
30	12	2.5	34	270	432	1000	3X47	13.0
33	12	3.3	49.9	330	909	600	5X47	31.6
34	12	3.3	49.9	330	909	600	7X47	21.2
35	12	3.3	49.9	270	549	1000	5X47	6.0
36	12	3.3	49.9	270	549	1000	3X47	10.2
39	12	5	90.9	390	1350	600	5X47	49.2
40	12	5	90.9	390	1350	600	7X47	36.0
41	12	5	90.9	180	909	1000	5X47	20.8
42	12	5	90.9	150	909	1000	3X47	28.8

Table 2: Typical Design Examples

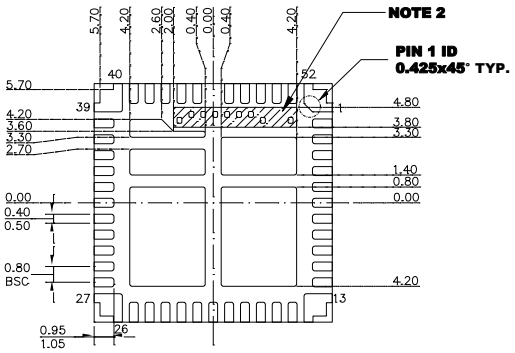
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.

PACKAGE INFORMATION

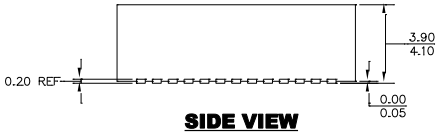
QFN-57 (12mmx12mmx4mm)



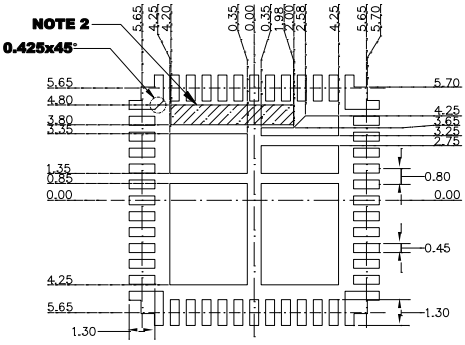
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) SHADED AREA IS THE KEEP-OUT ZONE. ANY PCB METAL TRACE AND VIA ARE NOT ALLOWED TO CONNECT TO THIS AREA ELECTRICALLY OR MECHANICALLY.
3) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
4) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-220.
6) DRAWING IS NOT TO SCALE.

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2016 MPS. All Rights Reserved.