Data Sheet
April 2012

DS3106
Line Card Timing IC

General Description

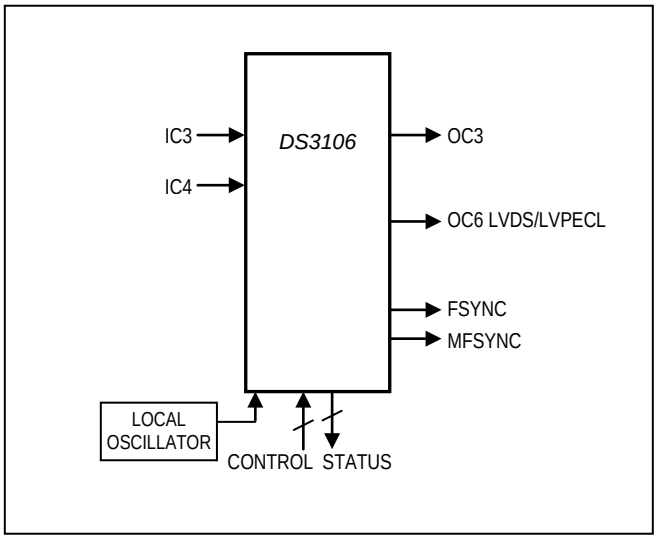
The DS3106 is a low-cost timing IC for telecom line cards. The device accepts two reference clocks from dual redundant system timing cards, continually monitors both inputs, and performs manual reference switching if the primary reference fails. The highly programmable DS3106 supports numerous input and output frequencies including frequencies required for SONET/SDH, Synchronous Ethernet (1G, 10G, and 100Mbps), wireless base stations, and CMTS systems. PLL bandwidths from 18Hz to 400Hz are supported, and a wide variety of PLL characteristics and device features can be configured to meet the needs of many different applications.

The DS3106 register set is backward compatible with Semtech's ACS8526 line card timing IC. The DS3106 pinout is similar but not identical to the ACS8526.

Applications

SONET/SDH, Synchronous Ethernet, PDH, and Other Line Cards in WAN Equipment Including MSPPs, Ethernet Switches, Routers, DSLAMs, and Wireless Base Stations

Simplified Functional Diagram



Features

- **Advanced DPLL Technology**
  - Programmable PLL Bandwidth: 18Hz to 400Hz
  - Manual Reference Switching
  - Holdover on Loss of All Input References
  - Frequency Conversion Among SONET/SDH, PDH, Ethernet, Wireless, and CMTS Rates
- **Two Input Clocks**
  - CMOS/TTL Signal Format (≤ 125MHz)
  - Numerous Input Clock Frequencies Supported
    Ethernet xMII: 2.5, 25, 125, 156.25MHz
    SONET/SDH: 6.48, N x 19.44, N x 51.84MHz
    PDH: N x DS1, N x E1, N x DS2, DS3, E3
    Frame Sync: 2kHz, 4kHz, 8kHz
    Custom Clock Rates: Any Multiple of 2kHz Up to 125MHz
- **Two Output Clocks**
  - One CMOS/TTL Output (≤ 125MHz)
  - One LVDS/LVPECL Output (≤ 312.50MHz)
  - Two Optional Frame-Sync Outputs: 2kHz, 8kHz
  - Numerous Output Clock Frequencies Supported
    Ethernet xMII: 2.5, 25, 125, 156.25, 312.5MHz
    SONET/SDH: 6.48, N x 19.44, N x 51.84MHz
    PDH: N x DS1, N x E1, N x DS2, DS3, E3
    Other: 10, 10.24, 13, 30.72MHz
    Frame Sync: 2kHz, 8kHz
    Custom Clock Rates: Any Multiple of 2kHz Up to 77.76MHz, Any Multiple of 8kHz Up to 311.04MHz, Any Multiple of 10kHz Up to 388.79MHz
- **General**
  - Suitable Line Card IC for Stratum 3/3E/4, SMC, SEC
  - Internal Compensation for Master Clock Oscillator
  - SPI™ Processor Interface
  - 1.8V Operation with 3.3V I/O (5V Tolerant)
  - Industrial Operating Temperature Range

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS3106LN	-40°C to +85°C	64 LQFP
DS3106LN+	-40°C to +85°C	64 LQFP

+Denotes a lead(Pb)-free/RoHS-compliant package.

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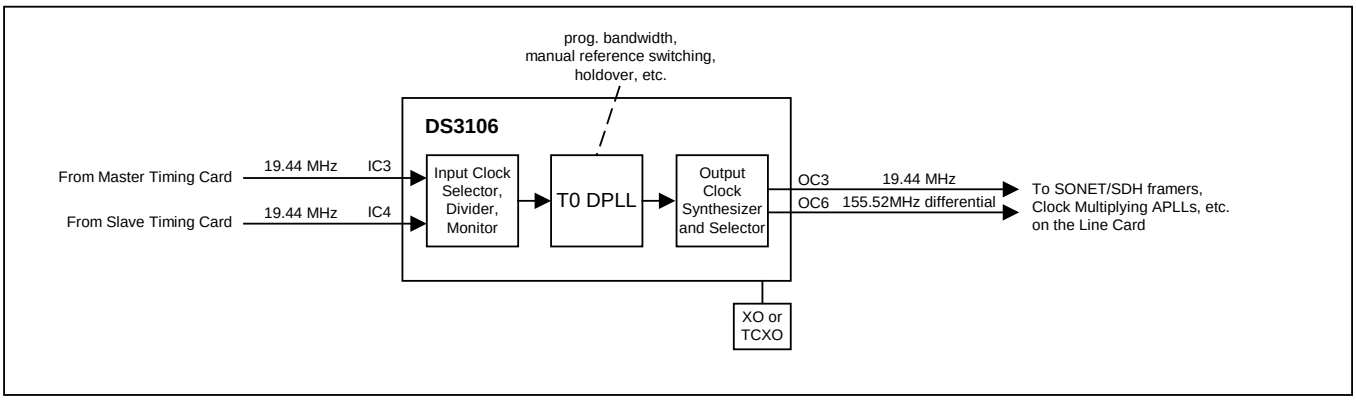
1. Standards Compliance

Table 1-1. Applicable Telecom Standards

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.101	*Synchronization Interface Standard*, 1999
TIA/EIA-644-A	*Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits,* 2001
ETSI	
EN 300 417-6-1	*Transmission and Multiplexing (TM); Generic requirements of transport functionality of equipment; Part 6-1: Synchronization layer functions*, v1.1.3 (1999-05)
EN 300 462-3-1	*Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 3-1: The control of jitter and wander within synchronization networks*, v1.1.1 (1998-05)
EN 300 462-5-1	*Transmission and Multiplexing (TM); Generic requirements for synchronization networks; Part 5-1: Timing characteristics of slave cocks suitable for operation in Synchronous Digital Hierarchy (SDH) Equipment*, v1.1.2 (1998-05)
IEEE	
IEEE 1149.1	*Standard Test Access Port and Boundary-Scan Architecture*, 1990
ITU-T	
G.783	*Characteristics of synchronous digital hierarchy (SDH) equipment functional blocks* (10/2000 plus Amendment 1 06/2002 and Corrigendum 2 03/2003)
G.813	*Timing characteristics of SDH equipment slave clocks (SEC)* (03/2003)
G.823	*The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy* (03/2000)
G.824	*The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy* (03/2000)
G.825	*The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH)* (03/2000)
G.8261	*Timing and synchronization aspects in packet networks* (05/2006, prepublished)
G.8262	*Timing characteristics of synchronous Ethernet equipment slave clock (EEC)* (08/2007, prepublished)
TELCORDIA	
GR-253-CORE	*SONET Transport Systems: Common Generic Criteria*, Issue 3, September 2000
GR-1244-CORE	*Clocks for the Synchronized Network: Common Generic Criteria,* Issue 2, December 2000

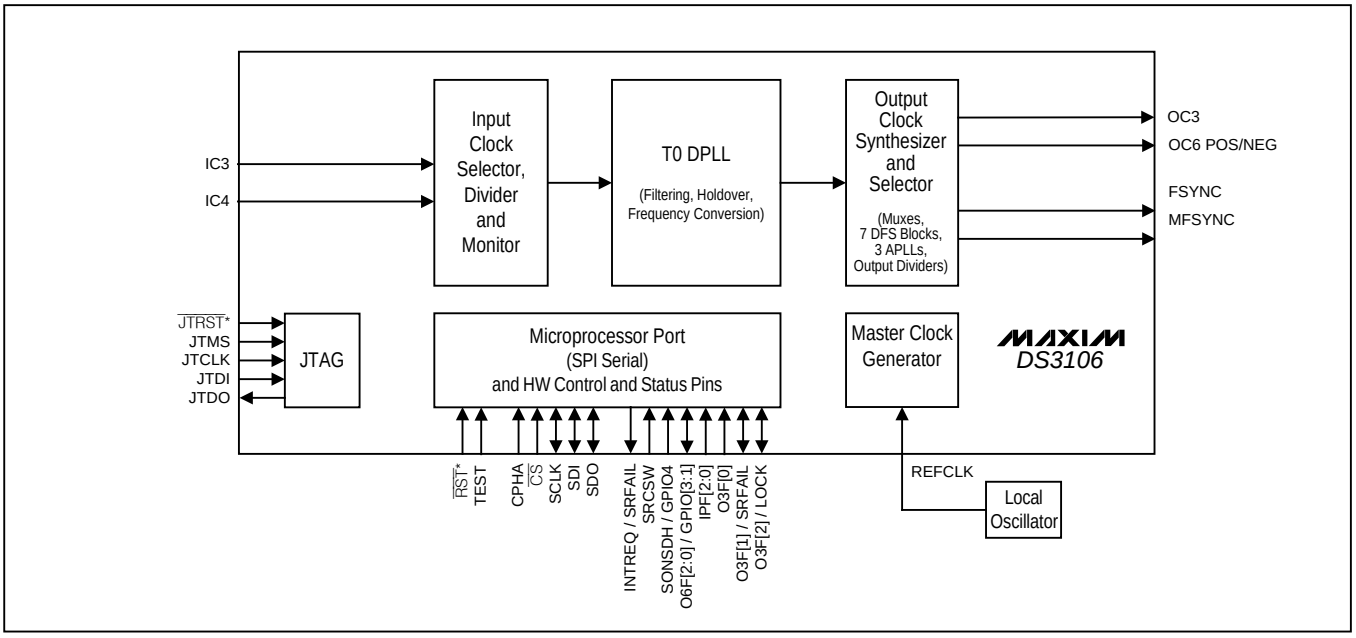
2. Application Example

Figure 2-1. Typical Application Example



3. Block Diagram

Figure 3-1. Block Diagram



4. Detailed Description

Figure 3-1 illustrates the blocks described in this section and how they relate to one another. Section 5 provides a detailed feature list.

The DS3106 is a complete line card timing IC. At the core of this device is a digital phase-locked loop (DPLL). DPLL technology makes use of digital-signal processing (DSP) and digital-frequency synthesis (DFS) techniques to implement PLLs that are precise, flexible, and have consistent performance over voltage, temperature, and manufacturing process variations. The DS3106's T0[1] DPLL is digitally configurable for input and output frequencies, loop bandwidth, damping factor, pull-in/hold-in range, and a variety of other factors. The T0 DPLL can directly lock to many common telecom frequencies and also can lock at 8kHz to any multiple of 8kHz up to 156.25MHz. The DPLL can also tolerate and filter significant amounts of jitter and wander.

In typical line card applications, the T0 DPLL takes reference clock signals from two redundant system timing cards, monitors both, selects one, and uses that reference to produce a variety of clocks that are needed to time the outgoing traffic interfaces of the line card (SONET/SDH, Synchronous Ethernet, etc.). To perform this role in a variety of systems with diverse performance requirements, the T0 DPLL has a sophisticated feature set and is highly configurable. T0 can automatically transition among free-run, locked, and holdover states without software intervention. In free-run, T0 generates a stable, low-noise clock with the same frequency accuracy as the external oscillator connected to the REFCLK pin. With software calibration the DS3106 can even improve the accuracy to within ±0.02ppm. When the selected input reference clock has been validated, T0 transitions to the locked state in which its output clock accuracy is equal to the accuracy of the input reference. While in the locked state, T0 acquires an average frequency value to use as the holdover frequency. When its selected reference fails, T0 can very quickly detect the failure and enter the holdover state to avoid affecting its output clock. From holdover it can be manually switched to another input reference. When all input references are lost, T0 stays in the holdover state, in which it generates a stable low-noise clock with initial frequency accuracy equal to its stored holdover value and drift performance determined by the quality of the external oscillator.

At the front end of the T0 DPLL is the Input Clock Selector, Divider, and Monitor (ICSDM) block. This block continuously monitors both input clocks for activity and coarse frequency accuracy. In addition, ICSDM can manually select one of the input clocks to be the selected reference for the T0 DPLL. The ICSDM block can also divide the selected clock down to a lower rate as needed by the DPLL.

The Output Clock Synthesizer and Selector (OCSS) block shown in Figure 3-1 and in more detail in Figure 7-1 contains three output APLLs—T0 APLL, T0 APLL2, and T4 APLL—and their associated DFS engines and output divider logic plus several additional DFS engines. The APLL DFS blocks perform frequency translation, creating clocks of other frequencies that are phase/frequency locked to the output clock of the T0 DPLL. The APLLs multiply the clock rates from the APLL DFS blocks and simultaneously attenuate jitter. Altogether the output blocks of the DS3106 can produce more than 90 different output frequencies including common SONET/SDH, PDH, and Synchronous Ethernet rates plus 2kHz and 8kHz frame-sync pulses.

The entire chip is clocked from the external oscillator connected to the REFCLK pin. Thus, the free-run and holdover stability of the DS3106 is entirely a function of the stability of the external oscillator, the performance of which can be selected to match the application: typically XO or TCXO. The 12.8MHz clock from the external oscillator is multiplied by 16 by the Master Clock Generator block to create the 204.8MHz master clock used by the remainder of the device.

[1] The labels T0 and T4 in this document are adapted from output ports of the SETS function specified in ITU-T and ETSI standards such as ETSI EN 300 462-2-1. Although strictly speaking these names are appropriate only for timing card ICs such as the DS3100 that can serve as the SETS function, the names have been carried over to the DS3106 so that all of the products in Maxim's timing IC product line have consistent nomenclature.

5. Detailed Features

5.1 Input Clock Features

- Two programmable-frequency CMOS/TTL input clocks
- Input clocks accept any multiple of 2kHz up to 125MHz
- All input clocks are constantly monitored by programmable activity monitors

5.2 DPLL Features

- High-resolution DPLL plus three low-jitter output APLLs
- Sophisticated state machine automatically transitions between free-run, locked, and holdover states
- Programmable bandwidth from 18Hz to 400Hz
- Separately configurable acquisition bandwidth and locked bandwidth
- Programmable damping factor to balance lock time with peaking: 1.2, 2.5, 5, 10, or 20
- Multiple phase detectors: phase/frequency, early/late, and multicycle
- Phase/frequency locking (±360° capture) or nearest edge phase locking (±180° capture)
- Multicycle phase detection and locking (up to ±8191UI) improves jitter tolerance and lock time
- High-resolution frequency and phase measurement
- Holdover frequency averaging over 1 second interval
- Fast detection of input clock failure and transition to holdover mode
- Low-jitter frame sync (8kHz) and multiframe sync (2kHz) aligned with output clocks

5.3 Output APLL Features

- Three separate clock-multiplying, jitter attenuating APLLs can simultaneously produce SONET/SDH rates, Fast/Gigabit Ethernet rates, and 10G Ethernet rates, all locked to a common reference clock
- The T0 APLL has frequency options suitable for N x 19.44MHz, N x DS1, N x E1, N x 25MHz, and N x 62.5MHz
- The T4 APLL has frequency options suitable for N x 19.44MHz, N x DS1, N x E1, N x DS2, DS3, E3, N x 10MHz, N x 10.24MHz, N x 13MHz, N x 25MHz, and N x 62.5MHz
- The T0 APLL2 produces 312.5MHz for 10G Synchronous Ethernet applications

5.4 Output Clock Features

- Two output clocks: one CMOS/TTL (≤ 125MHz) and one LVDS/LVPECL (≤ 312.50MHz)
- Output clock rates include 2kHz, 8kHz, N x DS1, N x E1, DS2, DS3, E3, 6.48MHz, 19.44MHz, 38.88MHz, 51.84MHz, 77.76MHz, 155.52MHz, 311.04MHz, 2.5MHz, 25MHz, 125MHz, 156.25MHz, 312.50MHz, 10MHz, 10.24MHz, 13MHz, 30.72MHz, and various multiples and submultiples of these rates
- Custom clock rates also available: any multiple of 2kHz up to 77.76MHz, any multiple of 8kHz up to 311.04MHz, and any multiple of 10kHz up to 388.79MHz
- All outputs have < 1ns peak-to-peak output jitter; outputs from APLLs have < 0.5ns peak-to-peak
- 8kHz frame-sync and 2kHz multiframe-sync outputs have programmable polarity and pulse width, and can be disciplined by a 2kHz or 8kHz sync input

5.5 General Features

- Operates from a single external 12.800MHz local oscillator (XO or TCXO)
- SPI serial microprocessor interface
- Four general-purpose I/O pins
- Register set can be write protected

6. Pin Descriptions

Table 6-1. Input Clock Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
REFCLK	I	**Reference Clock.** Connect to a 12.800MHz, high-accuracy, high-stability, low-noise local oscillator (XO or TCXO). See Section 7.3.
IC3	I_{PD}	**Input Clock 3.** CMOS/TTL. Programmable frequency. Default frequency selected by IPF[2:0] pins when the $\overline{RST}$ pin goes high, 8kHz if IPF[2:0] pins left open.
IC4	I_{PD}	**Input Clock 4.** CMOS/TTL. Programmable frequency. Default frequency selected by IPF[2:0] pins when the $\overline{RST}$ pin goes high, 8kHz if IPF[2:0] pins left open.

Table 6-2. Output Clock Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
OC3	O	**Output Clock 3.** CMOS/TTL. Programmable frequency. Default frequency selected by O3F[2:0] pins when the $\overline{RST}$ pin goes high, 19.44MHz if O3F[2:0] pins left open. See Table 7-17.
OC6POS, OC6NEG	O_{DIFF}	**Output Clock 6.** LVDS/LVPECL. Programmable frequency. Default frequency selected by O6F[2:0] pins when the $\overline{RST}$ pin goes high, 38.88MHz if O6F[2:0] pins left open. The output mode is selected by MCR8.OC6SF[1:0]. See Table 10-4, Table 10-5, Figure 10-1, and Figure 10-2.
FSYNC	O_3	**8kHz FSYNC.** CMOS/TTL. 8kHz frame sync or clock (default 50% duty cycle clock, noninverted). The pulse polarity and width are selectable using FSCR1.8KINV and FSCR1.8KPUL.
MFSYNC	O_3	**2kHz MFSYNC.** CMOS/TTL. 2kHz frame sync or clock (default 50% duty cycle clock, noninverted). The pulse polarity and width are selectable using FSCR1.2KINV and FSCR1.2KPUL.

Table 6-3. Global Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
$\overline{RST}$	I_{PU}	**Reset (Active Low).** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as $\overline{RST}$ is low. $\overline{RST}$ should be held low for at least two REFCLK cycles after the external oscillator has stabilized and is providing valid clock signals.
SRCSW	I_{PD}	**Source Switching.** Input reference selection pin. Selects IC3 when high and IC4 when low. See Section 7.6.
TEST	I_{PD}	**Factory Test Mode Select.** Wire this pin to VSS for normal operation.
IPF0	I_{PD}	**Input Frequency Select 0.** Together with IPF1 and IPF2, this pin sets the default frequency of the IC3 and IC4 input clock pins. The value is sampled when $\overline{RST}$ goes high, and the FREQ[3:0] fields of ICR3 and ICR4 are set accordingly. See Table 7-2. After $\overline{RST}$ goes high this pin is ignored.
IPF1	I_{PD}	**Input Frequency Select 1.** Together with IPF0 and IPF2, this pin sets the default frequency of the IC3 and IC4 input clock pins. The value is sampled when $\overline{RST}$ goes high, and the FREQ[3:0] fields of ICR3 and ICR4 are set accordingly. See Table 7-2. After $\overline{RST}$ goes high this pin is ignored.
IPF2	I_{PD}	**Input Frequency Select 2.** Together with IPF0 and IPF1, this pin sets the default frequency of the IC3 and IC4 input clock pins. The value is sampled when $\overline{RST}$ goes high, and the FREQ[3:0] fields of ICR3 and ICR4 are set accordingly. See Table 7-2. After $\overline{RST}$ goes high this pin is ignored.
O3F0	I_{PU}	**OC3 Frequency Select 0.** This pin is sampled when the $\overline{RST}$ pin goes high and the value is used as O3F0, which, together with O3F2 and O3F1, sets the default frequency of the OC3 output clock pin. See Table 7-17. After $\overline{RST}$ goes high this pin is ignored.
O3F1/SRFAIL	IO_{PU}	**OC3 Frequency Select 1/SRFAIL Status Pin.** This pin is sampled when the $\overline{RST}$ pin goes high and the value is used as O3F1, which, together with O3F2 and O3F0, sets the default frequency of the OC3 output clock pin. See Table 7-17. After $\overline{RST}$ goes high, if MCR10:SRFPIN = 1, this pin follows the state of the SRFAIL status bit in the MSR2 register. This gives the system a very fast indication of the failure of the selected reference. When MCR10:SRFPIN = 0, SRFAIL is disabled (high impedance).
O3F2/LOCK	IO_{PD}	**OC3 Frequency Select 2/T0 DPLL LOCK Status.** This pin is sampled when the $\overline{RST}$ pin goes high and the value is used as O3F2, which, together with O3F1 and O3F0, sets the default frequency of the OC3 output clock pin. See Table 7-17. After $\overline{RST}$ goes high, if MCR1.LOCKPIN = 1, this pin indicates the lock state of the T0 DPLL. When MCR1.LOCKPIN = 0, LOCK is disabled (low). 0 = Not locked 1 = Locked
O6F0/GPIO1	IO_{PD}	**OC6 Frequency Select 0/General-Purpose I/O Pin 1.** This pin is sampled when the $\overline{RST}$ pin goes high and the value is used as O6F0, which, together with O6F2 and O6F1, sets the default frequency of the OC6 output clock pin. See Table 7-16. After $\overline{RST}$ goes high, this pin can be used as a general-purpose I/O pin. GPCR:GPIO1D configures this pin as an input or an output. GPCR:GPIO1O specifies the output value. GPSR:GPIO1 indicates the state of the pin.
O6F1/GPIO2	IO_{PD}	**OC6 Frequency Select 1/General-Purpose I/O Pin 2.** This pin is sampled when the $\overline{RST}$ pin goes high and the value is used as O6F1, which, together with O6F2 and O6F0, sets the default frequency of the OC6 output clock pin. See Table 7-16. After $\overline{RST}$ goes high, this pin can be used as a general-purpose I/O pin. GPCR:GPIO2D configures this pin as an input or an output. GPCR:GPIO2O specifies the output value. GPSR:GPIO2 indicates the state of the pin.
O6F2/GPIO3	IO_{PU}	**OC6 Frequency Select 2/General-Purpose I/O Pin 3.** This pin is sampled when the $\overline{RST}$ pin goes high and the value is used as O6F2, which, together with O6F1 and O6F0, sets the default frequency of the OC6 output clock pin. See Table 7-16. After $\overline{RST}$ goes high, this pin can be used as a general-purpose I/O pin. GPCR:GPIO3D configures this pin as an input or an output. GPCR:GPIO3O specifies the output value. GPSR:GPIO3 indicates the state of the pin.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
SONSDH/ GPIO4	IO_{PD}	**SONET/SDH Frequency Select Input/General-Purpose I/O 4.** When $\overline{RST}$ goes high the state of this pin sets the reset-default state of MCR3:SONSDH, MCR6:DIG1SS, and MCR6:DIG2SS. After $\overline{RST}$ goes high, this pin can be used as a general-purpose I/O pin. GPCR:GPIO4D configures this pin as an input or an output. GPCR:GPIO4O specifies the output value. GPSR:GPIO4 indicates the state of the pin. Reset latched values: 0 = SDH rates (N x 2.048MHz) 1 = SONET rates (N x 1.544MHz)
INTREQ/LOS	O_3	**Interrupt Request/Loss of Signal.** Programmable (default: INTREQ). The INTCR:LOS bit determines whether the pin indicates interrupt requests or loss of signal (i.e., loss of selected reference). **INTCR:LOS = 0: INTREQ mode** The behavior of this pin is configured in the INTCR register. Polarity can be active high or active low. Drive action can be push-pull or open drain. The pin can also be configured as a general-purpose output if the interrupt request function is not needed. **INTCR:LOS = 1: LOS mode** This pin indicates the real-time state of the selected reference activity monitor (see Section 7.5.3).

Table 6-4. SPI Bus Mode Pin Descriptions

See Section 7.9 for functional description and Section 10.4 for timing specifications.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
$\overline{CS}$	I_{PU}	**Chip Select.** This pin must be asserted (low) to read or write internal registers.
SCLK	I	**Serial Clock.** SCLK is always driven by the SPI bus master.
SDI	I	**Serial Data Input.** The SPI bus master transmits data to the device on this pin.
SDO	O	**Serial Data Output.** The device transmits data to the SPI bus master on this pin.
CPHA	I	**Clock Phase.** See Figure 7-4. 0 = Data is latched on the leading edge of the SCLK pulse. 1 = Data is latched on the trailing edge of the SCLK pulse.

Table 6-5. JTAG Interface Pin Descriptions

See Section 9 for functional description and Section 10.5 for timing specifications.

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
$\overline{JTRST}$	I_{PU}	**JTAG Test Reset (Active Low).** Asynchronously resets the test access port (TAP) controller. If not used, $\overline{JTRST}$ can be held low or high.
JTCLK	I	**JTAG Clock.** Shifts data into JTDI on the rising edge and out of JTDO on the falling edge. If not used, JTCLK can be held low or high.
JTDI	I_{PU}	**JTAG Test Data Input.** Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, JTDI can be held low or high.
JTDO	O_3	**JTAG Test Data Output.** Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used, leave unconnected.
JTMS	I_{PU}	**JTAG Test Mode Select.** Sampled on the rising edge of JTCLK and is used to place the port into the various defined IEEE 1149.1 states. If not used connect to VDDIO or leave unconnected.

Table 6-6. Power-Supply Pin Descriptions

PIN NAME[1]	TYPE[2]	PIN DESCRIPTION
VDD	P	**Core Power Supply.** 1.8V ±10%.
VDDIO	P	**I/O Power Supply.** 3.3V ±5%.
VSS	P	**Ground Reference**
AVDD_DL	P	**Power Supply for OC6 Digital Logic.** 1.8V ±10%.
AVSS_DL	P	**Return for OC6 Digital Logic**
VDD_OC6	P	**Power Supply for Differential Output OC6POS/NEG.** 1.8V ±10%.
VSS_OC6	P	**Return for LVDS Differential Output OC6POS/NEG**
AVDD_PLL1	P	**Power Supply for Master Clock Generator APLL.** 1.8V ±10%.
AVSS_PLL1	P	**Return for Master Clock Generator APLL**
AVDD_PLL2	P	**Power Supply for T0 APLL.** 1.8V ±10%.
AVSS_PLL2	P	**Return for T0 APLL**
AVDD_PLL3	P	**Power Supply for T4 APLL.** 1.8V ±10%.
AVSS_PLL3	P	**Return for T4 APLL**
AVDD_PLL4	P	**Power Supply for T0 APLL2.** 1.8V ±10%.
AVSS_PLL4	P	**Return for T0 APLL2**

Note 1: All pin names with an overbar (e.g., $\overline{RST}$) are active low.

Note 2: All pins, except power and analog pins, are CMOS/TTL, unless otherwise specified in the pin description.

PIN TYPES
I = input pin
I_{DIFF} = input pin that is LVDS/LVPECL differential signal compatible
I_{PD} = input pin with internal 50kΩ pulldown
I_{PU} = input pin with internal 50kΩ pullup
I/O = input/output pin
IO_{PD} = input/output pin with internal 50kΩ pulldown
IO_{PU} = input/output pin with internal 50kΩ pullup
O = output pin
O_3 = output pin that can be placed in a high-impedance state
O_{DIFF} = output pin that is LVDS/LVPECL differential signal compatible
P = power-supply pin

Note 3: All digital pins, except OCn, are I/O pins in JTAG mode. OCn pins do not have JTAG functionality.

7. Functional Description

7.1 Overview

The DS3106 has two input clocks, two output clocks, and a high-performance DPLL known as T0. Figure 3-1. The two input clocks are CMOS/TTL (5V tolerant) and can accept signals from 2kHz to 125MHz. Each input clock is monitored continually for activity. SRFAIL is set or cleared based on the activity of the selected input.

The T0 DPLL can directly lock to many common datacom and telecom frequencies, including, but not limited to, 8kHz, DS1, E1, 10MHz, 19.44MHz, and 38.88MHz, as well as Ethernet frequencies including 25MHz, 62.5MHz, and 125MHz. The DPLL can also lock to multiples of the standard direct-lock frequencies including 8kHz. The T0 DPLL has all the features needed for synchronizing a line card to dual redundant system timing cards.

The T0 DPLL includes these features:

A full state machine for automatic transitions among free-run, locked, and holdover states
Adjustable PLL characteristics, including bandwidth, pull-in range, and damping factor
Six bandwidth selections from 18Hz to 400Hz
Frequency conversion between input and output using digital frequency synthesis
Combined performance of a stable, consistent digital PLL and low-jitter analog output PLLs
Ability to lock to several common telecom and Ethernet frequencies plus multiples of the standard direct lock frequencies including 8kHz
Instant digital one-second averaging and free-run holdover modes

Typically, the internal state machine controls the T0 DPLL, but manual control by system software is also available.

The outputs of the T0 DPLL can be connected to seven output DFS engines. See Figure 7-1. Three of these output DFS engines are associated with high-speed APLLs that multiply the DPLL clock rate and filter DPLL output jitter. The outputs of the APLLs are divided down to make a wide variety of possible frequencies available at the output clock pins.

The OC3 and OC6 output clocks can be configured for a variety of different frequencies that are frequency- and phase-locked to the T0 DPLL. The OC6 output is LVDS/LVPECL. The OC3 output is CMOS/TTL. Altogether more than 60 output frequencies are possible, ranging from 2kHz to 312.5MHz. The FSYNC output clock is always 8kHz, and the MFSYNC output clock is always 2kHz.

7.2 Device Identification and Protection

The 16-bit read-only ID field in the ID1 and ID2 registers is set to 0C22h = 3106 decimal. The device revision can be read from the REV register. Contact the factory to interpret this value and determine the latest revision. The register set can be protected from inadvertent writes using the PROT register.

7.3 Local Oscillator and Master Clock Configuration

The T0 DPLL and the output DFS engines operate from a 204.8MHz master clock. The master clock is synthesized from a 12.800MHz clock originating from a local oscillator attached to the REFCLK pin. The stability of the T0 DPLL in free-run or holdover is equivalent to the stability of the local oscillator. Selection of an appropriate local oscillator is therefore of crucial importance if the telecom standards listed in Table 1-1 are to be met. Simple XOs can be used in less stringent cases, but TCXOs or even OCXOs may be required in the most demanding applications. Careful evaluation of the local oscillator component is necessary to ensure proper performance. Contact Microsemi timing products technical support for recommended oscillators.

The stability of the local oscillator is very important, but its absolute frequency accuracy is less important because the DPLLs can compensate for frequency inaccuracies when synthesizing the 204.8MHz master clock from the

local oscillator clock. The MCLKFREQ field in registers MCLK1 and MCLK2 specifies the frequency adjustment to be applied. The adjust can be from -771ppm to +514ppm in 0.0196229ppm (i.e., ~0.02ppm) steps.

7.4 Input Clock Configuration

The DS3106 has two input clocks: IC3 and IC4. Table 7-1 provides summary information about each clock, including signal format and available frequencies. The device tolerates a wide range of duty cycles on input clocks, out to a minimum high time or minimum low time of 3ns or 30% of the clock period, whichever is smaller.

7.4.1 Signal Format Configuration

Both IC3 and IC4 accept TTL and 3.3V CMOS levels. One key configuration bit that affects the available frequencies is the SONSDH bit in MCR3. When SONSDH = 1 (SONET mode), the 1.544MHz frequency is available. When SONSDH = 0 (SDH mode), the 2.048MHz frequency is available. During reset the default value of this bit is latched from the SONSDH pin.

Table 7-1. Input Clock Capabilities

INPUT CLOCK	SIGNAL FORMATS	FREQUENCIES (MHz)	DEFAULT FREQUENCY
IC3	CMOS/TTL	Up to 125(1)	Determined by IPF[2:0] and SONSDH pins, see Table 7-2.
IC4	CMOS/TTL	Up to 125(1)	Determined by IPF[2:0] and SONSDH pins, see Table 7-2.

Note 1: Available frequencies for CMOS/TTL input clocks are: 2kHz, 4kHz, 8kHz, 1.544MHz (SONET mode), 2.048MHz (SDH mode), 6.312MHz, 6.48MHz, 19.44MHz, 25.0MHz, 25.92MHz, 38.88MHz, 51.84MHz, 62.5MHz, 77.76MHz, and any multiple of 2kHz up to 125MHz.

Table 7-2. Input Clock Default Frequency Configuration

IPF[2:0]	SONSDH	DEFAULT FREQUENCY, LOCK MODE
000	X	8kHz, direct lock
001	0	2.048MHz, direct lock
001	1	1.544MHz, direct lock
010	X	6.48MHz, direct lock
011	X	19.44MHz, direct lock
100	X	25.92MHz, direct lock
101	X	38.88MHz, direct lock
110	X	51.84MHz, direct lock
111	X	77.76MHz, direct lock

7.4.2 Frequency Configuration

Input clock frequencies are configured in the FREQ field of the ICR registers. The DIVN and LOCK8K bits of these same registers specify the locking frequency mode, as shown in Table 7-3.

Table 7-3. Locking Frequency Modes

DIVN	LOCK8K	LOCKING FREQUENCY MODE
0	0	Direct Lock
0	1	LOCK8K
1	0	DIVN
1	1	Alternate Direct Lock

7.4.2.1 Direct Lock Mode

In direct lock mode, the T0 DPLL locks to the selected reference at the frequency specified in the corresponding ICR register. Direct lock mode can only be used for input clocks with these specific frequencies: 2kHz, 4kHz, 8kHz, 1.544MHz, 2.048MHz, 5MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.92MHz, 31.25MHz, 38.88MHz, 51.84MHz, and 77.76MHz. The DIVN mode can be used to divide an input down to any of these frequencies except 155.52MHz.

MTIE figures may be marginally better in direct lock mode because the higher frequencies allow more frequent phase updates.

7.4.2.2 Alternate Direct Lock Mode

Alternate direct lock mode is the same as direct lock mode except an alternate list of direct lock frequencies is used (see the FREQ field definition in the ICR register description). The alternate frequencies are included to support clock rates found in Ethernet, CMTS, wireless, and GPS applications. The alternate frequencies are: 10MHz, 25MHz, 62.5MHz, and 125MHz. The frequencies 62.5MHz and 125MHz are internally divided down to 31.25MHz, while 10MHz and 25MHz are internally divided down to 5MHz.

7.4.2.3 LOCK8K Mode

In LOCK8K mode, an internal divider is configured to divide the selected reference down to 8kHz. The DPLL locks to the 8kHz output of the divider. LOCK8K mode can only be used for input clocks with the standard direct lock frequencies: 8kHz, 1.544MHz, 2.048MHz, 5MHz, 6.312MHz, 6.48MHz, 19.44MHz, 25.0MHz, 25.92MHz, 31.25MHz, 38.88MHz, 51.84MHz, 62.5MHz, and 77.76MHz. LOCK8K mode is enabled for a particular input clock by setting the LOCK8K bit in the corresponding ICR register.

LOCK8K mode gives a greater tolerance to input jitter when the multicycle phase detector is disabled because it uses lower frequencies for phase comparisons. The clock edge to lock to on the selected reference can be configured using the 8KPOL bit in the TEST1 register. For 2kHz and 4kHz clocks the LOCK8K bit is ignored and direct-lock mode is used.

7.4.2.4 DIVN Mode

In DIVN mode, an internal divider is configured from the value stored in the DIVN registers. The DIVN value must be chosen so that when the selected reference is divided by DIVN+1, the resulting clock frequency is the same as the standard direct lock frequency selected in the FREQ field of the ICR register. The DPLL locks to the output of the divider. DIVN mode can only be used for input clocks whose frequency is less than or equal to 125MHz. The DIVN register field can range from 0 to 65,535 inclusive. The same DIVN+1 factor is used for all input clocks configured for DIVN mode.

7.5 Input Clock Monitoring

Each input clock is continuously monitored for activity. Activity monitoring is described in Sections 7.5.2 and 7.5.3. The valid/invalid state of each input clock is reported in the corresponding real-time status bit in register VALSR1. When the valid/invalid state of a clock changes, the corresponding latched status bit is set in register MSR1, and an interrupt request occurs if the corresponding interrupt enable bit is set in register IER1. Input clocks marked invalid cannot be automatically selected as the reference for either DPLL.

7.5.1 Frequency Monitoring

The DS3106 monitors the frequency of each input clock and invalidates any clock whose frequency is more than 10,000ppm away from nominal. The frequency range monitor can be disabled by clearing the MCR1.FREN bit. The frequency range measurement uses the internal 204.8MHz master clock as the frequency reference.

7.5.2 Activity Monitoring

Each input clock is monitored for activity and proper behavior using a leaky bucket accumulator. A leaky bucket accumulator is similar to an analog integrator: the output amplitude increases in the presence of input events and

gradually decays in the absence of events. When events occur infrequently, the accumulator value decays fully between events and no alarm is declared. When events occur close enough together, the accumulator increments faster than it can decay and eventually reaches the alarm threshold. After an alarm has been declared, if events occur infrequently enough, the accumulator can decay faster than it is incremented and eventually reaches the alarm clear threshold. The leaky bucket events come from the frequency range and fast activity monitors.

There is one leaky bucket configuration common to both inputs that has programmable size, alarm declare threshold, alarm clear threshold, and decay rate, all of which are specified in the LB0x registers.

Activity monitoring is divided into 128ms intervals. The accumulator is incremented once for each 128ms interval in which the input clock is inactive for more than two cycles (more than four cycles for 125MHz, 62.5MHz, 25MHz, and 10MHz input clocks). Thus, the “fill” rate of the bucket is at most 1 unit per 128ms, or approximately 8 units/second. During each period of 1, 2, 4, or 8 intervals (programmable), the accumulator decrements if no irregularities occur. Thus, the “leak” rate of the bucket is approximately 8, 4, 2, or 1 units/second. A leak is prevented when a fill event occurs in the same interval.

When the value of an accumulator reaches the alarm threshold (LB0U register), the corresponding ACT alarm bit is set to 1 in the ISR2 register, and the clock is marked invalid in the VALSR1 register. When the value of an accumulator reaches the alarm clear threshold (LB0L register), the activity alarm is cleared by clearing the clock's ACT bit. The accumulator cannot increment past the size of the bucket specified in the LB0S register. The decay rate of the accumulator is specified in the LB0D register. The values stored in the leaky bucket configuration registers must have the following relationship at all times: LB0S ≥ LB0U > LB0L.

When the leaky bucket is empty, the minimum time to declare an activity alarm in seconds is LB0U / 8. The minimum time to clear an activity alarm in seconds is 2^LB0D × (LB0S – LB0L) / 8. As an example, assume LB0U = 8, LB0L = 1, LB0S = 10, and LB0D = 0. The minimum time to declare an activity alarm would be 8 / 8 = 1 second. The minimum time to clear the activity alarm would be 2^0 × (10 – 1) / 8 = 1.125 seconds.

7.5.3 Selected Reference Activity Monitoring

The input clock that T0 DPLL is currently locked to is called the selected reference. The quality of a DPLL’s selected reference is exceedingly important, since missing cycles and other anomalies on the selected reference can cause unwanted jitter, wander, or frequency offset on the output clocks. When anomalies occur on the selected reference, they must be detected as soon as possible to give the DPLL opportunity to temporarily disconnect from the reference until the reference is available again. By design, the regular input clock activity monitor (Section 7.5.2) is too slow to be suitable for monitoring the selected reference. Instead, each DPLL has its own fast activity monitor that detects that the frequency is within range (approximately 10,000ppm) and detects inactivity within approximately two missing reference clock cycles (approximately four missing cycles for 125MHz, 62.5MHz, 25MHz, and 10MHz references).

When the T0 DPLL detects a no-activity event, it immediately enters mini-holdover mode to isolate itself from the selected reference and sets the SRFAIL latched status bit in MSR2. The setting of the SRFAIL bit can cause an interrupt request if the corresponding enable bit is set in IER2. If MCR10:SRFPIN = 1, the SRFAIL output pin follows the state of the SRFAIL status bit. When PHLIM1:NALOL = 0 (default), the T0 DPLL does not declare loss-of-lock during no-activity events. If the selected reference becomes available again before any alarms are declared by the activity monitor, the T0 DPLL continues to track the selected reference using nearest edge locking (±180°) to avoid cycle slips. When NALOL = 1, the T0 DPLL declares loss-of-lock during no-activity events. This causes the T0 DPLL state machine to transition to the loss-of-lock state, which sets the MSR2:STATE bit and causes an interrupt request if enabled. If the selected reference becomes available again before any alarms are declared by the activity monitor, the T0 DPLL tracks the selected reference using phase/frequency locking (±360°) until phase lock is reestablished.

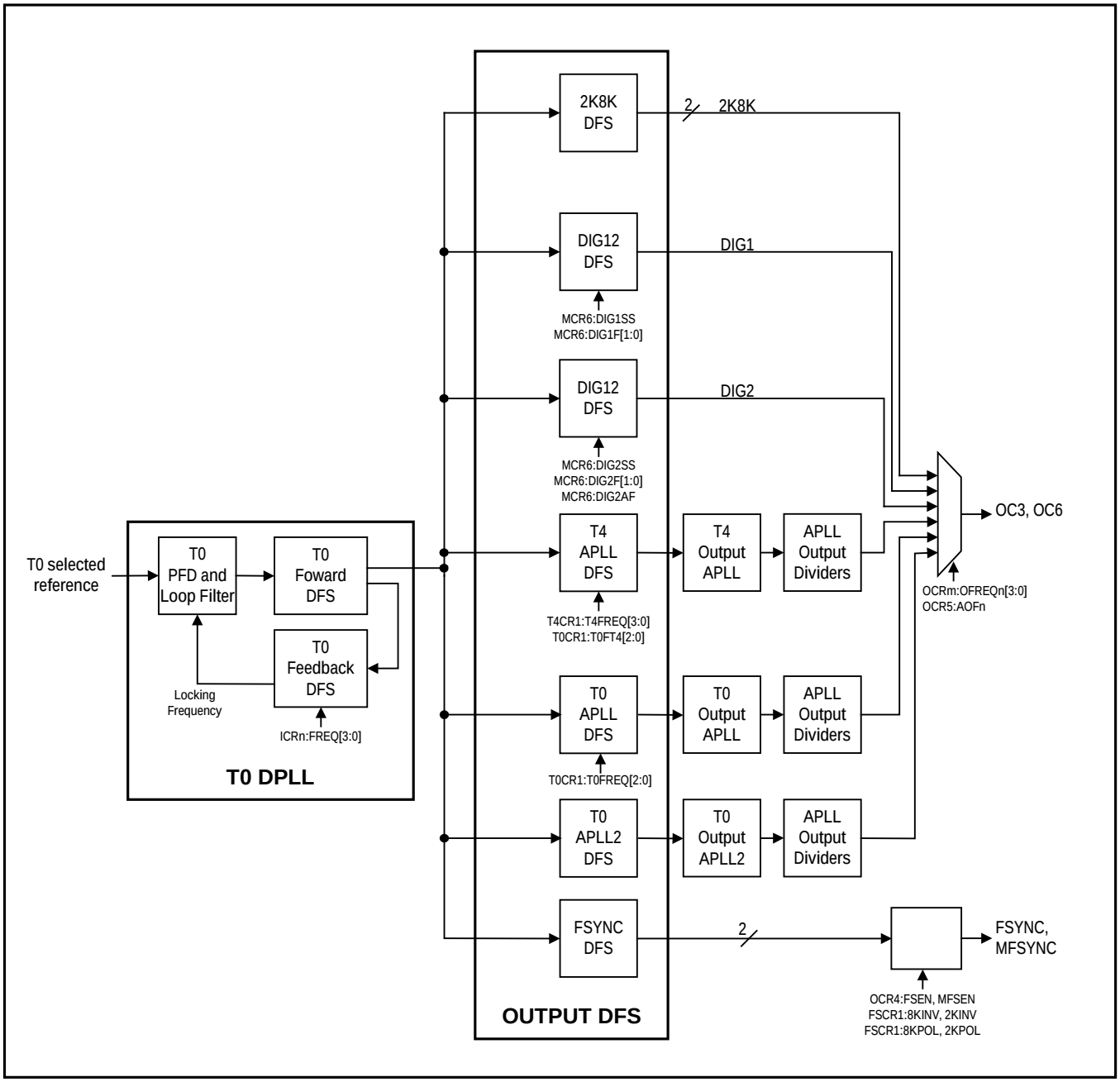
7.6 Input Clock Priority and Switching

The SRCSW input pin controls reference switching between two clock inputs. In this mode, if the SRCSW pin is high, the T0 DPLL is forced to lock to input IC3. If the SRCSW pin is low the device is forced to lock to input IC4. The currently selected reference is indicated in the PTAB1:SELREF field.

7.7 DPLL Architecture and Configuration

The T0 DPLL is a digital PLL with separate analog PLLs (APLLs) as output stages as well as some outputs that are not cleaned up by an APLL. This architecture combines the benefits of both PLL types. See Figure 7-1.

Figure 7-1. DPLL Block Diagram



Digital PLLs have two key benefits: (1) stable, repeatable performance that is insensitive to process variations, temperature, and voltage; and (2) flexible behavior that is easily programmed through the configuration registers. DPLLs use digital frequency synthesis (DFS) to generate various clocks. In DFS a high-speed master clock (204.8MHz) is multiplied up from the 12.800MHz local oscillator clock applied to the REFCLK pin. This master clock is then digitally divided down to the desired output frequency. The DFS output clock has jitter of about 1ns pk-pk.

The analog PLLs filter the jitter from the DPLLs, reducing the 1ns pk-pk jitter to less than 0.5ns pk-pk and 60ps RMS, typical, measured broadband (10Hz to 1GHz).

The DPLLs in the device are configurable for many PLL parameters including bandwidth, damping factor, input frequency, pull-in/hold-in range, and more. No knowledge of loop equations or gain parameters is required to configure and operate the device. No external components are required for the DPLL or the APLLs except the high-quality local oscillator connected to the REFCLK pin.

The T0 DPLL has a full free-run/locked/holdover state machine and full programmability.

7.7.1 T0 DPLL State Machine

The T0 DPLL has three main timing modes: locked, holdover, and free-run. The control state machine for the T0 DPLL has states for each timing mode as well as three temporary states: prelocked, prelocked 2, and loss-of-lock. The state transition diagram is shown in Figure 7-2. Descriptions of each state are given in the paragraphs below. During normal operation the state machine controls state transitions. When necessary, however, the state can be forced using the T0STATE field of the MCR1 register.

Whenever the T0 DPLL changes state, the STATE bit in MSR2 is set, which can cause an interrupt request if enabled. The current T0 DPLL state can be read from the T0STATE field of the OPSTATE register.

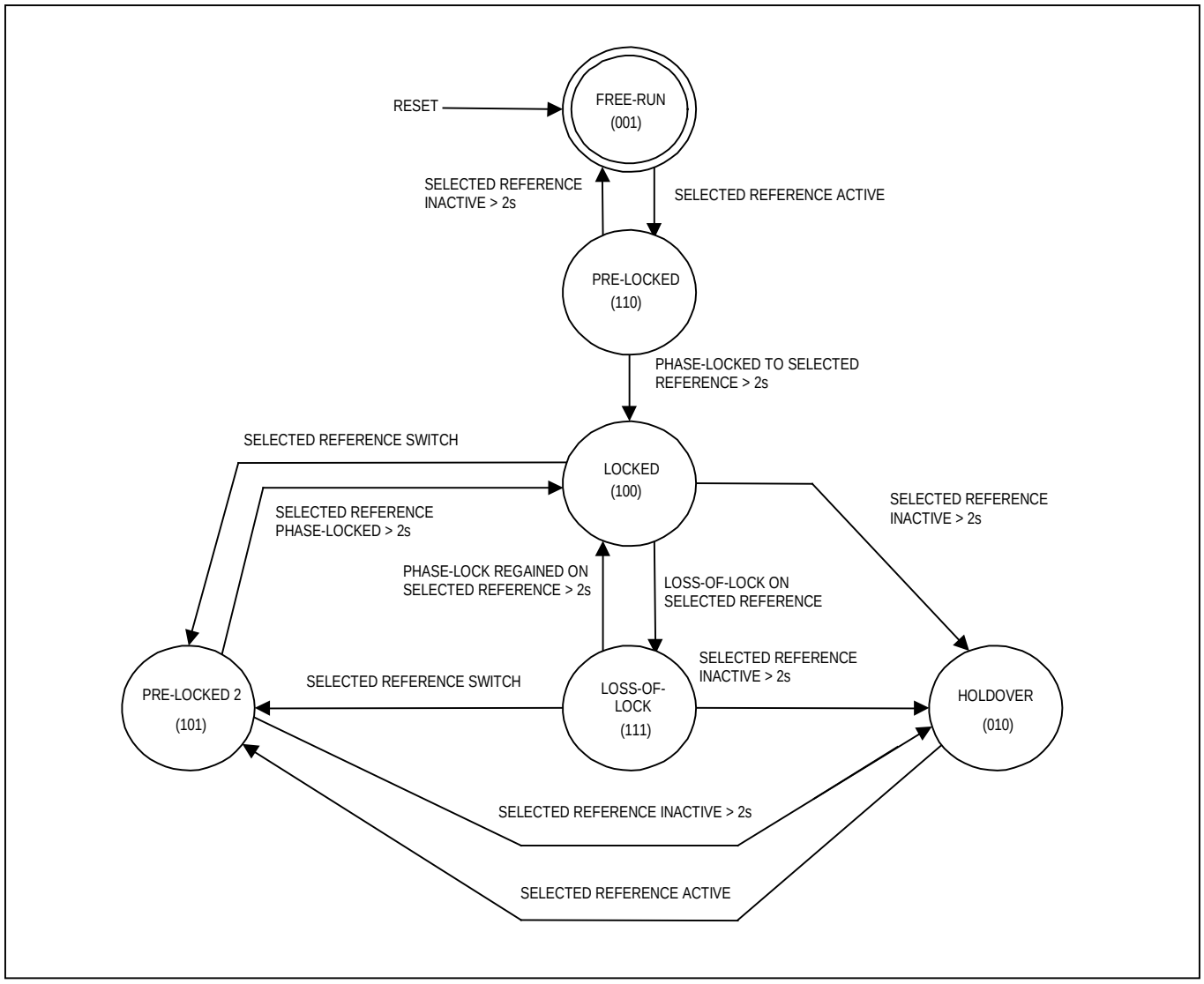
7.7.1.1 Free-Run State

Free-run mode is the reset default state. In free-run all output clocks are derived from the 12.800 MHz local oscillator attached to the REFCLK pin. The frequency of each output clock is a specific multiple of the local oscillator. The frequency accuracy of each output clock is equal to the frequency accuracy of the master clock, which can be calibrated using the MCLKFREQ field in registers MCLK1 and MCLK2 (see Section 7.3). The state machine transitions from free-run to the prelocked state when at least one input clock is valid.

7.7.1.2 Prelocked State

If phase lock (see Section 7.7.5) is achieved for 2 seconds during this period, the state machine transitions to locked mode. If the selected reference becomes inactive for 2 seconds then the state machine transitions back to the free-run state.

Figure 7-2. T0 DPLL State Transition Diagram



Note 1: Phase lock is declared internally when the DPLL has maintained phase lock continuously for approximately 1 to 2 seconds.

Note 2: When selected reference is invalid and the DPLL is not in free-run or holdover, the DPLL is in a temporary holdover state.

7.7.1.3 Locked State

The T0 DPLL state machine can reach the locked state from the prelocked, prelocked 2, or loss-of-lock states when the DPLL has locked to the selected reference for at least 2 seconds (see Section 7.7.5). In the locked state the output clocks track the phase and frequency of the selected reference.

If the MCR1.LOCKPIN bit is set, the LOCK pin is driven high when the T0 DPLL is in the locked state.

While in the locked state, if the selected reference becomes inactive and an activity alarm is raised (corresponding ACT bit set in the ISR2 register), the selected reference is marked invalid (ICn bit goes low in the VALSR1 register), and the LOS pin is asserted. If the input stays inactive for 2 seconds, the state machine transitions to the holdover state. If the DPLL is switched to the other input and that input is active, the state machine transitions to the prelocked 2 state.

7.7.1.4 Loss-of-Lock State

When the loss-of-lock detectors (see Section 7.7.5) indicate loss-of-phase lock, the state machine immediately transitions from the locked state to the loss-of-lock state. If phase lock is regained during that period for more than 2 seconds while in the loss-of-lock state, the state machine transitions back to the locked state.

While in the loss-of-lock state, if the selected reference is becomes inactive, an activity alarm is raised (corresponding ACT bit set in the ISR2 register), the selected reference is marked invalid (ICn bit goes low in the VALSR1 register), and the LOS pin is asserted. If the input stays inactive for 2 seconds, the state machine transitions to the holdover state. If the DPLL is switched to the other input and that input is active, the state machine transitions to the prelocked 2 state.

7.7.1.5 Prelocked 2 State

The prelocked and prelocked 2 states are similar. If phase lock (see Section 7.7.5) is achieved for more than 2 seconds, the state machine transitions to locked mode. While in the prelocked 2 state, if the selected reference is becomes inactive, an activity alarm is raised (corresponding ACT bit set in the ISR2 register), the selected reference is marked invalid (ICn bit goes low in the VALSR1 register), and the LOS pin is asserted. If the input stays inactive for 2 seconds, the state machine transitions to the holdover state.

7.7.1.6 Holdover State

The device reaches the holdover state when it declares its selected reference invalid for 2 seconds. During holdover the T0 DPLL is not phase-locked to any input clock but instead generates its output frequency based on previous frequencies while it was locked. When the selected reference becomes active, the state machine immediately transitions from holdover to the prelocked 2 state, and tries to lock to the selected reference.

7.7.1.6.1Automatic Holdover

For automatic holdover (FRUNHO = 0 in MCR3), the device can be further configured for instantaneous mode or averaged mode. In *instantaneous mode* (AVG = 0 in HOCR3), the holdover frequency is set to the DPLL's current frequency 50ms to 100ms before entry into holdover (i.e., the value of the FREQ field in the FREQ1, FREQ2, and FREQ3 registers). The FREQ field is the DPLL's integral path and, therefore, is an average frequency with a rate of change inversely proportional to the DPLL bandwidth. The DPLL's proportional path is not used in order to minimize the effect of recent phase disturbances on the holdover frequency.

In *averaged mode* (AVG = 1 in HOCR3 and FRUNHO = 1 in MCR3), the holdover frequency is set to an internally averaged value. During locked operation the frequency indicated in the FREQ field is internally averaged over a one-second period. The T0 DPLL indicates that it has acquired a valid holdover value by setting the HORDY status bit in MSR4 (latched status). If the T0 DPLL must enter holdover before the one-second average is available, an instantaneous value 50ms to 100ms old from the integral path is used instead.

7.7.1.6.2Free-Run Holdover

For free-run holdover (FRUNHO = 1 in MCR3), the output frequency accuracy is generated with the accuracy of the external oscillator frequency. The actual frequency is the frequency of the external oscillator plus the value of the MCLK offset specified in the MCLKFREQ field in registers MCLK1 and MCLK2 (see Section 7.3). When MCR3.FRUNHO is set the HOCR3:AVG bit is ignored.

7.7.1.7 Mini-Holdover

When the selected reference fails, the fast activity monitor (Section 7.5.3) isolates the T0 DPLL from the reference within one or two clock cycles to avoid adverse effects on the DPLL frequency. When this fast isolation occurs, the DPLL enters a temporary mini-holdover mode, with a frequency equal to an instantaneous value 50ms to 100 ms old from the integral path of the loop filter. Mini-holdover lasts until the selected reference becomes active or the state machine enters the holdover state. If the free-run holdover mode is set (FRUNHO = 1 in MCR3), the mini-holdover frequency accuracy is exactly the same as the external oscillator accuracy plus the offset set by the MCLKFREQ field in registers MCLK1 and MCLK2 (see Section 7.3).

7.7.2 Bandwidth

The bandwidth of the T0 DPLL is configured in the T0ABW and T0LBW registers for various values from 18Hz to 400Hz. The AUTOBW bit in the MCR9 register controls automatic bandwidth selection. When AUTOBW = 1, the T0 DPLL uses the T0ABW bandwidth during acquisition (not phase-locked) and the T0LBW bandwidth when phase-locked. When AUTOBW = 0 the T0 DPLL uses the T0LBW bandwidth all the time, both during acquisition and when phase-locked.

When LIMINT = 1 in the MCR9 register, the DPLL's integral path is limited (i.e., frozen) when the DPLL reaches minimum or maximum frequency. Setting LIMINT = 1 minimizes overshoot when the DPLL is pulling in.

7.7.3 Damping Factor

The damping factor for the T0 DPLL is configured in the DAMP field of the T0CR2 register. The reset default damping factor is chosen to give a maximum jitter/wander gain peak of approximately 0.1dB. Available settings are a function of DPLL bandwidth (configured in the T0ABW and T0LBW registers). See Table 7-4.

Table 7-4. Damping Factors and Peak Jitter/Wander Gain

BANDWIDTH (Hz)	DAMP[2:0] VALUE	DAMPING FACTOR	GAIN PEAK (dB)
18	1	1.2	0.4
	2	2.5	0.2
	3, 4, 5	5	0.1
35	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4, 5	10	0.06
70 to 400	1	1.2	0.4
	2	2.5	0.2
	3	5	0.1
	4	10	0.06
	5	20	0.03

7.7.4 Phase Detectors

Phase detectors are used to compare a PLL's feedback clock with its input clock. Several phase detectors are available in the T0 DPLL:

Phase/frequency detector (PFD)
Early/late phase detector (PD2) for fine resolution
Multicycle phase detector (MCPD) for large input jitter tolerance and/or faster lock times

These detectors can be used in combination to give fine phase resolution combined with large jitter tolerance. As with the rest of the DPLL logic, the phase detectors operate at input frequencies up to 77.76MHz. The multicycle

phase detector detects and remembers phase differences of many cycles (up to 8191UI). When locking to 8kHz or lower, the normal phase/frequency detectors are always used.

The T0 DPLL phase detectors can be configured for normal phase/frequency locking (±360° capture) or nearest edge phase locking (±180° capture). With nearest edge detection the phase detectors are immune to occasional missing clock cycles. The DPLL automatically switches to nearest edge locking when the multicycle phase detector is disabled and the other phase detectors determine that phase lock has been achieved. Setting D180 = 1 in the TEST1 register disables nearest edge locking and forces the T0 DPLL to use phase/frequency locking.

The early/late phase detector, also known as phase detector 2, is enabled and configured in the PD2 fields of the T0CR2 register. The reset default settings of this register is appropriate for all operating modes. Adjustments only affect small signal overshoot and bandwidth.

The multicycle phase detector is enabled by setting MCPDEN = 1 in the PHLIM2 register. The range of the MCPD—from ±1UI up to ±8191UI—is configured in the COARSELIM field of PHLIM2. The MCPD tracks phase position over many clock cycles, giving high jitter tolerance. Thus, the use of the MCPD is an alternative to the use of LOCK8K mode for jitter tolerance. When a DPLL is direct locking to 8kHz, 4kHz, or 2kHz, or in LOCK8K mode, the multicycle phase detector is automatically disabled.

When USEMCPD = 1 in PHLIM2, the MCPD is used in the DPLL loop, giving faster pull-in but more overshoot. In this mode the loop has similar behavior to LOCK8K mode. In both cases large phase differences contribute to the dynamics of the loop. When enabled by MCPDEN = 1, the MCPD tracks the phase position whether or not it is used in the DPLL loop.

When the input clock is divided before being sent to the phase detector, the divider output clock edge gets aligned to the feedback clock edge before the DPLL starts to lock to a new input clock signal or after the input clock signal has a temporary signal loss. This helps ensure locking to the nearest input clock edge, which reduces output transients and decreases lock times.

7.7.5 Loss-of-Lock Detection

Loss-of-lock can be triggered by any of the following in the T0 DPLL:

The fine phase-lock detector (measures phase between input and feedback clocks)
The coarse phase-lock detector (measures whole cycle slips)
Hard frequency limit detector
Inactivity detector

The fine phase-lock detector is enabled by setting FLEN = 1 in the PHLIM1 register. The fine phase limit is configured in the FINELIM field of PHLIM1.

The coarse phase-lock detector is enabled by setting CLEN = 1 in the PHLIM2 register. The coarse phase limit is configured in the COARSELIM field of PHLIM2. This coarse phase-lock detector is part of the multicycle phase detector (MCPD) described in Section 7.7.4. The COARSELIM field sets both the MCPD range and the coarse phase limit, since the two are equivalent. If loss-of-lock should not be declared for multiple-UI input jitter, the fine phase-lock detector should be disabled and the coarse phase-lock detector should be used instead.

The hard frequency limit detector is enabled by setting FLLOL = 1 in the DLIMIT3 register. The hard limit is configured in registers DLIMIT1 and DLIMIT2. When the DPLL frequency reaches the hard limit, loss-of-lock is declared. The DLIMIT3 register also has the SOFTLIM field to specify a soft frequency limit. Exceeding the soft frequency limit does not cause loss-of-lock to be declared. When the T0 DPLL frequency reaches the soft limit, the T0SOFT status bit is set in the OPSTATE register.

The inactivity detector is enabled by setting NALOL = 1 in the PHLIM1 register. When this detector is enabled the DPLL declares loss-of-lock after one or two missing clock cycles on the selected reference. See Section 7.5.3.

When the T0 DPLL declares loss-of-lock, the state machine immediately transitions to the loss-of-lock state, which sets the STATE bit in the MSR2 register and requests an interrupt if enabled.

7.7.6 Frequency and Phase Measurement

Accurate measurement of frequency and phase can be accomplished using the T0 DPLL. The REFCLK signal accuracy after being adjusted with MCLKFREQ is used for the frequency reference.

DPLL frequency measurements can be read from the FREQ field spanning registers FREQ1, FREQ2, and FREQ3. This field indicates the frequency of the selected reference. This frequency measurement has a resolution of 0.0003068ppm over a ±80ppm range. The value read from the FREQ field is the DPLL's integral path value, which is an averaged measurement with an averaging time inversely proportional to DPLL bandwidth.

DPLL phase measurements can be read from the PHASE field spanning registers PHASE1 and PHASE2. This field indicates the phase difference seen by the phase detector. This phase measurement has a resolution of approximately 0.703 degrees and is internally averaged with a -3dB attenuation point of approximately 100Hz. Thus, for low DPLL bandwidths the PHASE field gives input phase wander in the frequency band from the DPLL corner frequency up to 100Hz. This information could be used by software to compute a crude MTIE measurement.

7.7.7 Input Jitter Tolerance

The device is compliant with the jitter tolerance requirements of the standards listed in Table 1-1. When using the ±360°/±180° PFD, jitter can be tolerated up to the point of eye closure. Either LOCK8K mode (see Section 7.4.2.2) or the multicycle phase detector (see Section 7.7.4) should be used for high jitter tolerance.

7.7.8 Jitter Transfer

The transfer of jitter from the selected reference to the output clocks has a programmable transfer function that is determined by the DPLL bandwidth. (See Section 7.7.2.) In the T0 DPLL, the 3dB corner frequency of the jitter transfer function can be set to any of 7 positions from 18Hz to 400Hz.

7.7.9 Output Jitter and Wander

Several factors contribute to jitter and wander on the output clocks, including:

Jitter and wander amplitude on the selected reference (while in the locked state)
The jitter transfer characteristic of the device (while in the locked state)
The jitter and wander on the local oscillator clock signal (especially wander while in the holdover state)

The DPLL in the device has programmable bandwidth (see Section 7.7.2). With respect to jitter, the DPLL behaves as a lowpass filter with a programmable pole. The bandwidth of the DPLL is low enough to strongly attenuate jitter

7.8 Output Clock Configuration

A total of four output clock pins, OC3, OC6, FSYNC, and MFSYNC, are available on the device. Output clocks OC3 and OC6 are individually configurable for a variety of frequencies. Output clocks FSYNC and MFSYNC are more specialized, serving as an 8kHz frame sync (FSYNC) and a 2kHz multiframe sync (MFSYNC). Table 7-5 provides more detail on the capabilities of the output clock pins.

Table 7-5. Output Clock Capabilities

OUTPUT CLOCK	SIGNAL FORMAT	FREQUENCIES SUPPORTED
OC3	CMOS/TTL	Frequency selection per Section 7.8.2.3 and Table 7-6 to Table 7-12.
OC6	LVDS/LVPECL	
FSYNC	CMOS/TTL	8kHz frame sync with programmable pulse width and polarity.
MFSYNC		2kHz multiframe sync with programmable pulse width and polarity.

7.8.1 Signal Format Configuration

Output clock OC6 is an LVDS-compatible, LVPECL level-compatible outputs. The type of output can be selected or the output can be disabled using the OC6SF configuration bits in the MCR8 register. The LVPECL level-compatible mode generates a differential signal that is large enough for most LVPECL receivers. Some LVPECL receivers have a limited common-mode signal range that can be accommodated for by using an AC-coupled signal. The LVDS electrical specifications are listed in Table 10-4, and the recommended LVDS termination is shown in Figure 10-1. The LVPECL level-compatible electrical specifications are listed in Table 10-5, and the recommended LVPECL receiver termination is shown in Figure 10-2. These differential outputs can be easily interfaced to LVDS, LVPECL, and CML inputs on neighboring ICs using a few external passive components. See App Note HFAN-1.0 for details.

Output clocks OC3, FSYNC, and MFSYNC are CMOS/TTL signal format.

7.8.2 Frequency Configuration

The frequency of output clocks OC3 and OC6 is a function of the settings used to configure the components of the T0 PLL paths. These components are shown in the detailed block diagram of Figure 7-1.

The DS3106 uses digital frequency synthesis (DFS) to generate various clocks. In DFS a high-speed master clock (204.8MHz) is divided down to the desired output frequency by adding a number to an accumulator. The DFS output is a coding of the clock output phase that is used by a special circuit to determine where to put the edges of the output clock between the clock edges of the master clock. The edges of the output clock, however, are not ideally located in time, resulting in jitter with an amplitude typically less than 1ns pk-pk.

7.8.2.1 T0 DPLL and Feedback DFS Details

See Figure 7-1. The T0 forward-DFS block uses the 204.8MHz master clock and DFS technology to synthesize internal clocks from which the output and feedback clocks are derived.

The feedback DFS block synthesizes the appropriate locking frequencies for use by the phase-frequency detector (PFD). See Section 7.4.2.

7.8.2.2 Output DFS and APLL Details

See Figure 7-1. The output clock frequencies are determined by two 2kHz/8kHz DFS blocks, two DIG12 DFS blocks, and three APLL DFS blocks. The T0 APLL, the T0 APLL2, and the T4 APLL (and their output dividers) get their frequency references from three associated APLL DFS blocks. All the output DFS blocks are connected to the T0 DPLL.

The 2K8K DFS and FSYNC DFS blocks generate both 2kHz and 8kHz signals, which have about 1ns pk-pk jitter. The FSYNC (8kHz) and MFSYNC (2 kHz) signals come from the FSYNC DFS block. The 2kHz and 8 kHz signals that can be output on OC3 or OC6 always come from the 2K8K DFS.

The DIG1 DFS can generate an N x DS1 or N x E1 signal with about 1ns pk-pk jitter. The DIG2 DFS can generate an N x DS1, N x E1, 6.312MHz, 10MHz, or N x 19.44MHz clock with approximately 1ns pk-pk jitter. The frequency of the DIG1 clock is configured by the DIG1SS bit in MCR6 and the DIG1F[1:0] field in MCR7. The frequency of the DIG2 clock is configured by the DIG2AF and DIG2SS bits in MCR6 and the DIG2F[1:0] field in MCR7. DIG1 and DIG2 can be independently configured for any of the frequencies shown in Table 7-6 and Table 7-7, respectively.

The APLL DFS blocks and their associated output APLLs and output dividers can generate many different frequencies. The T0 APLL frequencies that can be generated are listed in Table 7-9. The T0 APLL2 frequency is always 312.500MHz. The T4 APLL frequencies that can be generated are listed in Table 7-11. The output frequencies that can be generated from the APLL circuits are listed in Table 7-8.

7.8.2.3 OC3 and OC6 Configuration

The following is a step-by-step procedure for configuring the frequencies of output clocks OC3 and OC6:

Use Table 7-8 to select a set of output frequencies for each APLL, T0 and T4. Each APLL can only generate one set of output frequencies. (In SONET/SDH equipment, the T0 APLL is typically configured for a frequency of 311.04MHz to get N x 19.44MHz output clocks to for use on line cards.)

Determine from Table 7-8 the T0 and T4 APLL frequencies required for the frequency sets chosen in step 2.

Configure the T0FREQ field in register T0CR1 as shown in Table 7-9 for the T0 APLL frequency determined in step 3. Configure fields T4CR1:T4FREQ, T0CR1:T4APT0, and T0CR1:T0FT4 as shown in Table 7-11 for the T4 APLL frequency determined in step 3.

Using Table 7-8 and Table 7-12, configure the frequencies of output clocks OC3 and OC6 in the OFREQn fields of registers OCR2 and OCR4 and the AOFn bits in the OCR5 register.

Table 7-13 lists all standard frequencies for the output clocks and specifies how to configure the T0 APLL and/or the T4 APLL to obtain each frequency. Table 7-13 also indicates the expected jitter amplitude for each frequency.

Table 7-6. Digital1 Frequencies

DIG1F[1:0] SETTING IN MCR7	DIG1SS SETTING IN MCR6	FREQUENCY (MHz)	JITTER (pk-pk, ns, typ)
00	0	2.048	< 1
01	0	4.096	< 1
10	0	8.192	< 1
11	0	16.384	< 1
00	1	1.544	< 1
01	1	3.088	< 1
10	1	6.176	< 1
11	1	12.352	< 1

Table 7-7. Digital2 Frequencies

DIG2AF SETTING IN MCR6	DIG2F[1:0] SETTING IN MCR7	DIG2SS SETTING IN MCR6	FREQUENCY (MHz)	JITTER (pk-pk, ns, typ)
1	00	0	6.312	< 1
1	10	0	10.000	<1
1	00	1	19.440	< 1
1	01	1	38.880	< 1
0	00	0	2.048	< 1
0	01	0	4.096	< 1
0	10	0	8.192	< 1
0	11	0	16.384	< 1
0	00	1	1.544	< 1
0	01	1	3.088	< 1
0	10	1	6.176	< 1
0	11	1	12.352	< 1

Table 7-8. APLL Frequency to Output Frequencies (T0 APLL and T4 APLL)

APLL FREQUENCY	APLL/ 2	APLL/ 4	APLL/ 5	APLL/ 6	APLL/ 8	APLL/ 10	APLL/ 12	APLL/ 16	APLL/ 20	APLL/ 48	APLL/ 64
312.5	**156.25**	—	**62.5**	—	—	31.25	—	—	—	—	—
311.04	**155.52**	**77.76**	62.208	**51.84**	**38.88**	31.104	25.92	**19.44**	15.552	**6.48**	4.86
274.944	137.472	68.376	—	45.824	**34.368**	—	22.912	17.184	—	5.728	4.296
250	**125**	**62.5**	50	—	31.25	**25**	—	—	12.5	—	—
178.944	89.472	**44.736**	—	29.824	22.368	—	14.912	11.184	—	3.728	2.796
160	80	40	32	—	20	16	—	**10**	8	—	2.5
148.224	74.112	37.056	—	24.704	18.528	—	12.352	9.264	—	**3.088**	2.316
131.072	65.536	**32.768**	—	—	**16.384**	—	—	**8.192**	—	—	**2.048**
122.88	61.44	**30.72**	24.576	20.48	15.36	12.288	**10.24**	7.68	6.144	2.56	1.92
104	52	26	20.8	—	**13**	10.4	—	6.5	5.2	—	—
100.992	50.496	25.248	—	16.832	12.624	—	8.416	**6.312**	—	2.104	1.578
98.816	49.408	24.704	—	—	12.352	—	—	**6.176**	—	—	**1.544**
98.304	49.152	24.576	—	**16.384**	12.288	—	**8.192**	6.144	—	**2.048**	1.536

Note: *All frequencies in MHz. Common telecom, datacom, and synchronization frequencies are in* ***bold*** *type.*

Table 7-9. T0 APLL Frequency Configuration

T0 APLL FREQUENCY (MHz)	T0 APLL DFS FREQUENCY (MHz)	T0 APLL FREQUENCY MODE	T0FREQ[2:0] SETTING IN T0CR1	OUTPUT JITTER (pk-pk, ns, typ)
311.04	77.76	77.76MHz	000	< 0.5
311.04	77.76	77.76MHz	001	< 0.5
98.304	24.576	12 x E1	010	< 0.5
131.072	32.768	16 x E1	011	< 0.5
148.224	37.056	24 x DS1	100	< 0.5
98.816	24.704	16 x DS1	101	< 0.5
100.992	25.248	4 x 6312kHz	110	< 0.5
250.000	62.500	GbE ÷ 16	111	< 0.5

Table 7-10. T0 APLL2 Frequency Configuration

T0 APLL2 FREQUENCY (MHz)	T0 APLL2 DFS FREQUENCY(MHz)	OUTPUT JITTER (pk-pk, ns, typ)
312.500	62.500	< 0.5

Table 7-11. T4 APLL Frequency Configuration

T4 APLL FREQUENCY (MHz)	T4 APLL DFS FREQUENCY (MHz)	T4 APLL FREQUENCY MODE	T4APT0 SETTING IN T0CR1	T4FREQ[3:0] SETTING IN T4CR1	T0FT4[2:0] SETTING IN T0CR1	OUTPUT JITTER (pk-pk, ns, typ)
Disabled	77.76	Squelched	0	0000	XXX	< 0.5
311.04	77.76	77.76MHz	0	0001	XXX	< 0.5
98.304	24.576	12 x E1	0	0010	XXX	< 0.5
131.072	32.768	16 x E1	0	0011	XXX	< 0.5
148.224	37.056	24 x DS1	0	0100	XXX	< 0.5
98.816	24.704	16 x DS1	0	0101	XXX	< 0.5
274.944	68.736	2 x E3	0	0110	XXX	< 0.5
178.944	44.736	DS3	0	0111	XXX	< 0.5
100.992	25.248	4 x 6312kHz	0	1000	XXX	< 0.5
250.000	62.500	GbE ÷ 16	0	1001	XXX	< 0.5
122.880	30.720	3 x 10.24	0	1010	XXX	< 0.5
160.000	40.000	4 x 10	0	1011	XXX	< 0.5
104.000	26.000	2 x 13	0	1100	XXX	< 0.5
98.304	24.576	T0 12 x E1	1	XXXX	000	< 0.5
250.000	62.500	T0 GbE ÷ 16	1	XXXX	001	< 0.5
131.072	32.768	T0 16 x E1	1	XXXX	010	< 0.5
148.224	37.056	T0 24 x DS1	1	XXXX	100	< 0.5
98.816	24.704	T0 16 x DS1	1	XXXX	110	< 0.5
100.992	25.248	T0 4 x 6312kHz	1	XXXX	111	< 0.5

Table 7-12. OC3 and OC6 Output Frequency Selection

AOF BIT	OFREQ(1)	FREQUENCY	
		OC3	OC6
0	0000	Disabled	Disabled
0	0001	2kHz	2kHz
0	0010	8kHz	8kHz
0	0011	Digital2	T0 / 2
0	0100	Digital1	Digital1
0	0101	T0 / 48	T0 / 1
0	0110	T0 / 16	T0 / 16
0	0111	T0 / 12	T0 / 12
0	1000	T0 / 8	T0 / 8
0	1001	T0 / 6	T0 / 6
0	1010	T0 / 4	T0 / 4
0	1011	T4 / 64	T4 / 64
0	1100	T4 / 48	T4 / 48
0	1101	T4 / 16	T4 / 16
0	1110	T4 / 8	T4 / 8
0	1111	T4 / 4	T4 / 4
1	0000	Disabled	Disabled
1	0001	T0 / 64	T4 / 5
1	0010	T4 / 20	T4 / 2
1	0011	T4 / 12	T4 / 1
1	0100	T4 / 10	T02 / 5
1	0101	T4 / 5	T02 / 2
1	0110	T4 / 2	T02 / 1

Note 1: The value of the OFREQn field (in the OCR2 and OCR3 registers) corresponding to output clock OCn.

Table 7-13. Standard Frequencies for Programmable Outputs

FREQUENCY (MHz)		T0 APLL	T4 APLL		OFREQn	JITTER (TYP)	
		T0FREQ	T4FT0	T4FREQ		RMS (ps)	pk-pk (ns)
2kHz					2kHz	100	1.00
8kHz					8kHz	100	1.00
1.536	Not OC6 from T0 APLL	12 x E1	12 x E1	12 x E1	APLL/64	100	1.00
1.544	Not OC6 from DIG2				DIG1, DIG2	100	1.00
1.544	Not OC6 from T0 APLL	16 x DS1	16 x DS1	16 x DS1	APLL/64	75	0.75
1.578	Not OC6 from T0 APLL	4 x 6.312	4 x 6.312	4 x 6.312	APLL/64	60	0.60
2.048	Not OC6 from DIG2				DIG1, DIG2	100	1.00
2.048	Not OC6 from T0 APLL	12 x E1	12 x E1	12 x E1	APLL/48	100	1.00
2.048	Not OC6 from T0 APLL	16 x E1	16 x E1	16 x E1	APLL/64	70	0.70
2.104	Not OC6 from T0 APLL	4 x 6.312	4 x 6.312	4 x 6.312	APLL/48	60	0.60
2.316	Not OC6 from T0 APLL	24 x DS1	24 x DS1	24 x DS1	APLL/64	60	0.60
2.500				4 x 10	APLL/64	80	0.80
2.560				3 x 10.24	APLL/48	90	0.90
2.796				DS3	APLL/64	50	0.50
3.088	Not OC6 from DIG2				DIG1, DIG2	100	1.00
3.088	Not OC6 from T0 APLL	24 x DS1	24 x DS1	24 x DS1	APLL/48	60	0.60
3.728				DS3	APLL/48	50	0.50
4.096	Not OC6 from DIG2				DIG1, DIG2	100	1.00
4.296				2 x E3	APLL/64	70	0.70
4.860	Not OC6 from T0 APLL	77.76		77.76	APLL/64	50	0.50
5.200	OC3 only			2 x 13	APLL/20	90	0.90
5.728				2 x E3	APLL/48	70	0.70
6.144	OC3 only			3 x 10.24	APLL/20	90	0.90
6.144		12 x E1	12 x E1	12 x E1	APLL/16	100	1.00
6.176	Not OC6 from DIG2				DIG1, DIG2	100	1.00
6.176		16 x DS1	16 x DS1	16 x DS1	APLL/16	75	075
6.312	OC3 only				DIG2	100	1.00
6.312		4 x 6.312	4 x 6.312	4 x 6.312	APLL/16	60	0.60
6.480	Not OC6 from T0 APLL	77.76		77.76	APLL/48	60	0.6
8.000	OC3 only			4 x 10	APLL/20	80	0.80
8.192	Not OC6 from DIG2				DIG1, DIG2	100	1.00
8.192		12 x E1			APLL/12	100	1.00
8.192		16 x E1	16 x E1	16 x E1	APLL/16	70	0.70
8.416		4 x 6.312			APLL/12	60	0.60
9.264		24 x DS1	24 x DS1	24 x DS1	APLL/16	60	0.60
10.000	Not OC6				DIG2	100	1.00
10.000				4 x 10	APLL/16	80	0.80
10.240	OC3 only			3 x 10.24	APLL/12	90	0.90
10.400	OC3 only			3 x 10.24	APLL/10	90	0.90
11.184				DS3	APLL/16	50	0.50
12.288		12 x E1	12 x E1	12 x E1	APLL/8	100	1.00
12.288	OC3 only			2 x 13	APLL/10	90	0.90
12.352		24 x DS1			APLL/12	60	0.60
12.352		16 x DS1	16 x DS1	16 x DS1	APLL/8	75	0.75
12.352	Not OC6 from DIG2				DIG1, DIG2	100	1.00
12.500	OC3 only		GbE ÷ 16	GbE ÷ 16	APLL/20	60	0.60
12.624		4 x 6.312	4 x 6.312	4 x 6.312	APLL/8	60	0.60
13.000				2 x 13	APLL/8	90	0.90
15.360				3 x 10.24	APLL/8	90	0.90
15.552	OC3 only			77.76	APLL/20	50	0.50
16.000	OC3 only			4 x 10	APLL/10	80	0.80
16.384	Not OC6 from DIG2				DIG1, DIG2	100	1.00
16.384		12 x E1			APLL/6	100	1.00

FREQUENCY (MHz)		T0 APLL	T4 APLL		OFREQn	JITTER (TYP)	
		T0FREQ	T4FT0	T4FREQ		RMS (ps)	pk-pk (ns)
16.384		16 x E1	16 x E1	16 x E1	APLL/8	70	0.70
16.832		4 x 6.312			APLL/6	60	0.60
17.184				2 x E3	APLL/16	70	0.70
18.528		24 x DS1	24 x DS1	24 x DS1	APLL/8	60	0.60
19.440	OC3 only				DIG2	100	1.00
19.440		77.76		77.76	APLL/16	50	0.50
20.000				4 x 10	APLL/8	80	0.80
20.800				2 x 13	APLL/5	90	0.90
22.368				DS3	APLL/8	50	0.50
24.576		12 x E1	12 x E1	12 x E1	APLL/4	100	1.00
24.576				3 x 10.24	APLL/5	90	0.90
24.704		24 x DS1			APLL/6	60	0.60
24.704		16 x DS1	16 x DS1	16 x DS1	APLL/4	75	0.75
25.000	OC3 only		GbE ÷ 16	GbE ÷ 16	APLL/10	60	0.60
25.248		4 x 6.312	4 x 6.312	4 x 6.312	APLL/4	60	0.60
25.920		77.76			APLL/12	50	0.50
26.000				2 x 13	APLL/4	90	0.90
30.720				3 x 10.24	APLL/4	90	0.90
31.104	OC3 only			77.76	APLL/10	50	0.50
31.250		GbE ÷ 16	GbE ÷ 16	GbE ÷ 16	APLL/8	60	0.60
31.250					APLL/10	60	0.60
32.000				4 x 10	APLL/5	80	0.80
32.768		16 x E1	16 x E1	16 x E1	APLL/4	70	0.70
34.368				2 x E3	APLL/8	70	0.70
37.056		24 x DS1	24 x DS1	24 x DS1	APLL/4	60	0.60
38.880		77.76		77.76	APLL/8	50	0.50
40.000				4 x 10	APLL/4	80	0.80
44.736				DS3	APLL/4	50	0.50
49.152	Not OC3 from T0 APLL	12 x E1	12 x E1	12 x E1	APLL/2	100	1.00
49.408	Not OC3 from T0 APLL	16 x DS1	16 x DS1	16 x DS1	APLL/2	75	0.75
50.000			GbE ÷ 16	GbE ÷ 16	APLL/5	60	0.60
50.496	Not OC3 from T0 APLL	4 x 6.312	4 x 6.312	4 x 6.312	APLL/2	60	0.60
51.840		77.76			APLL/6	50	0.50
52.000				2 x 13	APLL/2	90	0.90
61.440				3 x 10.24	APLL/2	90	0.90
62.208				77.76	APLL/5	50	0.50
62.500		GbE ÷ 16	GbE ÷ 16	GbE ÷ 16	APLL/4	60	0.60
62.500	OC6 only from T0 APLL2				APLL/5	60	0.60
65.536	Not OC3 from T0 APLL	16 x E1	16 x E1	16 x E1	APLL/2	70	0.70
68.736				2 x E3	APLL/4	70	0.70
74.112	Not OC3 from T0 APLL	24 x DS1	24 x DS1	24 x DS1	APLL/2	60	0.60
77.76		77.76		77.76	APLL/4	50	0.50
80.000				4 x 10	APLL/2	80	0.80
89.472				DS3	APLL/2	50	0.50
98.304	OC6 only	12 x E1	12 x E1	12 x E1	APLL/1	100	1.00
98.816	OC6 only	16 x DS1	16 x DS1	16 x DS1	APLL/1	75	0.75
100.992	OC6 only	4 x 6312 kHz	4 x 6312 kHz	4 x 6312 kHz	APLL/1	60	0.60
104.000	OC6 only			2 x 13	APLL/1	90	0.90
122.880	OC6 only			3 x 10.24	APLL/1	90	0.90
125.000	Not OC3 from T0 APLL	GbE ÷ 16	GbE ÷ 16	GbE ÷ 16	APLL/2	60	0.60
131.072	OC6 only	16 x E1	16 x E1	16 x E1	APLL/1	70	0.70
137.472	OC6 only			2 x E3	APLL/2	70	0.70
148.224	OC6 only	24 x DS1	24 x DS1	24 x DS1	APLL/1	60	0.60
155.520	Not OC3 from T0 APLL	77.76		77.76	APLL/2	50	0.50
156.250	OC6 only from T0 APLL2				APLL/2	60	0.60
160.000	OC6 only			4 x 10	APLL/1	80	0.80

FREQUENCY (MHz)		T0 APLL	T4 APLL		OFREQn	JITTER (TYP)	
		T0FREQ	T4FT0	T4FREQ		RMS (ps)	pk-pk (ns)
178.944	OC6 only			DS3	APLL/1	50	0.50
250.000	OC6 only	GbE ÷ 16			APLL/1	60	0.60
274.944	OC6 only					70	0.70
311.040	OC6 only	77.76			APLL/1	50	0.50
312.500	OC6 only from T0 APLL2				APLL/2	60	0.60

7.8.2.4 OC3 and OC6 Default Frequency Select Pins

There are two sets of frequency select pins, O3F[2:0] and O6F[2:0], that control the reset default frequencies of the OC3 and OC6 output clock pins, respectively. The SONSDH pin also selects the output frequencies for some of the pin settings. There is also an interaction between O3F[2:0] and O6F[2:0] when O6F[2:0] uses some internal resource that is needed to generate certain frequencies. After reset the O3F[2:0] and O6F[2:0] pins can be used as GPIO pins and status output pins. The default output frequencies are affected by changing the register bit values of four registers: OCR2, OCR3, T0CR1, and T4CR1. The register defaults can be changed after reset using the microprocessor interface.

Table 7-14. T0FREQ Default Settings

O6F[2:0]	O3F[2:0]	SONSDH	T0CR1.T0FREQ	
=001	=001	0	010	12 x E1 DFB
		1	100	24 x DS1 DFB
!=001	X	X	001	77.76 AFB
X	!=001	X	001	77.76 AFB

Table 7-15. T4FREQ Default Settings

O6F[2:0]	O3F[2:0]	SONSDH	T4CR1.T4FREQ	
=001	X	0	0110	E3
		1	0111	DS3
X	=010	0	0110	E3
		1	0111	DS3
!=001	!=010	0	0011	16 x E1
		1	0101	16 x DS1

Table 7-16. OC6 Default Frequency Configuration

O6F[2:0]	SONSDH	FREQUENCY (MHz)	OCR3. OFREQ6	APLL SRC
000	X	0	0000	—
001	0	68.736	1111	T4
	1	22.368	1110	T4
010	X	19.44	0110	T0
011	X	25.92	0111	T0
100*	X	38.88	1000	T0
101	X	51.84	1001	T0
110	X	77.76	1010	T0
111	X	155.52	0011	T0

**Occurs when O6F[2:0] are left unconnected.*

Table 7-17. OC3 Default Frequency Configuration

O3F[2:0]	SONSDH	FREQUENCY (MHz)	O6F[2:0] =001	OCR2. OFREQ3	APLL SRC
000	X	0	X	0000	—
001	0	8.192	FALSE	1101	T4
	1	6.176		1101	T4
001	0	8.192	TRUE	0111	T0
001	1	12.352		0111	T0
010	0	68.736	X	1111	T4
010	1	22.368	X	1110	T4
011*	X	19.44	X	0110	T0
100	X	25.92	X	0111	T0
101	X	38.88	X	1000	T0
110	X	51.84	X	1001	T0
111	X	77.76	X	1010	T0

**Occurs when O3F[2:0] are left unconnected.*

7.8.2.5 FSYNC and MFSYNC Configuration

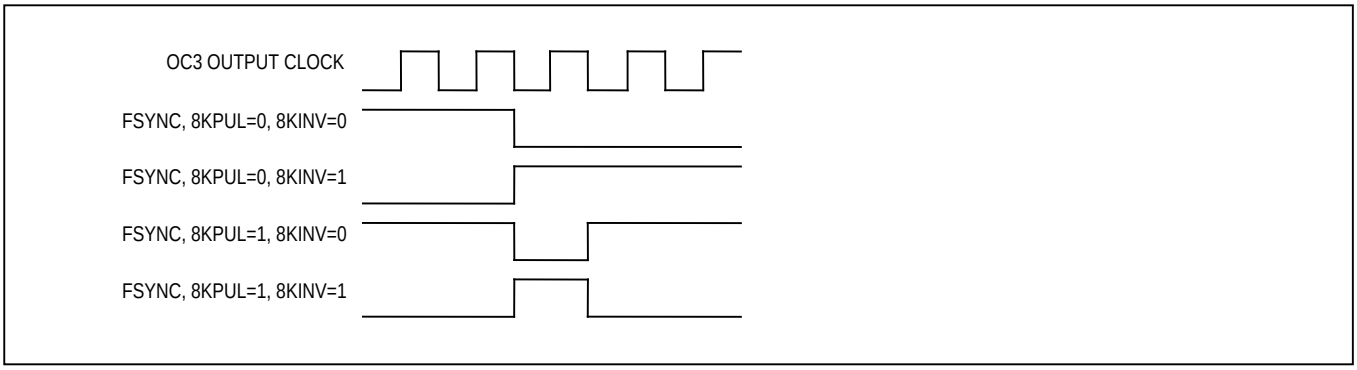
The FSYNC output is enabled by setting FSEN = 1 in the OCR4 register, while the MFSYNC output is enabled by setting MFSEN = 1 in OCR4. When disabled, these pins are driven low.

When 8KPUL = 0 in FSCR1, FSYNC is configured as an 8kHz clock with 50% duty cycle. When 8KPUL = 1, FSYNC is an 8kHz frame sync that pulses *low* once every 125µs with pulse width equal to one cycle of output clock OC3. When 8KINV = 1 in FSCR1, the clock or pulse polarity of FSYNC is inverted.

When 2KPUL = 0 in FSCR1, MFSYNC is configured as an 2kHz clock with 50% duty cycle. When 2KPUL = 1, MFSYNC is a 2kHz frame sync that pulses *low* once every 500µs with pulse width equal to one cycle of output clock OC3. When 2KINV = 1 in FSCR1, the clock or pulse polarity f MFSYNC is inverted.

If either 8KPUL = 1 or 2KPUL = 1, output clock OC3 must be generated from the T0 DPLL and must be configured for a frequency of 1.544MHz or higher or the FSYNC/MFSYNC pulses may not be generated correctly. Figure 7-3 shows how the 8KPUL and 8KINV control bits affect the FSYNC output. The 2KPUL and 2KINV bits have an identical effect on MFSYNC.

Figure 7-3. FSYNC 8kHz Options



7.8.2.6 Custom Output Frequencies

In addition to the many standard frequencies available in the device, any of the seven output DFS blocks can be configured to generate a custom frequency. Possible custom frequencies include any multiple of 2kHz up to 77.76MHz, any multiple of 8kHz up to 311.04MHz, and any multiple of 10kHz up to 388.79MHz. (An APLL must be used to achieve frequencies above 77.76MHz.) Any of the programmable output clocks can be configured to output the custom frequency or submultiples thereof. Contact Microsemi timing products technical support for help with custom frequencies.

7.9 Microprocessor Interface

The DS3106 presents an SPI interface on the $\overline{CS}$, SCLK, SDI, and SDO pins. SPI is a widely used master/slave bus protocol that allows a master device and one or more slave devices to communicate over a serial bus. The DS3106 is always a slave device. Masters are typically microprocessors, ASICs, or FPGAs. Data transfers are always initiated by the master device, which also generates the SCLK signal. The DS3106 receives serial data on the SDI pin and transmits serial data on the SDO pin. SDO is high impedance except when the DS3106 is transmitting data to the bus master.

Bit Order. When both bit 3 and bit 4 are low at device address 3FFFh, the register address and all data bytes are transmitted MSB first on both SDI and SDO. When either bit 3 or bit 4 is set to 1 at device address 3FFFh, the register address and all data bytes are transmitted LSB first on both SDI and SDO. The reset default setting and Motorola SPI convention is MSB first.

Clock Polarity and Phase. SCLK is normally low and pulses high during bus transactions. The CPHA pin sets the phase (active edge) of SCLK. When CPHA = 0, data is latched in on SDI on the leading edge of the SCLK pulse and updated on SDO on the trailing edge. When CPHA = 1, data is latched in on SDI on the trailing edge of the SCLK pulse and updated on SDO on the following leading edge. SCLK does not have to toggle between accesses, i.e., when $\overline{CS}$ is high. See Figure 7-4.

Device Selection. Each SPI device has its own chip-select line. To select the DS3106, pull its $\overline{CS}$ pin low.

Control Word. After $\overline{CS}$ is pulled low, the bus master transmits the control word during the first 16 SCLK cycles. In MSB-first mode the control word has the form:

R/$\overline{W}$ A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0 BURST

where A[13:0] is the register address, R/$\overline{W}$ is the data direction bit (1 = read, 0 = write), and BURST is the burst bit (1 = burst access, 0 = single-byte access). In LSB-first mode the order of the 14 address bits is reversed. In the discussion that follows, a control word with R/$\overline{W}$ = 1 is a read control word, while a control word with R/$\overline{W}$ = 0 is a write control word.

Single-Byte Writes. See Figure 7-5. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 0, followed by the data byte to be written. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

Single-Byte Reads. See Figure 7-5. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 0. The DS3106 then responds with the requested data byte. The bus master then terminates the transaction by pulling $\overline{CS}$ high.

Burst Writes. See Figure 7-5. After $\overline{CS}$ goes low, the bus master transmits a write control word with BURST = 1 followed by the first data byte to be written. The DS3106 receives the first data byte on SDI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the DS3106 continues to write the data received and increment its address counter. After the address counter reaches 3FFFh it rolls over to address 0000h and continues to increment.

Burst Reads. See Figure 7-5. After $\overline{CS}$ goes low, the bus master transmits a read control word with BURST = 1. The DS3106 then responds with the requested data byte on SDO, increments its address counter, and prefetches

the next data byte. If the bus master continues to demand data, the DS3106 continues to provide the data on SDO, increment its address counter, and prefetch the following byte. After the address counter reaches 3FFFh, it rolls over to address 0000h and continues to increment.

Early Termination of Bus Transactions. The bus master can terminate SPI bus transactions at any time by pulling $\overline{CS}$ high. In response to early terminations, the DS3106 resets its SPI interface logic and waits for the start of the next transaction. If a write transaction is terminated prior to the SCLK edge that latches the LSB of a data byte, the data byte is not written.

Design Option: Wiring SDI and SDO Together. Because communication between the bus master and the DS3106 is half-duplex, the SDI and SDO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the SDI/SDO line when the DS3106 is transmitting.

AC Timing. See Table 10-9 and Figure 10-3 for AC timing specifications for the SPI interface.

Figure 7-4. SPI Clock Phase Options

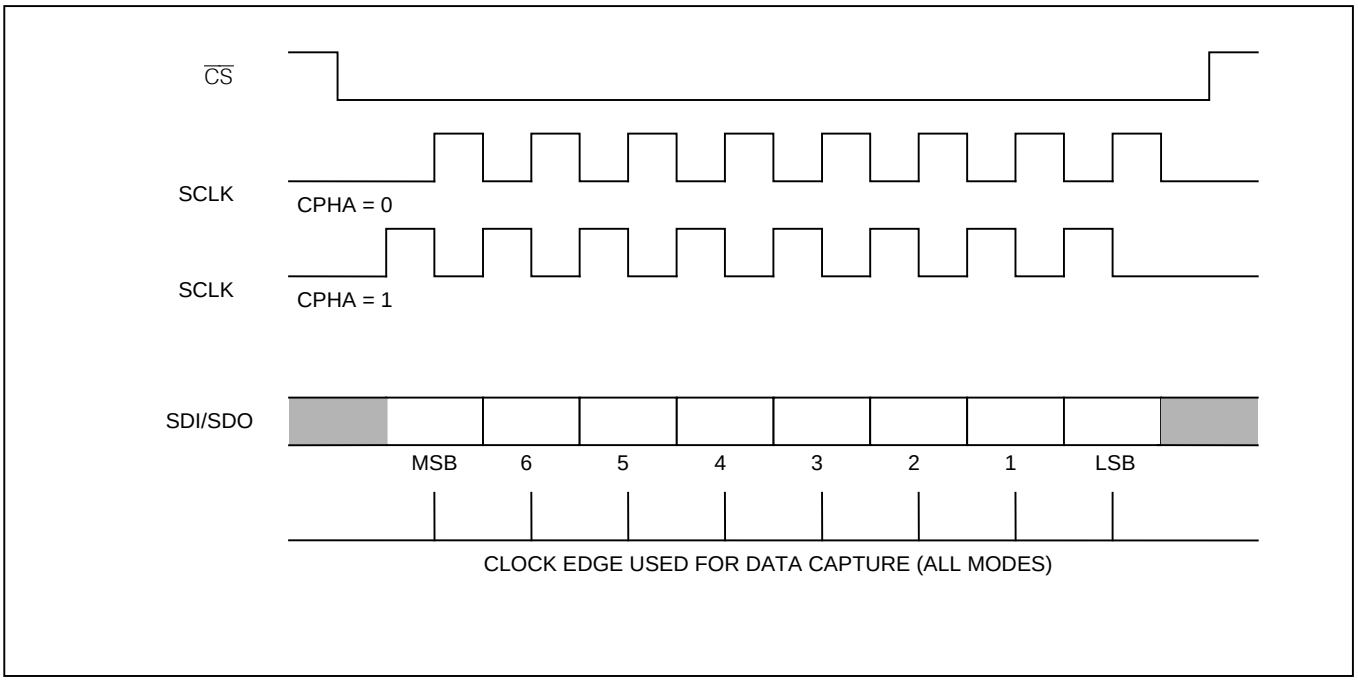
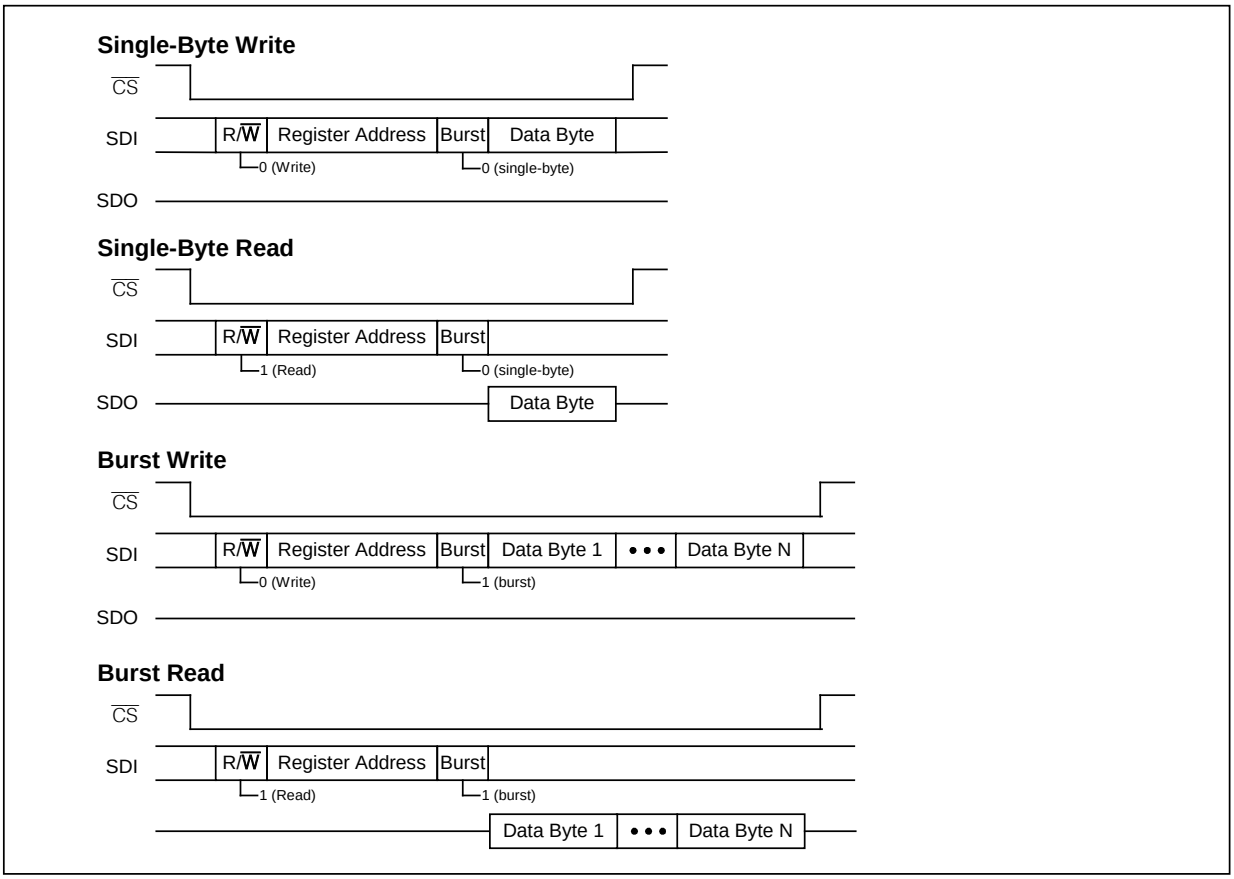


Figure 7-5. SPI Bus Transactions



7.10 Reset Logic

The device has three reset controls: the $\overline{RST}$ pin, the RST bit in MCR1, and the JTAG reset pin $\overline{JTRST}$. The $\overline{RST}$ pin asynchronously resets the entire device, except for the JTAG logic. When the $\overline{RST}$ pin is low all internal registers are reset to their default values, including those fields that latch their default values from, or based on, the states of configuration input pins when the $\overline{RST}$ goes high. **The $\overline{RST}$ pin must be asserted once after power-up while the external oscillator is stabilizing.**

The MCR1:RST bit resets the entire device (except for the microprocessor interface, the JTAG logic, and the RST bit itself), but when RST is active, the register fields with pin-programmed defaults do not latch their values from, or based on, the corresponding input pins. Instead, these fields are reset to the default values that were latched when the $\overline{RST}$ pin was last active.

Microsemi recommends holding $\overline{RST}$ low while the external oscillator starts up and stabilizes. An incorrect reset condition could result if $\overline{RST}$ is released before the oscillator has started up completely.

Important: System software must wait at least 100µs after reset ($\overline{RST}$ pin or RST bit) is deasserted before initializing the device as described in Section 7.12.

7.11 Power-Supply Considerations

Due to the DS3106's dual-power-supply nature, some I/Os have parasitic diodes between a 1.8V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the 1.8V supply and the 3.3V supply to force the 3.3V supply to be within one parasitic diode drop below the 1.8V supply (i.e., $V_{DDIO} > V_{DD}$ - ~0.4V). The second method is to ramp up the 3.3V supply first and then ramp up the 1.8V supply.

7.12 Initialization

After power-up or reset, a series of writes must be done to the DS3106 to tune it for optimal performance. This series of writes is called the initialization script. Each DS3106 die revision has a different initialization script. For the latest initialization scripts contact Microsemi timing products technical support.

Important: System software must wait at least 100µs after reset ($\overline{RST}$ pin or RST bit) is deasserted before initializing the device.

8. Register Descriptions

The DS3106 has an overall address range from 000h to 1FFh. Table 8-1 in Section 8.4 shows the register map. In each register, bit 7 is the MSB and bit 0 is the LSB. Register addresses not listed and bits marked "—" are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow Table 8-1.

Note: Systems must be able to access the entire address range from 0 to 01FFh. Proper device initialization requires a sequence of writes to addresses in the range 0180-01FFh.

8.1 Status Bits

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. When set, some latched status bits can cause an interrupt request on the INTREQ pin if enabled to do so by corresponding interrupt enable bits. ISR#.LOCK# are special-case latched status bits because they cannot create an interrupt request on the INTREQ pin and a "write 0" is needed to clear them.

8.2 Configuration Fields

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0.

8.3 Multiregister Fields

Multiregister fields—such as FREQ[18:0] in registers FREQ1, FREQ2, and FREQ3—must be handled carefully to ensure that the bytes of the field remain consistent. A write access to a multiregister field is accomplished by writing all the registers of the field in any order, with no other accesses to the device in between. If the write sequence is interrupted by another access, none of the bytes are written and the MSR4:MRAA latched status bit is set to indicate the write was aborted. A read access from a multiregister field is accomplished by reading the registers of the field in any order, with no other accesses to the device in between. When one register of a multiregister field is read, the other register(s) in the field are frozen until after they are all read. If the read sequence is interrupted by another access, the registers of the multibyte field are unfrozen and the MSR4:MRAA bit is set to indicate the read was aborted. For best results, interrupt servicing should be disabled in the microprocessor before a multiregister access and then enabled again after the access is complete. The multiregister fields are:

FIELD	REGISTERS	ADDRESSES	TYPE
FREQ[18:0]	FREQ1, FREQ2, FREQ3	0Ch, 0Dh, 07h	Read Only
MCLKFREQ[15:0]	MCLK1, MCLK2	3Ch, 3Dh	Read/Write
HARDLIM[9:0]	DLIMIT1, DLIMIT2	41h, 42h	Read/Write
DIVN[15:0]	DIVN1, DIVN2	46h, 47h	Read/Write
PHASE[15:0]	PHASE1, PHASE2	77h, 78h	Read Only

8.4 Register Definitions

Table 8-1. Register Map

Note: *Register names are hyperlinks to register definitions. Underlined fields are read-only.*

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	ID1	ID[7:0]							
01h	ID2	ID[15:8]							
02h	REV	REV[7:0]							
03h	TEST1	PALARM	D180	—	RA	0	8KPOL	0	0
05h	MSR1	—	—	—	—	IC4	IC3	—	—
06h	MSR2	STATE	SRFAIL	—	—	—	—	—	—
07h	FREQ3	—	—	—	—	—	FREQ[18:16]		
09h	OPSTATE	—	—	T0SOFT	—	—	T0STATE[2:0]		
0Ah	PTAB1	—	—	—	—	SELREF[3:0]			
0Ch	FREQ1	FREQ[7:0]							
0Dh	FREQ2	FREQ[15:8]							
0Eh	VALSR1	—	—	—	—	IC4	IC3	—	—
11h	ISR2	—	—	ACT4	—	—	—	ACT3	—
17h	MSR4	—	HORDY	MRAA	—	—	—	—	—
22h	ICR3	DIVN	LOCK8K	—	—	FREQ[3:0]			
23h	ICR4	DIVN	LOCK8K	—	—	FREQ[3:0]			
32h	MCR1	RST	—	FREN	LOCKPIN	—	T0STATE[2:0]		
34h	MCR3	—	—	XOEDGE	FRUNHO	—	SONSDH	—	—
38h	MCR6	DIG2AF	DIG2SS	DIG1SS	—	—	—	—	—
39h	MCR7	DIG2F[1:0]		DIG1F[1:0]		—	—		
3Ah	MCR8	—	—	—	—	—	—	OC6SF[1:0]	
3Bh	MCR9	AUTOBW	—	—	—	LIMINT	—	—	—
3Ch	MCLK1	MCLKFREQ[7:0]							
3Dh	MCLK2	MCLKFREQ[15:8]							
40h	HOCR3	AVG	—	—	—	—	—	—	—
41h	DLIMIT1	HARDLIM[7:0]							
42h	DLIMIT2	—	—	—	—	—	—	HARDLIM[9:8]	
43h	IER1	—	—	—	—	IC4	IC3	—	—
44h	IER2	STATE	SRFAIL	—	—	—	—	—	IC9
46h	DIVN1	DIVN[7:0]							
47h	DIVN2	DIVN[15:8]							
48h	MCR10	—	SRFPIN	—	—	—	—	—	—
4Dh	DLIMIT3	FLLOL	SOFTLIM[6:0]						
4Eh	IER4	—	HORDY	—	—	—	—	—	—
4Fh	OCR5	—	—	AOF6	—	—	AOF3	—	—
50h	LB0U	LB0U[7:0]							
51h	LB0L	LB0L[7:0]							
52h	LB0S	LB0S[7:0]							
53h	LB0D	—	—	—	—	—	—	LB0D[1:0]	
61h	OCR2	—	—	—	—	OFREQ3[3:0]			
62h	OCR3	OFREQ6[3:0]				—	—	—	—
63h	OCR4	MFSEN	FSEN	—	—	—	—	—	—
64h	T4CR1	—	—	—	—	T4FREQ[3:0]			

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
65h	T0CR1	—	T4APT0	T0FT4[2:0]			T0FREQ[2:0]		
67h	T0LBW	—	—	—	RSV1	RSV2	T0LBW[2:0]		
69h	T0ABW	—	—	—	RSV1	RSV2	T0ABW[2:0]		
6Bh	T0CR2	—	PD2G8K[2:0]			—	DAMP[2:0]		
6Dh	T0CR3	PD2EN	—	—	—	—	PD2G[2:0]		
6Eh	GPCR	GPIO4D	GPIO3D	GPIO2D	GPIO1D	GPIO4O	GPIO3O	GPIO2O	GPIO1O
6Fh	GPSR	—	—	—	—	GPIO4	GPIO3	GPIO2	GPIO1
73h	PHLIM1	FLEN	NALOL	1	—	—	FINELIM[2:0]		
74h	PHLIM2	CLEN	MCPDEN	USEMCPD	—	COARSELIM[3:0]			
76h	PHMON	NW	—	—	—	—			
77h	PHASE1	PHASE[7:0]							
78h	PHASE2	PHASE[15:8]							
7Ah	FSCR1	—	—	—	—	8KINV	8KPUL	2KINV	2KPUL
7Dh	INTCR	—	—	—	—	LOS	GPO	OD	POL
7Eh	PROT	PROT[7:0]							
7Fh-1FFh	reserved	—	—	—	—	—	—	—	—

Register Map Color Coding

	Device Identification and Protection
	Local Oscillator and Master Clock Configuration
	Input Clock Configuration
	Input Clock Monitoring
	Input Clock Selection
	DPLL Configuration
	DPLL State
	Output Clock Configuration
	Frame/Multiframe-Sync Configuration

Register Name: **ID1**
Register Description: **Device Identification Register, LSB**
Register Address: **00h**

Bit #	7	6	5	4	3	2	1	0
Name	ID[7:0]							
Default	0	0	1	0	0	0	0	0

Bits 7 to 0: Device ID (ID[7:0]). ID[15:0] = 0C22h = 3106 decimal.

Register Name: **ID2**
Register Description: **Device Identification Register, MSB**
Register Address: **01h**

Bit #	7	6	5	4	3	2	1	0
Name	ID[15:8]							
Default	0	0	0	0	1	1	0	0

Bits 7 to 0: Device ID (ID[15:8]). See the ID1 register description.

Register Name: **REV**
Register Description: **Device Revision Register**
Register Address: **02h**

Bit #	7	6	5	4	3	2	1	0
Name	REV[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Device Revision (REV[7:0]). Contact the factory to interpret this value and determine the latest revision.

Register Name: **TEST1**
Register Description: **Test Register 1 (Not Normally Used)**
Register Address: **03h**

Bit #	7	6	5	4	3	2	1	0
Name	PALARM	D180	—	RA	0	8KPOL	0	0
Default	0	0	0	1	0	1	0	0

Bit 7: Phase Alarm (PALARM). This real-time status bit indicates the state of the T0 DPLL phase-lock detector. See Section 7.7.5. (**Note:** This is not the same as T0STATE = locked.)

0 = T0 DPLL phase-lock parameters are met (FLEN, CLEN, NALOL, FLLOL)
1 = T0 DPLL loss-of-phase lock

Bit 6: Disable 180 (D180). When locking to a new reference, the T0 DPLL first tries nearest edge locking (±180°) for the first two seconds. If unsuccessful, it tries full phase/frequency locking (±360°). Disabling the nearest edge locking can reduce lock time by up to two seconds but may cause an unnecessary phase shift (up to 360°) when the new reference is close in frequency/phase to the old reference. See Section 7.7.4.

0 = Normal operation: try nearest edge locking then phase/frequency locking
1 = Phase/frequency locking only

Bit 4: Resync Analog Dividers (RA). When this bit is set the analog output dividers are always synchronized to ensure that low-frequency outputs are in sync with the higher frequency clock from the DPLL.

0 = Synchronized for the first two seconds after power-up
1 = Always synchronized

Bits 3, 1, and 0: Leave set to zero (test control).

Bit 2: 8kHz Edge Polarity (8KPOL). Specifies the input clock edge to lock to on the selected reference when it is configured for LOCK8K mode. See Section 7.4.2.

0 = Falling edge
1 = Rising edge

Register Name: **MSR1**
Register Description: **Master Status Register 1**
Register Address: **05h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	IC4	IC3	—	—
Default	1	0	1	1	1	1	1	1

Bits 3 and 2: Input Clock Status Change (IC[3:2]). Each of these latched status bits is set to 1 when the VALSR1 status bit changes state (set or cleared). Each bit is cleared when written with a 1 and not set again until the VALSR1 bit changes state again. When one of these latched status bits is set, it can cause an interrupt request on the INTREQ pin if the corresponding interrupt enable bit is set in the IER1 register. See Section 7.5 for input clock validation/invalidation criteria.

Register Name: **MSR2**
Register Description: **Master Status Register 2**
Register Address: **06h**

Bit #	7	6	5	4	3	2	1	0
Name	STATE	SRFAIL	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	1

Bit 7: T0 DPLL State Change (STATE). This latched status bit is set to 1 when the operating state of the T0 DPLL changes. STATE is cleared when written with a 1 and not set again until the operating state changes again. When STATE is set it can cause an interrupt request on the INTREQ pin if the STATE interrupt enable bit is set in the IER2 register. The current operating state can be read from the T0STATE field of the OPSTATE register. See Section 7.7.1.

Bit 6: Selected Reference Failed (SRFAIL). This latched status bit is set to 1 when the selected reference to the T0 DPLL fails, (i.e., no clock edges in two UI). SRFAIL is cleared when written with a 1. When SRFAIL is set it can cause an interrupt request on the INTREQ pin if the SRFAIL interrupt enable bit is set in the IER2 register. SRFAIL is not set in free-run mode or holdover mode. See Section 7.5.3.

Register Name: **FREQ3**
Register Description: **Frequency Register 3**
Register Address: **07h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	FREQ[18:16]		
Default	0	0	0	0	0	0	0	0

Bits 2 to 0: Current DPLL Frequency (FREQ[18:16]). See the FREQ1 register description.

Register Name: **OPSTATE**
Register Description: **Operating State Register**
Register Address: **09h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	T0SOFT	—	—	T0STATE[2:0]		
Default	1	0	0	0	0	0	0	1

Bit 5: T0 DPLL Frequency Soft Alarm (T0SOFT). This real-time status bit indicates whether the T0 DPLL is tracking its reference within the soft alarm limits specified in the SOFT[6:0] field of the DLIMIT3 register. See Section 7.7.5.

0 = No alarm; frequency is within the soft alarm limits
1 = Soft alarm; frequency is outside the soft alarm limits

Bits 2 to 0: T0 DPLL Operating State (T0STATE[2:0]). This real-time status field indicates the current state of the T0 DPLL state machine. Values not listed below correspond to invalid (unused) states. See Section 7.7.1.

001 = Free-run
010 = Holdover
100 = Locked
101 = Prelocked 2
110 = Prelocked
111 = Loss-of-lock

Register Name: **PTAB1**
Register Description: **Priority Table Register 1**
Register Address: **0Ah**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	SELREF[3:0]			
Default	0	0	0	0	see below			

Bits 3 to 0: Selected Reference (SELREF[3:0]). This real-time status field indicates the current selected reference for the T0 DPLL. The default value for this field is 0011b if the SRCSW pin is 1 during reset and 0100b if SRCSW is 0 during reset.

0000 = No valid input reference available
0001 to 0010 = {unused values}
0011 = Input IC3
0100 = Input IC4
0101 to 1111 = {unused values}

Register Name: **FREQ1**
Register Description: **Frequency Register 1**
Register Address: **0Ch**

Bit #	7	6	5	4	3	2	1	0
Name	FREQ[7:0]							
Default	0	0	0	0	0	0	0	0

Note: *The FREQ1, FREQ2, and FREQ3 registers must be read consecutively. See Section 8.3.*

Bits 7 to 0: Current DPLL Frequency (FREQ[7:0]). The full 19-bit FREQ[18:0] field spans this register, FREQ2, and FREQ3. FREQ is a two's-complement signed integer that expresses the current frequency as an offset with respect to the master clock frequency (see Section 7.3). Because the value in this register field is derived from the DPLL integral path, it can be considered an average frequency with a rate of change inversely proportional to the DPLL bandwidth. If LIMINT = 1 in the MCR9 register, the value of FREQ freezes when the DPLL reaches its minimum or maximum frequency. The frequency offset in ppm is equal to FREQ[18:0] × 0.0003068. See Section 7.7.1.6.

Application Note: Frequency measurements are relative, i.e., they measure the frequency of the selected reference with respect to the local oscillator. As such, when a frequency difference exists, it is difficult to distinguish whether the selected reference is off frequency or the local oscillator is off frequency. In systems with timing card redundancy, the use of two timing cards, master and slave, can address this difficulty. Both master and slave have separate local oscillators, and each measures the selected reference. These two measurements provide the necessary information to distinguish which reference is off frequency, if we make the simple assumption that at most one reference has a significant frequency deviation at any given time (i.e., a single point of failure). If both master and slave indicate a significant frequency offset, then the selected reference must be off frequency. If the master indicates a frequency offset but the slave does not, then the master's local oscillator must be off frequency. Likewise, if the slave indicates a frequency offset but the master does not, the slave's local oscillator must be off frequency.

Register Name: **FREQ2**
Register Description: **Frequency Register 2**
Register Address: **0Dh**

Bit #	7	6	5	4	3	2	1	0
Name	FREQ[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Current DPLL Frequency (FREQ[15:8]). See the FREQ1 register description.

Register Name: **VALSR1**
Register Description: **Input Clock Valid Status Register 1**
Register Address: **0Eh**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	IC4	IC3	—	—
Default	0	0	0	0	0	0	0	0

Bits 3 and 2: Input Clock Valid Status (IC[3:2]). Each of these real-time status bits is set to 1 when the corresponding input clock is valid. An input is valid if it has no active alarms (ACT = 0 in the ISR2 register). See also the MSR1 register and Section 7.5.

0 = Invalid
1 = Valid

Register Name: **ISR2**
Register Description: **Input Status Register 2**
Register Address: **11h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	ACT4	—	—	—	ACT3	—
Default	0	0	1	0	0	0	1	0

Bit 5: Activity Alarm for Input Clock 4 (ACT4). This real-time status bit is set to 1 when the leaky bucket accumulator for IC4 reaches the alarm threshold specified in the LBxU register (where x in LBxU is specified in the BUCKET field of ICR4). An activity alarm clears the IC4 status bit in the VALSR1 register, invalidating the IC4 clock. See Section 7.5.2.

Bit 1: Activity Alarm for Input Clock 3 (ACT3). This bit has the same behavior as the ACT4 bit but for the IC3 input clock.

Register Name: **MSR4**
Register Description: **Master Status Register 4**
Register Address: **17h**

Bit #	7	6	5	4	3	2	1	0
Name	—	HORDY	MRAA	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 6: Holdover Frequency Ready (HORDY). This latched status bit is set to 1 when the T0 DPLL has a holdover value that has been averaged over the one-second holdover averaging period. HORDY is cleared when written with a 1. When HORDY is set it can cause an interrupt request on the INTREQ pin if the HORDY interrupt enable bit is set in the IER4 register. See Section 7.7.1.6.

Bit 5: Multiregister Access Aborted (MRAA). This latched status bit is set to 1 when a multibyte access (read or write) is interrupted by another access to the device. MRAA is cleared when written with a 1. MRAA cannot cause an interrupt to occur. See Section 8.3.

Register Name: **ICR3, ICR4**
Register Description: **Input Configuration Register 3, 4**
Register Address: **22h, 23h**

Bit #	7	6	5	4	3	2	1	0
Name	DIVN	LOCK8K	—	—	FREQ[3:0]			
Default	0	0	0	0	see below			

Note: *These registers are identical in function. ICRx is the control register for input clock ICx.*

Bit 7: DIVN Mode (DIVN). When DIVN is set to 1 and LOCK8K = 0, the input clock is divided down by a programmable predivider. The resulting output clock is then passed to the DPLL. All input clocks for which DIVN = 1 are divided by the factor specified in DIVN1 and DIVN2. When DIVN = 1 and LOCK8K = 0 in an ICR register, the FREQ field of that register must be set to the input frequency divided by the divide factor. When DIVN = 1 and LOCK8K = 1 in an ICR register, the FREQ field of that register is decoded as the alternate frequencies. See Sections 7.4.2.2 and 7.4.2.4.

0 = Disabled
1 = Enabled

Bit 6: LOCK8K Mode (LOCK8K). When LOCK8K is set to 1 and DIVN = 0, the input clock is divided down by a preset predivider. The resulting output clock, which is always 8kHz, is then passed to the DPLL. LOCK8K is ignored when DIVN = 0 and FREQ[3:0] = 1001 (2kHz) or 1010 (4kHz). When DIVN = 1 and LOCK8K = 1 in an ICR register, the FREQ field of that register is decoded as the alternate frequencies. See Sections 7.4.2.2 and 7.4.2.3

0 = Disabled
1 = Enabled

Bits 3 to 0: Input Clock Frequency (FREQ[3:0]). When DIVN = 0 and LOCK8K = 0 (standard direct-lock mode), this field specifies the input clock's nominal frequency for direct-lock operation. When DIVN = 0 and LOCK8K = 1 (LOCK8K mode), this field specifies the input clock's nominal frequency for LOCK8K operation. When DIVN = 1 and LOCK8K = 0 (DIVN mode), this field specifies the frequency after the DIVN divider (i.e., input frequency divided by DIVN + 1). When DIVN = 1 and LOCK8K = 1 (alternate direct-lock frequencies), this field specifies the input clock's nominal frequency for direct-lock operation.

DIVN = 0 or LOCK8K = 0: (Standard direct-lock mode, LOCK8K mode, or DIVN mode)

0000 = 8kHz
0001 = 1544kHz or 2048kHz (as determined by SONSDH bit in the MCR3 register)
0010 = 6.48MHz
0011 = 19.44MHz
0100 = 25.92MHz
0101 = 38.88MHz
0110 = 51.84MHz
0111 = 77.76MHz
1000 = 155.52MHz (only valid for LVDS inputs)
1001 = 2kHz
1010 = 4kHz
1011 = 6312kHz
1100 = 5MHz
1101 = 31.25 MHz (not a multiple of 8 kHz and therefore not valid for LOCK8K mode)
1110–1111 = undefined

DIVN = 1 and LOCK8K = 1: (Alternate direct-lock frequency decode)

0000 = 10MHz (internally divided down to 5MHz)
0001 = 25MHz (internally divided down to 5MHz)
0010 = 62.5MHz (internally down to 31.25MHz)
0011 = 125MHz (internally down to 31.25MHz)
0101–1111 = undefined

FREQ[3:0] Default Values:

See Table 7-2.

Register Name: **MCR1**
Register Description: **Master Configuration Register 1**
Register Address: **32h**

Bit #	7	6	5	4	3	2	1	0
Name	RST	—	FREN	LOCKPIN	—	T0STATE[2:0]		
Default	0	0	1	0	0	0	0	0

Bit 7: Device Reset (RST). When this bit is high the entire device is held in reset, and all register fields, except the RST bit itself, are reset to their default states. When RST is active, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. Instead these fields are reset to the default values that were latched from the pins when the RST pin was last active. See Section 7.10.

0 = Normal operation
1 = Reset

Bit 5: Frequency Range Detect Enable (FREN). When this bit is high the frequency of each input clock is measured and used to quickly declare the input inactive. See Section 7.5.1.

0 = Frequency range detect disabled.
1 = Frequency range detect enabled.

Bit 4: T0 DPLL LOCK Pin Enable (LOCKPIN). When this bit is high the LOCK pin indicates when the T0 DPLL state machine is in the LOCK state (OPSTATE.T0STATE = 100).

0 = LOCK pin is not driven.
1 = LOCK pin is driven high when the T0 DPLL is in the lock state.

Bits 2 to 0: T0 DPLL State Control (T0STATE[2:0]). This field allows the T0 DPLL state machine to be forced to a specified state. The state machine remains in the forced state, and, therefore, cannot react to alarms and other events as long as T0STATE is not equal to 000. See Section 7.7.1.

000 = Automatic (normal state machine operation)
001 = Free-run
010 = Holdover
011 = {unused value}
100 = Locked
101 = Prelocked 2
110 = Prelocked
111 = Loss-of-lock

Register Name: **MCR3**
Register Description: **Master Configuration Register 3**
Register Address: **34h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	XOEDGE	FRUNHO	—	SONSDH	—	—
Default	1	1	0	0	0	see below	1	0

Bit 5: Local Oscillator Edge (XOEDGE). This bit specifies the significant clock edge of the local oscillator clock signal on the REFCLK input pin. The faster edge should be selected for best jitter performance. See Section 7.3.

0 = Rising edge
1 = Falling edge

Bit 4: Free-Run Holdover (FRUNHO). When this bit is set to 1 the T0 DPLL holdover frequency is set to 0ppm so the output frequency accuracy is set by the external oscillator accuracy. This affects both mini-holdover and the holdover state.

0 = Digital holdover
1 = Free-run holdover, 0ppm

Bit 2: SONET or SDH Frequencies (SONSDH). This bit specifies the clock rate for input clocks with FREQ = 0001 in the ICR registers (20h to 28h). During reset the default value of this bit is latched from the SONSDH pin. See Section 7.4.2.

0 = 2048kHz
1 = 1544kHz

Register Name: **MCR6**
Register Description: **Master Configuration Register 6**
Register Address: **38h**

Bit #	7	6	5	4	3	2	1	0
Name	DIG2AF	DIG2SS	DIG1SS	—	—	—	—	—
Default	0	see below	see below	1	1	1	1	1

Bit 7: Digital Alternate Frequency (DIG2AF). Selects alternative frequencies.

0 = Digital2 N x E1 or N x DS1 frequency specified by DIG2SS and MCR7:DIG2F.
1 = Digital2 6.312MHz, 10MHz, or N x 19.44MHz frequency specified by DIG2SS and MCR7:DIG2F.

Bit 6: Digital2 SONET or SDH Frequencies (DIG2SS). This bit specifies whether the clock rates generated by the Digital2 clock synthesizer are multiples of 1.544MHz (SONET compatible) or multiples of 2.048MHz (SDH compatible) or alternate frequencies. The specific multiple is set in the DIG2F field of the MCR7 register. When $\overline{RST}$ = 0 the default value of this bit is latched from the SONSDH pin.

DIG2AF = 0:
  0 = Multiples of 2048kHz
  1 = Multiples of 1544kHz
DIG2AF = 1:
  6.312MHz, 10MHz, or N x 19.44MHz

Bit 5: Digital1 SONET or SDH Frequencies (DIG1SS). This bit specifies whether the clock rates generated by the Digital1 clock synthesizer are multiples of 1544kHz (SONET compatible) or multiples of 2048kHz (SDH compatible). The specific multiple is set in the DIG1F field of the MCR7 register. When $\overline{RST}$ = 0 the default value of this bit is latched from the SONSDH pin.

0 = Multiples of 2048kHz
1 = Multiples of 1544kHz

Register Name: **MCR7**
Register Description: **Master Configuration Register 7**
Register Address: **39h**

Bit #	7	6	5	4	3	2	1	0
Name	DIG2F[1:0]		DIG1F[1:0]		—	—	—	—
Default	0	0	0	0	1	0	0	0

Bits 7 and 6: Digital2 Frequency (DIG2F[1:0]). This field, MCR6:DIG2SS, and MCR6:DIG2AF configure the frequency of the Digital2 clock synthesizer.

DIG2AF = 0		DIG2AF = 1	
DIG2SS = 1	**DIG2SS = 0**	**DIG2SS = 1**	**DIG2SS = 0**
00 = 1544kHz	00 = 2048kHz	00 = 19.44MHz	00 = 6.312MHz
01 = 3088kHz	01 = 4096kHz	01 = 38.88MHz	01 = undefined
10 = 6176kHz	10 = 8192kHz	10 = undefined	10 = 10MHz
11 = 12,352kHz	11 = 16,384kHz	11 = undefined	11 = undefined

Bits 5 and 4: Digital1 Frequency (DIG1F[1:0]). This field and MCR6:DIG1SS configure the frequency of the Digital1 clock synthesizer.

DIG1SS = 1	DIG1SS = 0
00 = 1544kHz	00 = 2048kHz
01 = 3088kHz	01 = 4096kHz
10 = 6176kHz	10 = 8192kHz
11 = 12,352kHz	11 = 16,384kHz

Register Name: **MCR8**
Register Description: **Master Configuration Register 8**
Register Address: **3Ah**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	OC6SF[1:0]	
Default	0	0	0	0	0	0	1	0

For Rev A2 devices, in LVPECL mode the differential output voltage will be higher than the MAX V_{ODPECL} spec in Table 10-5 unless an adjustment register is written with the proper value. If differential voltages larger than $V_{ODPECL,MAX}$ are unacceptable, the following procedures must be followed when writing the OC6SF fields in this register. If differential voltages larger than $V_{ODPECL,MAX}$ are acceptable, only the OC6SF field must be written.

Procedure to configure OC6 for LVPECL mode:
1) Set the OC6SF[1:0] field to 01b.
2) Write 01h to address 01FFh.
3) Write 55h to the adjustment register at address 01D8h.
4) Write 00h to address 01FFh.

Procedure to configure OC6 for LVDS mode:
1) Set the OC6SF[1:0] field to 10b.
2) Write 01h to address 01FFh.
3) Write 00h to the adjustment register at address 01D8h.
4) Write 00h to address 01FFh.

Bits 1 and 0: Output Clock 6 Signal Format (OC6SF[1:0]). See Section 7.8.1.

00 = Output disabled (powered down)
01 = 3V LVPECL level compatible
10 = 3V LVDS compatible (default)
11 = 3V LVDS compatible

Register Name: **MCR9**
Register Description: **Master Configuration Register 9**
Register Address: **3Bh**

Bit #	7	6	5	4	3	2	1	0
Name	AUTOBW	—	—	—	LIMINT	—	—	—
Default	1	1	1	1	1	0	1	1

Bit 7: Automatic Bandwidth Selection (AUTOBW). See Section 7.7.2.

0 = Always selects locked bandwidth from the T0LBW register.
1 = Automatically selects either locked bandwidth (T0LBW register) or acquisition bandwidth (T0ABW register) as appropriate.

Bit 3: Limit Integral Path (LIMINT). When this bit is set to 1, the T0 DPLL's integral path is limited (i.e., frozen) when the DPLL reaches minimum or maximum frequency, as set by the HARDLIM field in DLIMIT1 and DLIMIT2. When the integral path is frozen, the current DPLL frequency in registers FREQ1, FREQ2, and FREQ3 is also frozen. Setting LIMINT = 1 minimizes overshoot when the DPLL is pulling in. See Section 7.7.2.

0 = Do not freeze integral path at min/max frequency.
1 = Freeze integral path at min/max frequency.

Register Name: **MCLK1**
Register Description: **Master Clock Frequency Adjustment Register 1**
Register Address: **3Ch**

Bit #	7	6	5	4	3	2	1	0
Name	MCLKFREQ[7:0]							
Default	1	0	0	1	1	0	0	1

Note: *The MCLK1 and MCLK2 registers must be read consecutively and written consecutively. See Section 8.3.*

Bits 7 to 0: Master Clock Frequency Adjustment (MCLKFREQ[7:0]). The full 16-bit MCLKFREQ[15:0] field spans this register and MCLK2. MCLKFREQ is an unsigned integer that adjusts the frequency of the internal 204.8MHz master clock with respect to the frequency of the local oscillator clock on the REFCLK pin by up to +514ppm and -771ppm. The master clock adjustment has the effect of speeding up the master clock with a positive adjustment and slowing it down with a negative adjustment. For example, if the oscillator connected to REFCLK has an offset of +1ppm, the adjustment should be -1ppm to correct the offset.

The formulas below translate adjustments to register values and vice versa. The default register value of 39,321 corresponds to 0ppm. See Section 7.3.

MCLKFREQ[15:0] = adjustment_in_ppm / 0.0196229 + 39,321

adjustment_in_ppm = (MCLKFREQ[15:0] – 39,321) × 0.0196229

Register Name: **MCLK2**
Register Description: **Master Clock Frequency Adjustment Register 2**
Register Address: **3Dh**

Bit #	7	6	5	4	3	2	1	0
Name	MLCKFREQ[15:8]							
Default	1	0	0	1	1	0	0	1

Bits 7 to 0: Master Clock Frequency Adjustment (MCLKFREQ[15:8]). See the MCLK1 register description.

Register Name: **HOCR3**
Register Description: **Holdover Configuration Register 3**
Register Address: **40h**

Bit #	7	6	5	4	3	2	1	0
Name	AVG	—	—	—	—	—	—	—
Default	1	0	0	0	1	0	0	0

Note: *See Section 8.3 for important information about writing and reading this register.*

Bit 7: Averaging (AVG). When this bit is set to 1 the T0 DPLL uses the averaged frequency value during holdover mode. When FRUNHO = 1 in the MCR3 register, this bit is ignored. See Section 7.7.1.6.

0 = Not averaged frequency; holdover frequency is either free-run (FRUNHO = 1) or instantaneously frozen.
1 = Averaged frequency over the last one second while locked to the input.

Register Name: **DLIMIT1**
Register Description: **DPLL Frequency Limit Register 1**
Register Address: **41h**

Bit #	7	6	5	4	3	2	1	0
Name	HARDLIM[7:0]							
Default	1	1	1	1	1	1	1	1

Note: *The DLIMIT1 and DLIMIT2 registers must be read consecutively and written consecutively. See Section 8.3.*

Bits 7 to 0: DPLL Hard Frequency Limit (HARDLIM[7:0]). The full 10-bit HARDLIM[9:0] field spans this register and DLIMIT2. HARDLIM is an unsigned integer that specifies the hard frequency limit or pull-in/hold-in range of the T0 DPLL. When frequency limit detection is enabled by setting FLLOL = 1 in the DLIMIT3 register. If the DPLL frequency exceeds the hard limit the DPLL declares loss-of-lock. The hard frequency limit in ppm is ±HARDLIM[9:0] × 0.0782. The default value is normally ±79.794ppm (3FFh). See Section 7.7.5.

Register Name: **DLIMIT2**
Register Description: **DPLL Frequency Limit Register 1**
Register Address: **42h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	HARDLIM[9:8]	
Default	0	0	0	0	0	0	1	1

Bits 1 and 0: DPLL Hard Frequency Limit (HARDLIM[9:8]). See the DLIMIT1 register description.

Register Name: **IER1**
Register Description: **Interrupt Enable Register 1**
Register Address: **43h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	IC4	IC3	—	—
Default	0	0	0	0	0	0	0	0

Bits 3 and 2: Interrupt Enable for Input Clock Status Change (IC[3:2]). Each of these bits is an interrupt enable control for the corresponding bit in the MSR1 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: **IER2**
Register Description: **Interrupt Enable Register 2**
Register Address: **44h**

Bit #	7	6	5	4	3	2	1	0
Name	STATE	SRFAIL	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 7: Interrupt Enable for T0 DPLL State Change (STATE). This bit is an interrupt enable for the STATE bit in the MSR2 register.

0 = Mask the interrupt
1 = Enable the interrupt

Bit 6: Interrupt Enable for Selected Reference Failed (SRFAIL). This bit is an interrupt enable for the SRFAIL bit in the MSR2 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: **DIVN1**
Register Description: **DIVN Register 1**
Register Address: **46h**

Bit #	7	6	5	4	3	2	1	0
Name	DIVN[7:0]							
Default	1	1	1	1	1	1	1	1

Note: *The DIVN1 and DIVN2 registers must be read consecutively and written consecutively. See Section 8.3.*

Bits 7 to 0: DIVN Factor (DIVN[7:0]). The full 16-bit DIVN[15:0] field spans this register and DIVN2. This field contains the integer value used to divide the frequency of input clocks that are configured for DIVN mode. The frequency is divided by DIVN[15:0] + 1. See Section 7.4.2.4.

Register Name: **DIVN2**
Register Description: **DIVN Register 2**
Register Address: **47h**

Bit #	7	6	5	4	3	2	1	0
Name	DIVN[15:8]							
Default	0	0	1	1	1	1	1	1

Bits 7 to 0: DIVN Factor (DIVN[15:8]). See the DIVN1 register description.

Register Name: **MCR10**
Register Description: **Master Configuration Register 10**
Register Address: **48h**

Bit #	7	6	5	4	3	2	1	0
Name	—	SRFPIN	—	—	—	—	—	—
Default	1	0	0	1	0	0	0	0

Bit 6: SRFAIL Pin Enable (SRFPIN). When this bit is set to 1, the SRFAIL pin is enabled. When enabled the SRFAIL pin follows the state of the SRFAIL status bit in the MSR2 register. This gives the system a very fast indication of the failure of the current reference. See Section 7.5.3.

0 = SRFAIL pin disabled (high impedance)
1 = SRFAIL pin enabled

Register Name: **DLIMIT3**
Register Description: **DPLL Frequency Limit Register 3**
Register Address: **4Dh**

Bit #	7	6	5	4	3	2	1	0
Name	FLLOL	SOFTLIM[6:0]						
Default	1	0	0	0	1	1	1	0

Bit 7: Frequency Limit Loss-of-Lock (FLLOL). When this bit is set to 1, the T0 DPLL internally declares loss-of-lock when the hard frequency limit in the DLIMIT1 and DLIMIT2 registers is reached. See Section 7.7.5.

0 = DPLL declares loss-of-lock normally.
1 = DPLL also declares loss-of-lock when the hard frequency limit is reached.

Bits 6 to 0: DPLL Soft Frequency Limit (SOFTLIM[6:0]). This field is an unsigned integer that specifies the soft frequency limit for the T0 DPLL. The soft limit is only used for monitoring; exceeding this limit does not cause loss-of-lock. The limit in ppm is ±SOFTLIM[6:0] × 0.628. The default value is ±8.79ppm. When the T0 DPLL frequency reaches the soft limit, the T0SOFT status bit is set in the OPSTATE register. See Section 7.7.5.

Register Name: **IER4**
Register Description: **Interrupt Enable Register 4**
Register Address: **4Eh**

Bit #	7	6	5	4	3	2	1	0
Name	—	HORDY	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 6: Interrupt Enable for Holdover Frequency Ready (HORDY). This bit is an interrupt enable for the HORDY bit in the MSR4 register.

0 = Mask the interrupt
1 = Enable the interrupt

Register Name: **OCR5**
Register Description: **Output Configuration Register 1**
Register Address: **4Fh**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	AOF6	—	—	AOF3	—	—
Default	0	0	0	0	0	0	0	0

Bit 5: Alternate Output Frequency Mode Select 6 (AOF6). This bit controls the decoding of the OCR3.OFREQ6 field for the OC6 pin.

0 = Standard decodes
1 = Alternate decodes

Bit 2: Alternate Output Frequency Mode Select 3 (AOF3). This bit controls the decoding of the OCR2.OFREQ3 field for the OC3 pin.

0 = Standard decodes
1 = Alternate decodes

Register Name: **LB0U**
Register Description: **Leaky Bucket 0 Upper Threshold Register**
Register Address: **50h**

Bit #	7	6	5	4	3	2	1	0
Name	LB0U[7:0]							
Default	0	0	0	0	0	1	1	0

Bits 7 to 0: Leaky Bucket 0 Upper Threshold (LB0U[7:0]). When the leaky bucket accumulator is equal to the value stored in this field, the activity monitor declares an activity alarm by setting the input clock's ACT bit in the ISR2 register. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

Register Name: **LB0L**
Register Description: **Leaky Bucket 0 Lower Threshold Register**
Register Address: **51h**

Bit #	7	6	5	4	3	2	1	0
Name	LB0L[7:0]							
Default	0	0	0	0	0	1	0	0

Bits 7 to 0: Leaky Bucket 0 Lower Threshold (LB0L[7:0]). When the leaky bucket accumulator is equal to the value stored in this field, the activity monitoring logic clears the activity alarm (if previously declared) by clearing the input clock's ACT bit in the ISR2 register. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

Register Name: **LB0S**
Register Description: **Leaky Bucket 0 Size Register**
Register Address: **52h**

Bit #	7	6	5	4	3	2	1	0
Name	LB0S[7:0]							
Default	0	0	0	0	1	0	0	0

Bits 7 to 0: Leaky Bucket 0 Size (LB0S[7:0]). This field specifies the maximum value of the leaky bucket. The accumulator cannot increment past this value. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

Register Name: **LB0D**
Register Description: **Leaky Bucket 0 Decay Rate Register**
Register Address: **53h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	—	—	LB0D[1:0]	
Default	0	0	0	0	0	0	0	1

Bits 1 and 0: Leaky Bucket 0 Decay Rate (LB0D[1:0]). This field specifies the decay or "leak" rate of the leaky bucket accumulator. For each period of 1, 2, 4, or 8 128ms intervals in which no irregularities are detected on the input clock, the accumulator decrements by 1. Registers LB0U, LB0L, LB0S, and LB0D together specify leaky bucket configuration 0. See Section 7.5.2.

00 = decrement every 128ms (8 units/second)
01 = decrement every 256ms (4 units/second)
10 = decrement every 512ms (2 units/second)
11 = decrement every 1024ms (1 unit/second)

Register Name: **OCR2**
Register Description: **Output Configuration Register 2**
Register Address: **61h**

Bit #	7	6	5	4	3	2	1	0
Name	0	0	0	0	OFREQ3[3:0]			
Default	0	0	0	0	see below			

Bits 3 to 0: Output Frequency of OC3 (OFREQ3[3:0]). This field specifies the frequency of output clock OC3. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The default frequency is set by the O3F[2:0] bits. See Table 7-17. The decode of this field is controlled by the value of the OCR5.AOF3 bit.

AOF3 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = Digital2 (see Table 7-7)
0100 = Digital1 (see Table 7-6)
0101 = T0 APLL frequency divided by 48
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF3 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T0 APLL frequency divided by 64
0010 = T4 APLL frequency divided by 20
0011 = T4 APLL frequency divided by 12
0100 = T4 APLL frequency divided by 10
0101 = T4 APLL frequency divided by 5
0110 = T4 APLL frequency divided by 2
0111 = undefined
1000 = T0 selected reference (after dividing)
1001–1111 = undefined

Register Name: **OCR3**
Register Description: **Output Configuration Register 3**
Register Address: **62h**

Bit #	7	6	5	4	3	2	1	0
Name	OFREQ6[3:0]				0	0	0	0
Default	see below				0	0	0	0

Bits 7 to 4: Output Frequency of OC6 (OFREQ6[3:0]). This field specifies the frequency of output clock output OC6. The frequencies of the T0 APLL and T4 APLL are configured in the T0CR1 and T4CR1 registers. The Digital1 and Digital2 frequencies are configured in the MCR7 register. See Section 7.8.2.3. The default frequency is set by the OC6[2:0] bits. See Table 7-16. The decode of this field is controlled by the value of the OCR5.AOF6 bit.

AOF6 = 0: (standard decodes)

0000 = Output disabled (i.e., low)
0001 = 2kHz
0010 = 8kHz
0011 = T0 APLL frequency divided by 2
0100 = Digital1 (see Table 7-6)
0101 = T0 APLL frequency
0110 = T0 APLL frequency divided by 16
0111 = T0 APLL frequency divided by 12
1000 = T0 APLL frequency divided by 8
1001 = T0 APLL frequency divided by 6
1010 = T0 APLL frequency divided by 4
1011 = T4 APLL frequency divided by 64
1100 = T4 APLL frequency divided by 48
1101 = T4 APLL frequency divided by 16
1110 = T4 APLL frequency divided by 8
1111 = T4 APLL frequency divided by 4

AOF6 = 1: (alternate decodes)

0000 = Output disabled (i.e., low)
0001 = T4 APLL frequency divided by 5
0010 = T4 APLL frequency divided by 2
0011 = T4 APLL frequency
0100 = T0 APLL2 frequency divided by 5
0101 = T0 APLL2 frequency divided by 2
0110 = T0 APLL2 frequency
0111 = T4 selected reference (after dividing)
1000 = T0 selected reference (after dividing)
1001–1111 = undefined

Register Name: **OCR4**
Register Description: **Output Configuration Register 4**
Register Address: **63h**

Bit #	7	6	5	4	3	2	1	0
Name	MFSEN	FSEN	0	0	0	0	0	0
Default	1	1	0	0	0	0	0	0

Bit 7: MFSYNC Enable (MFSEN). This configuration bit enables the 2kHz output on the MFSYNC pin. See Section 7.8.2.5.

0 = Disabled, driven low
1 = Enabled, output is 2kHz

Bit 6: FSYNC Enable (FSEN). This configuration bit enables the 8kHz output on the FSYNC pin. See Section 7.8.2.5.

0 = Disabled, driven low
1 = Enabled, output is 8kHz

Register Name: **T4CR1**
Register Description: **T4 DPLL Configuration Register 1**
Register Address: **64h**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	T4FREQ[3:0]			
Default	0	0	0	0	see below			

Bits 3 to 0: T4 APLL Frequency (T4FREQ[3:0]). When T0CR1:T4APT0 = 0, this field configures the T4 APLL DFS frequency. The T4 APLL DFS frequency affects the frequency of the T4 APLL which, in turn, affects the available output frequencies on the output clock pins (see the OCR registers). See Section 7.8.2. The default value of this field is controlled by the O6F[2:0] and O3F[2:0] pins as described in Table 7-15.

T4FREQ[3:0]	T4 APLL DFS FREQUENCY	T4 APLL FREQUENCY (4 x T4 APLL DFS)
0000	APLL output disabled	Disabled, output is low
0001	77.76MHz	311.04MHz (4 x 77.76MHz)
0010	24.576MHz (12 x E1)	98.304MHz (48 x E1)
0011	32.768MHz (16 x E1)	131.072MHz (64 x E1)
0100	37.056MHz (24 x DS1)	148.224MHz (96 x DS1)
0101	24.704MHz (16 x DS1)	98.816MHz (64 x DS1)
0110	68.736MHz (2 x E3)	274.944MHz (8 x E3)
0111	44.736MHz (DS3)	178.944MHz (4 x DS3)
1000	25.248MHz (4 x 6312kHz)	100.992MHz (16 x 6312kHz)
1001	62.500MHz (GbE ÷ 16)	250.000MHz (GbE ÷ 4)
1010	30.720MHz (3 x 10.24)	122.880MHz (12 x 10.24)
1011	40.000MHz (4 x 10MHz)	160.000MHz (16 x 10MHz)
1100	26.000MHz (2 x 13MHz)	104.000MHz (8 x 13MHz)
1101–1111	{unused values}	{unused values}

Register Name: **T0CR1**
Register Description: **T0 DPLL Configuration Register 1**
Register Address: **65h**

Bit #	7	6	5	4	3	2	1	0
Name	—	T4APT0	T0FT4[2:0]			T0FREQ[2:0]		
Default	0	0	0	0	0	see below		

Bit 6: T4 APLL Source from T0 (T4APT0). When this bit is set to 0, T4CR1:T4FREQ configures the T4 APLL DFS frequency. The T4 APLL DFS frequency affects the frequency of the T4 APLL, which, in turn, affects the available output frequencies on the output clock pins (see the OCR registers). When this bit is set to 1, the frequency of the T4 APLL DFS is configured by the T0CR1:T0FT4[2:0] field below. See Section 7.8.2.

0 = T4 APLL frequency is determined by T4FREQ.
1 = T4 APLL frequency is determined by T0FT4.

Bits 5 to 3: T0 Frequency to T4 APLL (T0FT4[2:0]). When the T4APT0 bit is set to 1, this field specifies the frequency of the T4 APLL DFS. This frequency can be different than the frequency specified by T0CR1:T0FREQ. See Section 7.8.2.

T0FT4	T4 APLL DFS FREQUENCY	T4 APLL FREQUENCY (4 x T4 APLL DFS)
000 =	24.576MHz (12 x E1)	98.304MHz (48 x E1)
001 =	62.500MHz (GbE ÷ 16)	250.000MHz (GbE ÷ 4)
010 =	32.768MHz (16 x E1)	131.072MHz (64 x E1)
011 =	{unused value}	{unused value}
100 =	37.056MHz (24 x DS1)	148.224MHz (96 x DS1)
101 =	{unused value}	{unused value}
110 =	24.704MHz (16 x DS1)	98.816MHz (64 x DS1)
111 =	25.248MHz (4 x 6312kHz)	100.992MHz (16 x 6312kHz)

Bits 2 to 0: T0 DPLL Output Frequency (T0FREQ[2:0]). This field configures the T0 APLL DFS frequency. The T0 APLL DFS frequency affects the frequency of the T0 APLL, which, in turn, affects the available output frequencies on the output clock pins (see the OCR registers). See Section 7.8.2. The default frequency is controlled by the O6F[2:0] and O3F[2:0] pins as described in Table 7-14.

T0FREQ	T0 APLL DFS FREQUENCY	T0 APLL FREQUENCY (4 x T0 APLL DFS)
000 =	77.76MHz	311.04MHz (4 x 77.76MHz)
001 =	77.76MHz	311.04MHz (4 x 77.76MHz)
010 =	24.576MHz (12 x E1)	98.304MHz (48 x E1)
011 =	32.768MHz (16 x E1)	131.072MHz (64 x E1)
100 =	37.056MHz (24 x DS1)	148.224MHz (96 x DS1)
101 =	24.704MHz (16 x DS1)	98.816MHz (64 x DS1)
110 =	25.248MHz (4 x 6312kHz)	100.992MHz (16 x 6312kHz)
111 =	62.500MHz (GbE ÷ 16)	250.000MHz (GbE ÷ 4)

Register Name: **T0LBW**
Register Description: **T0 DPLL Locked Bandwidth Register**
Register Address: **67h**

Bit #	7	6	5	4	3	2	1	0
Name	0	0	0	RSV1	RSV2	T0LBW[2:0]		
Default	0	0	0	0	0	0	0	0

Bits 4 and 3: Reserved Bit 1 and 2 (RSV[1:2]). These bits are reserved for future use, and can be written to and read back.

Bits 2 to 0: T0 DPLL Locked Bandwidth (T0LBW[2:0]). This field configures the bandwidth of the T0 DPLL when locked to an input clock. When AUTOBW = 0 in the MCR9 register, the T0LBW bandwidth is used for acquisition and for locked operation. When AUTOBW = 1, T0ABW bandwidth is used for acquisition while T0LBW bandwidth is used for locked operation. See Section 7.7.2.

111 = 18Hz
000 = 35Hz (default)
001 = 70Hz
010 = {unused value, undefined}
011 = 18Hz
100 = 120Hz
101 = 250Hz
110 = 400Hz

Register Name: **T0ABW**
Register Description: **T0 DPLL Acquisition Bandwidth Register**
Register Address: **69h**

Bit #	7	6	5	4	3	2	1	0
Name	0	0	0	RSV1	RSV2	T0ABW[2:0]		
Default	0	0	0	0	0	0	0	1

Bits 4 and 3: Reserved Bit 1 and 2 (RSV[1:2]). These bits are reserved for future use, and can be written to and read back.

Bits 2 to 0: T0 DPLL Acquisition Bandwidth (T0ABW[2:0]). This field configures the bandwidth of the T0 DPLL when acquiring lock. When AUTOBW = 0 in the MCR9 register, the T0LBW bandwidth is used for acquisition and for locked operation. When AUTOBW = 1, T0ABW bandwidth is used for acquisition while T0LBW bandwidth is used for locked operation. See Section 7.7.2.

111 = 18Hz
000 = 35Hz
001 = 70Hz (default)
010 = {unused value, undefined}
011 = 18Hz
100 = 120Hz
101 = 250Hz
110 = 400Hz

Register Name: **T0CR2**
Register Description: **T0 Configuration Register 2**
Register Address: **6Bh**

Bit #	7	6	5	4	3	2	1	0
Name	—	PD2G8K[2:0]			—	DAMP[2:0]		
Default	0	0	0	1	0	1	0	0

Bits 6 to 4: Phase Detector 2 Gain, 8kHz (PD2G8K[2:0]). This field specifies the gain of the T0 phase detector 2 with an input clock of 8kHz or less. This value is only used if automatic gain selection is enabled by setting PD2EN = 1 in the T0CR3 register. See Section 7.7.4.

Bits 2 to 0: Damping Factor (DAMP[2:0]). This field configures the damping factor of the T0 DPLL. Damping factor is a function of both DAMP[2:0] and the T0 DPLL bandwidth (T0ABW and T0LBW). The default value corresponds to a damping factor of 5. See Section 7.7.3.

	18Hz	**35Hz**	**≥ 70Hz**
001 =	1.2	1.2	1.2
010 =	2.5	2.5	2.5
011 =	5	5	5
100 =	5	10	10
101 =	5	10	20
000, 110, and 111 =	{unused values}		

The gain peak for each damping factor is shown below:

DAMPING FACTOR	**GAIN PEAK (dB)**
1.2	0.4
2.5	0.2
5	0.1
10	0.06
20	0.03

Register Name: **T0CR3**
Register Description: **T0 Configuration Register 3**
Register Address: **6Dh**

Bit #	7	6	5	4	3	2	1	0
Name	PD2EN	—	—	—	—	PD2G[2:0]		
Default	1	1	0	0	0	0	1	0

Bit 7: Phase Detector 2 Gain Enable (PD2EN). When this bit is set to 1, the T0 phase detector 2 is enabled and the gain is determined by the input locking frequency. If the frequency is greater than 8kHz, the gain is set by the PD2G field. If the frequency is less than or equal to 8kHz, the gain is set by the PD2G8K field in the T0CR2 register. See Section 7.7.4.

0 = Disable
1 = Enable

Bits 2 to 0: Phase Detector 2 Gain (PD2G[2:0]). This field specifies the gain of the T0 phase detector 2 when the input frequency is greater than 8kHz. This value is only used if automatic gain selection is enabled by setting PD2EN = 1. See Section 7.7.4.

Register Name: **GPCR**
Register Description: **GPIO Configuration Register**
Register Address: **6Eh**

Bit #	7	6	5	4	3	2	1	0
Name	GPIO4D	GPIO3D	GPIO2D	GPIO1D	GPIO4O	GPIO3O	GPIO2O	GPIO1O
Default	0	0	0	0	0	0	0	0

Bit 7: GPIO4 Direction (GPIO4D). This bit configures the data direction for the GPIO4 pin. When GPIO4 is an input, its current state can be read from GPSR:GPIO4. When GPIO4 is an output, its value is controlled by the GPIO4O configuration bit.

0 = Input
1 = Output

Bit 6: GPIO3 Direction (GPIO3D). This bit configures the data direction for the GPIO3 pin. When GPIO3 is an input, its current state can be read from GPSR:GPIO3. When GPIO3 is an output, its value is controlled by the GPIO3O configuration bit.

0 = Input
1 = Output

Bit 5: GPIO2 Direction (GPIO2D). This bit configures the data direction for the GPIO2 pin. When GPIO2 is an input, its current state can be read from GPSR:GPIO2. When GPIO2 is an output, its value is controlled by the GPIO2O configuration bit.

0 = Input
1 = Output

Bit 4: GPIO1 Direction (GPIO1D). This bit configures the data direction for the GPIO1 pin. When GPIO1 is an input, its current state can be read from GPSR:GPIO1. When GPI13 is an output, its value is controlled by the GPIO1O configuration bit.

0 = Input
1 = Output

Bit 3: GPIO4 Output Value (GPIO4O). When GPIO4 is configured as an output (GPIO4D = 1), this bit specifies the output value.

0 = Low
1 = High

Bit 2: GPIO3 Output Value (GPIO3O). When GPIO3 is configured as an output (GPIO3D = 1), this bit specifies the output value.

0 = Low
1 = High

Bit 1: GPIO2 Output Value (GPIO2O). When GPIO2 is configured as an output (GPIO2D = 1), this bit specifies the output value.

0 = Low
1 = High

Bit 0: GPIO1 Output Value (GPIO1O). When GPIO1 is configured as an output (GPIO1D = 1), this bit specifies the output value.

0 = Low
1 = High

Register Name: **GPSR**
Register Description: **GPIO Status Register**
Register Address: **6Fh**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	GPIO4	GPIO3	GPIO2	GPIO1
Default	0	0	0	0	0	1	0	0

Bit 3: GPIO4 State (GPIO4). This bit indicates the current state of the GPIO4 pin.

0 = Low
1 = High

Bit 2: GPIO3 State (GPIO3). This bit indicates the current state of the GPIO3 pin.

0 = Low
1 = High

Bit 2: GPIO2 State (GPIO2). This bit indicates the current state of the GPIO2 pin.

0 = Low
1 = High

Bit 1: GPIO1 State (GPIO1). This bit indicates the current state of the GPIO1 pin.

0 = Low
1 = High

Register Name: **PHLIM1**
Register Description: **Phase Limit Register 1**
Register Address: **73h**

Bit #	7	6	5	4	3	2	1	0
Name	FLEN	NALOL	1	—	—	FINELIM[2:0]		
Default	1	0	1	0	0	0	1	0

Bit 7: Fine Phase Limit Enable (FLEN). This configuration bit enables the fine phase limit specified in the FINELIM[2:0] field. The fine limit must be disabled for multi-UI jitter tolerance (see PHLIM2 fields). See Section 7.7.5.

0 = Disabled
1 = Enabled

Bit 6: No Activity Loss-of-Lock (NALOL). The T0 and the T4 DPLLs can detect that an input clock has no activity very quickly (within two clock cycles). When NALOL = 0, loss-of-lock is not declared when clock cycles are missing, and nearest edge locking (±180°) is used when the clock recovers. This gives tolerance to missing cycles. When NALOL = 1, loss-of-lock is indicated as soon as no activity is detected, and the device switches to phase/frequency locking (±360°). See Sections 7.5.3 and 7.7.5.

0 = No activity does not trigger loss-of-lock.
1 = No activity does trigger loss-of-lock.

Bit 5: Leave set to 1 (test control).

Bits 2 to 0: Fine Phase Limit (FINELIM[2:0]). This field specifies the fine phase limit window, outside of which loss-of-lock is declared. The FLEN bit enables this feature. The phase of the input clock has to be inside the fine limit window for two seconds before phase lock is declared. Loss-of-lock is declared immediately if the phase of the input clock is outside the phase limit window. The default value of 010 is appropriate for most situations. See Section 7.7.5.

000 = Always indicates loss-of-phase lock—do not use
001 = Small phase limit window, ±45° to ±90°
010 = Normal phase limit window, ±90° to ±180° (default)
100, 101, 110, 111 = Proportionately larger phase limit window

Register Name: **PHLIM2**
Register Description: **Phase Limit Register 2**
Register Address: **74h**

Bit #	7	6	5	4	3	2	1	0
Name	CLEN	MCPDEN	USEMCPD	—	COARSELIM[3:0]			
Default	1	1	1	0	0	1	0	1

Bit 7: Coarse Phase Limit Enable (CLEN). This configuration bit enables the coarse phase limit specified in the COARSELIM[3:0] field. See Section 7.7.5.

0 = Disabled
1 = Enabled

Bit 6: Multicycle Phase Detector Enable (MCPDEN). This configuration bit enables the multicycle phase detector and allows the DPLL to tolerate large-amplitude jitter and wander. The range of this phase detector is the same as the coarse phase limit specified in the COARSELIM[3:0] field. See Section 7.7.4.

0 = Disabled
1 = Enabled

Bit 5: Use Multicycle Phase Detector in the DPLL Algorithm (USEMCPD). This configuration bit enables the DPLL algorithm to use the multicycle phase detector so that a large phase measurement drives faster DPLL pull-in. When USEMCPD = 0, phase measurement is limited to ±360°, giving slower pull-in at higher frequencies but with less overshoot. When USEMCPD = 1, phase measurement is set as specified in the COARSELIM[3:0] field, giving faster pull-in. MCPDEN should be set to 1 when USEMCPD = 1. See Section 7.7.4.

0 = Disabled
1 = Enabled

Bits 3 to 0: Coarse Phase Limit (COARSELIM[3:0]). This field specifies the coarse phase limit and the tracking range of the multicycle phase detector. The CLEN bit enables this feature. If jitter tolerance greater than 0.5UI is required and the input clock is a high-frequency signal, the DPLL can be configured to track phase errors over many UI using the multicycle phase detector. See Section 7.7.4 and 7.7.5.

0000 = ±1UI
0001 = ±3UI
0010 = ±7UI
0011 = ±15UI
0100 = ±31UI
0101 = ±63UI
0110 = ±127UI
0111 = ±255UI
1000 = ±511UI
1001 = ±1023UI
1010 = ±2047UI
1011 = ±4095UI
1100–1111 = ±8191UI

Register Name: **PHMON**
Register Description: **Phase Monitor Register**
Register Address: **76h**

Bit #	7	6	5	4	3	2	1	0
Name	NW	—	—	—	—	—	—	—
Default	0	0	0	0	0	1	1	0

Bit 7: Low-Frequency Input Clock Noise Window (NW). For 2kHz, 4kHz, or 8kHz input clocks, this configuration bit enables a ±5% tolerance noise window centered around the expected clock edge location. Noise-induced edges outside this window are ignored, reducing the possibility of phase hits on the output clocks. This only applies to the T0 DPLL and should be enabled only when the T0 DPLL is locked to an input and the 180° phase detector is being used (TEST1.D180=0).

0 = All edges are recognized by the T0 DPLL.
1 = Only edges within the ±5% tolerance window are recognized by the T0 DPLL.

Register Name: **PHASE1**
Register Description: **Phase Register 1**
Register Address: **77h**

Bit #	7	6	5	4	3	2	1	0
Name	PHASE[7:0]							
Default	0	0	0	0	0	0	0	0

Note: *The PHASE1 and PHASE2 registers must be read consecutively. See Section 8.3.*

Bits 7 to 0: Current DPLL Phase (PHASE[7:0]). The full 16-bit PHASE[15:0] field spans this register and the PHASE2 register. PHASE is a two's-complement signed integer that indicates the current value of the phase detector. The value is the output of the phase averager. The averaged phase difference in degrees is equal to PHASE × 0.707. See Section 7.7.6.

Register Name: **PHASE2**
Register Description: **Phase Register 2**
Register Address: **78h**

Bit #	7	6	5	4	3	2	1	0
Name	PHASE[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Current DPLL Phase (PHASE[15:8]). See the PHASE1 register description.

Register Name: **FSCR1**
Register Description: **Frame-Sync Configuration Register 1**
Register Address: **7Ah**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	8KINV	8KPUL	2KINV	2KPUL
Default	0	0	0	0	0	0	0	0

Bit 3: 8kHz Invert (8KINV). When this bit is set to 1, the 8kHz signal on clock output FSYNC is inverted. See Section 7.8.2.5.

0 = FSYNC not inverted
1 = FSYNC inverted

Bit 2: 8kHz Pulse (8KPUL). When this bit is set to 1, the 8kHz signal on clock output FSYNC is pulsed rather than 50% duty cycle. In this mode output clock OC3 must be enabled, and the pulse width of FSYNC is equal to the clock period of OC3. See Section 7.8.2.5.

0 = FSYNC not pulsed; 50% duty cycle
1 = FSYNC pulsed, with pulse width equal to OC3 period

Bit 1: 2kHz Invert (2KINV). When this bit is set to 1, the 2kHz signal on clock output MFSYNC is inverted. See Section 7.8.2.5.

0 = MFSYNC not inverted
1 = MFSYNC inverted

Bit 0: 2kHz Pulse (2KPUL). When this bit is set to 1, the 2kHz signal on clock output MFSYNC is pulsed rather than 50% duty cycle. In this mode output clock OC3 must be enabled, and the pulse width of MFSYNC is equal to the clock period of OC3. See Section 7.8.2.5.

0 = MFSYNC not pulsed; 50% duty cycle
1 = MFSYNC pulsed, with pulse width equal to OC3 period

Register Name: **INTCR**
Register Description: **Interrupt Configuration Register**
Register Address: **7Dh**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	LOS	GPO	OD	POL
Default	0	0	0	0	1	0	1	0

Bit 3: INTREQ Pin Mode (LOS). When GPO = 0, this bit selects the function of the INTREQ pin.

0 = The INTREQ/LOS pin indicates interrupt requests.
1 = The INTREQ/LOS pin indicates the real-time state of the selected reference activity monitor (see Section 7.5.3).

Bit 2: INTREQ Pin General-Purpose Output Enable (GPO). When set to 1, this bit configures the interrupt request pin to be a general-purpose output whose value is set by the POL bit.

0 = INTREQ is function determined by the LOS bit.
1 = INTREQ is a general-purpose output.

Bit 1: INTREQ Pin Open-Drain Enable (OD)

When GPO = 0:
0 = INTREQ is driven in both inactive and active states.
1 = INTREQ is driven high or low in the active state but is high impedance in the inactive state.
When GPO = 1:
0 = INTREQ is driven as specified by POL.
1 = INTREQ is high impedance and POL has no effect.

Bit 0: INTREQ Pin Polarity (POL)

When GPO = 0:
0 = INTREQ goes low to signal an interrupt request or LOS = 1 (active low).
1 = INTREQ goes high to signal interrupt request or LOS = 1 (active high).
When GPO = 1:
0 = INTREQ driven low.
1 = INTREQ driven high.

Register Name: **PROT**
Register Description: **Protection Register**
Register Address: **7Eh**

Bit #	7	6	5	4	3	2	1	0
Name	PROT[7:0]							
Default	1	0	0	0	0	1	0	1

Bits 7 to 0: Protection Control (PROT[7:0]). This field can be used to protect the rest of the register set from inadvertent writes. In protected mode writes to all other registers are ignored. In single unprotected mode, one register (other than PROT) can be written, but after that write the device reverts to protected mode (and the value of PROT is internally changed to 00h). In fully unprotected mode all registers can be written without limitation. See Section 7.2.

1000 0101 = Fully unprotected mode
1000 0110 = Single unprotected mode
All other values = Protected mode

9. JTAG Test Access Port and Boundary Scan

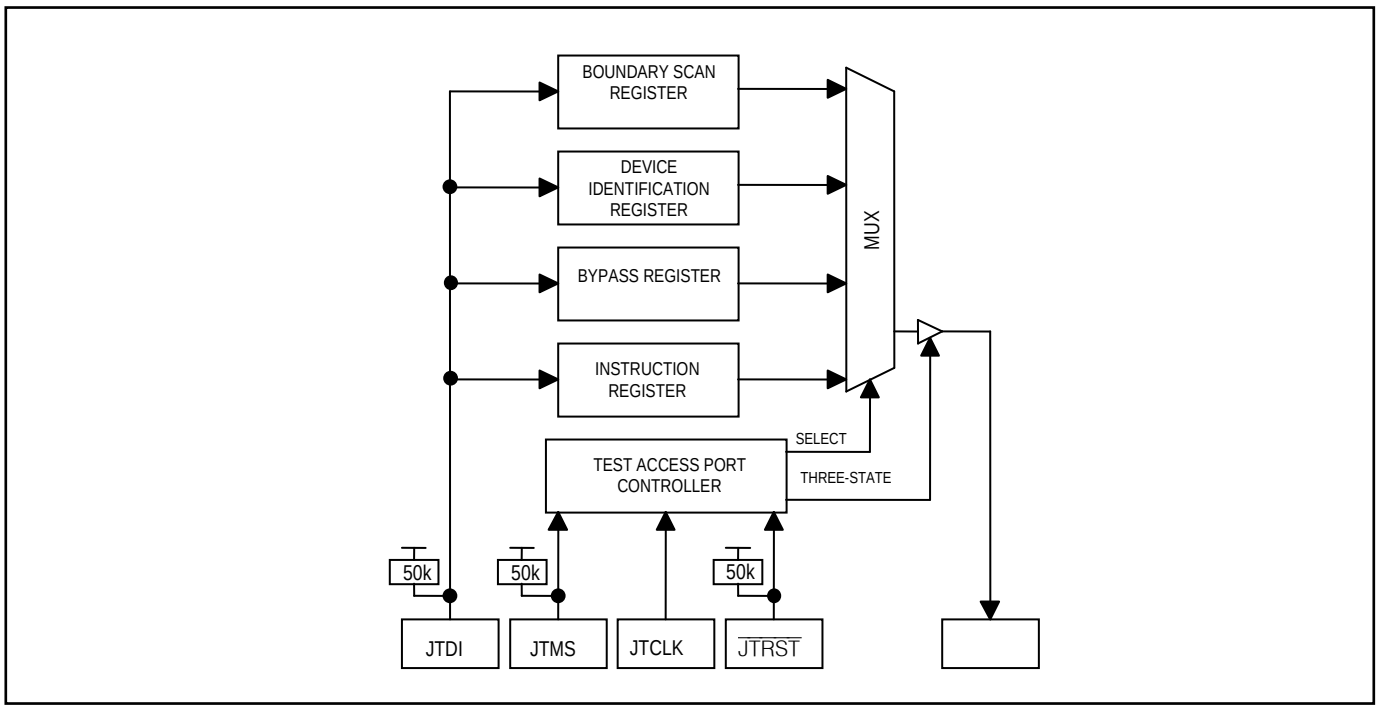
9.1 JTAG Description

The DS3106 supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. Figure 9-1 shows a block diagram. The DS3106 contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture:

Test Access Port (TAP)	Bypass Register
TAP Controller	Boundary Scan Register
Instruction Register	Device Identification Register

The TAP has the necessary interface pins, namely JTCLK, $\overline{\text{JTRST}}$, JTDI, JTDO, and JTMS. Details on these pins can be found in Table 6-5. Details about the boundary scan architecture and the TAP can be found in IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994.

Figure 9-1. JTAG Block Diagram



9.2 JTAG TAP Controller State Machine Description

This section discusses the operation of the TAP controller state machine. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK. Each of the states denoted in Figure 9-2 is described in the following paragraphs.

Test-Logic-Reset. Upon device power-up, the TAP controller starts in the Test-Logic-Reset state. The instruction register contains the IDCODE instruction. All system logic on the device operates normally.

Run-Test-Idle. Run-Test-Idle is used between scan operations or during specific tests. The instruction register and all test registers remain idle.

Select-DR-Scan. All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-SCAN state.

Capture-DR. Data can be parallel-loaded into the test register selected by the current instruction. If the instruction does not call for a parallel load or the selected test register does not allow parallel loads, the register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or to the Exit1-DR state if JTMS is high.

Shift-DR. The test register selected by the current instruction is connected between JTDI and JTDO and data is shifted one stage toward the serial output on each rising edge of JTCLK. If a test register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state, which terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

Pause-DR. Shifting of the test registers is halted while in this state. All test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

Exit2-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

Update-DR. A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the test registers into the data output latches. This prevents changes at the parallel output because of changes in the shift register. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan. All test registers retain their previous state. The instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR. The Capture-IR state is used to load the shift register in the instruction register with a fixed value. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

Shift-IR. In this state, the instruction register's shift register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK toward the serial output. The parallel register and the test registers remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state, while moving data one stage through the instruction shift register.

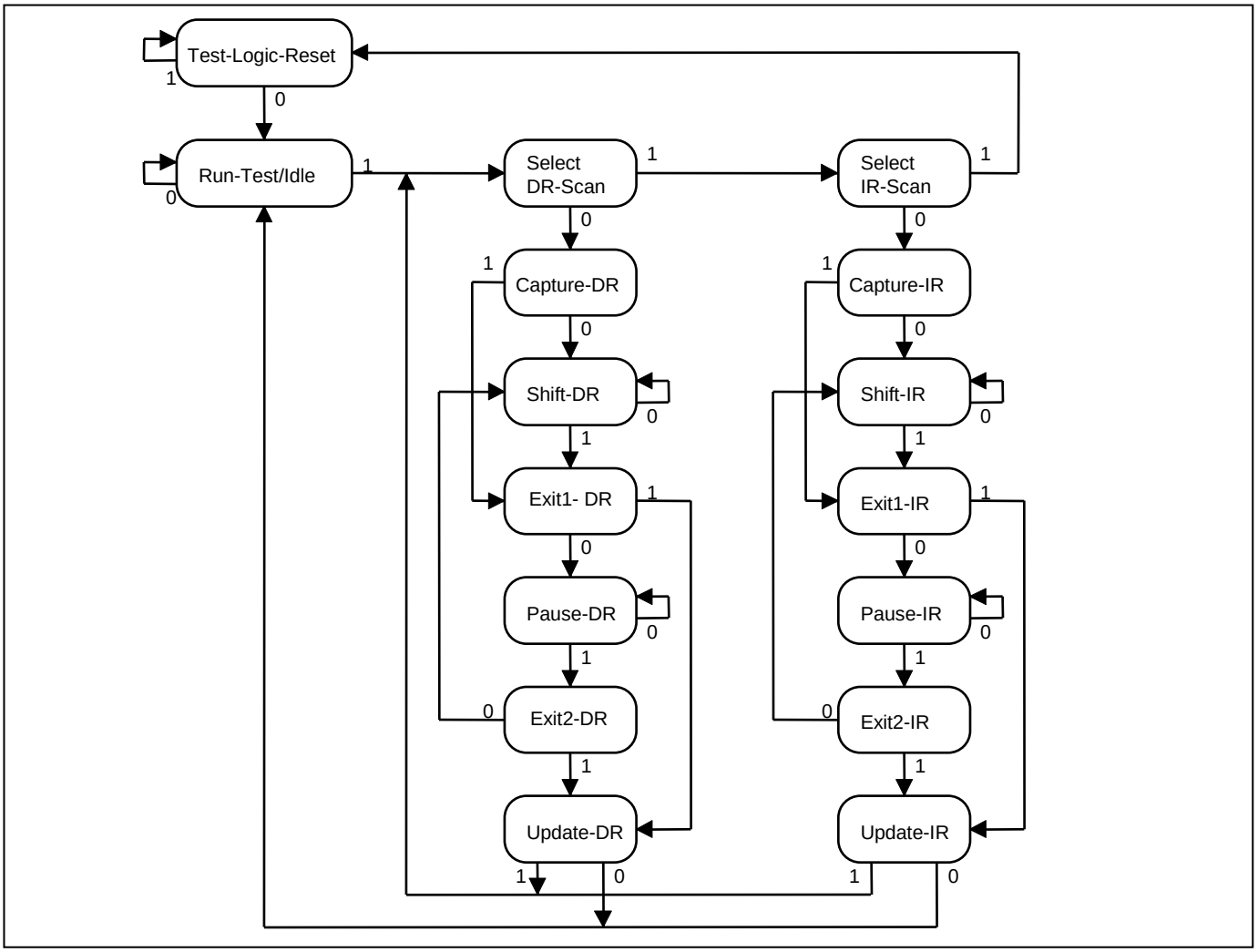
Exit1-IR. A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminates the scanning process.

Pause-IR. Shifting of the instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR. A rising edge on JTCLK with JTMS high puts the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

Update-IR. The instruction shifted into the instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Figure 9-2. JTAG TAP Controller State Machine



9.3 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Table 9-1 shows the instructions supported by the DS3106 and their respective operational binary codes.

Table 9-1. JTAG Instruction Codes

INSTRUCTIONS	SELECTED REGISTER	INSTRUCTION CODES
SAMPLE/PRELOAD	Boundary Scan	010
BYPASS	Bypass	111
EXTEST	Boundary Scan	000
CLAMP	Bypass	011
HIGHZ	Bypass	100
IDCODE	Device Identification	001

SAMPLE/PRELOAD. SAMPLE/RELOAD is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. First, the digital I/Os of the device can be sampled at the boundary scan register, using the Capture-DR state, without interfering with the device's normal operation. Second, data can be shifted into the boundary scan register through JTDI using the Shift-DR state.

EXTEST. EXTEST allows testing of the interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur: (1) Once the EXTEST instruction is enabled through the Update-IR state, the parallel outputs of the digital output pins are driven. (2) The boundary scan register is connected between JTDI and JTDO. (3) The Capture-DR state samples all digital inputs into the boundary scan register.

BYPASS. When the BYPASS instruction is latched into the parallel instruction register, JTDI is connected to JTDO through the 1-bit bypass register. This allows data to pass from JTDI to JTDO without affecting the device's normal operation.

IDCODE. When the IDCODE instruction is latched into the parallel instruction register, the device identification register is selected. The device ID code is loaded into the device identification register on the rising edge of JTCLK, following entry into the Capture-DR state. Shift-DR can be used to shift the ID code out serially through JTDO. During Test-Logic-Reset, the ID code is forced into the instruction register's parallel output.

HIGHZ. All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO.

CLAMP. All digital output pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction.

9.4 JTAG Test Registers

IEEE 1149.1 requires a minimum of two test registers—the bypass register and the boundary scan register. An optional test register, the identification register, has been included in the device design. It is used with the IDCODE instruction and the Test-Logic-Reset state of the TAP controller.

Bypass Register. This is a single 1-bit shift register used with the BYPASS, CLAMP, and HIGHZ instructions to provide a short path between JTDI and JTDO.

Boundary Scan Register. This register contains a shift register path and a latched parallel output for control cells and digital I/O cells. The BSDL file is available on the DS3106 page of Microsemi's website.

Identification Register. This register contains a 32-bit shift register and a 32-bit latched parallel output. It is selected during the IDCODE instruction and when the TAP controller is in the Test-Logic-Reset state. The device identification code for the DS3106 is shown in Table 9-2.

Table 9-2. JTAG ID Code

DEVICE	REVISION	DEVICE CODE	MANUFACTURER CODE	REQUIRED
DS3106	Consult factory	0000000010100100	00010100001	1

10. Electrical Characteristics

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin with Respect to V_{SS} (except V_{DD}).....-0.3V to +5.5V
Supply Voltage Range (V_{DD}) with Respect to V_{SS}.....-0.3V to +1.98V
Supply Voltage Range (V_{DDIO}) with Respect to V_{SS}.....-0.3V to +3.63V
Ambient Operating Temperature Range.....-40°C to +85°C (**Note 1**)
Junction Operating Temperature Range.....-40°C to +125°C
Storage Temperature Range.....-55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow)
Lead(Pb)-free .....+260°C
Containing lead(Pb).....+240°C

Note 1: Specifications to -40°C are guaranteed by design and not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device. Ambient operating temperature range when device is mounted on a four-layer JEDEC test board with no airflow.

Note: The typical values listed in the tables of Section 10 are not production tested.

10.1 DC Characteristics

Table 10-1. Recommended DC Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage, Core	V_{DD}		1.62	1.8	1.98	V
Supply Voltage, I/O	V_{DDIO}		3.135	3.3	3.465	V
Ambient Temperature Range	T_A		-40		+85	°C
Junction Temperature Range	T_J		-40		+125	°C

Table 10-2. DC Characteristics

(V_{DD} = 1.8V ±10%; V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current, Core	I_{DD}	(Notes 2, 3)		151	185	mA
Supply Current, I/O	I_{DDIO}	(Notes 2, 3)		37	50	mA
Supply Current from VDD_OC6 When Output OC6 Enabled	I_{DDOC6}	(Note 4)		16		mA
Input Capacitance	C_{IN}			5		pF
Output Capacitance	C_{OUT}			7		pF

Note 2: 12.800MHz clock applied to REFCLK and 19.44MHz clock applied to one CMOS/TTL input clock pin. Output clock pin OC3 at 19.44MHz driving 100pF load; all other inputs at V_{DDIO} or grounded; all other outputs disabled and open.

Note 3: TYP current measured at V_{DD} = 1.8V and V_{DDIO} = 3.3V, MAX current measured at V_{DD} = 1.98V and V_{DDIO} = 3.465V.

Note 4: 19.44MHz output clock frequency, driving the load shown in Figure 10-1. Enabled means MCR8:OC6SF ≠ 00.

Table 10-3. CMOS/TTL Pins

(V_{DD} = 1.8V ±10%; V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2.0		5.5	V
Input Low Voltage	V_{IL}		-0.3		+0.8	V
Input Leakage	I_{IL}	(Note 1)	-10		+10	µA
Input Leakage, Pins with Internal Pullup Resistor (50kΩ typ)	I_{ILPU}	(Note 1)	-100		+10	µA
Input Leakage, Pins with Internal Pulldown Resistor (50kΩ typ)	I_{ILPD}	(Note 1)	-10		+100	µA
Output Leakage (when High-Z)	I_{LO}	(Note 1)	-10		+10	µA
Output High Voltage (I_O = -4.0mA)	V_{OH}		2.4		V_{DDIO}	V
		(Note 2)	2.0		V_{DDIOB}	
Output Low Voltage (I_O = +4.0mA)	V_{OL}		0		0.4	V

Note 1: 0V < V_{IN} < V_{DDIO} for all other digital inputs.

Note 2: For OC1B to OC5B when V_{DDIOB} = 2.5V.

Table 10-4. LVDS Output Pins

(V_{DD} = 1.8V ±10%; V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OHLVDS}	(Note 1)			1.6	V
Output Low Voltage	V_{OLLVDS}	(Note 1)	0.9			V
Differential Output Voltage	V_{ODLVDS}		247	350	454	mV
Output Offset (Common Mode) Voltage	V_{OSLVDS}	25°C (Note 1)	1.125	1.25	1.375	V
Difference in Magnitude of Output Differential Voltage for Complementary States	$V_{DOSLVDS}$				25	mV

Note 1: With 100Ω load across the differential outputs.

Note 2: The differential outputs can easily be interfaced to LVDS, LVPECL, and CML inputs on neighboring ICs using a few external passive components. See App Note HFAN-1.0 for details.

Table 10-5. LVPECL Level-Compatible Output Pins

(V_{DD} = 1.8V ±10%; V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Output Voltage	V_{ODPECL}		595	700	930	mV
Output Offset (Common Mode) Voltage	V_{OSPECL}	25°C (Note 1)		0.8		V
Difference in Magnitude of Output Differential Voltage for Complementary States	$V_{DOSPECL}$				50	mV

Note 1: With 100Ω load across the differential outputs.

Note 2: The differential outputs can easily be interfaced to LVDS, LVPECL, and CML inputs on neighboring ICs using a few external passive components. See App Note HFAN-1.0 for details.

Figure 10-1. Recommended Termination for LVDS Output Pins

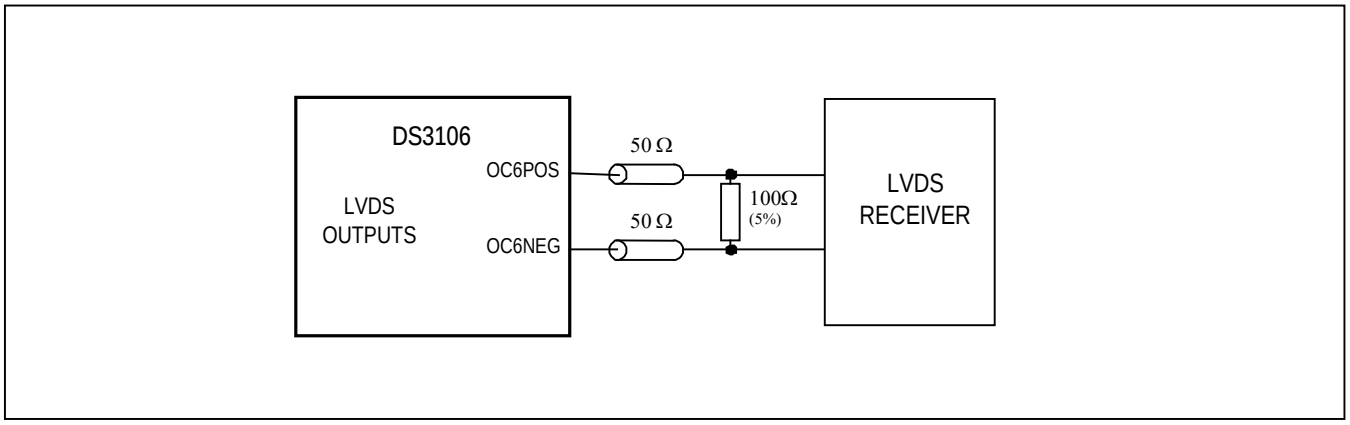
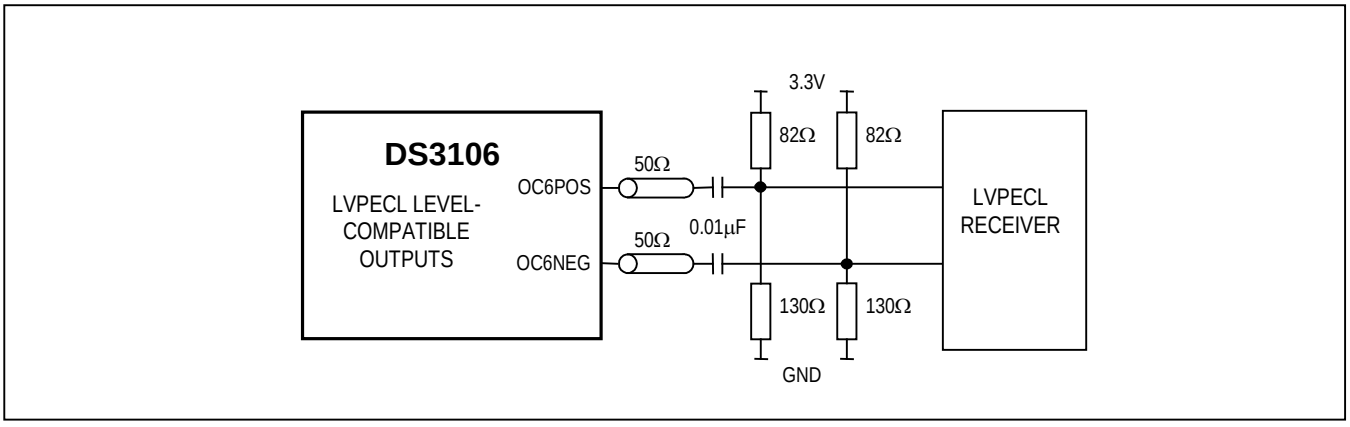


Figure 10-2. Recommended Termination for LVPECL-Compatible Output Pins



10.2 Input Clock Timing

Table 10-6. Input Clock Timing

(V_{DD} = 1.8V ±10%; V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Duty Cycle			30		70	%

10.3 Output Clock Timing

Table 10-7. Input Clock to Output Clock Delay

INPUT FREQUENCY	OUTPUT FREQUENCY	INPUT CLOCK EDGE TO OUTPUT CLOCK EDGE DELAY (ns)
8kHz	8kHz	0 ± 1.5
6.48MHz	6.48MHz	0 ± 1.5
19.44MHz	19.44MHz	0 ± 1.5
25.92MHz	25.92MHz	0 ± 1.5
38.88MHz	38.88MHz	0 ± 1.5
51.84MHz	51.84MHz	0 ± 1.5
77.76MHz	77.76MHz	0 ± 1.5
155.52MHz	155.52MHz	0 ± 1.5

Table 10-8. Output Clock Phase Alignment, Frame-Sync Alignment Mode

OUTPUT FREQUENCY	MFSYNC FALLING EDGE TO OUTPUT CLOCK FALLING EDGE DELAY (ns)
8kHz (FSYNC)	0 ± 0.5
2kHz	0 ± 0.5
8kHz	0 ± 0.5
1.544MHz	0 ± 1.25
2.048MHz	0 ± 1.25
44.736MHz	-2.0 ± 1.25
34.368MHz	-2.0 ± 1.25
6.48MHz	-2.0 ± 1.25
19.44MHz	-2.0 ± 1.25
25.92MHz	-2.0 ± 1.25
38.88MHz	-2.0 ± 1.25
51.84MHz	-2.0 ± 1.25
77.76MHz	-2.0 ± 1.25
155.52MHz	-2.0 ± 1.25
311.04MHz	-2.0 ± 1.25

10.4 SPI Interface Timing

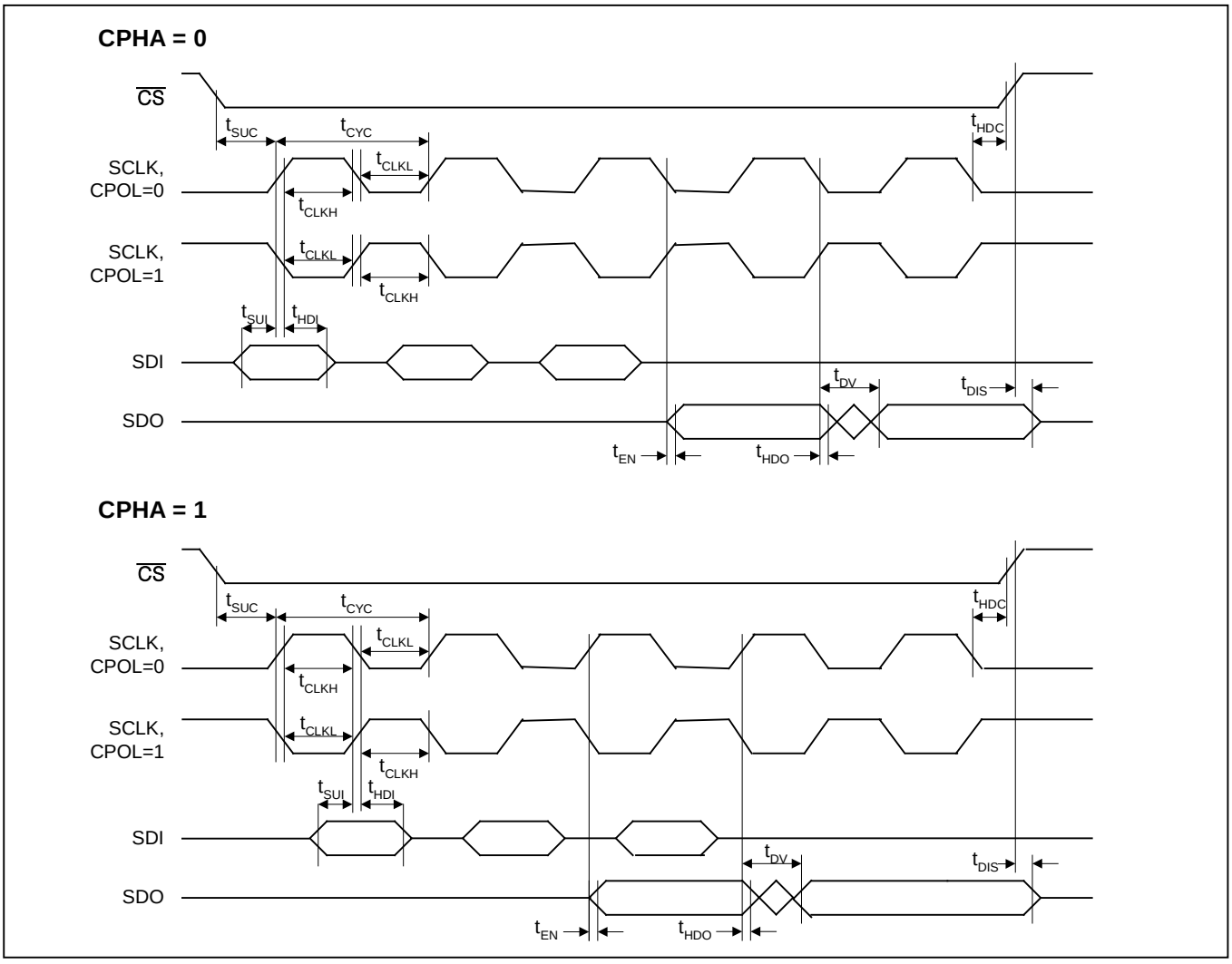
Table 10-9. SPI Interface Timing

(V_{DD} = 1.8V ±10%; V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.) (See Figure 10-3.)

PARAMETER (Note 1)	SYMBOL	MIN	TYP	MAX	UNITS
SCLK Frequency	f_{BUS}			6	MHz
SCLK Cycle Time	t_{CYC}	100			ns
$\overline{CS}$ Setup to First SCLK Edge	t_{SUC}	15			ns
$\overline{CS}$ Hold Time After Last SCLK Edge	t_{HDC}	15			ns
SCLK High Time	t_{CLKH}	50			ns
SCLK Low Time	t_{CLKL}	50			ns
SDI Data Setup Time	t_{SUI}	5			ns
SDI Data Hold Time	t_{HDI}	15			ns
SDO Enable Time (High-Z to Output Active)	t_{EN}	0			ns
SDO Disable Time (Output Active to High-Z)	t_{DIS}			25	ns
SDO Data Valid Time	t_{DV}			50	ns
SDO Data Hold Time After Update SCLK Edge	t_{HDO}	5			ns

Note 1: All timing is specified with 100pF load on all SPI pins.

Figure 10-3. SPI Interface Timing Diagram



10.5 JTAG Interface Timing

Table 10-10. JTAG Interface Timing

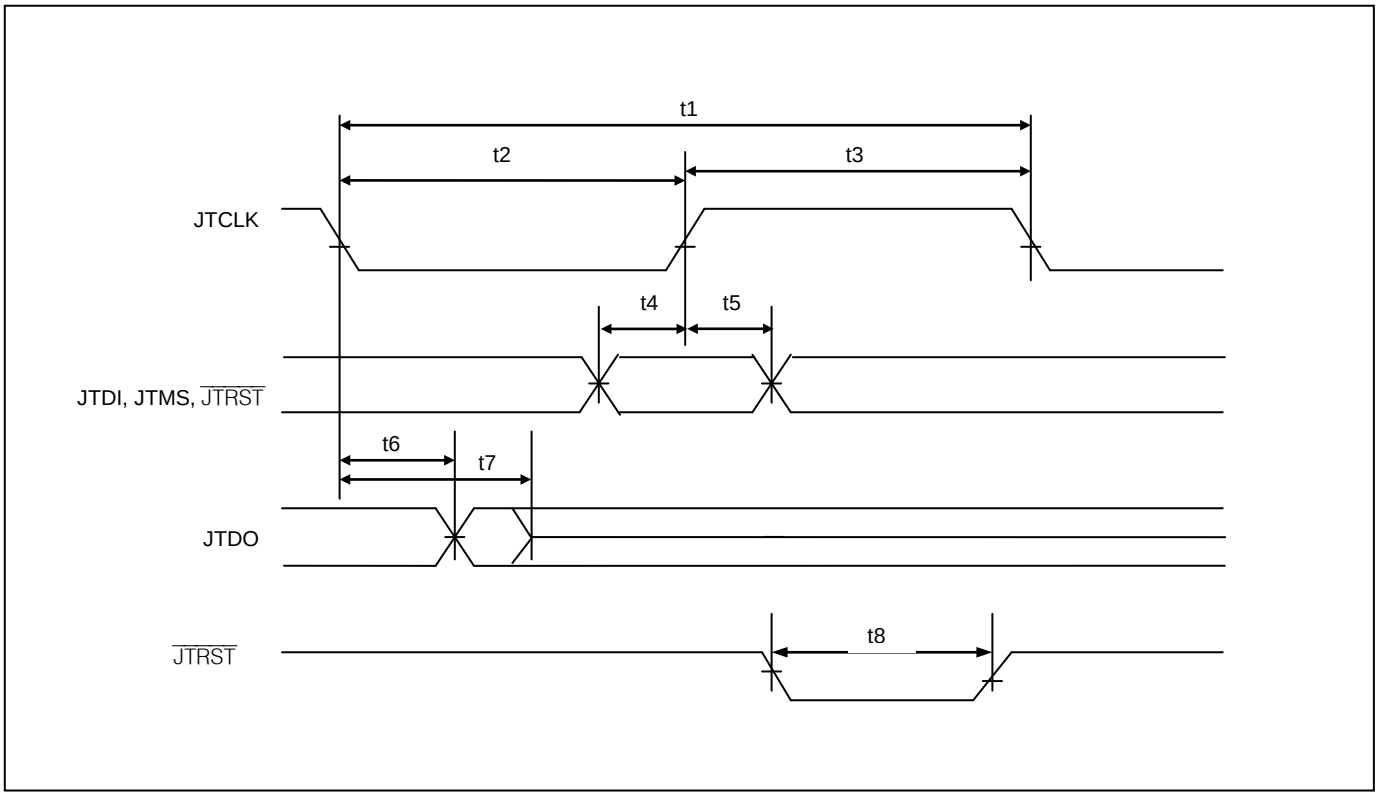
(V_{DD} = 1.8V ±10%; V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.) (See Figure 10-4.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
JTCLK Clock Period	t1		1000		ns
JTCLK Clock High/Low Time (Note 1)	t2/t3	50	500		ns
JTCLK to JTDI, JTMS Setup Time	t4	50			ns
JTCLK to JTDI, JTMS Hold Time	t5	50			ns
JTCLK to JTDO Delay	t6	2		50	ns
JTCLK to JTDO High-Z Delay (Note 2)	t7	2		50	ns
$\overline{\text{JTRST}}$ Width Low Time	t8	100			ns

Note 1: Clock can be stopped high or low.

Note 2: Not tested during production test.

Figure 10-4. JTAG Timing Diagram



10.6 Reset Pin Timing

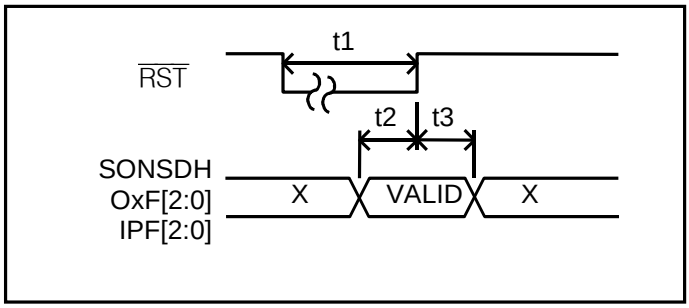
Table 10-11. Reset Pin Timing

(V_{DD} = 1.8V ±10%; V_{DDIO} = 3.3V ±5%, T_A = -40°C to +85°C.) (See Figure 10-5.)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
$\overline{RST}$ Low Time (Note 1)	t1	1000			ns
SONSDH, IPF[2:0], O3F[2:0], O6F[2:0] Setup Time to $\overline{RST}$	t2	0			ns
SONSDH, IPF[2:0], O3F[2:0], O6F[2:0] Hold Time from $\overline{RST}$	t3	50			ns

Note 1: $\overline{RST}$ should be held low while the REFCLK oscillator stabilizes. It is recommended to force $\overline{RST}$ low during power-up. The 1000ns minimum time applies if the $\overline{RST}$ pulse is applied any time after the device has powered up and the oscillator has stabilized.

Figure 10-5. Reset Pin Timing Diagram



11. Pin Assignments

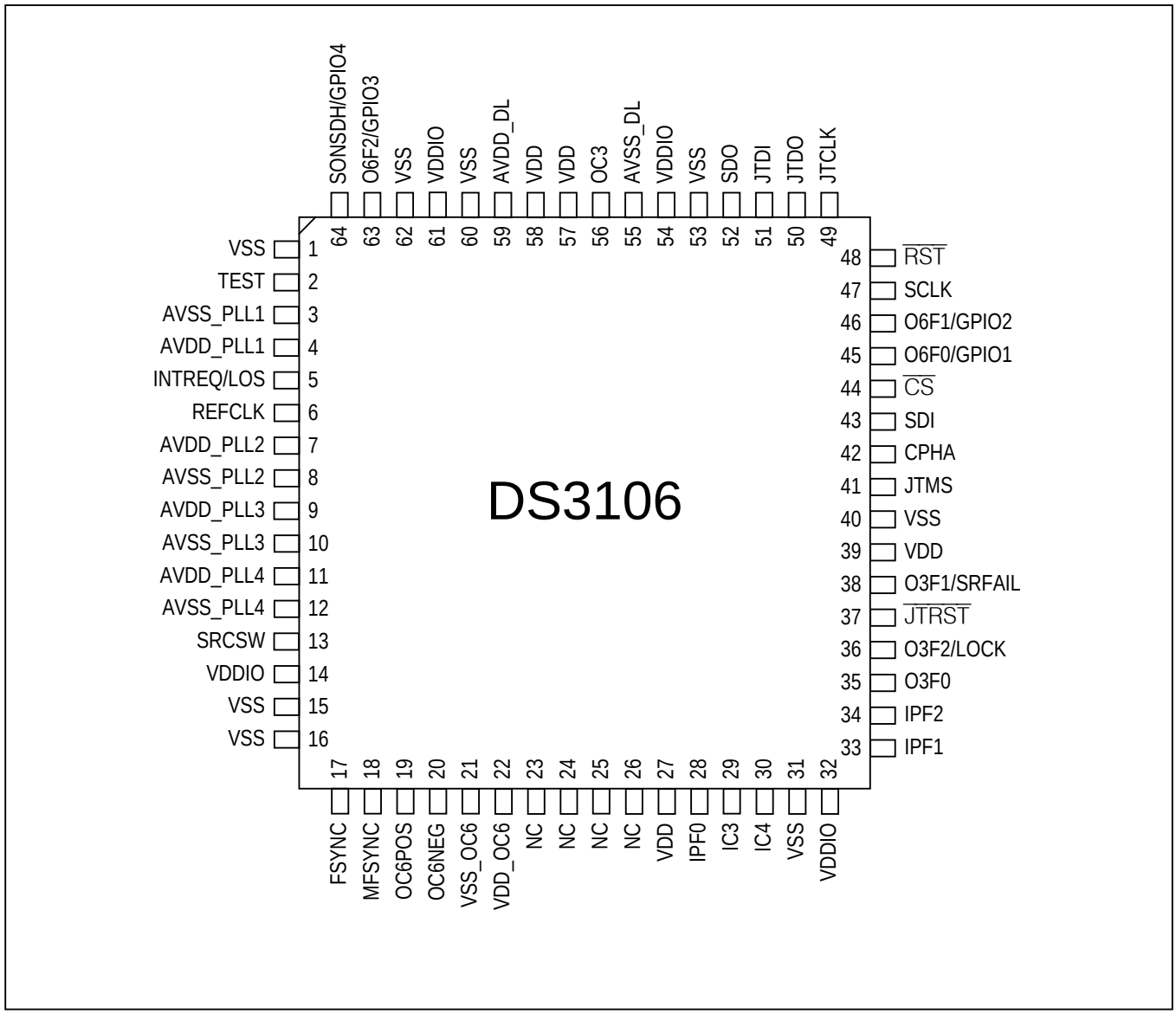
Table 11-1 lists pin assignments sorted in alphabetical order by pin name. Figure 11-1 shows pin assignments arranged by pin number.

Table 11-1. Pin Assignments Sorted by Signal Name

PIN NAME	PIN NUMBER
AVDD_DL	59
AVDD_PLL1	4
AVDD_PLL2	7
AVDD_PLL3	9
AVDD_PLL4	11
AVSS_DL	55
AVSS_PLL1	3
AVSS_PLL2	8
AVSS_PLL3	10
AVSS_PLL4	12
CPHA	42
$\overline{CS}$	44
FSYNC	17
IC3	29
IC4	30
IPF0	28
IPF1	33
IPF2	34
INTREQ/LOS	5
JTCLK	49
JTDI	51
JTDO	50
JTMS	41
$\overline{JTRST}$	37

PIN NAME	PIN NUMBER
N.C.	23–26
O3F0	35
MFSYNC	18
O3F1/SRFAIL	38
O3F2/LOCK	36
O6F0/GPIO1	45
O6F1/GPIO2	46
O6F2/GPIO3	63
OC3	56
OC6NEG	20
OC6POS	19
REFCLK	6
$\overline{RST}$	48
SCLK	47
SDI	43
SDO	52
SONSDH/GPIO4	64
SRCSW	13
TEST	2
VDD	27, 39, 57, 58
VDDIO	14, 32, 54, 61
VDD_OC6	22
VSS	1, 15, 16, 31, 40, 53, 60, 62
VSS_OC6	21

Figure 11-1. Pin Assignment Diagram



12. Package Information

For the latest package outline information and land patterns, contact Microsemi timing products technical support. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
64 LQFP	C64-1	21-0083	90-0141

13. Thermal Information

Table 13-1. LQFP Package Thermal Properties, Natural Convection

PARAMETER	MIN	TYP	MAX
Ambient Temperature (Note 1)	-40°C		+85°C
Junction Temperature	-40°C		+125°C
Theta-JA (θ_{JA}) (Note 2)		45.4°C/W	
Psi-JB		23.8°C/W	
Psi-JT		0.3°C/W	

Note 1: The package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

Note 2: Theta-JA (θ_{JA}) is the junction to ambient thermal resistance, when the package is mounted on a four-layer JEDEC standard test board with no airflow and dissipating maximum power.

Table 13-2. LQFP Theta-JA (θ_{JA}) vs. Airflow

FORCED AIR (METERS PER SECOND)	THETA-JA (θ_{JA})
0	45.4°C/W
1	37.3°C/W
2.5	34.5°C/W

14. Acronyms and Abbreviations

AIS	Alarm Indication Signal
AMI	Alternate Mark Inversion
APLL	Analog Phase-Locked Loop
BITS	Building Integrated Timing Supply
BPV	Bipolar Violation
DFS	Digital Frequency Synthesis
DPLL	Digital Phase-Locked Loop
ESF	Extended Superframe
EXZ	Excessive Zeros
GbE	Gigabit Ethernet
I/O	Input/Output
LOS	Loss of Signal
LVDS	Low-Voltage Differential Signal
LVPECL	Low-Voltage Positive Emitter-Coupled Logic
MTIE	Maximum Time Interval Error
OCXO	Oven-Controlled Crystal Oscillator
OOF	Out of Frame Alignment
PBO	Phase Build-Out
PFD	Phase/Frequency Detector
PLL	Phase-Locked Loop
ppb	Parts per Billion
ppm	Parts per Million
pk-pk	Peak-to-Peak
RMS	Root-Mean-Square
RAI	Remote Alarm Indication
RO	Read-Only
R/W	Read/Write
SDH	Synchronous Digital Hierarchy
SEC	SDH Equipment Clock
SETS	Synchronous Equipment Timing Source
SF	Superframe
SONET	Synchronous Optical Network
SSM	Synchronization Status Message
SSU	Synchronization Supply Unit
STM	Synchronous Transport Module
TDEV	Time Deviation
TCXO	Temperature-Compensated Crystal Oscillator
UI	Unit Interval
UI_{P-P}	Unit Interval, Peak-to-Peak
XO	Crystal Oscillator

15. Data Sheet Revision History

REVISION DATE	DESCRIPTION
121407	Initial data sheet release.
100108	In Section 7.7.8, corrected the PLL bandwidth range to have the correct range of 18Hz to 400Hz to match the register descriptions for T0ABW and T0LBW
030909	Corrected several frequencies in Table 7-16 and Table 7-17 to match actual device operation.
2009-05	In Section 8, added note indicating systems must be able to access entire address range 0-1FFh.
2010-08	In Figure 9-1 corrected pullup resistors values to 50kΩ. In PHMON.NW bit description, added "(TEST1.D180 = 0)". In Table 6-3 edited SRFAIL pin description to indicate state is high impedance when MCR10.SRFPIN = 0. Edited MCR10.SRFPIN decription to say this also. In Section 7.7.5 deleted sentence that said the hard and soft limits have hysteresis. Replaced the term "floating" with "unconnected" in several places. Updated soldering temperature information in Section 10.
2012-04	Reformatted for Microsemi. No content change.



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