LMK00804B-Q1EVM User's Guide

The LMK00804B-Q1 is an AEC-Q100 qualified low skew, high performance clock fanout buffer, which distributes up to four LVCMOS/LVTTL outputs (3.3-V, 2.5-V, 1.8-V, or 1.5-V levels). The clocks are derived from one of two selectable inputs, which can accept differential or single-ended input signals.

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1 Introduction

The LMK00804B-Q1 is a low skew, high performance clock fanout buffer, which distributes up to four LVCMOS/LVTTL outputs (3.3-V, 2.5-V, 1.8-V, or 1.5-V levels). The clocks are derived from one of two selectable inputs, which can accept differential or single-ended input signals.

This evaluation module (EVM) is designed to demonstrate the functionality and electrical performance of the LMK00804B-Q1 device. For optimum performance, the board is equipped with 50-Ω SMA connectors and 50-Ω controlled impedance traces.

Table 1. Device and Package Configurations

DESIGNATOR	IC	PACKAGE
U1	LMK00804B-Q1	VQFN (16)

2 Features

- Easy to use evaluation board to fan-out up to four LVCMOS clocks with low phase noise/jitter
- Accepts differential or single-ended/LVCMOS input clock
- Device control pins configurable through jumpers
- Board power at 3.3-V for VDD and VDDO (single supply) or 2.5/1.8/1.5 V for VDDO (dual supply)

3 Setup

This section describes the jumpers and connectors on the EVM as well and how to properly connect, set up and use the LMK00804B-Q1EVM.

3.1 Input/ Output Connector Description

Connectors:

- **LVCMOS_CLK** SMA connector is used to interface an external single-ended clock input (50-Ω source impedance) to the LVCMOS_CLK input of the device.
- **CLK_P and CLK_N** SMA connectors are used to interface an external AC-coupled clock input to the differential input pairs (CLK, nCLK) of the device.
- **Q0 – Q3** SMA connectors are used to distribute the four LVCMOS clock outputs.

Power Supply Test Points:

- **VDD** test point is used to connect 3.3-V power to the VDD supply of the board/device.
- **VDDO** test point is used to connect 3.3-/2.5-/1.8-/1.5-V power to the VDDO supply of the board/device.
- **GND** test point is used to connect the power supply ground to GND of the board/device.

Jumpers:

- **CLK_SEL** selects between one of the two selectable inputs.
  - 0 (position 1-2) = Select LVCMOS_CLK input
  - 1 (position 2-3) = Select CLK_P/CLK_N input
- **CLK_EN** selects between U1 clock enabled or disabled modes.
  - 0 (position 1-2) = Clock Disabled (output drivers still enabled)
  - 1 (position 2-3) = Clock Enabled (normal operation)

NOTE: Some versions of the board may have an OUT EN header. This header and NC must be left floating. Do not place a shunt on the header.

3.2 Equipment

With this EVM, one could distribute any one of two clocks to up to four LVCMOS outputs. Therefore, a minimum of one clock source is needed and appropriate test equipment to observe or measure the outputs.

3.3 Operation

3.3.1 Power with Single Supply (VDD = VDDO = 3.3 V)

Before applying any clock inputs, short VDDO_SEL jumper pins 1-2 to set VDD = VDDO and supply the board with 3.3 V and ground at VDD and GND test points. Make sure the total supply current (IDD+IDDO) being drawn is less than 26 mA without any output loading.

3.3.2 Alternative Power with Separate Core and Output Supplies (VDD = 3.3 V, VDDO = 3.3/2.5/1.8/1.5 V)

Before applying any clock inputs, short VDDO_SEL jumper pins 2-3 to allow VDD and VDDO to be powered separately and supply the board with VDD = 3.3 V, VDDO = 3.3/2.5/1.8/1.5 V, and GND. Make sure the IDD current is less than 21 mA and IDDO current is less than 5 mA without any output loading.

3.3.3 Inputs

Figure 1 shows the LMK00804B-Q1 input structure and default on-board input termination. The internal 51-kΩ pullup and pulldown resistors on CLK/nCLK work with the external 50-Ω termination resistors, which causes the device inputs to be biased to about 1.1 V. Therefore, AC-coupled clock sources from 0.15Vpp to 1.4Vpp (50-Ω terminated) can be tied to the CLK/nCLK clock inputs directly. The input SMAs expect a 100-Ω differential clock source. Note that with the default input configuration, the differential input has only very small offset voltage (approximately 3.2 mV) so that, when the selected clock inputs are left open/floating, the outputs could have the tendency to chatter.

With DC-coupled clock sources, use a “DC-block” at the input SMAs to ensure DUT input voltage range compliance. Alternatively, adjust the clock source DC bias (if available) to make sure the LMK00804B-Q1 input voltage range is not violated.

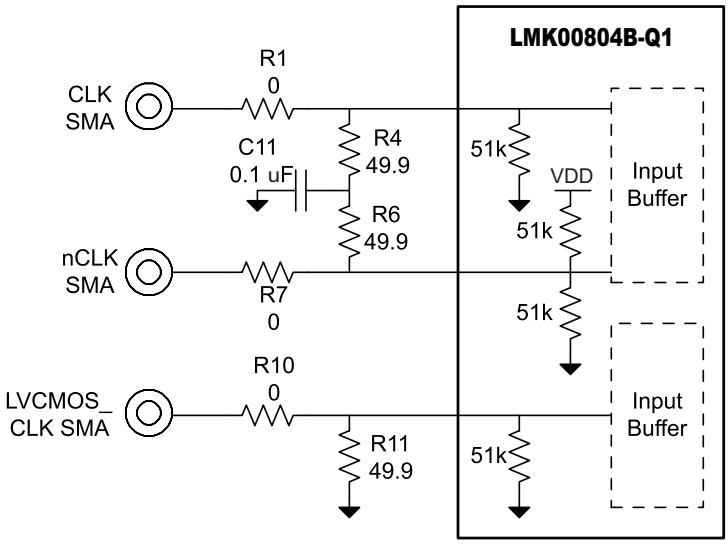

Figure 1. On-Board Input Termination With Internal Pullup/Pulldown Resistors

The clock inputs can accommodate a differential input or single-ended input signal with the proper external input termination using the various component options on the board. Refer to the data sheet for input interface application circuits.

To achieve the best possible additive jitter and noise floor performance, TI recommends driving the CLK/nCLK pair using an input signal with fast slew rate of 3 V/ns (differential) or higher. Driving the input with a lower slew rate can degrade the additive jitter and noise floor performance. For this reason, a differential input signal (for example, LVPECL), is recommended because it typically provides higher slew rate and common-mode noise rejection compared to a single-ended input (for example, LVCMOS/LVTTL or sine-wave).

The LVCMOS_CLK input is terminated on-board with 50 Ω to ground (R11), and can accommodate a single-ended input source expecting a 50-Ω load. When connecting a source-terminated LVCMOS input that expects a high-impedance input, remove R11 to disconnect the 50-Ω termination.

Outputs:

All four LVCMOS outputs (Rout = 7 Ω typical) are configured with 43-Ω series resistors for source termination (Ro + Rs = 50 Ω) and routed through 50-Ω traces. By default, two of the four output traces are configured with SMA connectors, which can be connected through a 50-Ω coax cable to a high-impedance load/receiver, such as a 1-MΩ scope input. When driving a high-impedance load, the typical output voltage swing measured at the load should be nearly rail-to-rail (GND to VDDO) over the specified operating frequency. When driving a 50-Ω load, the output voltage swing will be attenuated by about 50% (GND to VDDO/2) due to the divider formed source and load resistors.

4 PCB Layout

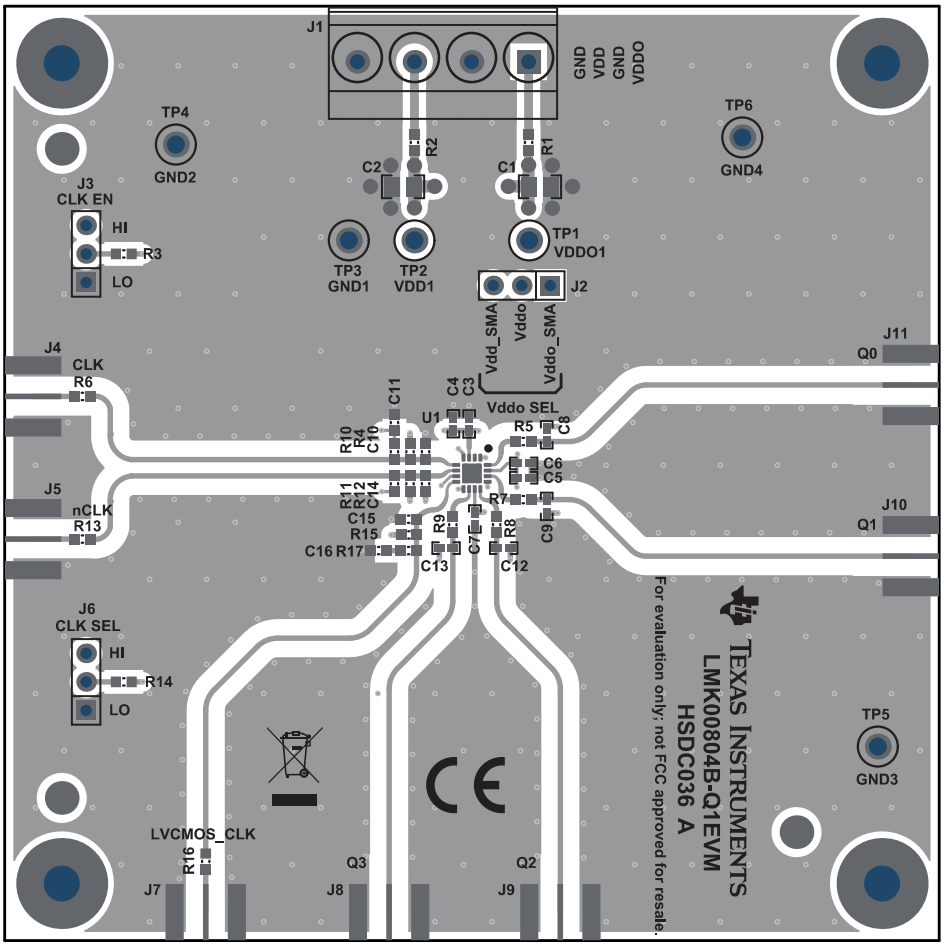

Figure 2. Top Layer

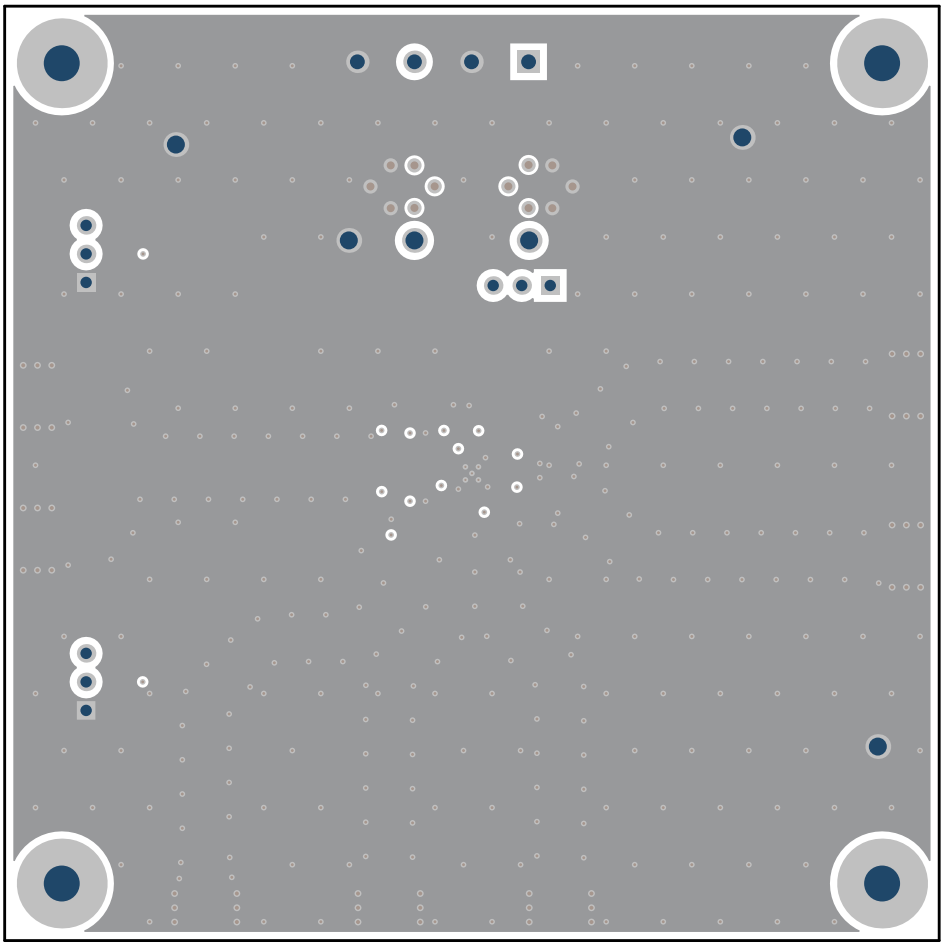

Figure 3. Inner Layer 2 (Ground Plane)

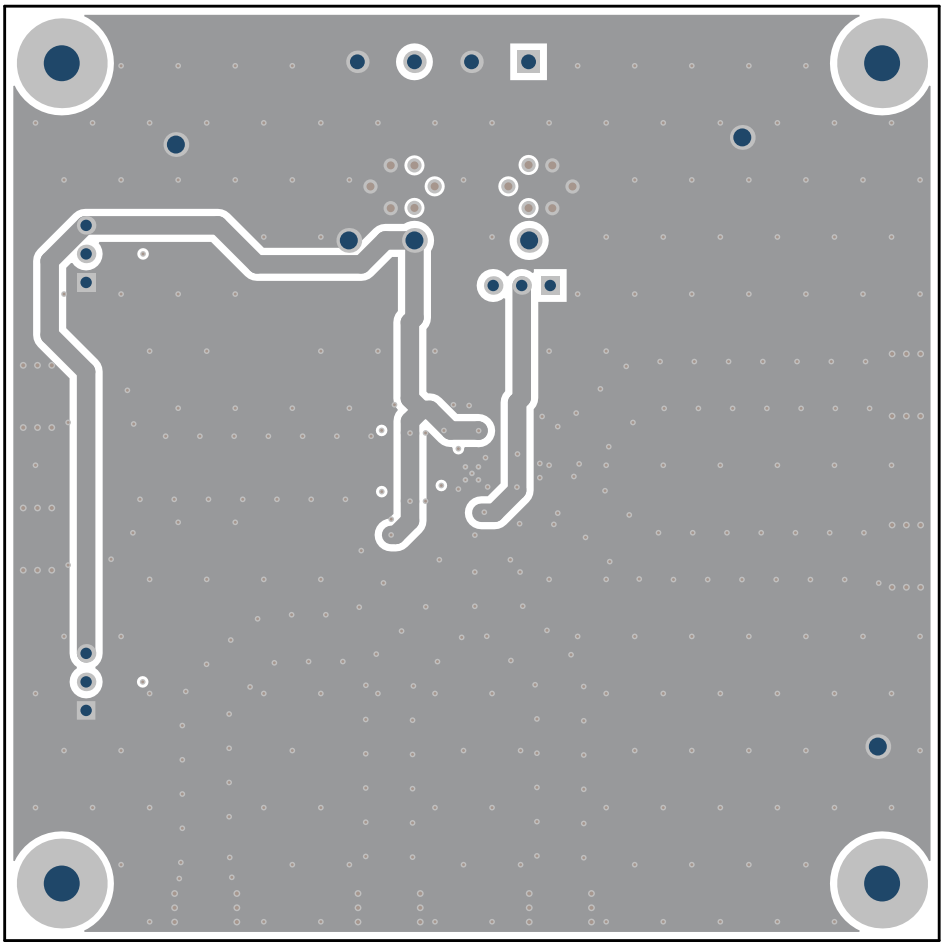

Figure 4. Inner Layer 3 (VDD Traces and GND Fill)

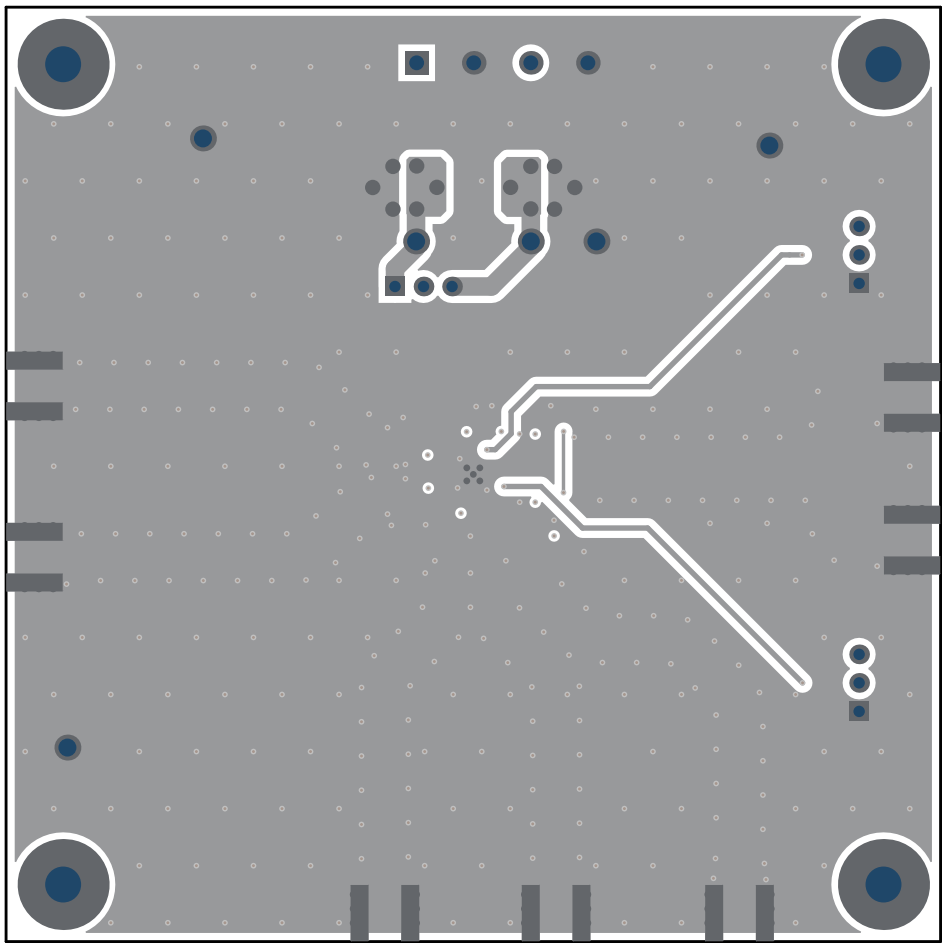

Figure 5. Bottom Layer

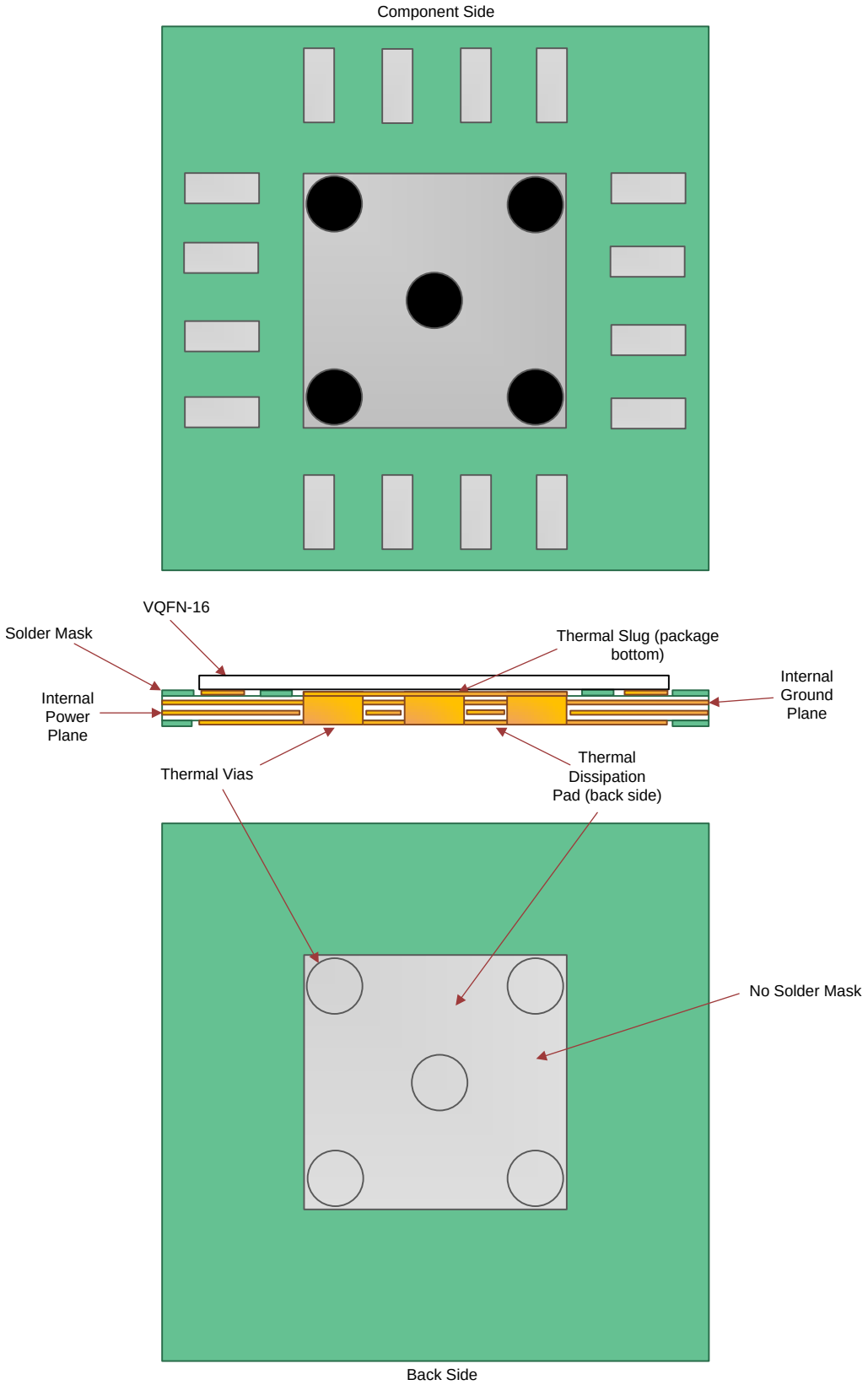

Figure 6. Layout Example

5 Schematic

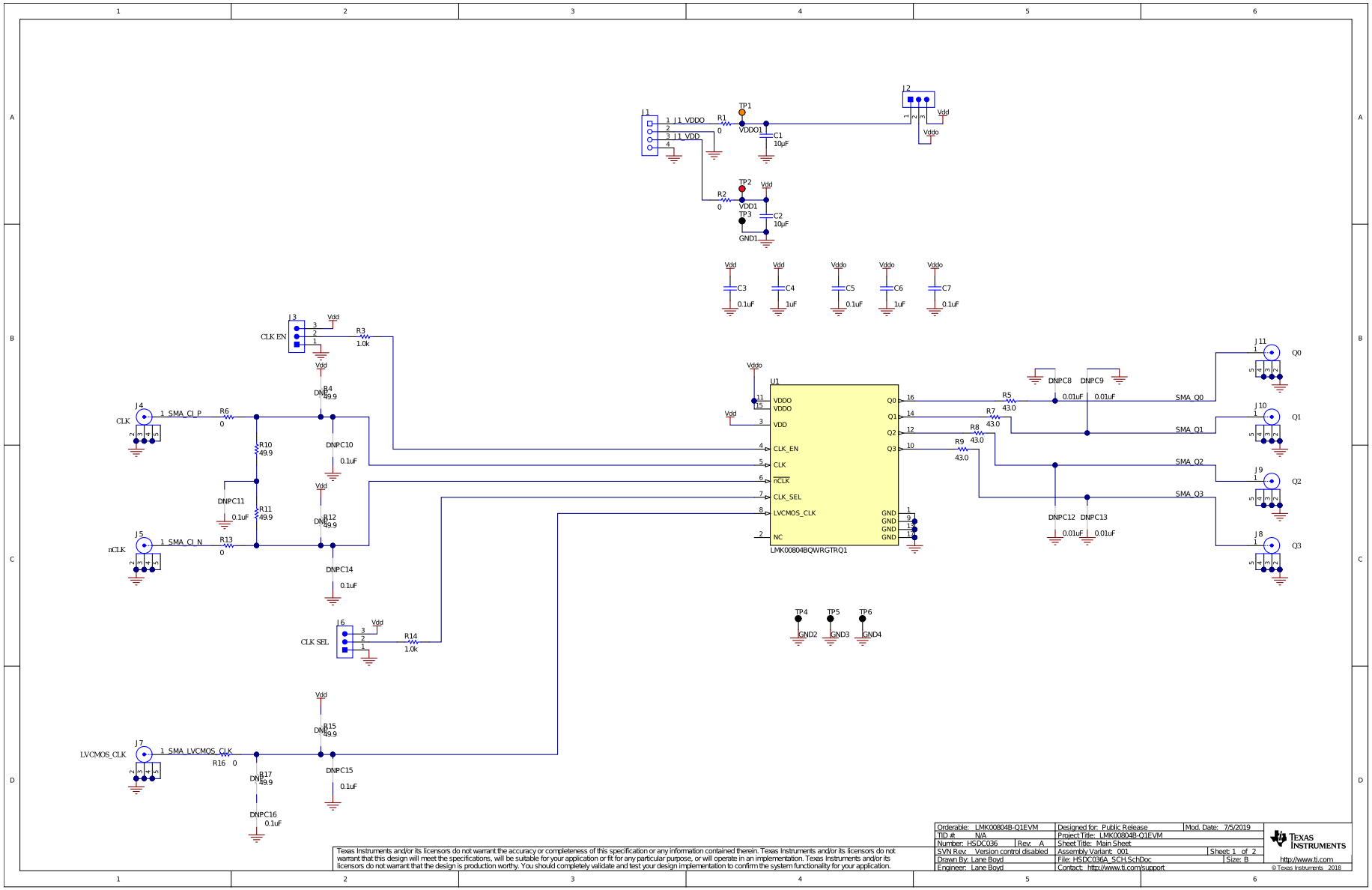

Figure 7. LMK00804B-Q1EVM Schematic

6 Bill of Materials

Table 2. LMK00804B-Q1EVM Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PKG REF	PART NUMBER	MANUFACTURER
!PCB	1		Printed-Circuit Board		HSDC036	Any
C1, C2	2	10uF	CAP, CERM, 10 µF, 10 V, +/- 5%, X7R, AEC-Q200 Grade 1, 0805	0805	C0805C106J8RACAUTO	Kemet
C3, C5, C7	3	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402	0402	0402YC104KAT2A	AVX
C4, C6	2	1uF	CAP, CERM, 1 uF, 6.3 V, +/- 20%, X7R, 0402	0402	GRM155R70J105MA12D	MuRata
H1, H2, H3, H4	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
H5, H6, H7, H8	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	Screw	NY PMS 440 0025 PH	B&F Fastener Supply
J1	1		Terminal Block, 4x1, 5.08mm, TH	4x1 Terminal Block	39544-3004	Molex
J2, J3, J6	3		Header, 100mil, 3x1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
J4, J5, J7, J8, J9, J10, J11	7		CONN SMA JACK STR EDGE MNT	CONN_JACK	CON-SMA-EDGE-S	RF Solutions Ltd.
R1, R2, R6, R13, R16	5	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R3, R14	2	1.0k	RES, 1.0 k, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW06031K00JNEA	Vishay-Dale
R5, R7, R8, R9	4	43.0	RES, 43.0, 1%, 0.1 W, 0603	0603	RC0603FR-0743RL	Yageo
R10, R11	2	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
SH1, SH2, SH3	3	1x2	Shunt, 100mil, Gold plated, Black	Shunt	SNT-100-BK-G	Samtec
TP1	1		Test Point, Compact, Orange, TH	Orange Compact Testpoint	5008	Keystone
TP2	1		Test Point, Compact, Red, TH	Red Compact Testpoint	5005	Keystone
TP3, TP4, TP5, TP6	4		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint	5011	Keystone
U1	1		Automotive Low Skew, 1-to-4 Multiplexed Differential/LVCMOS-to-LVCMOS/TTL Fanout Buffer, RGT0016H (VQFN-16)	RGT0016H	LMK00804BQWRGTRQ1	Texas Instruments
C8, C9, C12, C13	0	0.01uF	CAP, CERM, 0.01 uF, 10 V, +/- 10%, X7R, 0402	0402	0402ZC103KAT2A	AVX
C10, C14, C15	0	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X7R, 0603	0603	C0603C104K8RACTU	Kemet
C11, C16	0	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 5%, X7R, 0603	0603	0603YC104JAT2A	AVX
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
R4, R12, R15, R17	0	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2019) to A Revision	Page
• Updated *Setup* section	2
• Added *PCB Layout* section	5
• Added *Bill of Materials* section	11

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WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

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NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

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http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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