MP8868

High-Efficiency, 10A, 17V, Synchronous Step-Down Converter with I²C Interface

The Future of Analog IC Technology

DESCRIPTION

The MP8868 is a high-frequency, synchronous, rectified, stepdown, switch-mode converter with an I2C control interface. Its fully integrated solution achieves a 10A output current with excellent load and line regulation over a wide input-supply range.

The reference voltage level is controlled on-the-fly by the I²C serial interface with the reference voltage range adjustable from 0.6V to 1.87V in 10mV steps. In addition, the voltage scaling slew rate, the switching frequency, enable, and power-save mode are selectable through the I2C interface.

Current-mode operation provides fast transient response and eases loop stabilization. EN/SYNC supports external clock synchronization, and an open-drain power good pin indicates when the output voltage is in the nominal range. Full protection features include:

- Over-voltage protection (OVP)
- Hiccup over-current protection (OCP)
- Thermal shutdown

The MP8868 requires a minimal number of readily available, standard, external components, and it is available in a QFN-14 (3x4mm) package.

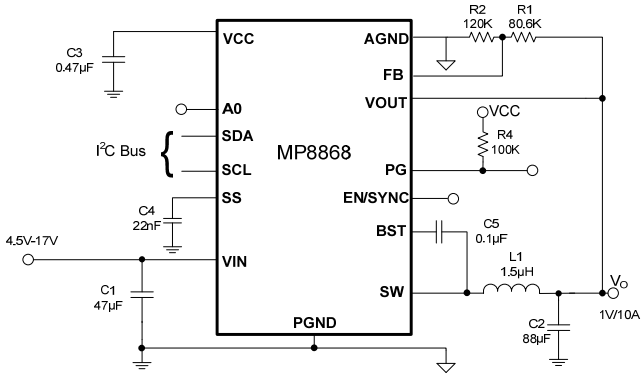
FEATURES

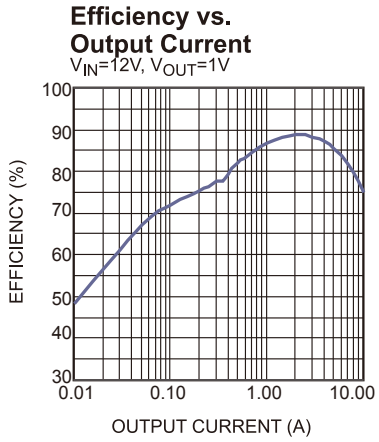
- Wide 4.5V-to-17V Operating Input Range
- 1% Internal Reference Accuracy
- I²C Programmable Reference Output Voltage
- Range from 0.6V to 1.87V in 10mV Steps with Slew Rate Control
- I²C Selectable Switching Frequency
- 200kHz-2MHz Synchronized External Clock
- OTP, OCP Hiccup Indication Via I2C
- Selectable PSM and Fs Through I2C
- Programmable Soft-Start Time
- Open-Drain Power Good Indicator
- Small 3x4mm QFN14 Package

APPLICATIONS

- SoC and Media Processors
- FPGA-based Systems
- ASIC Supplies
- Distributed Power Systems

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP8868GLE	QFN-14 (3mmx4mm)	*See Below*

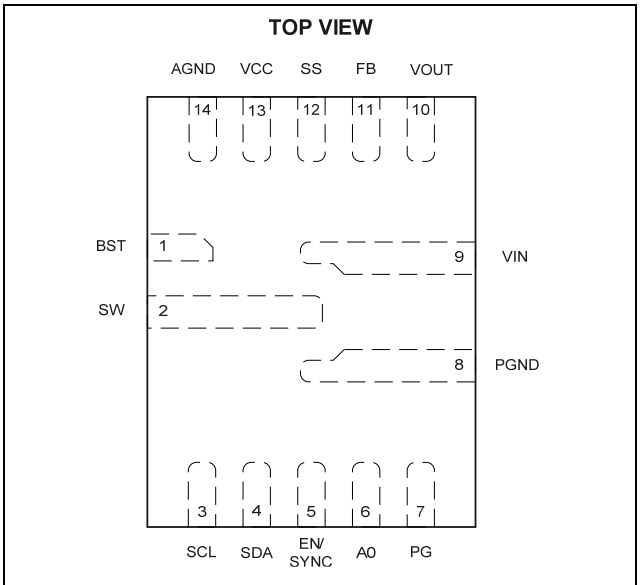
* For Tape & Reel, add suffix –Z (e.g. MP8868GLE–Z);

TOP MARKING

MPYW
8868
LLL
E

MP: MPS prefix:
Y: year code;
W: week code:
8868: first four digits of the part number;
LLL: lot number;
E: product code;

PACKAGE REFERENCE



QFN-14 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} …….. .....-0.3V to 19V
V_{SW}.....
-0.3V (-6V for <10ns) to 20V (24V for <10ns)
V_{BST}…… ..... V_{SW}+5.5V
All Other Pins…… ..... -0.3V to 5.5V (2)
Continuous Power Dissipation (T_A = +25°C) (3)
QFN 3x4……2.6W
Junction Temperature……150°C
Lead Temperature……260°C
Storage Temperature……-65°C to 150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN}……..4.5V to 17V
Output Voltage V_{OUT} ……0.6V to V_{IN} x D_{MAX} or 5.5V(5)
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (6)	θ_{JA}	θ_{JC}	
QFN (3x4)…. …….. …….....	48	11...	°C/W

Notes:
1) Exceeding these ratings may damage the device.
2) About the details of EN pin's ABS MAX rating, please refer to Page 15, Enable/SYNC control section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) The output voltage can't exceed 5.5V absolute maximum value at any input condition.
6) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to 125°C[7], unless otherwise noted, typical value is based on average value when T_J=25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		9	13	μA
Supply Current (Quiescent)	I_q	V_{EN} = 2V, No Switching, PFM mode		560	800	μA
HS Switch-On Resistance	HS_{RDS-ON}	V_{BST-SW} = 5V		26		mΩ
LS Switch-On Resistance	LS_{RDS-ON}	V_{CC} = 5V		11		mΩ
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} =12V or 0V, T_J = 25°C			1	μA
High Side Current Limit[8]	I_{LIMIT_H}	Under 40% Duty Cycle	11.7	14		A
Oscillator Frequency	f_{SW}	T_J = 25°C	400	500	570	kHz
		T_J = -40°C to 125°C	350		600	
Fold-Back Frequency	f_{VOUT}	V_{FB} = 150mV		0.5		f_{SW}
SYNC Frequency Range	f_{SYNC}		200		2000	kHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 500mV, fs=500kHz	93	95		%
Minimum On Time[8]	t_{ON_MIN}			40		ns
FB Voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to 85°C [8]	588		612	
VOUT	V_{OUT}=1.2V	T_J = 25°C	1188	1200	1212	mV
	V_{OUT}=1.2V	T_J = -40°C to 85°C [8]	1182		1218	
FB pin Current	I_{FB}	V_{FB} = 620mV		10	50	nA
A0 pin High Level	V_{ADD_H}		2			V
A0 pin Low Level	V_{ADD_L}				0.4	V
EN Pull-up Current	I_{EN_PU}	V_{EN} = 0V, T_J = 25°C	4.3	6.2	7.5	μA
		V_{EN}= 0V, T_J= -40°C to 125°C	3.2		8	
EN Rising Threshold	V_{EN_Rise}	T_J = 25°C	1.28	1.4	1.5	V
		T_J = -40°C to 125°C	1.26		1.52	
EN Hysteresis	V_{EN_HYS}	T_J = 25°C	120	170	220	mV
		T_J = -40°C to 125°C	100		240	
EN Turn Off Delay	EN_{td-off}			10		μs
VIN Under-Voltage Lockout Threshold-Rising	$INUV_{Vth}$	T_J = 25°C	4.04	4.2	4.36	V
		T_J = -40°C to 125°C	4.02		4.38	
VIN Under-Voltage Lockout Threshold-Hysteresis	$INUV_{HYS}$		560	660	740	mV
Power Good UV Threshold Rising	PGV_{th-Hi}	T_J = 25°C	0.85	0.9	0.94	VOUT
		T_J = -40°C to 125°C	0.84		0.95	
Power Good UV Threshold Falling	PGV_{th-Lo}	T_J = 25°C	0.64	0.7	0.73	VOUT
		T_J = -40°C to 125°C	0.63		0.74	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = -40°C to 125°C(7), unless otherwise noted, typical value is based on average value when T_J=25°C.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Good Deglitch time	PG_{Td}			100	160	µs
OVP Discharge Resistor	R_{OV}	From VOUT pin to GND		35	70	Ω
OVP Rising Threshold	V_{EN_Rise}	VOUT and FB pins, T_J =25°C	114%	120%	126%	V_{REF}
		VOUT and FB pins, T_J = -40°C to 125°C	113%		127%	
OVP Falling Threshold	V_{EN_Fall}	VOUT and FB pins	101%	105%	108%	V_{REF}
Soft-Start Current	i_{SS}		7	10	12	µA
VCC Voltage	V_{CC}	T_J = -40°C to 125°C	4.75	4.95	5.1	V
VCC Load Regulation		I_{CC}=5mA		1	3	%
Thermal Shutdown (8)	T_{TSD}			160		°C
Thermal Hysteresis (8)	T_{TSD_HYS}			20		°C

Notes:

7) Not tested in production and guaranteed by over-temperature correlation.

8) Guaranteed by Design and Characterization Test.

I/O Level Characteristics

Parameter	Symbol	Condition	HS-Mode		LS-Mode		Units
			Min	Max	Min	Max	
Low-level input voltage	V_{IL}		-0.5	0.3 V_{Bus}	-0.5	0.3V_{Bus}	V
High-level input voltage	V_{IH}		0.7 3V_{Bus}	V_{Bus}+ 0.5	0.7 V_{Bus}	V_{Bus}+ 0.5	V
Hysteresis of Schmitt trigger inputs	V_{HYS}	V_{Bus}>2V	0.05V_{Bus}	-	0.05 V_{Bus}	-	V
		V_{Bus}<2V	0.1 V_{Bus}	-	0.1 V_{Bus}	-	
Low-level output voltage(Open drain) at 3mA sink current	V_{OL}	V_{Bus}>2V	0	0.4	0	0.4	V
		V_{Bus}<2V	0	0.2 V_{Bus}	0	0.2V_{Bus}	
Low-level output current	I_{OL}		-	3	-	3	mA
Transfer gate on resistance for currents between SDA and SCAH, or SCL and SCLH	R_{onL}	VOL level, IOL=3mA	-	50	-	50	Ω
Transfer gate on resistance between SDA and SCAH, or SCL and SCLH	R_{onH}	Both signals (SDA and SDAH, or SCL and SCLH) at VBus level	50	-	50	-	kΩ
Pull-up current of the SCLH current source	I_{cs}	SCLH output levels between 0.3VBus and 0.7V_{Bus}	2	6	2	6	mA
Rise time of the SCLH or SCL signal	t_{rCL}	Output rise time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80			ns
Fall time of the SCLH or SCL signal	t_{fCL}	Output fall time (current source enabled) with an external pull-up current source of 3mA					
		Capacitive load from 10pF to 100pF	10	40			ns
		Capacitive load of 400pF	20	80	20	250	ns
Rise time of SDAH signal	t_{rDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Fall time of SDAH signal	t_{fDA}	Capacitive load from 10pF to 100pF	10	80	-	-	ns
		Capacitive load of 400pF	20	160	20	250	ns
Pulse width of spikes that must be suppressed by the input filter	t_{SP}		0	10	0	50	ns
Input current each I/O pin	I_i	Input voltage between 0.1V_{Bus} and 0.9V_{Bus}	-	10	-10	+10	uA
Capacitance for each I/O pin	C_i		-	10	-	10	pF

Notes:

V_{Bus} is the I^2C Bus Voltage, 3.0V to 3.6V range, 3.3V typical

I²C Port Signal Characteristics

Parameter	Symbol	Condition	Cb=100pF		Cb=400pF		Units
			Min	Max	Min	Max	
SCLH and SCL clock frequency	f_{SCHL}		0	3.4	0	0.4	MHz
Set-up time for a repeated START condition	$T_{SU;STA}$		160	-	600	-	ns
Hold time (repeated) START condition	$T_{HD;STA}$		160	-	600	-	ns
Low period of the SCL clock	t_{LOW}		160	-	1300	-	ns
High period of the SCL clock	t_{HIGH}		60	-	600	-	ns
Data set-up time	$T_{SU:DAT}$		10	-	100	-	ns
Data hold time	$T_{HD;DAT}$		0	70	0	-	ns
Rise time of SCLH signal	t_{rCL}		10	40	20*0.1Cb	300	ns
Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	t_{fCL1}		10	80	20*0.1Cb	300	ns
Fall time of SCLH signal	T_{fCL}		10	40	20*0.1Cb	300	ns
Rise time of SDAH signal	t_{fDA}		10	80	20*0.1Cb	300	ns
Fall time of SDAH signal	T_{fDA}		10	80	20*0.1Cb	300	ns
Set-up time for STOP condition	$T_{SU;STO}$		160	-	600	-	ns
Bus free time between a STOP and START condition	T_{BUF}		160	-	1300	-	ns
Data Valid Time	$T_{VD;DAT}$		-	16	-	90	ns
Data valid acknowledge time	$T_{VD;ACK}$		-	160	-	900	ns
Capacitive load for each bus line	C_b	SDAH and SCLH line	-	100	-	400	pF
		SDAH+SDA line and SCLH+SCL line	-	400	-	400	pF
Noise margin at the LOW level	C_i	For each connected device	-	$0.1V_{Bus}$	$0.1V_{Bus}$	-	V
Noise margin at the HIGH level	V_{nH}	For each connected device	-	$0.2V_{Bus}$	$0.2V_{Bus}$	-	V

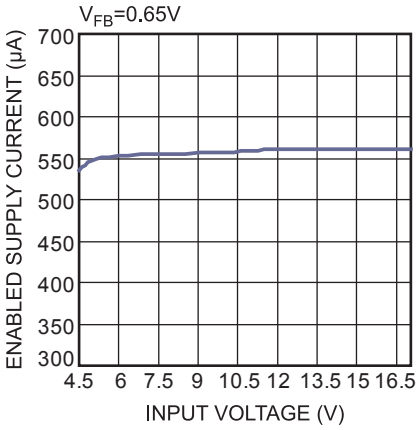
Notes:

V_{Bus} is the I²C Bus Voltage, 3.0V to 3.6V range, 3.3V typical

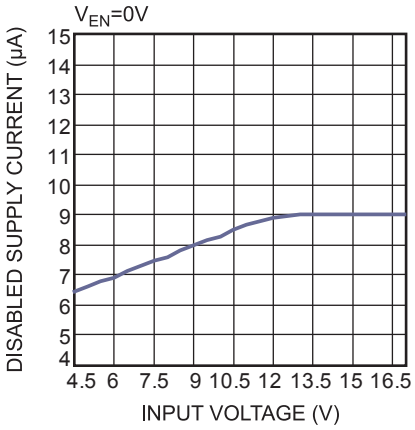
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

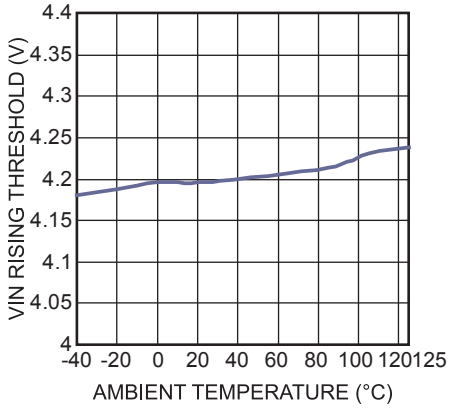
Enabled Supply Current vs. Input Voltage



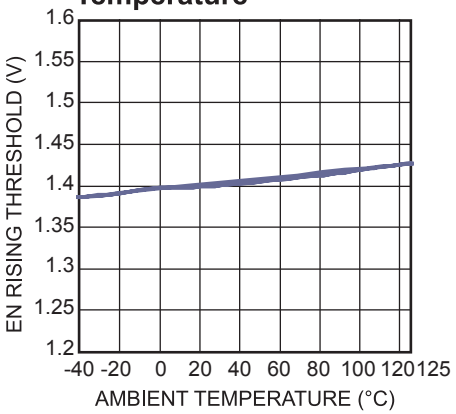
Disabled Supply Current vs. Input Voltage



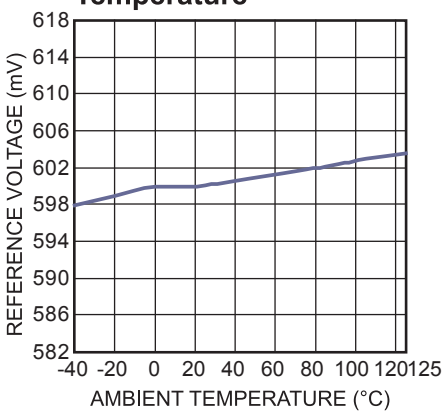
VIN UVLO Rising Threshold vs. Temperature



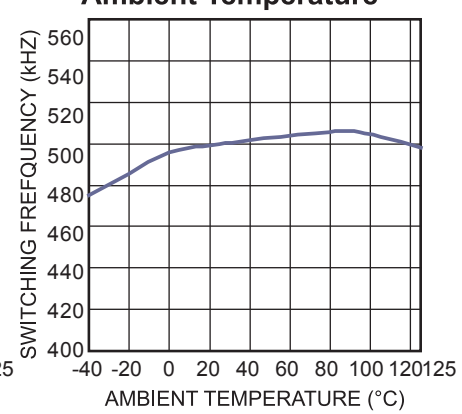
EN Rising Threshold vs. Temperature



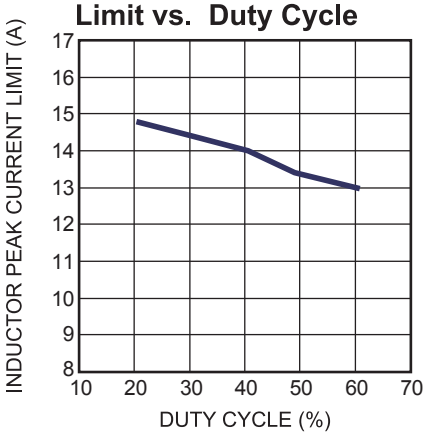
Reference Voltage vs. Temperature



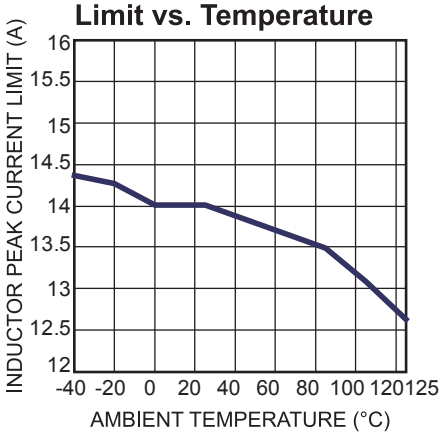
Switching Frequency vs. Ambient Temperature



Inductor Peak Current Limit vs. Duty Cycle



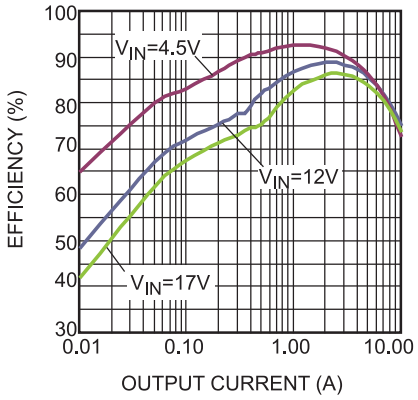
Inductor Peak Current Limit vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

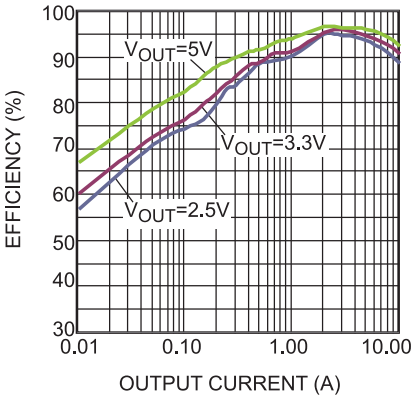
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Efficiency vs. Output Current

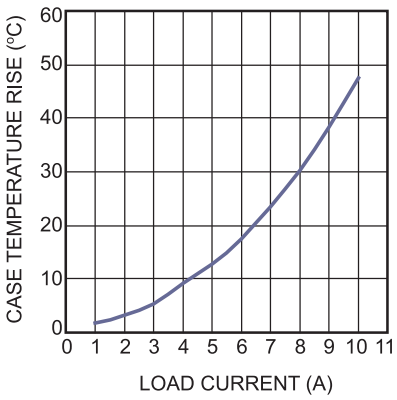


Efficiency vs. Output Current

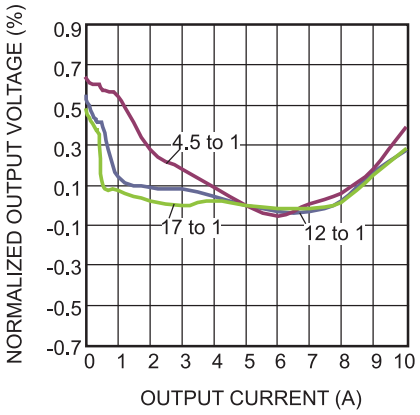
V_{IN}=12V



Case Temperature Rise vs. I_{OUT}

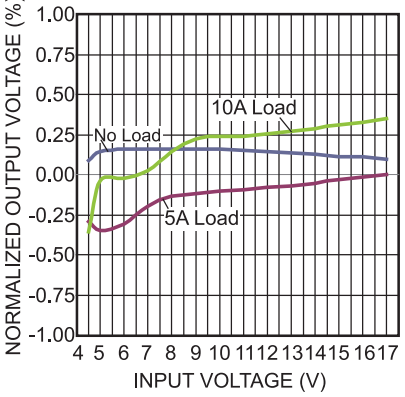


Load Regulation



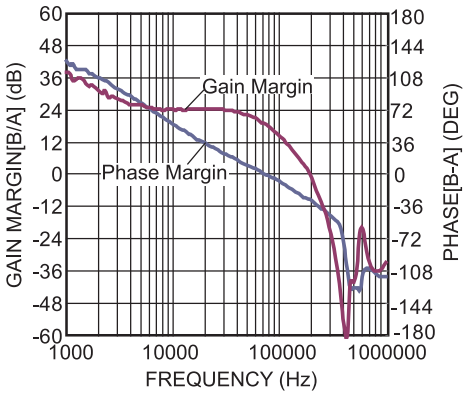
Line Regulation

V_{IN}=4.5V-17V



Bode Plot

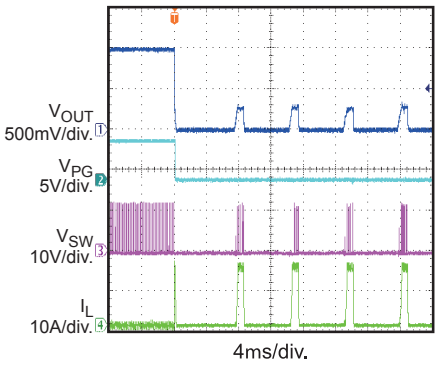
I_{OUT}=10A



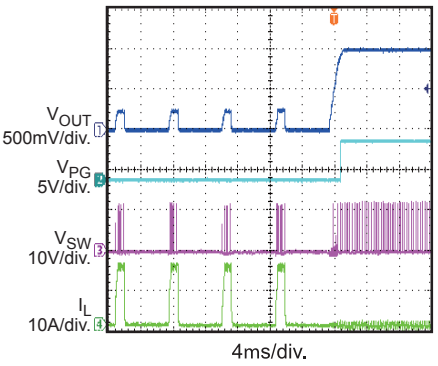
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

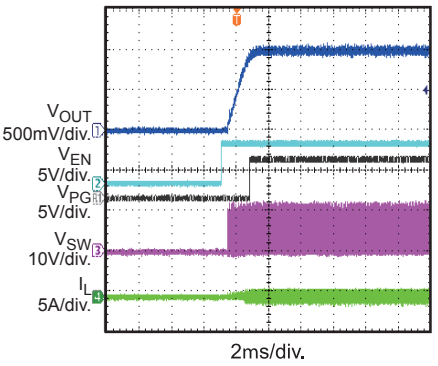
Short Entry
I_{OUT} = 0A



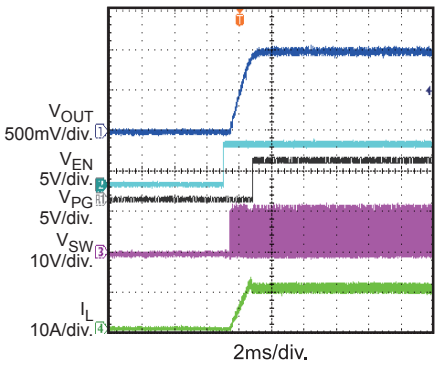
Short Recovery
I_{OUT} = 0A



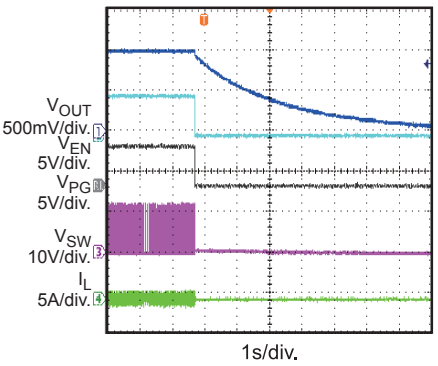
Start-Up through Enable
I_{OUT} = 0A



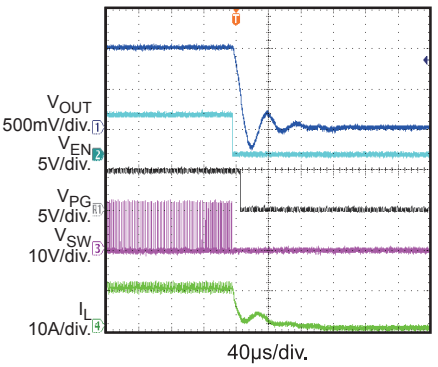
Start-Up through Enable
I_{OUT} = 10A



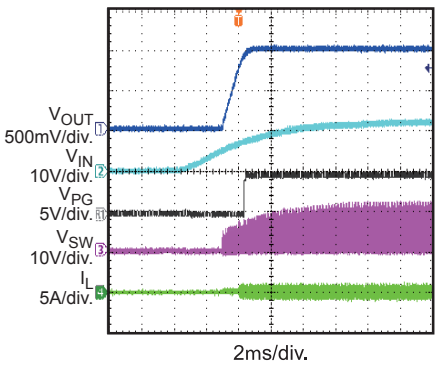
Shutdown through Enable
I_{OUT} = 0A



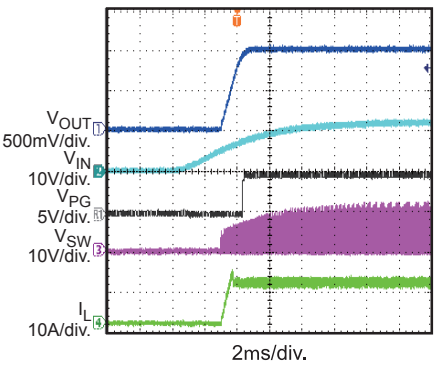
Shutdown through Enable
I_{OUT} = 10A



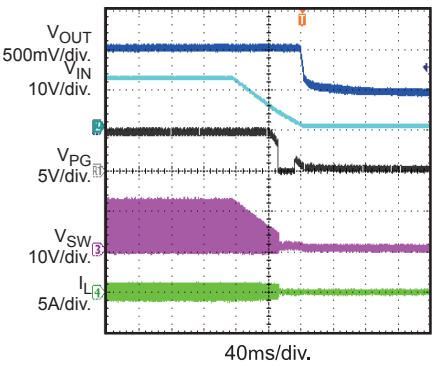
Start-Up through Input Voltage
I_{OUT} = 0A



Start-Up through Input Voltage
I_{OUT} = 10A



Shutdown through Input Voltage
I_{OUT} = 0A

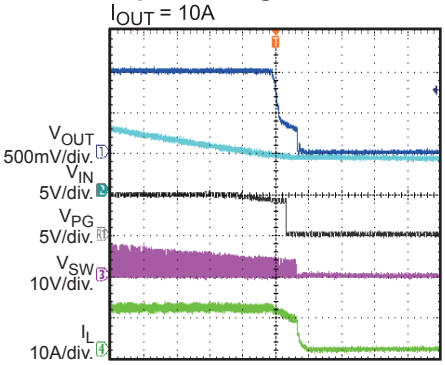


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 1V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

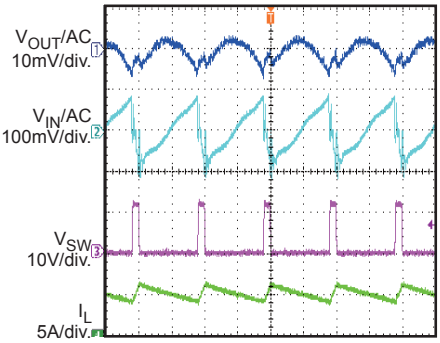
Shutdown through Input Voltage

I_{OUT} = 10A



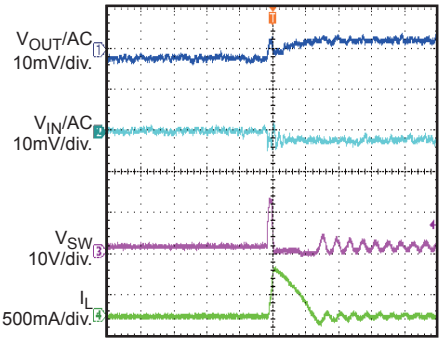
Input/Output Ripple

I_{OUT} = 10A



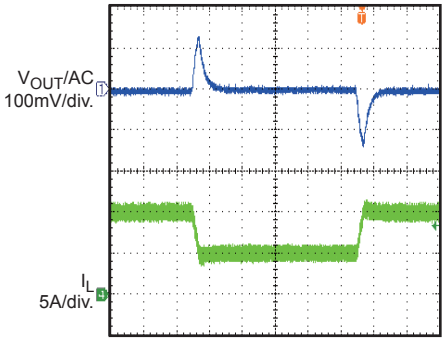
Input/Output Ripple

I_{OUT} = 0A, PFM



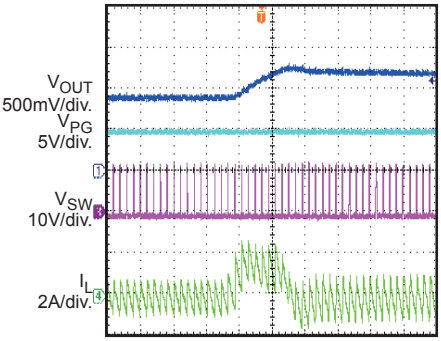
Load Transient Response

I_{OUT} = 5A to 10A



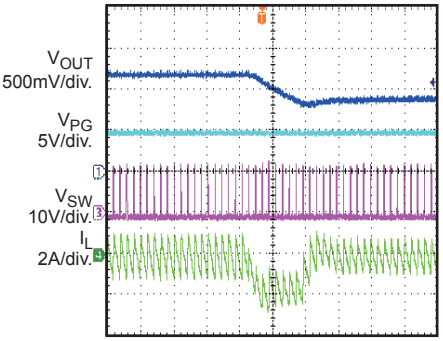
I²C Control Slew Rate

Slew Rate=16mV/µs, I_{OUT} = 0A, from 0.9V to 1.2V



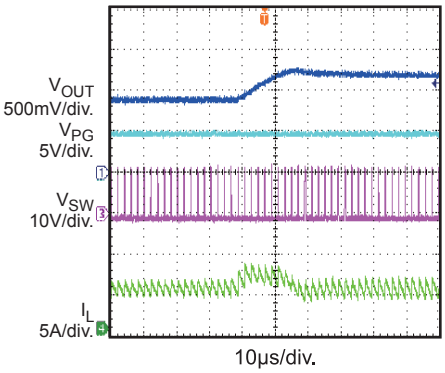
I²C Control Slew Rate

Slew Rate=16mV/µs, I_{OUT} = 0A, from 1.2V to 0.9V



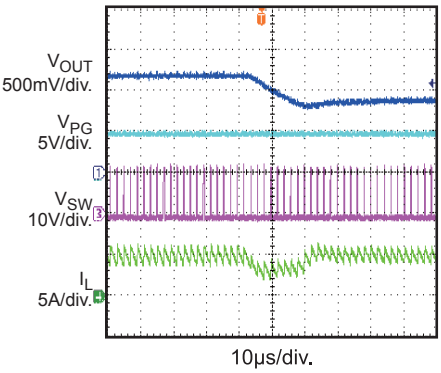
I²C Control Slew Rate

Slew Rate=16mV/µs, I_{OUT} = 5A, from 0.9V to 1.2V



I²C Control Slew Rate

Slew Rate=16mV/µs, I_{OUT} = 5A, from 1.2V to 0.9V



PIN FUNCTIONS

QFN14 PIN#	Name	Description
1	BST	Bootstrap. Requires a capacitor between SW and BST pins to form a floating supply across the high-side switch driver.
2	SW	Switch Output. Connect using a wide PCB trace.
3	SCL	I^2C Serial Clock.
4	SDA	I^2C Serial Data.
5	EN/SYNC	EN high to enable the MP8868. EN pin has internal 5.4uA pull-up current to 5V, so it can auto startup when EN floating. Apply an external clock can to the EN pin to change the switching frequency.
6	A0	I^2C address set pin. Left this pin float or pull it to VCC can set one address. Pull A0 pin to ground can set another different address.
7	PG	Power Good Indication. Open drain structure. PG switches low if the output voltage is out of regulation window. PG only indicates UV condition.
8	PGND	System Power Ground. Reference ground of the regulated output voltage. Requires special consideration during PCB layout. Connect to ground plane with copper traces and vias.
9	VIN	Supply Voltage. The MP8868 operates from a 4.5V-to-17V input rail. Requires ceramic capacitor to decouple the input rail. Connect using a wide PCB trace.
10	VOUT	Sense input of output voltage. Connect it to the positive terminal of loading.
11	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage in FB control loop.
12	SS	Soft start pin. Connect a capacitor from SS to ground can set the soft start time.
13	VCC	Internal LDO regulator output. Decouple with 0.47μF capacitor.
14	AGND	Signal Ground. AGND is not internally directly connected to System Ground, make sure AGND connected to system Ground in PCB layout.

FUNCTIONAL BLOCK DIAGRAM

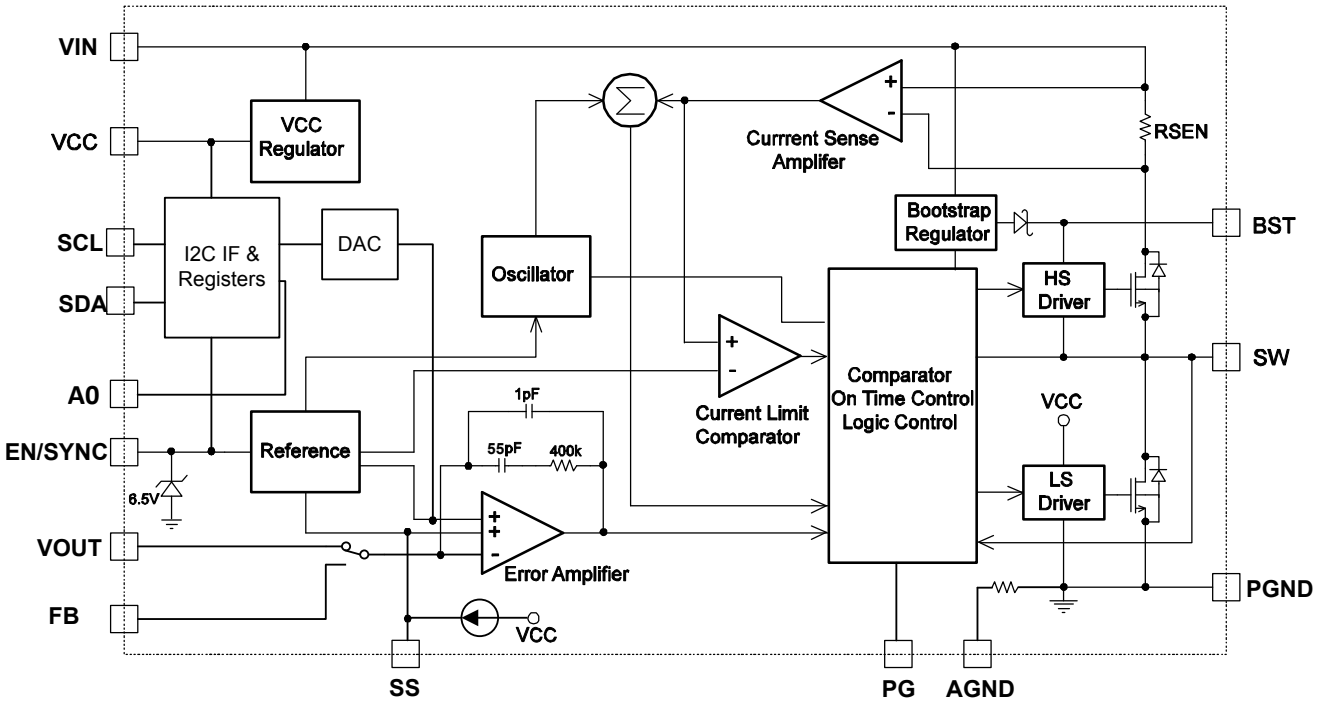


Figure 1: Functional Block Diagram

OPERATION

The MP8868 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution that achieves a 10A output current with excellent load and line regulation over a wide input supply range.

The MP8868 has three working modes: CCM (Continues-Conduction Mode), AAM mode (Advanced Asynchronous Modulation) and DCM (Discontinues-Conduction Mode). The MP8868 default operation mode is CCM. When set MODE bit(reg01[0]) in the I^2C register to "0". MP8868 can works in the AAM mode.

CCM Control Operation

In CCM the internal clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}, after a period of dead time, the LS-FET will turn on and remain on until the next clock cycle starts. The device will repeat the same operation in every clock cycle to regulate the output voltage.

If within 95% (500kHz switching frequency) of one PWM period, $V_{ILsense}$ does not reach the value set by V_{COMP}, the HS power MOSFET is forced off.

AAM Control Operation

In the light load condition, MP8868 works in AAM (Advanced Asynchronous Modulation) mode if Mode bit is set to "0". Refer to Figure 2, the V_{AAM} is an internal fixed voltage when input and output voltages are fixed. V_{COMP} is the error amplifier output which represents the peak inductor current information. When V_{COMP} is lower than V_{AAM}, the internal clock is blocked, thus the MP8868 skips some pulses and achieves the light load power save. Refer to AN032 for more detail.

The internal clock resets every time when V_{COMP} is higher than V_{AAM}. At the same time the HS-FET(High-Side MOSFET) turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}.

The light load feature in this device is optimized for 12V input applications.

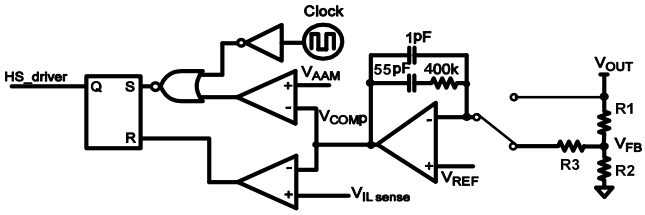


Figure 2: Simplified AAM Control Logic

DCM Control Operation

The V_{COMP} voltage ramps up with the increasing of the output current, when its minimum value exceeds V_{AAM}, the device will enter DCM (Discontinues-Conduction Mode). In this mode the internal clock initiates the PWM cycle, the HS-FET turns on and remains on until $V_{ILsense}$ reaches the value set by V_{COMP}, after a period of dead time, the LS-FET (Low-Side MOSFET) will turn on and remain on until the inductor current value decreases to zero. The device will repeat the same operation in every clock cycle to regulate the output voltage.

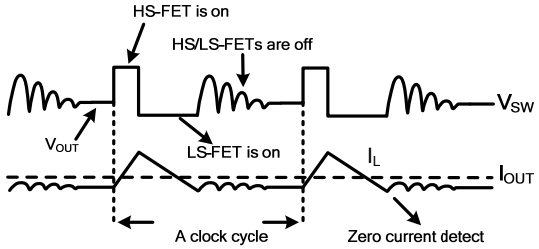


Figure 3: DCM Control Operation

VCC Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than 5.0V, the output of the regulator is in full regulation. When V_{IN} is lower than 5.0V, the output voltage decreases and follows the input voltage. A 0.47µF ceramic capacitor for decoupling purpose is required.

Error Amplifier

The error amplifier compares the FB pin voltage against the internal reference (REF) for FB control loop and outputs the COMP voltage—which controls the power MOSFET current. In I^2C mode, the FB pin is opened and VOUT pin is connected to the EA non-inverter input. The optimized internal compensation network

minimizes the external component count and simplifies the control loop design.

EN/SYNC Control

EN/SYNC is a digital control pin that turns the regulator including I²C block on and off. Drive EN/SYNC high to turn on the regulator; drive it low to turn it off. An internal 5.4μA pull-up current to 5V power supply allows auto startup when EN/SYNC pin is floating.

The EN/SYNC pin is clamped internally using a 5.7 V series-Zener-diode as shown in Figure 4. Connecting the EN/SYNC input pin through a pull-up resistor to the voltage on the V_{IN} pin limits the EN/SYNC input current to less than 100μA.

For example, with 12V connected to Vin, $R_{PULLUP} \geq (12V - 5.7V) \div 100\mu A = 63k\Omega$.

Connecting the EN/SYNC pin is directly to a voltage source without any pullup resistor requires limiting the amplitude of the voltage source to ≤5.5V to prevent damage to the Zener diode.

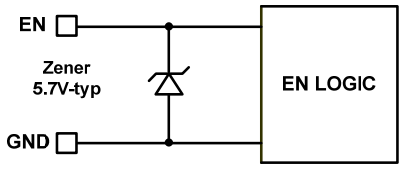


Figure 4: 5.7V Zener Diode Connection

For external clock synchronization, connect a clock with a frequency range between 200kHz and 2MHz to EN/SYNC pin. The internal clock rising edge will synchronize with the external clock rising edge once external clock is present. Set the external clock signal with a pulse width less than 80% of one internal clock cycle time.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at insufficient supply voltage. The MP8868 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.2V while its falling threshold is 3.54V.

Soft-Start

The MP8868 employs soft start (SS) mechanism to ensure smooth output during power-up. When the EN pin becomes high, an internal current source (10μA) charges up the SS capacitor. The SS capacitor voltage takes over the REF voltage to the PWM comparator. The output voltage smoothly ramps up with the SS voltage. Once the SS voltage reaches the same level as the REF voltage, it keeps ramping up while V_{REF} takes over the PWM comparator. At this point, the soft start finishes and it enters into steady state operation.

The SS capacitor value can be determined as follows:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times I_{SS}(\mu A)}{V_{REF}(V)}$$

If the output capacitors have large capacitance value, it's not recommended to set the SS time too small. Otherwise, it's easy to hit the current limit during SS.

Pre-Bias Startup

The MP8868 has been designed for monotonic startup into pre-biased output voltage. If the output is pre-biased to a certain voltage during startup, the voltage on the soft-start capacitor will be charged. When the soft-Start capacitor's voltage exceeds the sensed output voltage at the FB pin [(9)], the part starts to turn on high side and low side power switches sequentially. Output voltage starts to ramp up following with soft-start slew rate.

Note:

9) FB pin voltage in FB control loop, or VOUT pin voltage in I²C control loop.

Power Good Indicator

The MP8868 has power good (PG) output used to indicate whether the output voltage of the module is ready or not. The PG pin is an open drain output. Connect PG pin to VCC or other voltage source through a pull up resistor (e.g. 100kΩ). When the input voltage is applied, the PG pin is pulled down to GND. When V_{FB}[(9)] is above 90% of V_{REF}, the PG pin will be pulled high after 100us delay time. During normal operation, the PG pin will be pulled low when the V_{FB}[(9)]. drops below 70% of V_{REF} after 100us delay.

When UVLO or OTP happens, the PG pin will be pulled low immediately; When OC(Over current) happens, the PG pin will be pulled low

when V_{FB}(9). drops below 70% of V_{REF} after 100us delay.

The PG won't response to output over voltage condition.

The PG bit in the I^2C register have the same indication as the external PG pin.

Output over Voltage Protection (OVP)

MP8868 monitors both FB pin and VOUT pin to detect over voltage event. When "V_BOOT" bit=1, internal comparator monitors FB pin while "V_BOOT" bit=0, it monitors VOUT pin. When the feedback voltage becomes higher than 120% of the internal reference voltage, the controller will enter linear discharge mode. During this period, there is a 35Ω resistor connected between VOUT pin and ground, this will then discharge the output and try to keep it within the normal range. Once output voltage falls lower than 105% of reference, controller exits linear discharge mode.

Over-Current-Protection and Hiccup

The MP8868 has a cycle-by-cycle over-current limit. When the inductor current peak value exceeds the set current limit threshold, the HS-FET will turn off and the LS-FET will turn on and remains on until the inductor current falls below the internal "valley" current limit threshold. The "valley" current limit circuit is employed to decrease the operation frequency after the "peak" current limit threshold is triggered. Meanwhile, the output voltage drops until V_{FB}(9) is below the Under-Voltage (UV) threshold—typically 30% below the reference. Once UV is triggered, the MP8868 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. The average short circuit current is greatly reduced to alleviate thermal issues and to protect the regulator. The MP8868 exits the hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die reaches temperatures that exceed 160°C, it shuts down the whole chip. When the temperature is less than its lower threshold, typically 140°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C5, L1 and C2 (Figure). If (V_{IN}-V_{SW}) exceeds 5V, U1 will regulate M1 to maintain a 5V BST voltage across C5.

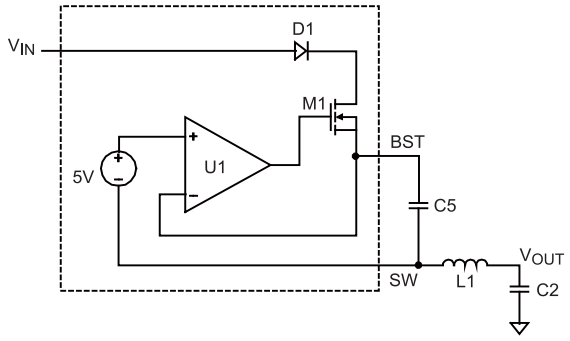


Figure 5: Internal Bootstrap Charging Circuit

Startup and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

I^2C Control and Default Output Voltage

When the MP8868 is enabled which means EN=high and VIN>UVLO, the chip starts up to an output voltage which is set by FB feedback resistors with programmed soft-start time. After that, the I^2C bus can communicate with master. If the chip doesn't receive I^2C communication signal all the time, it works well through FB pin feedback and performs the similar behavior as traditional non-I^2C part.

Once the I²C receives valid output reference voltage scaling instruction, if V_BOOT="1", output voltage is determined by the resistor divider R1, R2 and V_{REF} voltage. V_{OUT} value can be calculated by following equation (V_{REF} default value is 0.6V):

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2})$$

If V_BOOT="0", the output voltage will be determined by I²C control and the FB feedback loop is disabled.

The output reference voltage scaling is realized by adjusting internal reference voltage V_REF which is the non-invert input of error amplifier. After MP8868 receives a valid data byte of output reference voltage setting, it searches the corresponding reference voltage from the truth table and then sends the command of adjusting Vref with controlled slew rate. The slew rate is determined by 3 bits of another register which can be read and write accordingly.

I²C INTERFACE

I²C Serial Interface Description

I²C is a 2-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are externally pulled to a bus voltage when they are “idle”. Connecting to the line, a master device generates the SCL signal and device address and arranges the communication sequence. MP8868 interface is an I²C slave. The I²C interface adds flexibility to the power supply solution. The output voltage, transition slew rate or other interesting parameters can be instantaneously controlled by I²C interface. The default I²C address of MP8868 is “62” (HEX) or “1100010” (BINARY) and is “6A” (HEX) or “1101010” if pull A0 pin to ground.

Data validity

One clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (see Figure.6).

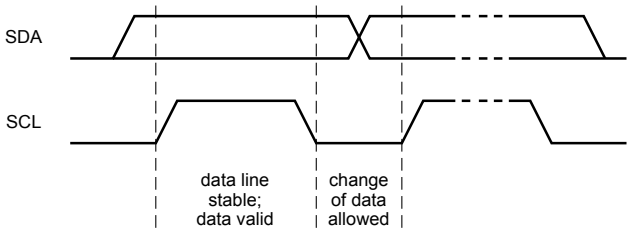


Figure 6: Bit transfer on the I²C-bus

The START and STOP are signaled by the master device which signifies the beginning and the end of the I²C transfer. The START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL is HIGH. The STOP condition is defined as the SDA signal transitioning from LOW to HIGH while the SCL is HIGH as shown in Figure 7.

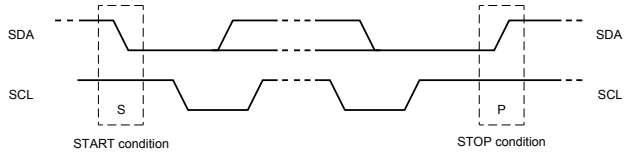


Figure 7: START and STOP Conditions

START and STOP conditions are always generated by the master. The bus is considered to be busy after the START condition. The bus is considered to be free again after a minimum of 4.7uS after the STOP condition. The bus stays busy if a repeated START (Sr) is generated instead of a STOP condition. The START (S) and repeated START (Sr) conditions are functionally identical.

Transfer Data

Every byte put on the SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse.

Data transfers follow the format shown in Figure 8. After the START condition (S), a slave address is sent. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W) - a ‘zero’ indicates a transmission (WRITE), a ‘one’ indicates a request for data (READ). A data transfer is always terminated by a STOP condition (P) generated by the master. However, if a master still wishes to communicate on the bus, it can generate a repeated START condition (Sr) and address another slave without first generating a STOP condition.

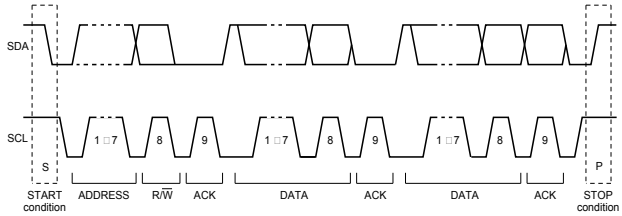


Figure 8: A complete data transfer

The MP8868 requires a start condition, a valid I²C address, a register address byte, and a data byte for a single data update. After receipt of each byte, MP8868 acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I²C address selects the MP8868. MP8868 performs an update on the falling edge of the LSB byte.

REGISER DESCRIPTION

Register Map

ADD	NAME	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00	VSEL	R/W	V_BOOT	Output Reference						
01	SysCntlreg1	R/W	EN	GO_BIT	Slew Rate			Switching Frequency		Mode
02	ID1	R	Vendor ID				Die id			
03	Status	R	Reserved			VID_OK	OC	OTEW	OT	PG

Register Description

1. **Reg00 VSEL**

NAME	BITS	DEFAULT	DESCRIPTION
V_BOOT	D7	1	"FB" control loop enable bit. V_BOOT="1" means the output voltage is determined by resistor divider connecting to "FB" (FB control loop). V_BOOT="0" means the output voltage is controlled by I^2C through "VOUT" (I^2C control loop). This bit is helpful for the default output voltage setting before I^2C signal comes. If the I^2C is not used, the part works well with "FB" pin.
Output Reference	D[6:0]	0000000	Set output voltage from 0.6V to 1.87V as Table 1. Default value is 0.6V.

Table 1 Output Voltage Chart

D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT	D[6:0]	VOUT
000 0000	0.60	010 0000	0.92	100 0000	1.24	110 0000	1.56
000 0001	0.61	010 0001	0.93	100 0001	1.25	110 0001	1.57
000 0010	0.62	010 0010	0.94	100 0010	1.26	110 0010	1.58
000 0011	0.63	010 0011	0.95	100 0011	1.27	110 0011	1.59
000 0100	0.64	010 0100	0.96	100 0100	1.28	110 0100	1.60
000 0101	0.65	010 0101	0.97	100 0101	1.29	110 0101	1.61
000 0110	0.66	010 0110	0.98	100 0110	1.30	110 0110	1.62
000 0111	0.67	010 0111	0.99	100 0111	1.31	110 0111	1.63
000 1000	0.68	010 1000	1.00	100 1000	1.32	110 1000	1.64
000 1001	0.69	010 1001	1.01	100 1001	1.33	110 1001	1.65
000 1010	0.70	010 1010	1.02	100 1010	1.34	110 1010	1.66
000 1011	0.71	010 1011	1.03	100 1011	1.35	110 1011	1.67
000 1100	0.72	010 1100	1.04	100 1100	1.36	110 1100	1.68
000 1101	0.73	010 1101	1.05	100 1101	1.37	110 1101	1.69
000 1110	0.74	010 1110	1.06	100 1110	1.38	110 1110	1.70
000 1111	0.75	010 1111	1.07	100 1111	1.39	110 1111	1.71
001 0000	0.76	011 0000	1.08	101 0000	1.40	111 0000	1.72
001 0001	0.77	011 0001	1.09	101 0001	1.41	111 0001	1.73
001 0010	0.78	011 0010	1.10	101 0010	1.42	111 0010	1.74
001 0011	0.79	011 0011	1.11	101 0011	1.43	111 0011	1.75
001 0100	0.80	011 0100	1.12	101 0100	1.44	111 0100	1.76
001 0101	0.81	011 0101	1.13	101 0101	1.45	111 0101	1.77
001 0110	0.82	011 0110	1.14	101 0110	1.46	111 0110	1.78
001 0111	0.83	011 0111	1.15	101 0111	1.47	111 0111	1.79
001 1000	0.84	011 1000	1.16	101 1000	1.48	111 1000	1.80
001 1001	0.85	011 1001	1.17	101 1001	1.49	111 1001	1.81
001 1010	0.86	011 1010	1.18	101 1010	1.50	111 1010	1.82
001 1011	0.87	011 1011	1.19	101 1011	1.51	111 1011	1.83
001 1100	0.88	011 1100	1.20	101 1100	1.52	111 1100	1.84
001 1101	0.89	011 1101	1.21	101 1101	1.53	111 1101	1.85
001 1110	0.90	011 1110	1.22	101 1110	1.54	111 1110	1.86
001 1111	0.91	011 1111	1.23	101 1111	1.55	111 1111	1.87

2. Reg01 SysCntlreg1

NAME	BITS	DEFAULT	DESCRIPTION
EN	D[7]	1	I^2C controlled turn-on or turn-off the part. When external EN pin is low, the converter is off and I^2C is also shutdown. When EN pin is high, the EN bit will take over. The default EN bit is “1”.
GO_BIT	D[6]	0	Switch bit of I^2C writing authority for output reference command only. Set GO_BIT=”1” to enable the I^2C authority of writing output reference. When the command is finished, GO_BIT will auto reset to “0” to prevent false operation of VOUT scaling. If reference adjust is within 50mV, GO_BIT won’t be auto reset to “0”. In this case need manually set GO_BIT to “0”. Suggest writing GO_BIT=”1” first, then write the output reference voltage.
Slew Rate	D[5:3]	100	D[5:3] SLEW RATE D[5:3] SLEW RATE 000 64 mV/uS 100 4 mV/uS 001 32 mV/uS 101 2 mV/uS 010 16 mV/uS 110 1 mV/uS 011 8 mV/uS 111 0.5 mV/uS
Switching Frequency	D[2:1]	00	D[2:1] Fs 00 500kHz 01 750KHz 10 1MHz 11 1.5MHz
Mode	D0	1	A “0” enables PFM mode, a high disables PFM mode. Default in force CCM.

3. Reg02 ID1

NAME	BITS	DESCRIPTION
Vendor ID	D[7:4]	1000
IC Revision ID	D[3:0]	IC Revision

4. Reg03 Status

NAME	BITS	DESCRIPTION
Reserved	D[7:5]	Reserved for future use. Always set at 0
VID_OK	D[4]	I^2C controlled voltage adjustment is done. Internal circuit compares DAC output with “VOUT” pin voltage, if “VOUT” is in the 90%-110% range of DAC output, VID_OK bit is high which means the voltage scaling is finished. Otherwise, VID_OK=”0”. VID_OK compares DAC with VOUT/FB. UV 90%+-3%, OV 110%+-3%
OC	D[3]	Output over current indication. When bit is high, IC is in hiccup mode.
OTEW	D[2]	Die temperature early warning bit. When the bit is high, the die temperature is higher than 120˚C.
OT	D[1]	Over temperature indication. When bit is high the IC is in thermal shutdown
PG	D[0]	Output power good indication. When bit is high the VOUT power is good now. It means the VOUT is higher than 90% of designed regulation voltage. See details in “Power Good Indicator” Section.

APPLICATION INFORMATION

Setting the Output Voltage in FB control Loop

Reference voltage and external resistor divider and can set the output voltage through FB. The feedback resistor R1 and R3 also sets the feedback loop bandwidth with the internal compensation capacitor. Choose R1 value firstly, R2 is then given by (10):

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{REF}} - 1}$$

Notes:

10) VREF is 0.6V when Power up or EN on. After MP8868 is enabled, VREF can be programmed through I²C. Set V_BOOT=1 to enable FB control loop.

The T-type network (as shown in Figure 10) is highly recommended.

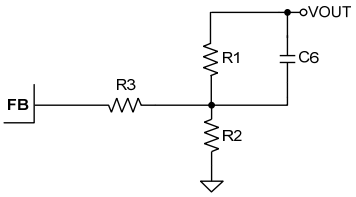


Figure 9: T-Type Network

Table 2 lists the recommended feedback resistors value for common output voltages.

Table 2: Resistor Selection for Common Output Voltages with Default 0.6V V_{REF}(11)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	C6 (pF)	L (μH)
0.9	80.6 (1%)	162 (1%)	51 (1%)	22	1.5
1.0	80.6 (1%)	120 (1%)	51 (1%)	22	1.5
1.2	80.6 (1%)	80.6 (1%)	40.2 (1%)	22	1.5
2.5	60.4 (1%)	19.1 (1%)	30 (1%)	22	2.2
3.3	60.4 (1%)	13.3 (1%)	20 (1%)	33	3.3
5	60.4 (1%)	8.25 (1%)	20 (1%)	33	3.3

Note:

11) The recommended parameters is basing on 12V input voltage and 22μFx4 output capacitor, different input voltage and output capacitor value may affect the selection of R1, R2, R3, C6. For other components' parameters, please refer to TYPICAL APPLICATION CIRCUITS on page 26.

Setting the Output Voltage in I²C control Loop

Besides setting the output voltage through FB loop, I²C loop also can set the output voltage through VOUT pin by setting V_BOOT=0. In this case, output voltage is the set reference voltage. Please refer to Table 1 for more details about output voltage setting.

Output Voltage Dynamic Scale

To dynamic scale the output voltage during MP8868 normal operating, it suggests following below two steps and referring to the Figure 10:

Step1: Write the GO_Bit (reg01[6]) to "1";

Step2: Write reg00 to select the feedback loop by setting V_BOOT(reg00[7]) and set reference voltage by Output Reference (reg00[0:6]) simultaneously. If reference adjust is within 50mV, GO_BIT won't be auto reset to "0", in this case it needs manually set GO_BIT to "0".

Repeat above two steps if need dynamic scale to other voltage.

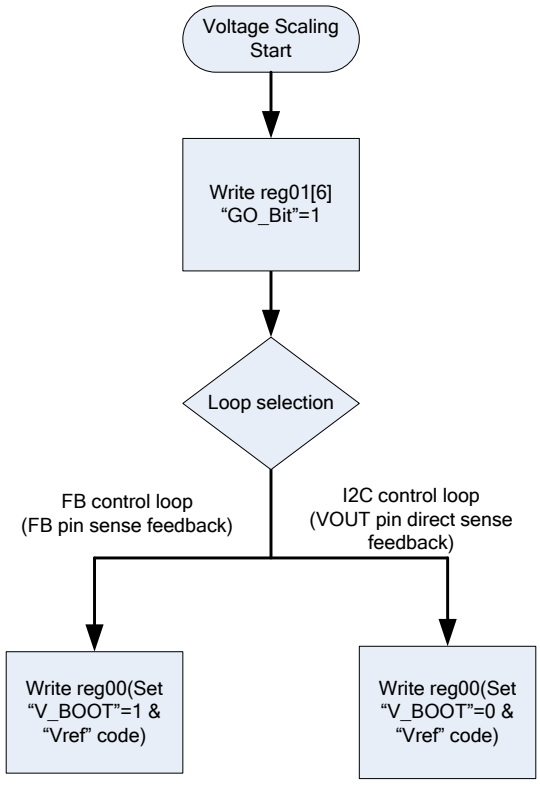


Figure 10: Output Voltage Dynamic Scale Flow Chart

Selecting the Inductor

Use a 0.47μH-to-10μH inductor with a DC current rating of at least 25% percent higher than the maximum load current for most applications. For highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from the following equation.

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔIL is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Use a larger inductor for improved efficiency under light-load conditions—below 100mA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore requires a capacitor is to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use two piece 22μF capacitors.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at VIN = 2VOUT, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, add a small, high quality ceramic capacitor (e.g. 0.1μF) placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low-ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP8868 can be optimized for a wide range of capacitance and ESR values.

PC Board Layout [12]

PCB layout is very important for stable operation. Follow these guidelines for best results.

1. The high current paths (PGND, VIN, and SW) should be placed very close to the device with short, direct and wide traces.
2. Keep the IN and GND pads connected with large copper and use at least two layers for IN and GND trace to achieve better thermal performance. Also, add several Vias close to the IN and GND pads to help on thermal dissipation.
3. Put the input capacitors as close to the VIN and GND pins as possible.
4. Put the decoupling capacitor as close to the VCC and GND pins as possible.
5. The external feedback resistors should be placed next to the FB pin. Make sure that there is no via on the FB trace.
6. Keep the switching node SW short and away from the feedback network.
7. Keep the BST voltage path (BST, C5, and SW) as short as possible.
8. Four-layer layout is strongly recommended to achieve better thermal performance.

Notes:

12) The recommended layout is based on the Figure 13 Typical Application circuit in page26.

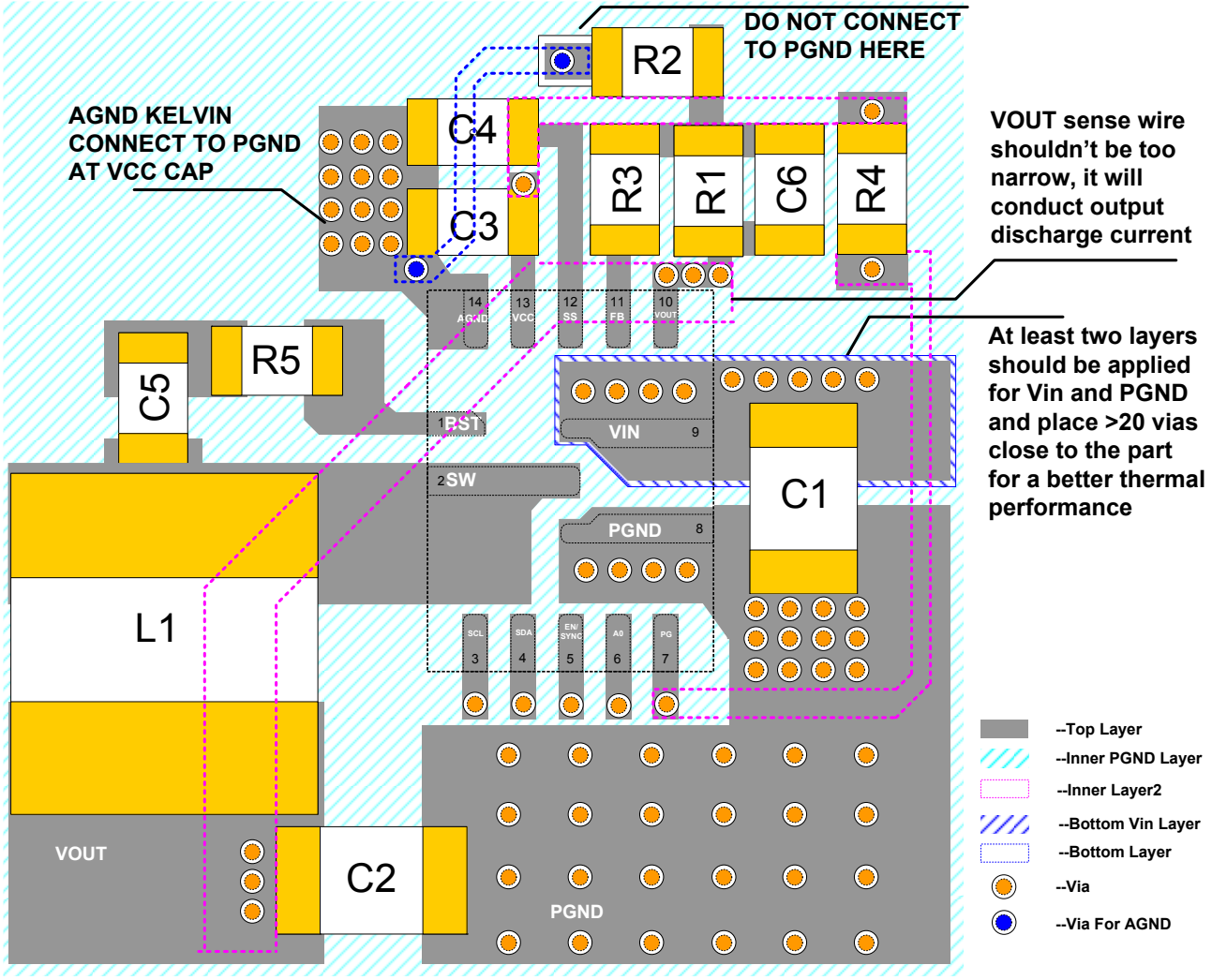


Figure 11: Recommend Layout

Design Example

Below is a design example following the application guidelines for the specifications:

Table 3 Design Example

V_{IN}	12V
V_{OUT}	1V
I_O	10A

The detailed application schematics are shown in Figure 13. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related Evaluation Board Datasheets.

TYPICAL APPLICATION CIRCUITS (13)

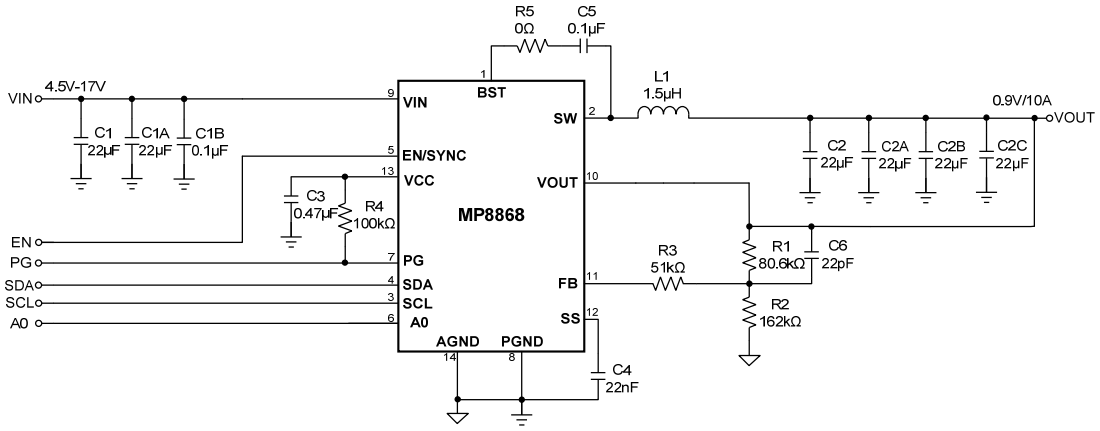


Figure 12: V_{IN}=4.5-17V, V_{OUT}=0.9V, I_{OUT}=10A

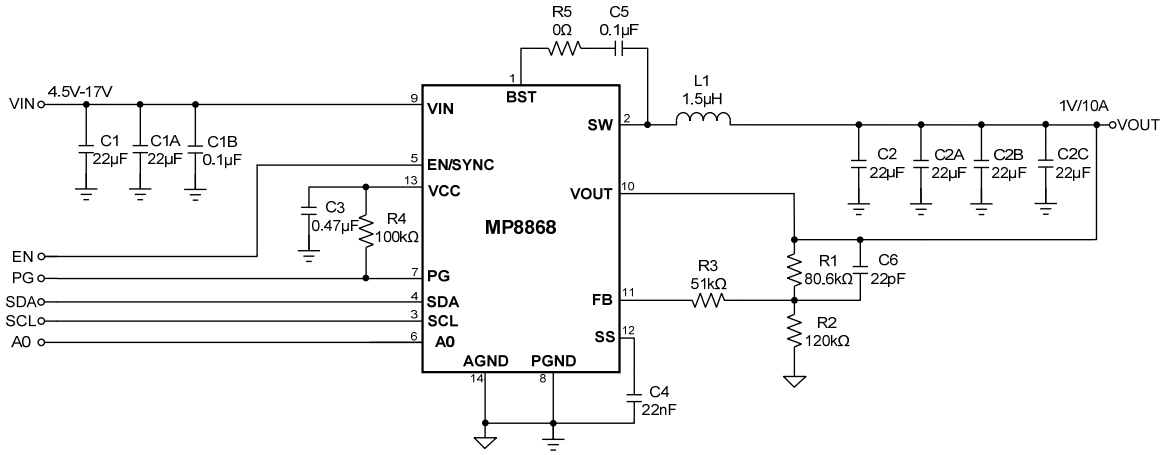


Figure 13: V_{IN}=4.5-17V, V_{OUT}=1V, I_{OUT}=10A

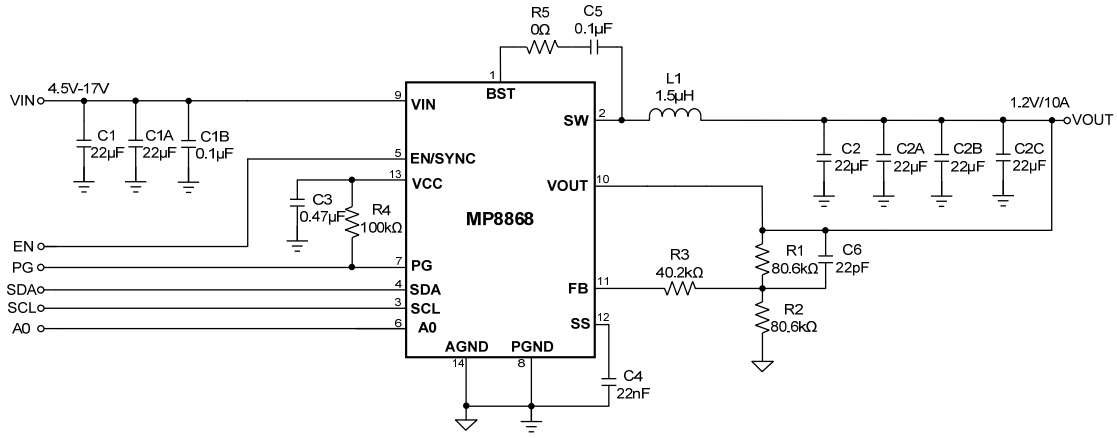


Figure 14: V_{IN}=4.5-17V, V_{OUT}=1.2V, I_{OUT}=10A

Notes:

13) All circuits are basing on 0.6V default reference voltage.

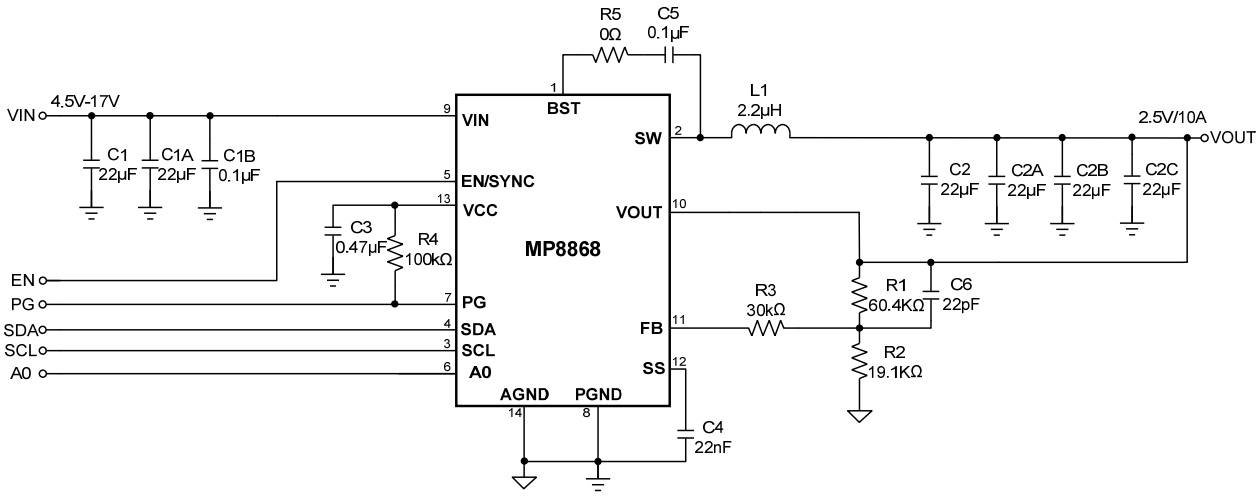


Figure 15: V_{IN}=4.5-17V, V_{OUT}=2.5V, I_{OUT}=10A

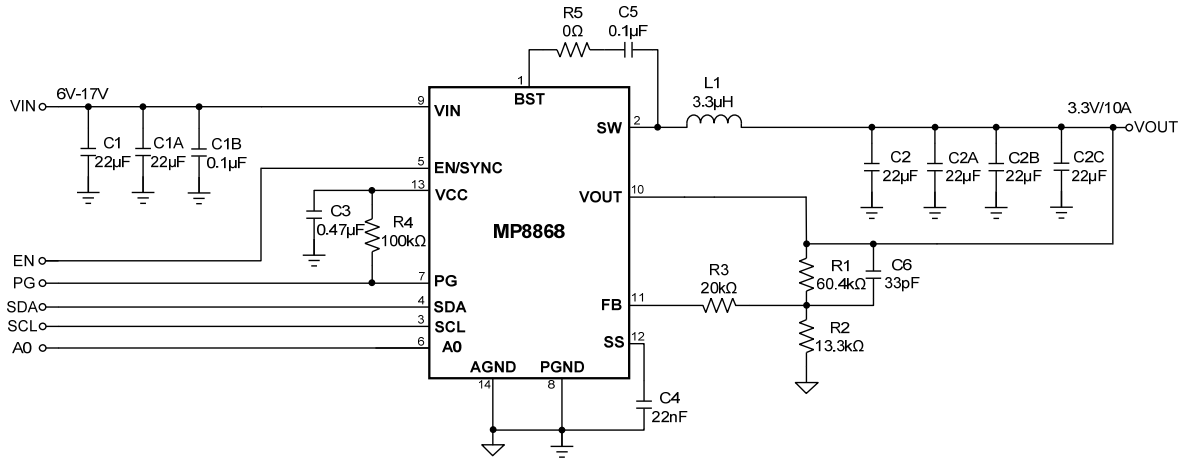


Figure 16: V_{IN}=6-17V, V_{OUT}=3.3V, I_{OUT}=10A(14)

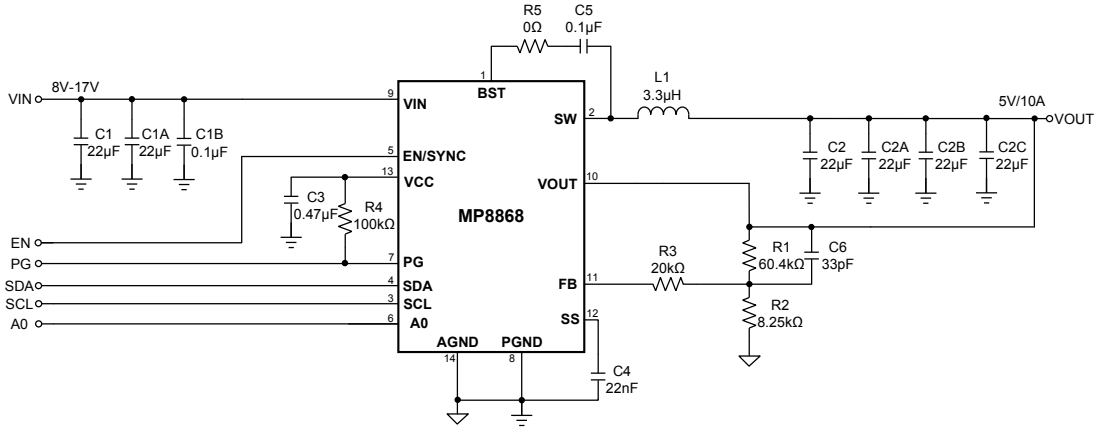


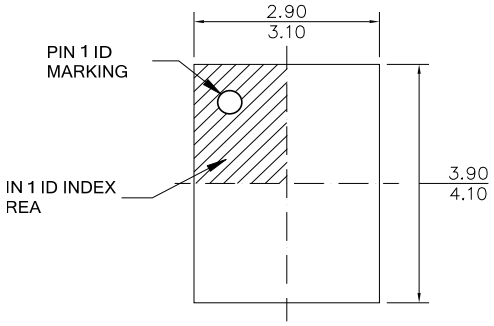
Figure 17: V_{IN}=8-17V, V_{OUT}=5V, I_{OUT}=10A(14)

Notes:

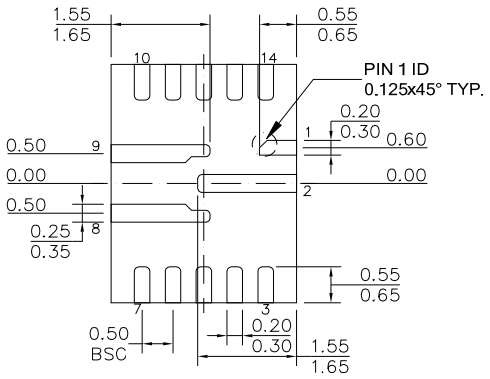
14) Basing on Evaluation Board test result at 25℃ ambient temperature, lower input voltage will trigger over temperature protection with full load.

PACKAGE INFORMATION

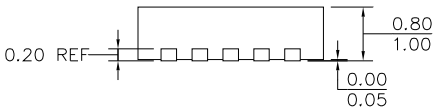
QFN14 (3x4mm)



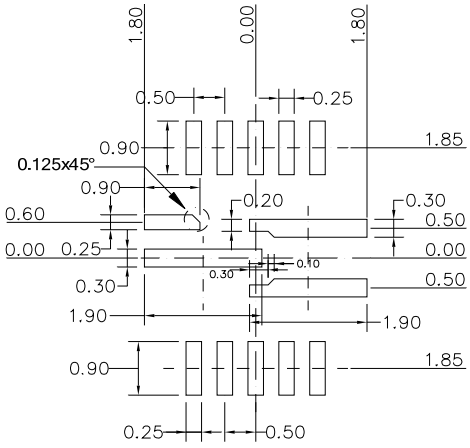
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMET MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.