Full-Featured, Dual-Slot AdvancedMC™ Controller

Check for Samples: TPS2359

FEATURES

- ATCA AdvancedMC™ Compliant
- Full Control for Two AdvancedMC™ Modules
- Independent 12-V Current Limit and Fast Trip
- 3.3-V and 12-V FET ORing for MicroTCA™
- Internal 3.3-V Current Limit and ORing
- Power Good and Fault Reporting Through I^2C
- I^2C Programmable Fault Times and Current Limits
- FET Status Bits for all Channels
- 36-Pin PQFN Package
- 3-V and 12-V Interlock for AdvancedMC Compliance

APPLICATIONS

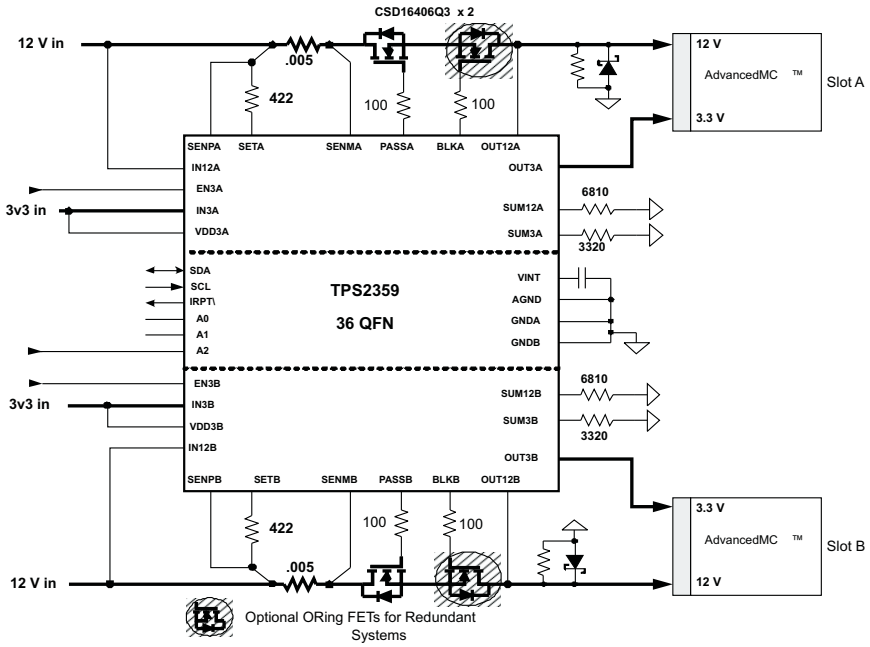
- ATCA Carrier Boards
- MicroTCA™ Power Modules
- AdvancedMC™ Slots
- Systems Using 12 V and 3.3 V
- Base Stations

DESCRIPTION

The TPS2359 dual-slot hot-plug controllers perform all necessary power interface functions for two AdvancedMC™ (Advanced Mezzanine Card) modules.

Two fully integrated 3.3-V channels provide inrush control, over-current protection, and FET ORing. Two 12-V channels provide the same functions using external FETs and sense resistors. The 3.3-V current limits are factory set to AdvancedMC™ compliant levels and the 12-V current limits are programmed using external sense resistors. The accurate current sense comparators of the TPS2359 satisfy the narrow ATCA™ AdvancedMC™ current limit requirements.

Figure 1. TPS2359 Application Diagram



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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ORDERING INFORMATION (1)

DEVICE	TEMPERATURE	PACKAGE(2)	ORDERING INFORMATION
TPS2359	-40°C to 85°C	QFN36	TPS2359RHH

(1) Add an R suffix to the device type for tape and reel.
(2) For the most current package and ordering information see the Package Option Addendum at the end of this document or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	VALUE	UNIT
PASSx, BLKx	-0.3 to 30	V
IN12x; OUT12x; SENPx; SENMx; SETx; $\overline{IRPT}$	-0.3 to 17	
IN3x; OUT3x; EN3x; VDDx; SUMx; SDA, SCL	-0.3 to 5	
AGND, GNDx	-0.3 to 0.3	
A0, A1, A2	0 to VINT	
SUMx	5	mA
VINT	-1 to 1	
OUT3x	Internally limited	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device under any conditions beyond those indicated under recommended operating conditions is neither implied nor guaranteed. Exposure to absolute maximum rated conditions for extended periods of time may affect device reliability.

ELECTROSTATIC DISCHARGE (ESD) PROTECTION

TEST METHOD	MIN	UNITS
Human Body Model (HBM)	2	kV
Charged Device model (CDM)	0.5	

DISSIPATION RATINGS

PACKAGE	θJA - High-k (°C/W)
36 QFN	35

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN12x}	Payload power input voltage	8.5	12	15	V
V_{IN3x}	Management power input voltage	3	3.3	4	
$V_{VDD3x,3}$	Management power supply voltage	3	3.3	4	
I_{OUT3x}	Management power output current			165	mA
I_{SUMx}	Summing pin current		100	1000	µA
	PASSx pin board leakage current	-1		1	
	VINT bypass capacitance	1	10	250	nF
T_J	Operating junction temperature range	-40		125	°C

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ELECTRICAL CHARACTERISTICS

IN3A = IN3B = VDD3A = VDD3B = 3.3 V. IN12A = IN12B = SENPA = SENPB = SENMA = SENMB = SETPA = SETPB = 12 V. EN3A = EN3B = AGND = GNDA = GNDB = 0 V. SUM12A = SUM12B = 6.8 kΩ to ground. SUM3A = SUM3B = 3.3 kΩ to ground. All other pins open. All I2C bits at default values. Over free air temperature operating range and all voltages referenced to AGND, -40°C ≤ T_A ≤ 85°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
ENABLE Inputs					
Threshold voltage, falling edge		1.2	1.3	1.4	V
Hysteresis		20	50	80	mV
Pullup current	EN3x = 0 V	5	8	15	µA
Input bias current	EN3x = 5 V		1	5	
3.3-V turn off time	EN3x deasserts to V_{OUT3x} < 1.0 V, C_{OUT} = 0 µF			10	µs
12-V turn off time	EN3x deasserts to V_{OUT12x} < 1.0 V, C_{OUT} = 0 µF, Q_{GATE} = 35 nF			20	
VINT					
Output voltage	0 < I_{VINT} < 50 µA	2	2.3	2.8	V
Power GOOD Comparators					
Threshold voltage	$\overline{12xPG}$, falling OUT12x	10.2	10.5	10.8	V
	$\overline{3xPG}$, falling OUT3x	2.7	2.8	2.9	
Hysteresis	$\overline{12xPG}$, measured at OUT12x		130		mV
	$\overline{3xPG}$, measured at OUT3x		50		
Fault Timer					
Fault time bit weight	3xFT[4:0] = 12xFT[4:0] = 00001B		0.45		ms
Timer duty cycle	= (fault time) / (retry period)	0.70%	0.77%	0.80%	
12-V Summing node					
Input referred offset	V_{SENMx} = 10.8 – 13.2 V, V_{SENPx} = V_{SENMx} + 50 mV, measure V_{SETx} – V_{SENMx}	–2		2	mV
Summing threshold	12xCL[3:0] = 1111B, VPASSx = 15 V	0.66	0.675	0.69	V
Leakage current	VSETx = VSENMx – 10 mV			1	µA
12-V Current limit					
Current limit threshold	R_{SUMx} = 6.8 kΩ, R_{SETx} = 422 Ω, increase I_{LOADx} and measure V_{SENPx} – V_{SENMx} when V_{PASSx} = 15 V	47.5	50	52.5	mV
Sink current in current limit	V_{SUMx} = 1 V, V_{PASSx} = 12 V, measure I_{PASSx}	20		40	µA
Fast trip threshold	Measure V_{SENPx} – V_{SENMx}	80	100	120	mV
Fast turn-off delay	20-mV overdrive, C_{PASSx} = 0 pF, t_{p50-50}		200	300	ns
Bleed down resistance	V_{OUT} = 6 V	1.1	1.6	2.1	kΩ
Bleed down threshold		75	100	130	mV
Timer start threshold	V_{PASSx} – V_{INx} when fault timer starts	5	6	7	V

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ELECTRICAL CHARACTERISTICS (continued)

IN3A = IN3B = VDD3A = VDD3B = 3.3 V. IN12A = IN12B = SENPA = SENPB = SENMA = SENMB = SETPA = SETPB = 12 V. EN3A = EN3B = AGND = GNDA = GNDB = 0 V. SUM12A = SUM12B = 6.8 kΩ to ground. SUM3A = SUM3B = 3.3 kΩ to ground. All other pins open. All I2C bits at default values. Over free air temperature operating range and all voltages referenced to AGND, -40°C ≤ T_A ≤ 85°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
12-V UVLO					
UVLO rising	IN12x rising	8.1	8.5	8.9	V
UVLO hysteresis	IN12x falling	0.44	0.5	0.59	
12-V BLOCKING					
Turn-on threshold	Measure $V_{SENPx} – V_{OUTx}$	5	10	15	mV
Turn-off threshold	Measure $V_{SENPx} – V_{OUTx}$	–5	–3	0	
Turn-off delay	20-mV overdrive, C_{BLKx} = 0 pF, t_{p50-50}		200	300	ns
12-V Gate drivers (PASSx, BLKx)					
Output voltage	$V_{INx} = V_{OUTx}$ = 10 V	21.5	23	24.5	V
Sourcing current	$V_{IN12x} = V_{OUT12x}$ = 10 V, $V_{PASSx} = V_{BLKx}$ = 17 V	20	30	40	µA
Sinking current	Fast turnoff, $V_{PASSx} = V_{BLKx}$ = 14 V	0.5	1		A
	Sustained, $V_{PASSx} = V_{BLKx}$ = 4 – 25 V	6	14	25	mA
Pulldown resistance	In OTSD (at 150 °C)	14	20	26	kΩ
Fast turnoff duration		5	10	15	ms
Safety gate pulldown	IRF3710, slew S or D 15 V in 1 ms			1.25	V
Startup time	IN12x rising to PASSx and BLKx sourcing			0.25	ms
3.3-V Summing node					
Summing threshold		655	675	695	mV
3.3-V Current limit					
On resistance	I_{OUT3x} = 150 mA		290	500	mΩ
Current limit	R_{SUM3x} = 3.3 kΩ , V_{OUT3x} = 0 V	170	195	225	mA
Fast trip threshold		240	300	400	
Fast turn-off delay	I_{OUT3x} = 400 mA, t_{p50-50}		750	1300	ns
Bleed down resistance	V_{OUT3x} = 1.65 V	280	400	500	Ω
Bleed down threshold		75	100	130	mV
3.3-V UVLO					
UVLO rising	IN3x rising	2.65	2.75	2.85	V
UVLO hysteresis	IN3x falling	200	240	300	mV
3.3-V Blocking					
Turn-on threshold	Measure $V_{IN3x} – V_{OUT3x}$	5	10	15	mV
Turn-off threshold	Measure $V_{IN3x} – V_{OUT3x}$	–5	–3	0	
ORing turn-on delay	V_{IN3x} = 3.3 V, V_{OUT3x} = 3.5 V, OUT3x = 100 Ω to GND, 3ORON = 1. Remove 3.5 V from OUT3x. Measure time from V_{OUT3x} thru 2.9 V to V_{OUT3x} = 3.2 V		300	350	µs
Fast turnoff delay	20 mV overdrive, t_{p50-50}		250	350	ns

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ELECTRICAL CHARACTERISTICS (continued)

IN3A = IN3B = VDD3A = VDD3B = 3.3 V. IN12A = IN12B = SENPA = SENPB = SENMA = SENMB = SETPA = SETPB = 12 V. EN3A = EN3B = AGND = GNDA = GNDB = 0 V. SUM12A = SUM12B = 6.8 kΩ to ground. SUM3A = SUM3B = 3.3 kΩ to ground. All other pins open. All I2C bits at default values. Over free air temperature operating range and all voltages referenced to AGND, -40°C ≤ T_A ≤ 85°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Currents (I_{INx} + I_{SENPx} + I_{SENMx} + I_{SETx} + I_{VDDx})					
All channels enabled	I_{OUT3A} = I_{OUT3B} = 0		3.1	4	mA
All channels disabled			2.0	2.8	
Thermal Shutdown					
Whole-chip shutdown temperature	T_J rising, I_{OUT3A} = I_{OUT3B} = 0	140	150		°C
3.3-V channel shutdown temperature	T_J rising, I_{OUT3A} or I_{OUT3B} in current limit	130	140		
Hysteresis	Whole chip or 3.3-V channel		10		
Serial Interface (SDA, SCL, A0–2, IRPT					
Lower logic threshold	A0 – A2	0.33	0.35	0.37	V
Upper logic threshold	A0 – A2	1.32	1.35	1.38	
Input pullup resistance	A0 – A2, V_{Ax} = 0 V	400	700	1000	kΩ
Input pulldown resistance	A0 – A2, V_{Ax} = VINT	200	350	550	
Input open-circuit voltage	IAx = 0 V	0.5	0.8	1.0	V
Threshold voltage, rising	SDA, SCL			2.3	
Threshold voltage, falling	SDA, SCL	1.0			
Hysteresis	SDA, SCL	165			mV
Leakage	SDA, IRPT			1	µA
Input clock frequency	SCL			400	kHz

Figure 2. Signal and Pin Naming Convention

SIGNAL AND PIN NAMING

The PICMG™ AdvancedMC™ specification refers to 3.3 V power as Management Power and refers to 12 V power as Payload Power. This datasheet uses a naming convention that reflects the associated voltage (12 or 3.3 V) and arbitrary AdvancedMC™ slot (A or B).

- Signals and pins associated with slot A 12 V payload power end with 12A
- Signals and pins associated with slot A 3.3 V management power end with 3A
- Signals and pins associated with slot B 12 V payload power end with 12B
- Signals and pins associated with slot B 3.3 V management power end with 3B

Pins and signals unique to 12 V channels have only an A or B suffix.
The register names are similar except the voltage/slot identifier is at the beginning of the bit name.

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DEVICE INFORMATION

TPS2359 BLOCK DIAGRAMS

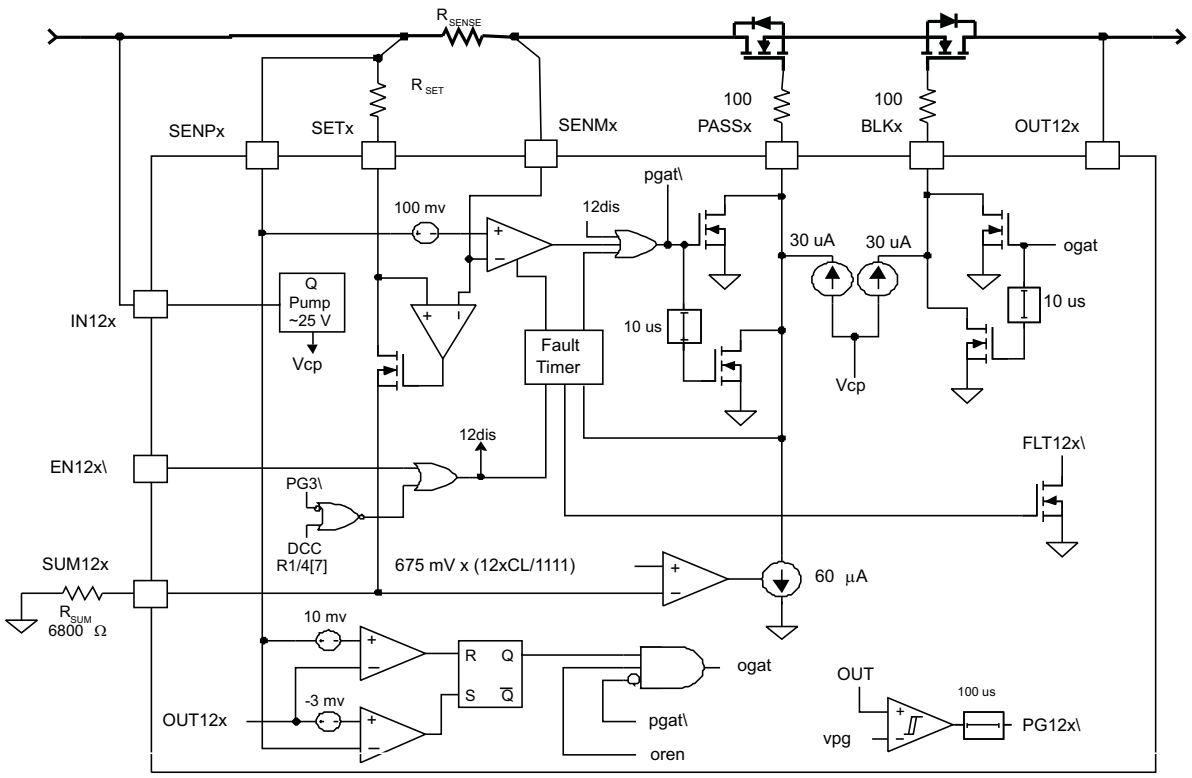
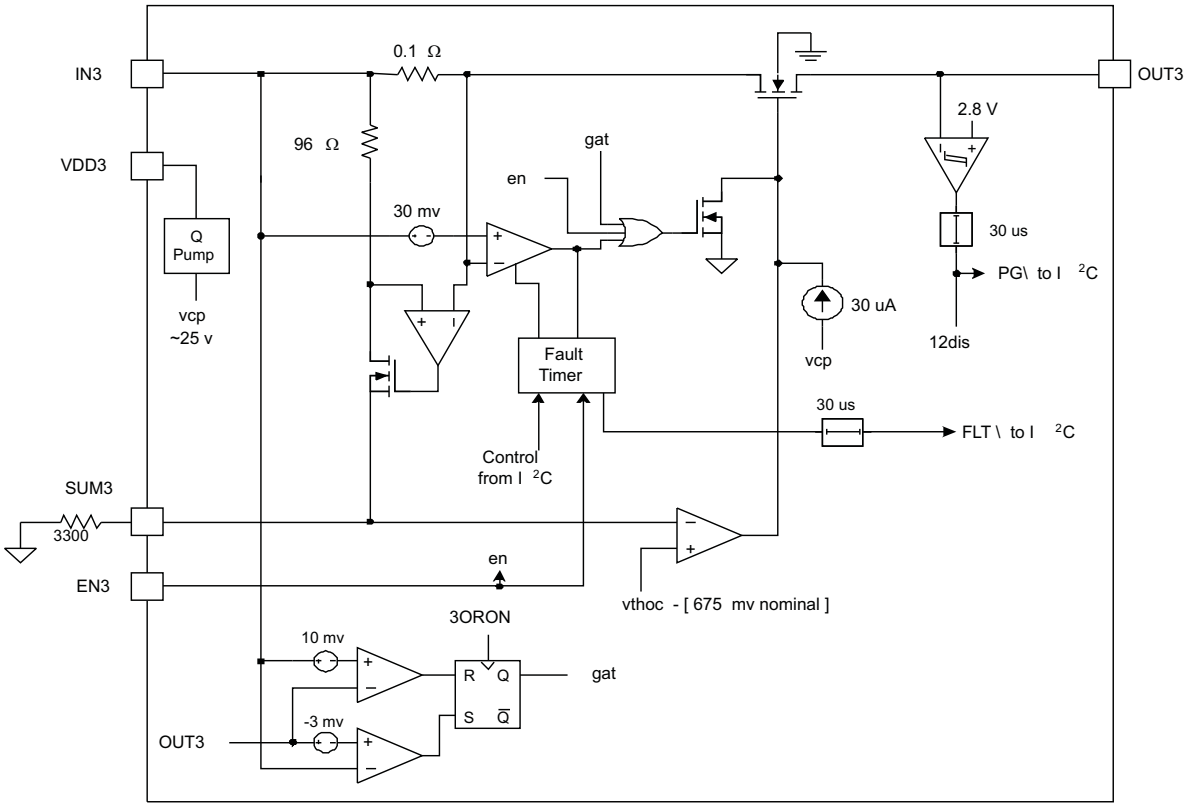


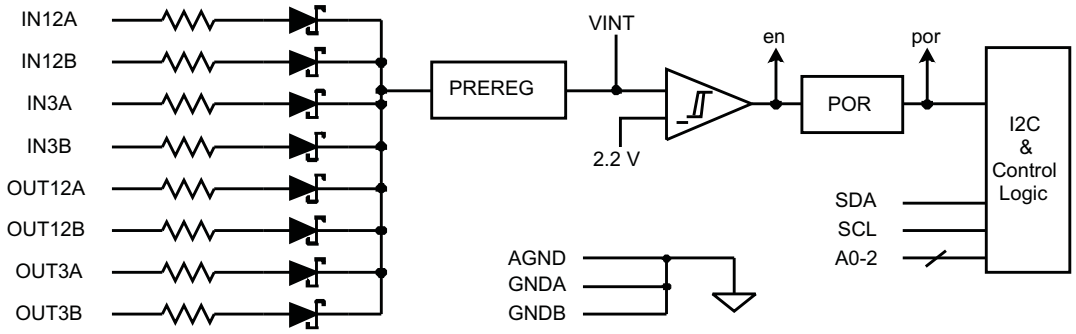
Figure 3. Payload Power Channel (two channels per device)

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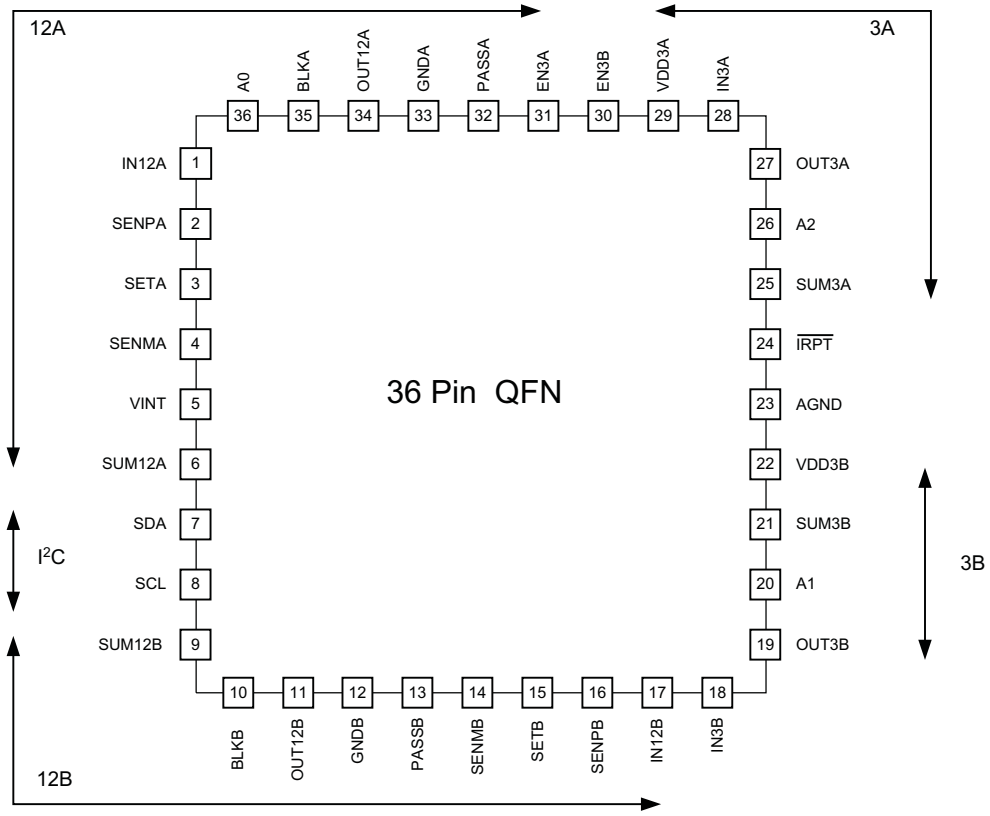
Management Power Channel (two channels per device)



Common Circuitry



Top View 36-Pin QFN



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TPS2359 TERMINAL FUNCTIONS

PIN #	NAME	TYPE	DESCRIPTION
1	IN12A	V_{DD}	12A input
2	SENPA	I	12A input sense
3	SETA	I	12A current limit set
4	SENMA	I	12A current limit sense
5	VINT	I/O	Bypass capacitor connection point for internal supply, pullup for A0 – A2
6	SUM12A	I/O	12A summing node
7	SDA	I/O	Serial data input/output
8	SCL	I	Serial data clock
9	SUM12B	I/O	12B summing node
10	BLKB	O	12B blocking transistor gate drive
11	OUT12B	I/O	12B output
12	GNDB	GND	12B power ground
13	PASSB	O	12B pass transistor gate drive
14	SENMB	I	12B current limit sense
15	SETB	I	12B current limit set
16	SENPB	I	12B input sense
17	IN12B	V_{DD}	12B input
18	IN3B	V_{DD}	3B input
19	OUT3B	I/O	3B output
20	A1	I	I^2C address programming bit, LSB+1
21	SUM3B	I/O	3B summing node
22	VDD3B	V_{DD}	3B charge pump input
23	AGND	GND	Analog ground
24	$\overline{IRPT}$	O	Active low interrupt, asserts when a PG deasserts or when a FLT\ asserts
25	SUM3A	I/O	3A summing node
26	A2	I	I^2C address programming bit, LSB+2
27	OUT3A	I/O	3A output
28	IN3A	V_{DD}	3A input
29	VDD3A	V_{DD}	3A charge pump input
30	EN3B	I	3B enable, active high
31	EN3A	I	3A enable, active high
32	PASSA	O	12A pass transistor gate drive
33	GNDA	GND	12A power ground
34	OUT12A	I/O	12A output
35	BLKA	O	12A blocking transistor gate drive
36	A0	I	I^2C address programming bit, LSB

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DETAILED PIN DESCRIPTION

A0, A1, A2 These three pins select one of 27 unique I^2C addresses for address of the TPS2359. Each pin may be tied to ground, tied to the VINT pin, or left open. See TPS2359 I^2C Interface section for details and Table 17 for specific addresses.

AGND Ground pin for analog circuitry inside the TPS2359.

BLKx Gate drive pin for the 12x channel BLK FET. This pin sources 30 µA to turn the FET on. An internal clamp prevents this pin from rising more than 14.5 V above OUT12x. Setting the ORENx bit low holds the BLKx pin low. BLKx is pulled low when PASSx is commanded low.

EN3x Active-high enable input. Pulling this pin low turns off channel 3x by pulling the gate of the internal pass FET to GND. An internal 200-kΩ resistor pulls this pin up to VINTwhen disconnected.

GNDx Ground pin for power circuitry associated with the 12x channel. These pins should connect to a ground plane shared with the AGND pin.

IN12x Supply pin for channel 12x internal circuitry.

IN3x Supply pin for channel 3x internal pass FET.

$\overline{\text{IRPT}}$ Open drain output that pulls low when internal circuitry sets any of the eight status bits in Register 7. Reading Register 7 restores $\overline{\text{IRPT}}$ to its high-Z state. Register 7 contains FLT and PG bits for all 4 channels.

OUT12x Senses the output voltage of the channel 12x path.

OUT3x Output of the channel 3x internal pass FET. If DCC R6 [7] = 0, then OUT3x must be > 2.85 V before the 12-V channel is allowed to turn on.

PASSx Gate drive pin for the 12x channel PASS FET. This pin sources 30 µA to turn the FET on. An internal clamps prevents this pin from rising more than 14.5 V above IN12x.

SCL Serial clock input for the I^2C interface. For details of the SCL line, see TPS2359 I^2C Interface section.

SDA Bidirectional I^2C data line. For details of the SDA line, see TPS2359 I^2C Interface section for details.

SENMx Senses the voltage on the low side of the channel 12x current sense resistor.

SENPx Senses the voltage on the high side of the channel 12x current sense resistor.

SETx A resistor connected from this pin to SENPx sets the current limit level in conjunction with the current sense resistor and the resistor connected to the SUM12x pin, as described in 12-V thresholds – setting current limit and fast over current trip section. The internal amplifier attemps to keep $V_{SET} = V_{SENM}$.

SUMx A resistor connected from this pin to ground forms part of the channel x current limit. As the current delivered to the load increases, so does the voltage on this pin. When the voltage on this pin reaches a threshold (by default 675 mV), the current limit amplifier acts to prevent the current from further increasing.

VDD3x Supply pin for channel3x internal circuitry.

VINT This pin connects to the internal 2.35-V rail. A 0.1-µF capacitor must be connected from this pin to ground. One can connect the A0–A2 pins to this supply to pull them high, but no other external circuitry should connect to VINT.

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TYPICAL CHARACTERISTICS

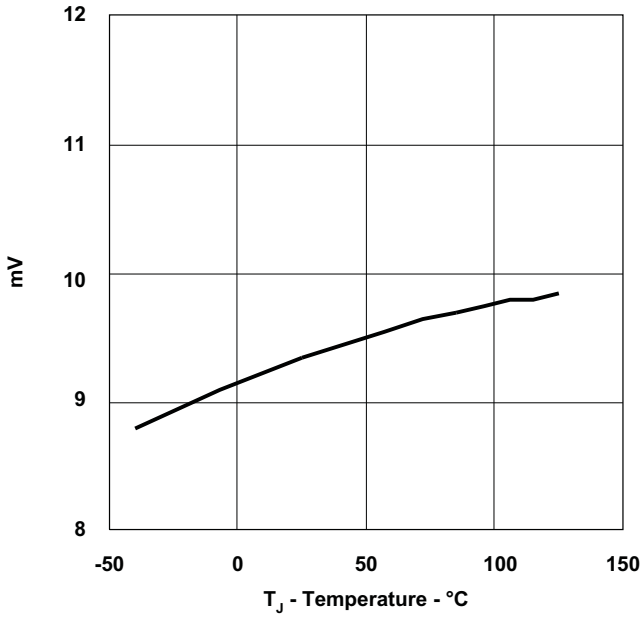


Figure 4.

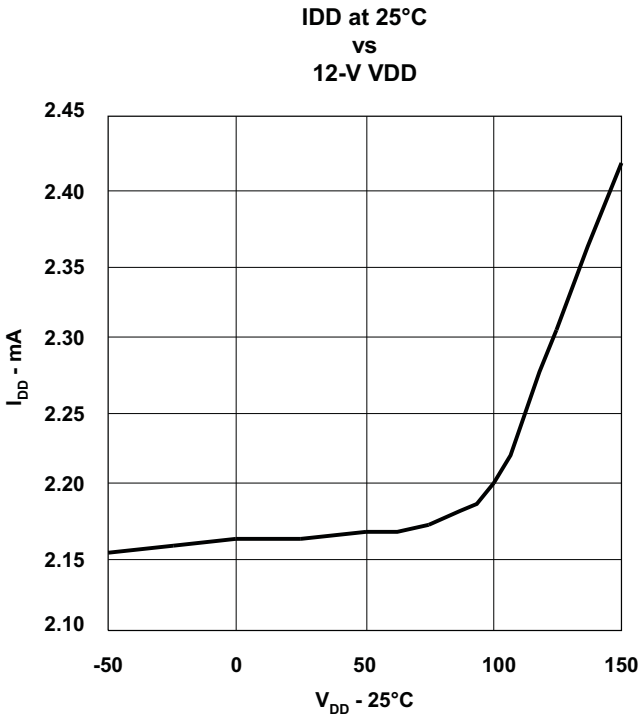


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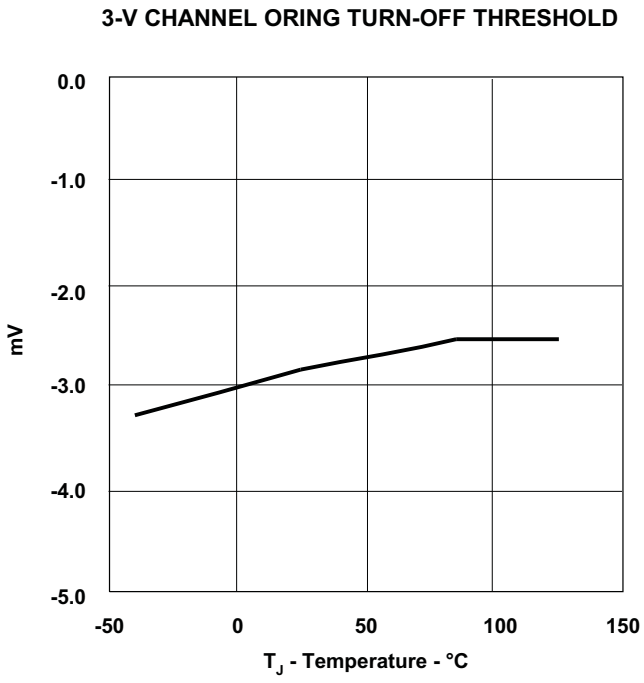


Figure 6.

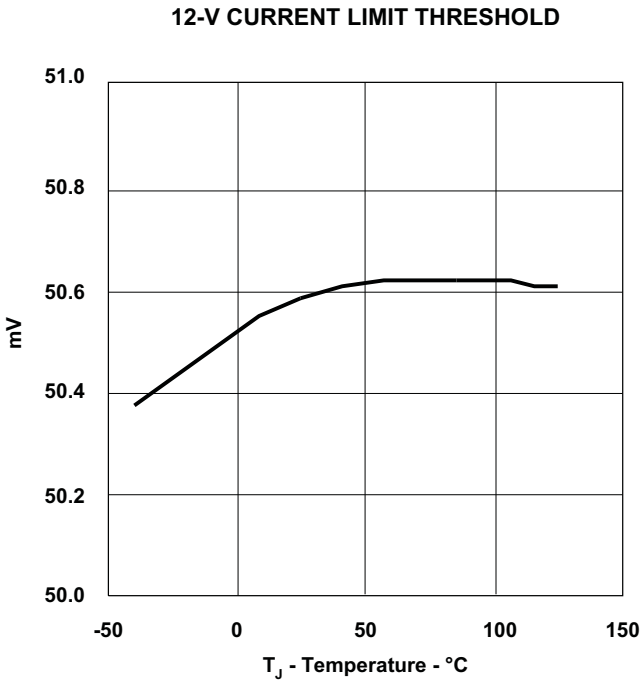


Figure 7.

TYPICAL CHARACTERISTICS (continued)

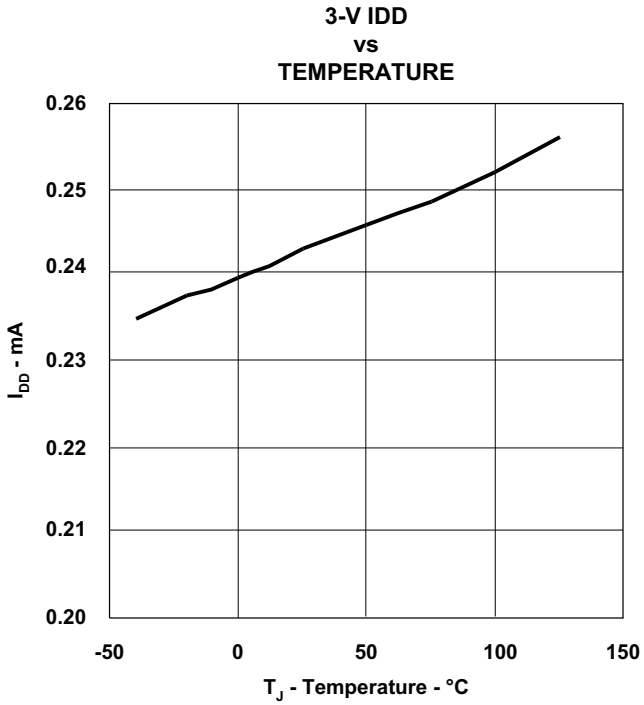


Figure 8.

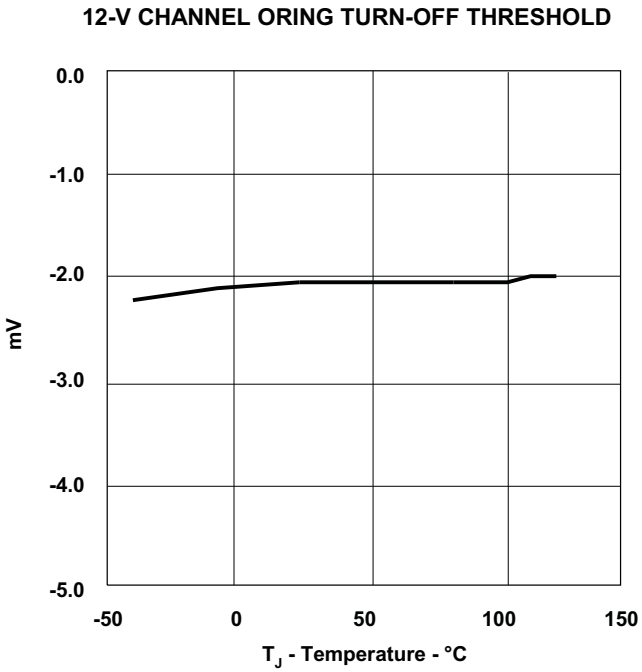


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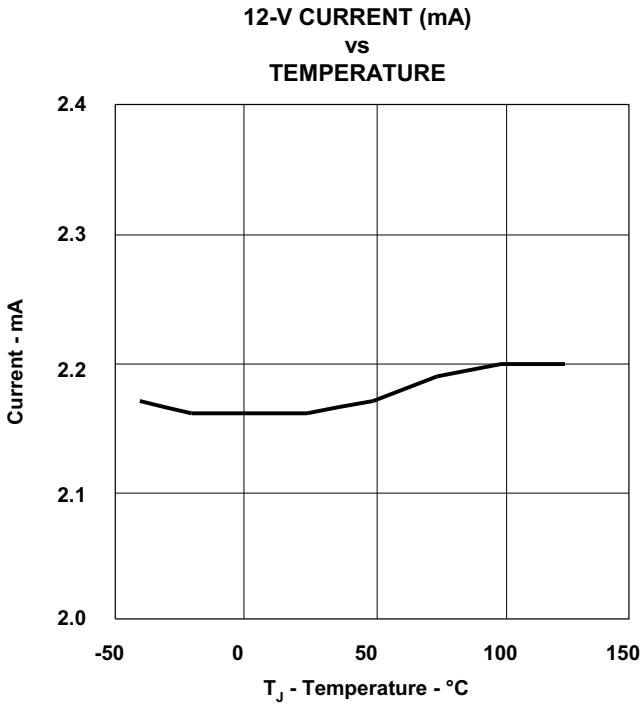


Figure 10.

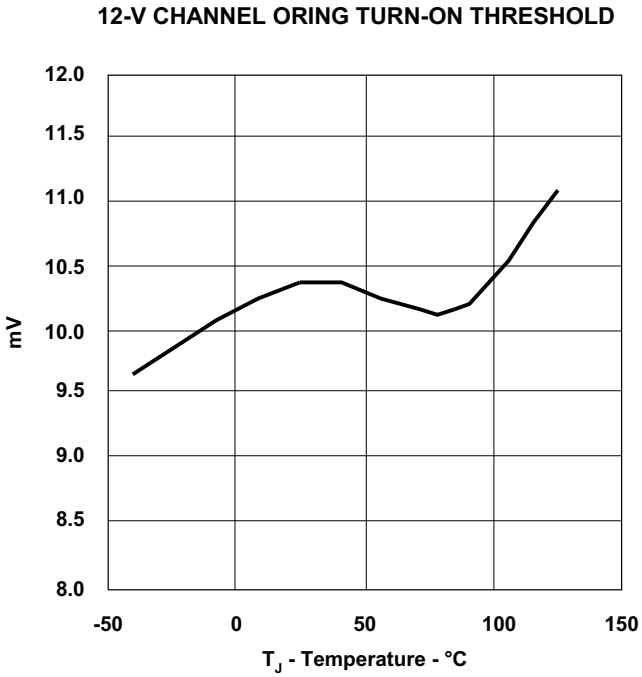


Figure 11.

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TYPICAL CHARACTERISTICS (continued)

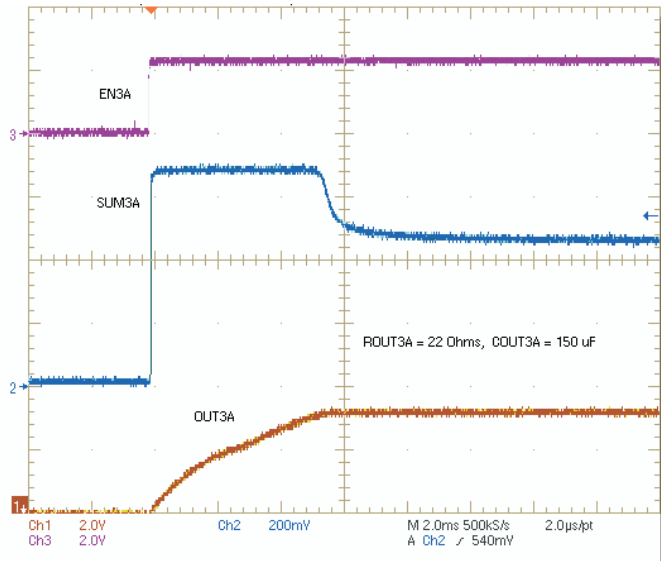


Figure 12. OUT3A Startup Into 22-Ω (150 mA) 150-µF Load

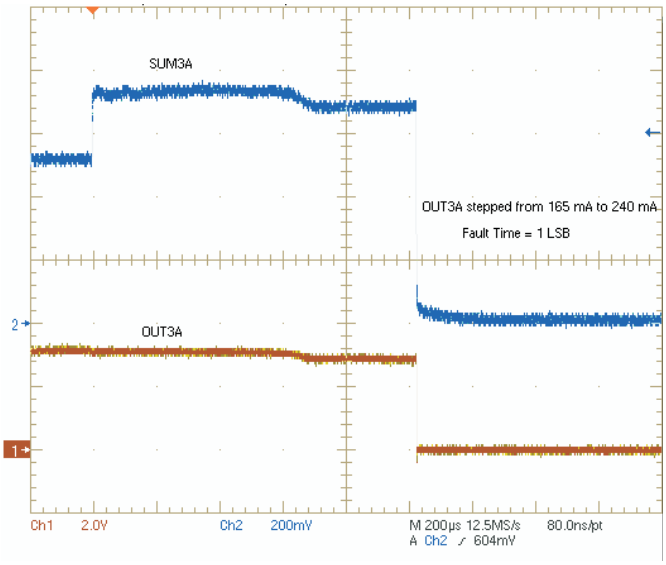


Figure 13. OUT3A Load Stepped from 165 mA to 240 mA

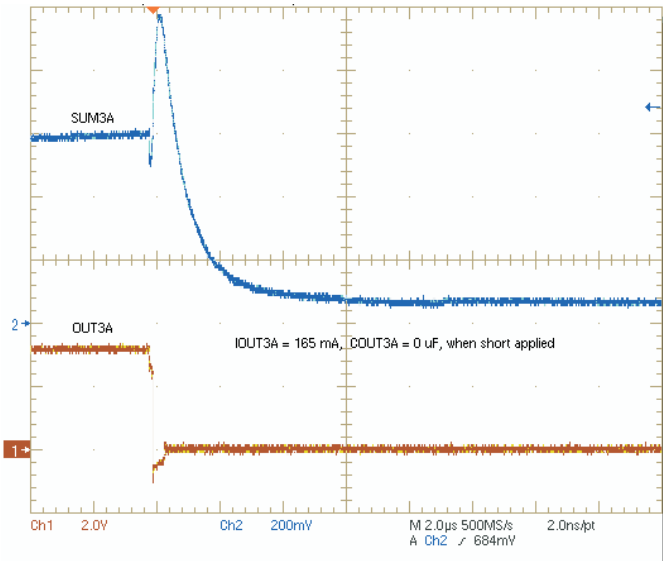


Figure 14. OUT3A Short Circuit Under Full Load (165 mA) Zoom View

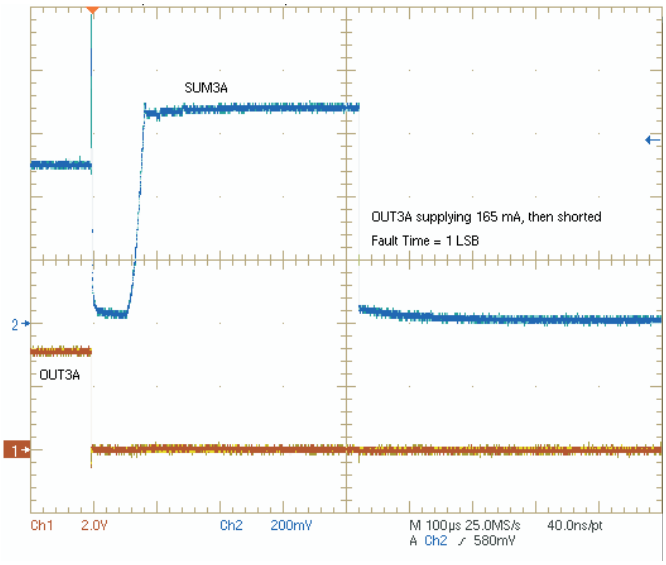


Figure 15. OUT3A Short Circuit Under Full Load (165 mA) Wide View

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TYPICAL CHARACTERISTICS (continued)

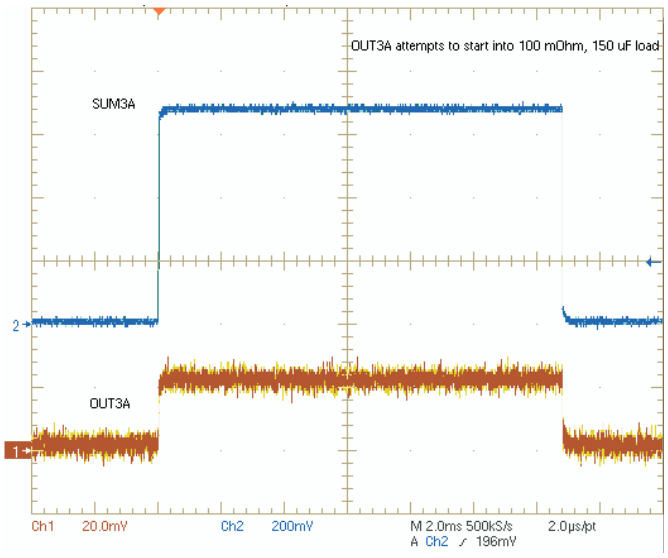


Figure 16. OUT3A Startup Into Short Circuit

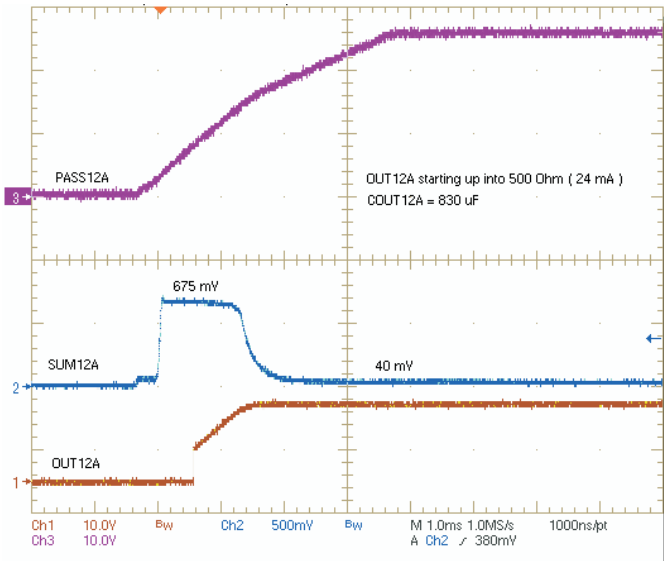


Figure 17. OUT12A Startup Into 500-Ω, 830-µF Load

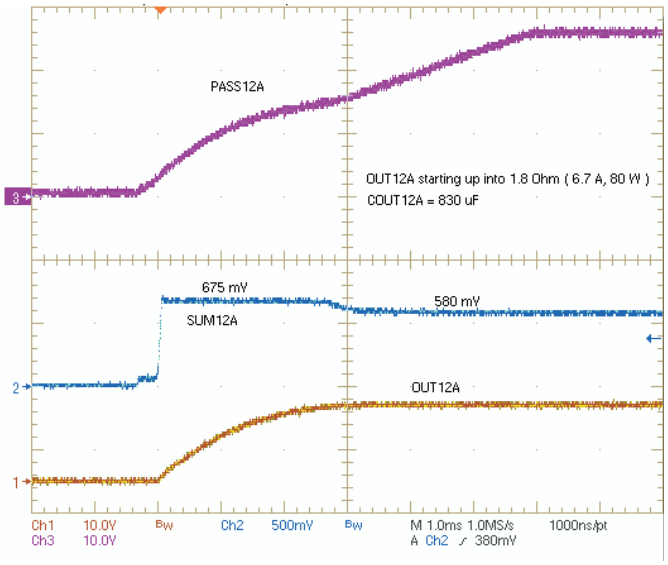


Figure 18. OUT12A Startup Into 80-Watt, 830-µF Load

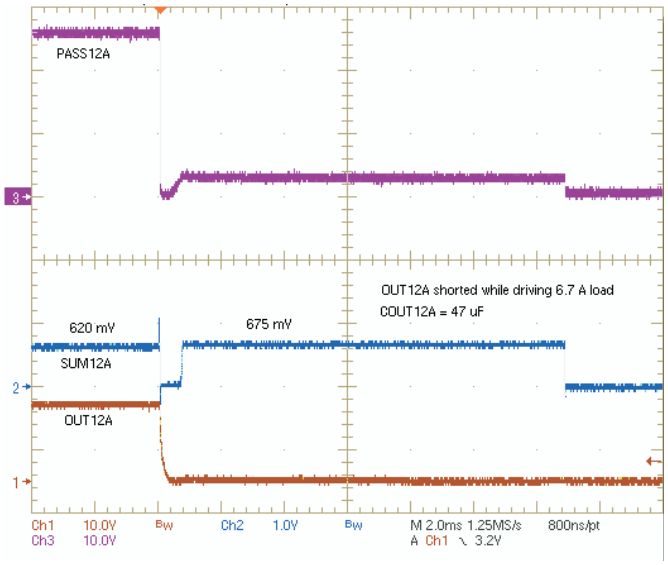


Figure 19. OUT12A Short Circuit Under Full Load (6.7 A) Wide View

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TYPICAL CHARACTERISTICS (continued)

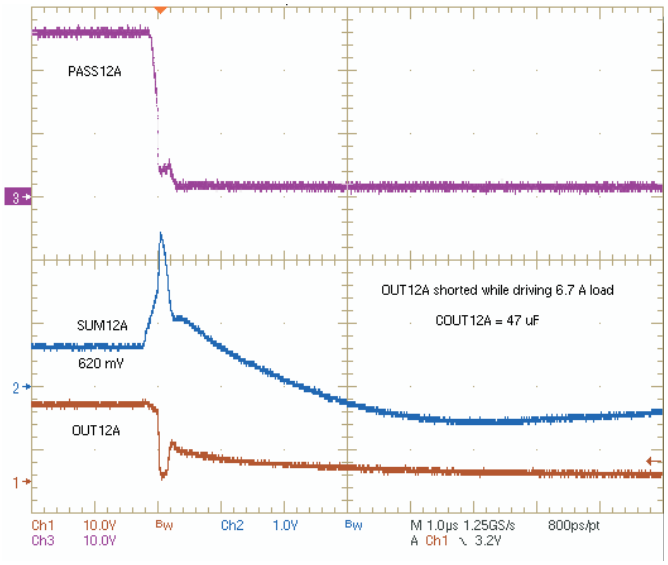


Figure 20. OUT12A Short Circuit Under Full Load (6.7 A) Zoom View

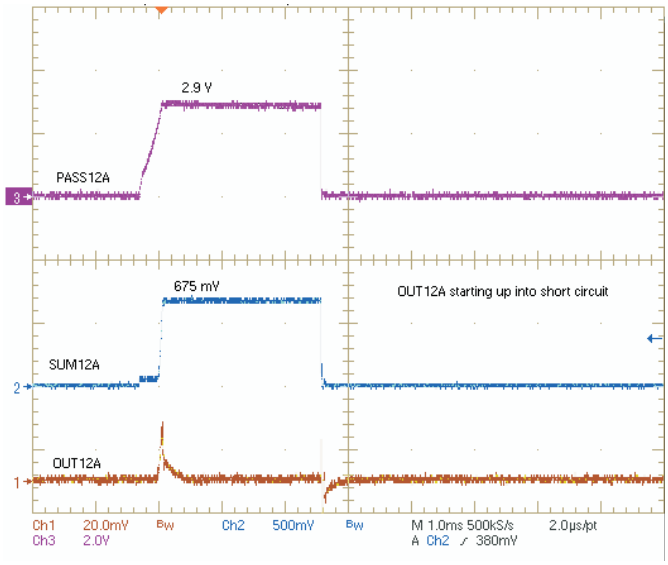


Figure 21. OUT12A Startup Into Short Circuit

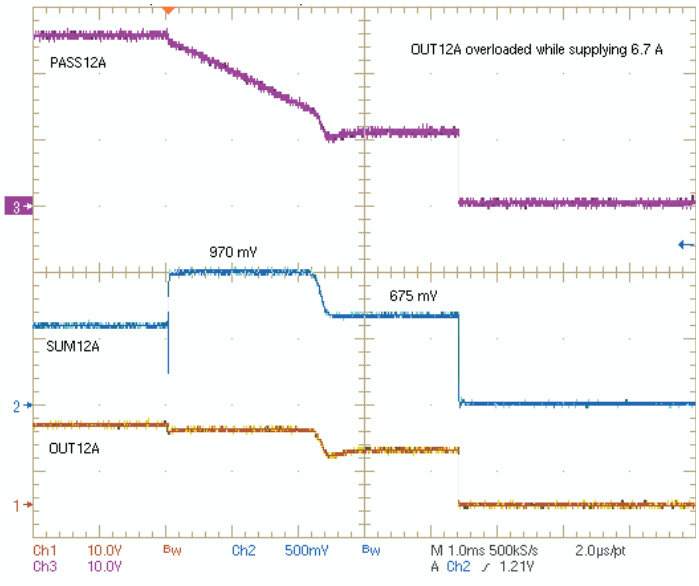


Figure 22. OUT12A Overloaded While Supplying 6.7 A

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REFERENCE INFORMATION

The TPS2359 has been designed to simplify compliance with the PICMG-AMC.R2.0 and PICMG-MTCA.0 specifications. These specifications were developed by the PCI Industrial Computer Manufacturers Group (PICMG). These two specifications are derivations of the PICMG-ATCA (Advanced Telecommunication Computing Architecture) specification originally released in December, 2002.

PICMG-AMC Highlights

- AMC - Advanced Mezzanine Cards
- Designed to Plug into ATCA Carrier Boards
- AdvancedMC™ Focuses on Low Cost
- 1 to 8 AdvancedMC™ per ATCA Carrier Board
- 3.3-V Management Power – Maximum Current Draw of 150 mA
- 12-V Payload Power – Converted to Required Voltages on AMC
- Maximum 80-W Dissipation per AdvancedMC™
- Hotswap and Current Limiting Must Be Present on Carrier Board
- For Details, see www.picmg.org/v2internal/AdvancedMC.htm

PICMG-MTCA Highlights

- MTCA – MicroTelecommunications Computing Architecture
- Architecture for Using AMCs Without an ATCA Carrier Board
- Up to 12 AMCs per System, Plus Two MCHs, Plus Two CUs
- Focuses on Low Cost
- All functions of ATCA Carrier Board Must Be Provided
- MicroTCA is also known as MTCA, mTCA, or uTCA For Details, see www.picmg.org/v2internal/microTCA.htm

Control and Status Registers

Ten 8 bit registers are used to control and read the status of the TPS2359. Registers 0 and 1 control the 12A channel and register 2 controls the 3A channel. Similarly, registers 3 and 4 control the 12B channel and register 5 controls the 3B channel. Register 6 contains eight general configuration bits. Read-only registers 7, 8, and 9 report back system status to the I^2C controller. All ten registers use the I^2C protocol and are organized as follows:

Table 1. Top Level Register Functions

REG	R/W	SLOT	VOLTAGE	FUNCTION
0	R/W	A	12	Set current limit, power good threshold, and OR functions of 12A.
1	R/W	A	12	Set fault time, enable, and bleed down functions of 12A.
2	R/W	A	3.3	Set fault time, enable, and bleed down functions of 3A.
3	R/W	B	12	Set current limit, power good threshold, and OR functions of 12B.
4	R/W	B	12	Set fault time, enable, and bleed down functions of 12B.
5	R/W	B	3.3	Set fault time, enable, and bleed down functions of 3B.
6	R/W	A, B	3.3, 12	System configuration controls.
7	R	A, B	3.3, 12	Fault and PG outputs for 3A, 12A, 3B, 12B – these bits set $\overline{\text{IRPT}}$.
8	R	A, B	12	Over current and fast trip latches for 3A, 12A, 3B, 12B.
9	R	A, B	3.3, 12	Channel status indicators for 3A, 12A, 3B, 12B.

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Summary of Registers

Table 2. Summary of Registers

BIT	NAME	DEFAULT	DESCRIPTION
Register 0 Read/Write channel 12A configuration			
0	12ACL0	1	Clearing bit reduces 12A current limit and fast threshold by 5%.
1	12ACL1	1	Clearing bit reduces 12A current limit and fast threshold by 10%.
2	12ACL2	1	Clearing bit reduces 12A current limit and fast threshold by 20%.
3	12ACL3	1	Clearing bit reduces 12A current limit and fast threshold by 40%.
4	12APG0	1	Clearing bit reduces 12A power good threshold by 600mV.
5	12APG1	1	Clearing bit reduces 12A power good threshold by 1.2 V.
6	12AHP	0	Setting bit shifts 12A OR VTURNOFF from –3 mV to +3 mV nominal.
7	12AOR	1	Clearing bit turns off 12A ORing FET by pulling BLKA low.
Register 1 Read/Write channel 12A configuration			
0	12AFT0	1	Setting bit increases 12A fault time by 0.45 ms.
1	12AFT1	0	Setting bit increases 12A fault time by 0.9 ms.
2	12AFT2	0	Setting bit increases 12A fault time by 1.8 ms.
3	12AFT3	0	Setting bit increases 12A fault time by 3.6 ms.
4	12AFT4	0	Setting bit increases 12A fault time by 7.2 ms.
5	12AEN	0	Clearing bit disables 12A by pulling PASSA and BLKA to 0 V.
6	12AUV	0	Setting bit prevents enabling unless OUT12A < bleed down threshold.
7	12ADS	0	Clearing bit disconnects OUT12A bleed down resistor.
Register 2 Read/Write channel 3A configuration			
0	3AFT0	1	Setting bit increases 3A fault time by 0.45 ms.
1	3AFT1	0	Setting bit increases 3A fault time by 0.9 ms.
2	3AFT2	0	Setting bit increases 3A fault time by 1.8 ms.
3	3AFT3	0	Setting bit increases 3A fault time by 3.6 ms.
4	3AFT4	0	Setting bit increases 3A fault time by 7.2 ms.
5	3AEN	0	Clearing bit disables 3A.
6	3AUV	0	Setting bit prevents enabling unless OUT3A < bleed down threshold.
7	3ADS	0	Clearing bit disconnects OUT3A bleed down resistor.
Register 3 Read/Write channel 12B configuration			
0	12BCL0	1	Clearing bit reduces 12B current limit and fast threshold by 5%.
1	12BCL1	1	Clearing bit reduces 12B current limit and fast threshold by 10%.
2	12BCL2	1	Clearing bit reduces 12B current limit and fast threshold by 20%.
3	12BCL3	1	Clearing bit reduces 12B current limit and fast threshold by 40%.
4	12BPG0	1	Clearing bit reduces 12B power good threshold by 600 mV.
5	12BPG1	1	Clearing bit reduces 12B power good threshold by 1.2 V.
6	12BHP	0	Setting bit shifts 12B OR VTURNOFF from –3 mV to +3 mV nominal.
7	12BOR	1	Clearing bit turns off 12B ORing FET by pulling BLKB low.
Register 4 Read/Write channel 12B configuration			
0	12BFT0	1	Setting bit increases 12B fault time by 0.45 ms.
1	12BFT1	0	Setting bit increases 12B fault time by 0.9 ms.
2	12BFT2	0	Setting bit increases 12B fault time by 1.8 ms.
3	12BFT3	0	Setting bit increases 12B fault time by 3.6 ms.
4	12BFT4	0	Setting bit increases 12B fault time by 7.2 ms.
5	12BEN	0	Clearing bit disables 12B by pulling PASSB and BLKB to 0 V.
6	12BUV	0	Setting bit prevents enabling unless OUT12B < bleed down threshold.
7	12BDS	0	Clearing bit disconnects OUT12B bleed down resistor.
Register 5 Read/Write channel 3B configuration			

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Table 2. Summary of Registers (continued)

BIT	NAME	DEFAULT	DESCRIPTION
0	3BFT0	1	Setting bit increases 3B fault time by 0.45 ms.
1	3BFT1	0	Setting bit increases 3B fault time by 0.9 ms.
2	3BFT2	0	Setting bit increases 3B fault time by 1.8 ms.
3	3BFT3	0	Setting bit increases 3B fault time by 3.6 ms.
4	3BFT4	0	Setting bit increases 3B fault time by 7.2 ms.
5	3BEN	0	Clearing bit disables 3B.
6	3BUV	0	Setting bit prevents enabling unless OUT3B < bleed down threshold.
7	3BDS	0	Clearing bit disconnects OUT3B bleed down resistor.
Register 6 Read/Write system configuration			
0	PPTEST	0	12-V pulldown test pin. Setting pin pulls the PASSx and BLKx pins to 0 V.
1	FLTMODE	0	Clearing bit latchs off channels after over-current fault. Setting bit allows channels to automatically attempt restart after fault.
2	SPARE	0	This bit must always be set to 0.
3	3ORON	0	Setting bit enables 3A and 3B to prevent reverse current flow.
4	12VNRS	0	Non Redundant System in rush control bit. Setting bit allows increased inrush current in 12A and 12B with proper setting of 12xCLx bits.
5	AIRM	0	Setting this masking bit prevents REG7 bits 3:0 from setting IRPT.
6	BIRM	0	Setting this masking bit prevents REG7 bits 7:4 from setting IRPT.
7	DCC	0	Setting bit allows the 12 V channels to operate despite loss of 3.3 V. This bit should be low for uTCA and AMC applications
Register 7 Read only latched $\overline{\text{IRPT}}$ channel status indicators, cleared on read			
0	$\overline{\text{12APG}}$	0	Latches high when OUT12A goes from above V_{TH_PG} to below V_{TH_PG}.
1	12AFLT	0	Latches high when 12A fault timer has run out.
2	$\overline{\text{3APG}}$	0	Latches high when OUT3A goes from above V_{TH_PG} to below V_{TH_PG}.
3	3AFLT	0	Latches high when 3A fault timer has run out.
4	$\overline{\text{12BPG}}$	0	Latches high when OUT12B goes from above V_{TH_PG} to below V_{TH_PG}.
5	12BFLT	0	Latches high when 12B fault timer has run out.
6	$\overline{\text{3BPG}}$	0	Latches high when OUT3B goes from above V_{TH_PG} to below V_{TH_PG}.
7	3BFLT	0	Latches high when 3B fault timer has run out.
Register 8 Read only latched overcurrent indicators, cleared on Read			
0	12AOC	0	Latches high when 12A enters over-current.
1	12AFTR	0	Latches high if 12A fast trip threshold exceeded.
2	3AOC	0	Latches high when 3A enters over-current.
3	3AFTR	0	Latches high if 3A fast trip threshold exceeded.
4	12BOC	0	Latches high when 12B enters over-current.
5	12BFTR	0	Latches high if 12B fast trip threshold exceeded.
6	3BOC	0	Latches high when 3B enters over-current.
7	3BFTR	0	Latches high if 3B fast trip threshold exceeded.
Register 9 Read only unlatched FET status indicators			
0	12ABS	-	High indicates BLKA commanded high.
1	$\overline{\text{12APS}}$	-	Low indicates $V_{PASSA} > V_{OUT12A} + 6$ V.
2	$\overline{\text{3ABS}}$	-	Low indicates IN3A > OUT3A.
3	12BBS	-	High indicates BLKB commanded high.
4	$\overline{\text{12BPS}}$	-	Low indicates $V_{PASSB} > V_{OUTB} + 6$ V.
5	$\overline{\text{3BBS}}$	-	Low indicates IN3B > OUT3B.
6	$\overline{\text{3AGS}}$	-	Low indicates channel 3A gate is driven on ($V_{GATE} > (V_{IN} + 1.75$ V).
7	$\overline{\text{3BGS}}$	-	Low indicates channel 3B gate is driven on ($V_{GATE} > (V_{IN} + 1.75$ V).

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Detailed Description of Registers

Register 0

Table 3. Register 0: Channel 12A Configuration (Read/Write)

BIT	NAME	DEFAULT	DESCRIPTION
0	12ACL0	1	Clearing bit reduces 12A current limit and fast threshold by 5%.
1	12ACL1	1	Clearing bit reduces 12A current limit and fast threshold by 10%.
2	12ACL2	1	Clearing bit reduces 12A current limit and fast threshold by 20%.
3	12ACL3	1	Clearing bit reduces 12A current limit and fast threshold by 40%.
4	12APG0	1	Clearing bit reduces 12A power good threshold by 600 mV.
5	12APG1	1	Clearing bit reduces 12A power good threshold by 1.2 V.
6	12AHP	0	Setting bit shifts 12A OR VTURNOFF from –3 mV to +3 mV nominal.
7	12AOR	1	Clearing bit turns off 12A ORing FET by pulling BLKA low.

12ACL[3:0] These four bits adjusts the 12A current limit and fast trip threshold using the I^2C interface. Setting the bits to 1111B places the 12A current limit at its maximum level, corresponding to 675 mV at SUM12A. The fast trip threshold then equals 100 mV. Clearing all bits reduces the current limit and fast trip threshold to 25% of these maximums.

12APG[1:0] These two bits adjust the 12A power good threshold. Setting the bits to 11B places the power good threshold at its maximum level of 10.5 V . Setting the bits to 00B places the threshold at its minimum level of 8.7 V. The lower thresholds may prove desirable in systems that routinely experience large voltage droops.

12AHP Setting this bit moves the 12A ORing turn off threshold from –3 mV to +3 mV. A positive threshold prevents reverse current from flowing through the channel, but it may cause the ORing FET to repeatedly cycle on-and-off if the load cannot maintain the required positive voltage drop across the combined resistance of the external FETs and the sense resistor. For further information, see Adjusting Oring Turn Off threshold For High Power Loads section

12AOR Clearing this bit forces the BLKA pin low, keeping the 12A ORing FET off. Clearing this bit does not prevent current from flowing through the FET's body diode.

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Register 1

Table 4. Register 1: Channel 12A Configuration (Read/Write)

BIT	NAME	DEFAULT	DESCRIPTION
0	12AFT0	1	Setting bit increases 12A fault time by 0.45 ms.
1	12AFT1	0	Setting bit increases 12A fault time by 0.9 ms.
2	12AFT2	0	Setting bit increases 12A fault time by 1.8 ms.
3	12AFT3	0	Setting bit increases 12A fault time by 3.6 ms.
4	12AFT4	0	Setting bit increases 12A fault time by 7.2 ms.
5	12AEN	0	Clearing bit disables 12A by pulling PASSA and BLKA to 0 V.
6	12AUV	0	Setting bit prevents enabling unless OUT12A < bleed down threshold.
7	12ADS	0	Clearing bit disconnects OUT12A bleed down resistor.

12AFT[4:0] These five bits adjust the 12A channel fault time. The least-significant bit has a nominal weight of 0.45 ms, so fault times ranging from 0.45 ms (for code 00001B) to 13.95 ms (for code 11111B) can be programmed. The code xFT = 00000B should not be used. In general the shortest fault time that fully charges downstream bulk capacitors without generating a fault should be used. Once the load capacitors have fully charged, the fault time can be reduced to provide faster short circuit protection. See Setting Fault Time section.

12AEN This bit serves as a master enable for channel 12A. Setting this bit allows the 12A channel to operate normally. Clearing this bit disables the channel by pulling PASSA and BLKA low.

12AUV Setting this bit prevents channel 12A from turning on until OUT12A falls below the bleed down threshold of 100 mV. This feature ensures that downstream devices reset by requiring their supply voltage to fall to nearly zero before the channel can enable them.

12ADS Clearing this bit disconnects the bleed down resistor that otherwise connects from OUT12A to ground. Systems using redundant power supplies should clear 12ADS to prevent the bleed down resistor from continuously sinking current.

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Register 2

Table 5. Register 2: Channel 3A Configuration (Read/Write)

BIT	NAME	DEFAULT	DESCRIPTION
0	3AFT0	1	Setting bit increases 3A fault time by 0.45 ms.
1	3AFT1	0	Setting bit increases 3A fault time by 0.9 ms.
2	3AFT2	0	Setting bit increases 3A fault time by 1.8 ms.
3	3AFT3	0	Setting bit increases 3A fault time by 3.6 ms.
4	3AFT4	0	Setting bit increases 3A fault time by 7.2 ms.
5	3AEN	0	Clearing bit disables 3A.
6	3AUV	0	Setting bit prevents enabling unless OUT3A < bleed down threshold.
7	3ADS	0	Clearing bit disconnects OUT3A bleed down resistor.

3AFT[4:0] These five bits adjust the 3A channel fault time. The least-significant bit has a nominal weight of 0.45 ms, so fault times ranging from 0.45 ms (for code 00001B) to 13.95 ms (for code 11111B) can be programmed. The code xFT = 00000B should not be used. In general the shortest fault time that fully charges downstream bulk capacitors without generating a fault should be used. See Setting Fault Time section.

3AEN This bit serves as a master enable for channel 3A. Setting this bit allows the 3A channel to operate normally, provided the EN3A pin is also asserted. Clearing this bit disables the channel by removing gate drive to the internal pass FET, regardless of the state of the EN3A pin.

3AUV Setting this bit prevents channel 3A from turning on until OUT3A falls below the bleed down threshold of 100 mV. This feature ensures that downstream devices reset by requiring their supply voltage to fall to nearly zero before the channel can enable them.

3ADS Clearing this bit disconnects the bleed down resistor that otherwise connects from OUT3A to ground. Systems using redundant power supplies should clear 3ADS to prevent the bleed down resistor from continuously sinking current.

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Register 3

Table 6. Register 3: Channel 12B Configuration (Read/Write)

BIT	NAME	DEFAULT	DESCRIPTION
0	12BCL0	1	Clearing bit reduces 12B current limit and fast threshold by 5%.
1	12BCL1	1	Clearing bit reduces 12B current limit and fast threshold by 10%.
2	12BCL2	1	Clearing bit reduces 12B current limit and fast threshold by 20%.
3	12BCL3	1	Clearing bit reduces 12B current limit and fast threshold by 40%.
4	12BPG0	1	Clearing bit reduces 12B power good threshold by 600 mV.
5	12BPG1	1	Clearing bit reduces 12B power good threshold by 1.2 V.
6	12BHP	0	Setting bit shifts 12B OR VTURNOFF from –3 mV to +3 mV nominal.
7	12BOR	1	Clearing bit turns off 12B ORing FET by pulling BLKB low.

12BCL[3:0] These four bits adjusts the 12B current limit and fast trip threshold using the I^2C interface. Setting the bits to 1111B places the 12B current limit at its maximum level, corresponding to 675 mV at SUM12B. The fast trip threshold then equals 100 mV. Clearing all bits reduces the current limit and fast trip threshold to 25% of these maximums.

12BPG[1:0] These two bits adjust the 12B power good threshold. Setting the bits to 11B places the power good threshold at its maximum level of 10.5 V . Setting the bits to 00B places the threshold at its minimum level of 8.7 V. The lower thresholds may prove desirable in systems that routinely experience large voltage droops.

12BHP Setting this bit moves the 12B ORing turn off threshold from –3 mV to +3 mV. A positive threshold prevents reverse current from flowing through the channel, but it may cause the ORing FET to repeatedly cycle on-and-off if the load cannot maintain the required positive voltage drop across the combined resistance of the external FETs and the sense resistor. For further information, see Adjusting ORing Turn Off threshold For High Power Loads section.

12BOR Clearing this bit forces the BLKB pin low, keeping the 12B ORing FET off. Clearing this bit does not prevent current from flowing through the FET's body diode.

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Register 4

Table 7. Register 4: Channel 12B Configuration (Read/Write)

BIT	NAME	DEFAULT	DESCRIPTION
0	12BFT0	1	Setting bit increases 12B fault time by 0.45 ms.
1	12BFT1	0	Setting bit increases 12B fault time by 0.9 ms.
2	12BFT2	0	Setting bit increases 12B fault time by 1.8 ms.
3	12BFT3	0	Setting bit increases 12B fault time by 3.6 ms.
4	12BFT4	0	Setting bit increases 12B fault time by 7.2 ms.
5	12BEN	0	Clearing bit disables 12B by pulling PASSB and BLKB to 0 V.
6	12BUV	0	Setting bit prevents enabling unless OUT12B < bleed down threshold.
7	12BDS	0	Clearing bit disconnects OUT12B bleed down resistor.

12BFT[4:0] These five bits adjust the 12B channel fault time. The least-significant bit has a nominal weight of 0.45 ms, so fault times ranging from 0.45 ms (for code 00001B) to 13.95 ms (for code 11111B) can be programmed. The code xFT = 00000B should not be used. In general the shortest fault time that fully charges downstream bulk capacitors without generating a fault should be used. Once the load capacitors have fully charged, the fault time can be reduced to provide faster short circuit protection. See Setting Fault Time section.

12BEN This bit serves as a master enable for channel 12B. Setting this bit allows the 12B channel to operate normally. Clearing this bit disables the channel by pulling PASSB and BLKB low.

12BUV Setting this bit prevents channel 12B from turning on until OUT12B falls below the bleed down threshold of 100 mV. This feature ensures that downstream devices reset by requiring their supply voltage to fall to nearly zero before the channel can enable them.

12BDS Clearing this bit disconnects the bleed down resistor that otherwise connects from OUT12B to ground. Systems using redundant power supplies should clear 12BDS to prevent the bleed down resistor from continuously sinking current.

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Register 5

Table 8. Register 5: Channel 3B Configuration (Read/Write)

BIT	NAME	DEFAULT	DESCRIPTION
0	3BFT0	1	Setting bit increases 3B fault time by 0.45 ms.
1	3BFT1	0	Setting bit increases 3B fault time by 0.9 ms.
2	3BFT2	0	Setting bit increases 3B fault time by 1.8 ms.
3	3BFT3	0	Setting bit increases 3B fault time by 3.6 ms.
4	3BFT4	0	Setting bit increases 3B fault time by 7.2 ms.
5	3BEN	0	Clearing bit disables 3B.
6	3BUV	0	Setting bit prevents enabling unless OUT3B < bleed down threshold.
7	3BDS	0	Clearing bit disconnects OUT3B bleed down resistor.

3BFT[4:0] These five bits adjust the 3B channel fault time. The least-significant bit has a nominal weight of 0.45 ms, so fault times ranging from 0.45 ms (for code 00001B) to 13.95 ms (for code 11111B) can be programmed. The code xFT = 00000B should not be used. In general the shortest fault time that fully charges downstream bulk capacitors without generating a fault should be used. See Setting Fault Time section.

3BEN This bit serves as a master enable for channel 3B. Setting this bit allows the 3B channel to operate normally, provided the EN3B pin is also asserted. Clearing this bit disables the channel by removing gate drive to the internal pass FET, regardless of the state of the EN3B pin.

3BUV Setting this bit prevents channel 3B from turning on until OUT3B falls below the bleed down threshold of 100 mV. This feature ensures that downstream devices reset by requiring their supply voltage to fall to nearly zero before the channel can enable them.

3BDS Clearing this bit disconnects the bleed down resistor that otherwise connects from OUT3B to ground. Systems using redundant power supplies should clear 3BDS to prevent the bleed down resistor from continuously sinking current.

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Register 6

Table 9. Register 6: System Configuration (Read/Write)

BIT	NAME	DEFAULT	DESCRIPTION
0	PPTEST	0	12-V pulldown test pin. Asserting this pulls the PASSx and BLKx pins to 0 V.
1	FLTMODE	0	Clearing bit forces channels to latch off after over-current fault. Setting bit allows channels to automatically attempt restart after fault.
2	SPARE	0	This bit must always be set to 0.
3	3ORON	0	Setting bit enables 3A and 3B to prevent reverse current flow.Clearing bit disables 3A and 3B ORing.
4	12VNRS	0	Non Redundant System in rush control bit. Setting bit allows increased inrush current in 12A and 12B.
5	AIRM	0	Setting this masking bit prevents REG7 bits 3:0 from setting IRPT.
6	BIRM	0	Setting this masking bit prevents REG7 bits 7:4 from setting IRPT.
7	DCC	0	Setting bit allows the 12 V channels to operate despite loss of 3.3 V. For uTCA and AMC applications this bit should be low.

PPTEST This bit is used for testing the fast turnoff feature of the PASSx and BLKx pins. Setting this bit enables the fast turnoff drivers for all four pins. Clearing this bit restores normal operation. PPTEST allows the fast turnoff drivers to operate at full current indefinitely, whereas they would normally operate for only about 15 S. While using PPTEST the energy dissipated in the fast turnoff drivers must be externally limited to 1 mJ per driver to prevent damage to the TPS2359.

FLTMODE Setting this bit allows a channel to attempt an automatic restart after an overcurrent condition has caused it to time out and shut off. The retry interval equals approximately 100 times the programmed fault time. The FLTMODE bit affects all four channels. If cross-connection is enabled (DCC = 0), a fault on channel 3A turns off channel 12A, and a fault on channel 3B turns off channel 12B. If a 3.3-V channel automatically restarts because FLTMODE = 1, the associated 12-V channel remains disabled until its enable bit (12AEN or 12BEN) is cycled on and off.

SPARE This bit must always be set to 0.

3ORON Setting this bit allows the 3.3-V ORing function to operate normally. Clearing this bit prevents the 3.3-V channels from disabling if their output voltage exceeds their input voltage . This bit is typically cleared for non-redundant systems.

12VNRS Setting this bit increases the current limit for either 12-V channel to its maximum value during the initial inrush period that immediately follows the enabling of the channel. During inrush, the current limit behaves as if 12xCL[3:0] = 1111B. After the current drops below this limit, signifying the end of the inrush period, the current limit returns to normal operation.

AIRM Setting this bit prevents the $\overline{\text{12APG}}$, 12AFLT, $\overline{\text{3APG}}$, and 3AFLT bits from setting the $\overline{\text{IRPT}}$ pin.

BIRM Setting this bit prevents the $\overline{\text{12APG}}$, 12BFLT, $\overline{\text{3BPG}}$, and 3BFLT bits from setting the $\overline{\text{IRPT}}$ pin.

DCC Setting this bit disables cross-connection. If DCC = 0, when a 3.3-V channel experiences a fault, both it and its associated 12-V channel turn off. Specifically, a fault on channel 3A turns off channel 12A, and a fault on channel 3B turns off channel 12B. If DCC = 1, then the 12-V channels continue to operate even if their associated 3.3-V channels experience faults.

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Register 7

Table 10. Register 7: Latched $\overline{\text{IRPT}}$ Channel Status Indicators (Read-only, cleared on read)

BIT	NAME	DEFAULT	DESCRIPTION
0	$\overline{\text{12APG}}$	1	Latches high when OUT12A goes from above V_{TH_PG} to below V_{TH_PG}.
1	12AFLT	0	Latches high when 12A fault timer has run out.
2	$\overline{\text{3APG}}$	1	Latches high when OUT3A goes from above V_{TH_PG} to below V_{TH_PG}.
3	3AFLT	0	Latches high when 3A fault timer has run out.
4	$\overline{\text{12BPG}}$	1	Latches high when OUT12B goes from above V_{TH_PG} to below V_{TH_PG}.
5	12BFLT	0	Latches high when 12B fault timer has run out.
6	$\overline{\text{3BPG}}$	1	Latches high when OUT3B goes from above V_{TH_PG} to below V_{TH_PG}.
7	3BFLT	0	Latches high when 3B fault timer has run out.

$\overline{\text{12APG}}$ This bit is set at startup and each time OUT12A drops below the PG threshold set by the 12APG[1:0] bits. It is cleared on read if OUT12A is above the PG threshold. If AIRM = 0, setting this bit asserts the $\overline{\text{IRPT}}$ pin.

12AFLT This bit is set if the fault timer on channel 12A has run out, and it remains set until Register 7 is read. If AIRM = 0, setting this bit asserts the $\overline{\text{IRPT}}$ pin.

$\overline{\text{3APG}}$ This bit is set at startup and each time OUT3A drops below the PG threshold. It is cleared on read if OUT3A is above the PG threshold. If AIRM = 0, setting this bit asserts the $\overline{\text{IRPT}}$ pin.

3AFLT This bit is set if the fault timer on channel 3A has run out, and it remains set until Register 7 is read. If AIRM = 0, setting this bit asserts the $\overline{\text{IRPT}}$ pin.

$\overline{\text{12BPG}}$ This bit is set at startup and each time OUT12B drops below the PG threshold set by the 12BAPG[1:0] bits. It is cleared on read if OUT12B is above the PG threshold. If BIRM = 0, setting this bit asserts the $\overline{\text{IRPT}}$ pin.

12BFLT This bit is set if the fault timer on channel 12B has run out, and it remains set until Register 7 is read. If BIRM = 0, setting this bit asserts the $\overline{\text{IRPT}}$ pin.

$\overline{\text{3BPG}}$ This bit is set at startup and each time OUT3B drops below the PG threshold.It is cleared on read if OUT3B is above the PG threshold. If BIRM = 0, setting this bit asserts the $\overline{\text{IRPT}}$ pin.

3BFLT This bit is set if the fault timer on channel 3B has run out, and it remains set until Register 7 is read. If BIRM = 0, setting this bit asserts the $\overline{\text{IRPT}}$ pin.

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Register 8

Table 11. Register 8: Latched Status Indicators (Read-only, cleared on read)

BIT	NAME	DEFAULT	DESCRIPTION
0	12AOC	0	Latches high when 12A enters over-current.
1	12AFTR	0	Latches high if 12A fast trip threshold exceeded.
2	3AOC	0	Latches high when 3A enters over-current.
3	3AFTR	0	Latches high if 3A fast trip threshold exceeded.
4	12BOC	0	Latches high when 12B enters over-current.
5	12BFTR	0	Latches high if 12B fast trip threshold exceeded.
6	3BOC	0	Latches high when 3B enters over-current.
7	3BFTR	0	Latches high if 3B fast trip threshold exceeded.

12AOC This bit is set if the voltage on the PASSA pin drops below the timer start threshold, signifying a current limit condition. This bit remains set until Register 8 is read.

12AFTR This bit is set if the voltage across the sense resistor for channel 12A exceeds the fast trip threshold. This bit remains set until Register 8 is read.

3AOC This bit is set if the gate-to-source voltage on the channel 3A pass FET drops low enough to start the fault timer. This bit remains set until Register 8 is read.

3AFTR This bit is set if the current through channel 3A exceeds the fast trip threshold. This bit remains set until Register 8 is read.

12BOC This bit is set if the voltage on the PASSB pin drops below the timer start threshold, signifying a current limit condition. This bit remains set until Register 8 is read.

12BFTR This bit is set if the voltage across the sense resistor for channel 12B exceeds the fast trip threshold. This bit remains set until Register 8 is read.

3BOC This bit is set if the gate-to-source voltage on the channel 3B pass FET drops low enough to start the fault timer. This bit remains set until Register 8 is read.

3BFTR This bit is set if the current through channel 3B exceeds the fast trip threshold. This bit remains set until Register 8 is read.

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Register 9

Table 12. Register 9: Unlatched Status Indicators (Read-only)

BIT	NAME	DEFAULT	DESCRIPTION
0	12ABS	-	High indicates BLKA commanded high.
1	$\overline{12APS}$	-	Low indicates V_{PASSA} > VOUT12A + 6 V.
2	$\overline{3ABS}$	-	Low indicates IN3A > OUT3A.
3	12BBS	-	High indicates BLKB commanded high.
4	$\overline{12BPS}$	-	Low indicates V_{PASSB} > VOUTB + 6 V.
5	$\overline{3BBS}$	-	Low indicates IN3B > OUT3B.
6	$\overline{3AGS}$	-	Low indicates channel 3A gate is driven on (VGATE > VIN + 1.75 V).
7	$\overline{3BGS}$	-	Low indicates channel 3B gate is driven on (VGATE > VIN + 1.75 V).

12ABS This bit goes high when the 12A ORing logic commands the BLKA pin high (25 V) and the BLKA FET should be on.

$\overline{12APS}$ This bit goes low when the 12A PASS pin is above the timer start threshold (OUT12A + 7 V), indicating that the 12A PASS FET should be on.

$\overline{3ABS}$ This bit goes low when the 3A ORing logic commands the pass 3A FET on, indicating that a reverse blocking condition does not exist.

12BBS This bit goes high when the 12B ORing logic commands the BLKB pin high (25 V) and the BLKB FET should be on.

$\overline{12BPS}$ This bit goes low when the 12B PASS pin is above the timer start threshold (OUT12B + 7 V), indicating that the 12B PASS FET should be on.

$\overline{3BBS}$ This bit goes low when the 3B ORing logic commands the 3B pass FET on, indicating that a reverse blocking condition does not exist.

$\overline{3AGS}$ This bit goes low when the 3A FET gate-to-source voltage exceeds 1.75 V, indicating that the 3A FET should be on.

$\overline{3BGS}$ This bit goes low when the 3B FET gate-to-source voltage exceeds 1.75 V, indicating that the 3B FET should be on.

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APPLICATION INFORMATION

Introduction

The TPS2359 controls two 12-V power paths and two 3.3-V power paths. Each power path can draw from a single common supply, or from two independent supplies. The TPS2359 occupies a 36-pin QFN package. An I^2C interface not only enables the implementation of two AdvancedMC™ slots using one small integrated circuit, but it also provides many opportunities for design customization. The following sections describe the main functions of the TPS2359 and provide guidance for designing systems around this device.

Control Logic and Power-On Reset

The TPS2359's circuitry, including the I^2C interface, draws power from an internal bus fed by a preregulator. A capacitor attached to the VINT pin provides decoupling and output filtering for this preregulator. It can draw power from any of four inputs (IN12A, IN12B, IN3A, or IN3B) or from any of four outputs (OUT12A, OUT12B, OUT3A, or OUT3B). This feature allows the internal circuitry to function regardless of which channels receive power, or from what source. The four external FET drive pins (PASSA, PASSB, BLKA, and BLKB) are held low during startup to ensure that the two 12-V channels remain off. The internal 3.3-V channels are also held off. When the voltage on the internal VINT rail exceeds approximately 1 V, the power-on reset circuit loads the internal registers with the default values listed in Detailed Description of Registers section.

Enable Functions

Table 13 lists the specific conditions required to enable each of the four channels of the TPS2359. The 3.3-V channels each have an active-high enable pin with a 200-kΩ internal pullup resistor. The enable pin must be pulled high, or allowed to float high, in order to enable the channel. The I^2C interface includes an enable bit for each of the four channels. The bit corresponding to a channel must be set in order to enable it. All four channels also include bleed down threshold comparators. Setting the bleed down control bit ensures that a channel cannot turn on until its output voltage drops below about 100 mV. This feature supports applications in which removal and restoration of power re-initializes the state of downstream loads. The 12-V channels also include a cross-connection feature to support PICMG.AMC™ and MicroTCA™ requirements. When enabled, this feature ensures that when a 3.3-V output drops below 2.85 V the associated 12-V channel will automatically shut off. This feature can be disabled by setting the DCC bit in Register 6.

Table 13. Enable Requirements

Channel	Enable pins	Enable bits	Bleed down	Cross connection
3A	EN3A > 1.4 V	3AEN = 1	OUT3A < 0.1 V or 3AUV = 0	
3B	EN3B > 1.4 V	3BEN = 1	OUT3B < 0.1 V or 3BUV = 0	
12A		12AEN = 1	OUT12A < 0.1 V or 12AUV = 0	$\overline{3APG}$ = 0 or DCC = 1
12B		12BEN = 1	OUT12B < 0.1 V or 12BUV = 0	$\overline{3BPG}$ = 0 or DCC = 1

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Fault, Power Good, Overcurrent, and FET Status Bits

The TPS2359 I^2C interface includes six status bits for each channel, for a total of 24 bits. These status bits occupy registers 7, 8, and 9. The following table summarizes the locations of these bits:

Table 14. TPS2359 Status Bit Locations(1)

FUNCTION	12A	3A	12B	3B
	REGISTER [bit]			
Power Good ($\overline{PG}$)	R7[0]	R7[2]	R7[4]	R7[6]
Overcurrent Time out Fault ($\overline{FLT}$)	R7[1]	R7[3]	R7[5]	R7[7]
Momentary Overcurrent (OC)	R8[0]	R8[2]	R8[4]	R8[6]
Overcurrent Fast Trip (FTR)	R8[1]	R8[3]	R8[5]	R8[7]
12-V Block FET Status (12xBS)	R9[0]		R9[3]	
12-V Pass FET Status ($\overline{12xPS}$)	R9[1]		R9[4]	
3-V Block Status ($\overline{3xBS}$)		R9[2]		R9[5]
3-V Gate Status ($\overline{3xGS}$)		R9[6]		R9[7]

(1) For a description of each bit, refer to Detailed Description of Registers section.

Current Limit and Fast Trip Thresholds

All four channels monitor current by sensing the voltage across a resistor. The 3.3-V channels use internal sense resistors with a nominal value of 290 mΩ. The 12-V channels use external sense resistors that typically lie in the range of 4 - 10 mΩ. Each channel features two distinct thresholds: a current limit threshold and a fast trip threshold.

The current limit threshold sets the regulation point of a feedback loop. If the current flowing through the channel exceeds the current limit threshold, then this feedback loop reduces the gate-to-source voltage imposed on the pass FET. This causes the current flowing through the channel to settle to the value determined by the current limit threshold. For example, when a module first powers up, it draws an inrush current to charge its load capacitance. The current limit feedback loop ensures that this inrush current does not exceed the current limit threshold.

The current limit feedback loop has a finite response time. Serious faults such as shorted loads require a faster response in order to prevent damage to the pass FETs or voltage sags on the supply rails. A comparator monitors the current flowing through the sense resistor, and if it ever exceeds the fast trip threshold, then it immediately shuts off the channel. The channel turns back on slowly, allowing the current limit feedback loop time to respond. One normally sets the fast trip threshold some 2 – 5 times higher than the current limit.

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3.3V Current Limiting

The 3.3-V management power channels include internal pass FETs and current sense resistors. The on-resistance of a management channel - including pass FET, sense resistor, metallization resistance, and bond wires - typically equals 290 mΩ and never exceeds 500 mΩ. The AdvancedMC™ specification allows a total of 1 Ω between the power source and the load. The TPS2359 never consumes more than half of this budget.

The 3.3-V fast trip function protects the channel against short-circuit events. If the current through the channel exceeds a nominal value of 300 mA, then the TPS2359 immediately disables the internal pass transistor and then allows it to slowly turn back on into current limiting.

The 3.3-V current limit function internally limits the current to comply with the AdvancedMC™ and MicroTCA™ specifications. External resistor RSUM3x allows the user to adjust the current limit threshold. The nominal current limit threshold ILIMIT equals

$$I_{LIMIT} = \frac{650V}{R_{SUM3x}} \quad (1)$$

A 3320-Ω resistor gives a nominal current limit of I_{LIMIT} = 195 mA which complies with AdvancedMC™ and MicroTCA™ specifications. This resistance corresponds to an EIA 1% value. Alternatively, a 3.3-kΩ resistor will also suffice. Whenever a 3.3-V channel enters current limit, its fault timer begins to operate (see Fault Timer Programming section).

The 3.3-V over-temperature shutdown trips if a 3.3-V channel remains in current limit so long that the die temperature exceeds approximately 140°C. When this occurs, any 3.3-V channel operating in current limit turns off until the chip cools by approximately 10°C. This feature prevents a prolonged fault on one 3.3-V channel from disabling the other 3.3-V channel, or disabling either of the 12-V channels.

3.3-V ORing

The 3.3-V channels limit reverse current flow by sensing the input-to-output voltage differential and turning off the internal pass FET when this differential drops below -3 mV, which corresponds to a nominal reverse current flow of 10 mA. The pass FET turns back on when the differential exceeds +10 mV. These thresholds provide a nominal 13 mV of hysteresis to help prevent false triggering. This feature allows the implementation of redundant power supplies (also known as supply ORing).

If the 3.3-V channels do not use redundant supplies, then one can clear the 3ORON bit to disable the ORing circuitry. This precaution eliminates the chance that transients might trigger the ORing circuitry and upset system operation.

12-V Fast Trip and Current Limiting

Figure 23 shows a simplified block diagram of the circuitry associated with the fast trip and current limit circuitry within a 12-V channel. Each 12-V channel requires an external N-channel pass FET and three external resistors. These resistors allow the user to independently set the fast trip threshold and the current limit threshold, as described below.

The 12-V fast trip function protects the channel against short-circuit events. If the voltage across external resistor R_{SENSE} exceeds the 100-mV fast trip threshold, then the TPS2359 immediately disables the pass transistor. The 12xCL bits set the magnitude of the fast trip threshold. When 12xCL = 1111B, the fast trip threshold nominally equals 100 mV. The fast trip current I_{FT} corresponding to this threshold equals

$$I_{FT} = \frac{100mV}{R_{SENSE}} \quad (2)$$

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The recommended value of R_{SENSE} = 5 mΩ sets the fast trip threshold at 20 A for 12xCL = 1111B. This choice of sense resistor corresponds to the maximum 19.4-A inrush current allowed by the MicroTCA™ specification.

The 12-V current limit function regulates the PASSx pin voltage to prevent the current through the channel from exceeding I_{LIMIT}. The current limit circuitry includes two amplifiers, A1 and A2, as shown in Figure 23. Amplifier A1 forces the voltage across external resistor R_{SET} to equal the voltage across external resistor R_{SENSE}. The current that flows through R_{SET} also flows through external resistor R_{SUM}, generating a voltage on the 12SUMx pin equal to:

$$V_{12SUMx} = \left(\frac{R_{SENSE} R_{SUM}}{R_{SET}} \right) I_{SENSE} \tag{3}$$

Amplifier A2 senses the voltage on the 12SUMx pin. As long as this voltage is less than the reference voltage on its positive input (nominally 0.675 V for 12xCL = 1111B), the TPS2359 sources current to PASSx. When the voltage on the 12SUMx pin exceeds the reference voltage, amplifier A2 begins to sink current from PASSx. The gate-to-source voltage of the pass FET drops until the the voltages on the two inputs of amplifier A2 balance. The current flowing through the channel then nominally equals:

$$I_{LIMIT} = \left(\frac{R_{SET}}{R_{SUM} R_{SENSE}} \right) \times 0.675V \tag{4}$$

$$R_{SET} = \frac{I_{LIM} R_{SUM} R_{SENSE}}{0.675} \tag{5}$$

The recommended value of R_{SUM} is 6810 Ω. This resistor should never equal less than 675 Ω to prevent excessive currents from flowing through the internal circuitry. Using the recommended values of R_{SENSE} = 5 mΩ and R_{SUM} = 6810 Ω gives:

$$I_{LIMIT} = \frac{(0.0198A)}{\Omega} \times R_{SET} \tag{6}$$

A system capable of powering an 80-Watt AdvancedMC™ module should provide 8.25 A, +/- 10%, according to MicroTCA™ specifications. The above equation suggests R_{SET} = 417 Ω. The nearest 1% EIA value equals 422 Ω. The selection of R_{SET} for MicroTCA™ power modules is described in the Redundant vs. Non-redundant Inrush Current Limiting section.

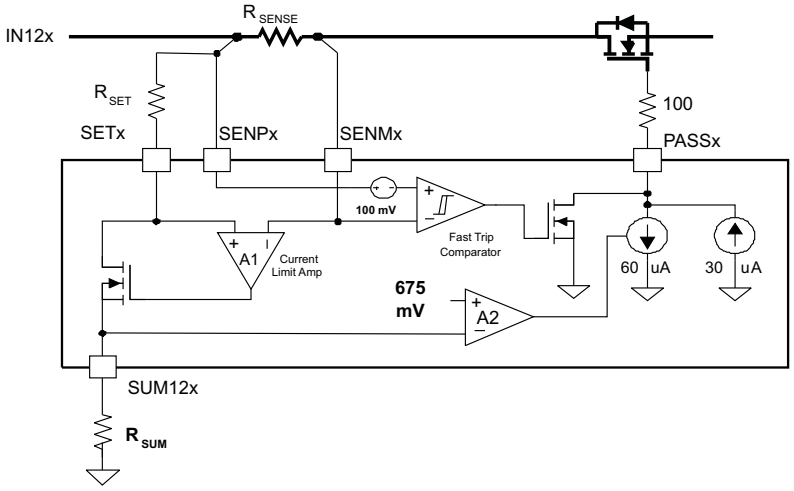


Figure 23. 12-V Channel Threshold Circuitry

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Redundant vs Non-Redundant Inrush Current Limiting

The TPS2359 can support either redundant or non-redundant systems. Redundant systems generally use a single fixed current limit, as described above. Non-redundant systems can benefit from a higher current limit during inrush to compensate for the lack of a redundant supply. The MicroTCA™ standard allows up to 19.4 A for up to 200 ms in non-redundant systems, while limiting individual supplies in redundant systems to 9.1 A at all times. One can optimize the performance of the system for either application by properly setting the 12VNRS bit that controls inrush limiting. The ability to change the inrush profile using 12VNRS makes it possible to reconfigure a controller for redundant or non-redundant operation with a single bit. This is particularly useful for MicroTCA Power Modules which may be deployed in redundant or non-redundamnt systems.

The 12VNRS bit affects the value of the 12xCL bits during inrush. Setting 12VNRS causes the current limit threshold and fast trip threshold to behave as if 12xCL = 1111B during inrush. Once the current flowing through the channel falls below the current limit threshold, the current limit threshold and fast trip threshold correspond to the actual values of the 12xCL bits.

Figure 24 helps illustrate the behavior of the 12VNRS bit. Figure 24A shows that setting the 12xCL bits to 1111B results in a current limit equal to IMAX. Figure 24B shows how the 12xCL bits affect the current limit when the 12VNRS bit is cleared. Setting 12xCL = 0111B reduces the current limit to 60% of I_{MAX}. Figure 24C shows how the 12xCL bits affect the current limit when the 12VNRS bit is set. The current limit initially equals I_{MAX}, but as soon as the current drops below this level, the current limit resets to 60% of I_{MAX} and remains there so long as the channel remains enabled.

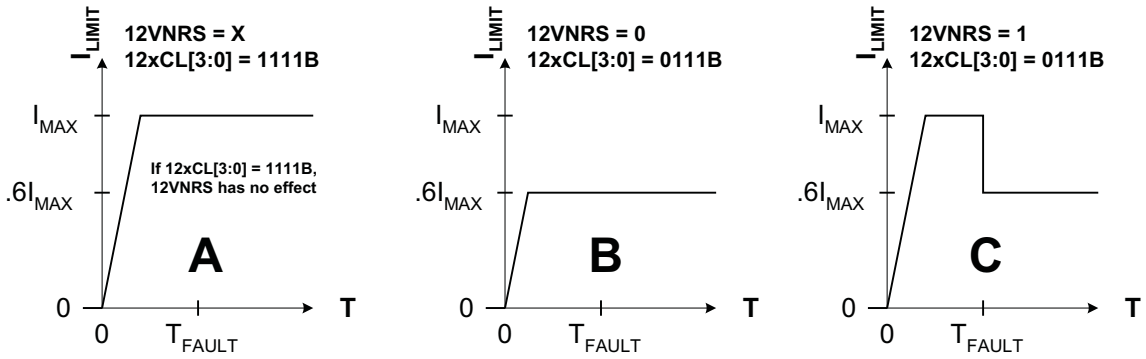


Figure 24. Current Limits in Redundant and Non-Redundant Systems

Example 1:
Set up 12A to start into an 80 W load and charge a 1600 uF capacitor in less than 3 ms. Set an operational I_{LIMIT} of 8.25 A +/- 10%.

First, calculate how much current is needed for capacitor charging and powering the load;

$I_{STARTUP} = I_{CHARGE} + I_{LOAD} = 6.4A + 6.67 A = 13.7 A$

Where;
$I_{CHARGE} = CV/T = 1600uF \times 12V / .003 s = 6.4 A$
$I_{LOAD} = P_{LOAD} / V_{LOAD} = 80 W / 12V = 6.67 A$

Now calculate R_{SET} for an I_{LIMIT} of 13.7 A.

$R_{SET} = (I_{LIMIT} \times R_{SENSE} \times R_{SUM}) / 0.675$
$= 691$ (closest 1% value = 698)

Where;
$R_{SUM} = 6810$
$R_{SENSE} = 5 m$

Now $I_{LIMIT} = 0.675 R_{SET} / (R_{SUM} R_{SENSE}) = 13.83 A$

If R0 [3:0] are set to 0111 and R6 [4] = 1 the current limit will drop to 60% of the programmed maximum after dropping out of current limit following inrush. The operational current limit is now;

$I_{LIMIT} = 0.6 \times I_{INRUSH} = 0.6 \times 13.83 = 8.3 A$

The 8.3 A limit complies with 8.25 A +/- 10 %.

Note - These calculations use all nominal values and neglect di/dt rates at turn on.

Figure 25. Inrush Current Limiting Example 1

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Example 2:
Set up 12A to startup into an 80 W load and charge a 1600 uF at not more than 17 A nominal. Then drop to an operational I_{LIMIT} of 8.25 A +/- 10%.

$I_{STARTUP}$ = 17 A

First, the correct R_{SET} must be found to set maximum I_{LIMIT} to less than 17 A.

R_{SET} = (I_{LIMIT} x R_{SENSE} x R_{SUM}) / 0.675
= 857 (closest 1% value = 845)

Where;
R_{SUM} = 6810
R_{SENSE} = 5 m

Now I_{LIMIT} = 0.675R_{SET} / (R_{SUM} R_{SENSE}) = 16.75 A

Neglecting current slew time, this will charge the 1600 uF capacitor in 1.9 ms.

If R0 [3:0] are set to 0101 and R6 [4] = 1 the current limit will drop to 50% of the programmed maximum after dropping out of current limit following inrush. The operational current limit is now;

I_{LIMIT} = 0.5 x I_{INRUSH} = 0.5 x 16.75 = 8.38 A

The new 8.38 A current limit is within the spec of 8.25 A +/- 10 %.

Note - These calculations use all nominal values.

Figure 26. Inrush Current Limiting Example 2

Table 15. Configuring 12-V Current Limits in Non-Redundant Systems

R_{SET}	12xCLx [3:0]	I_{LIMIT} - INRUSH 12VNRS		I_{LIMIT} OPERATIONAL 12VNRS = 1	P_{LOAD} (W)	C_{BULK} CHARGE TIME (ms)		FAULT TIME (ms)	
		R6[4]=0	R6[4]=1			800 µF	1600 µF	800 µF	1600 µF
412	1111	8.17	8.17	8.17	80	6.4	12.8	8.5	17
698	111	13.84	8.3	8.3	80	1.34	2.68	2	3.5
845	101	16.75	8.38	8.38	80	0.95	1.9	1.5	3

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Multiswap Operation in Redundant Systems

TheTPS2359 features an additional mode of operation called Multiswap redundancy. This technique does not require a microcontroller, making it simpler and faster than the redundancy schemes described in the MicroTCA™ standard. Multiswap is especially attractive for AdvancedMC™ applications requiring redundancy, but need not comply with the MicroTCA™ power module standard.

In order to implement multiswap redundancy, connect the SUM pins of the redundant channels together and tie a single R_{SUM} resistor from this node to ground. The current limit thresholds now apply to the sum of the currents delivered by the redundant supplies. When implementing multiswap redundancy on 12-V channels, all of the channels must use the same values of resistors for R_{SENSE} and R_{SET}.

Figure 27 compares the redundancy technique advocated by the MicroTCA™ specification with multiswap redundancy. MicroTCA™ redundancy independently limits the current delivered by each power source. The current drawn by the load cannot exceed the sum of the current limits of the individual power sources. Multiswap redundancy limits the current drawn by the load to a fixed value regardless of the number of operational power sources. Removing or inserting power sources within a multiswap system does not affect the current limit seen by the load.

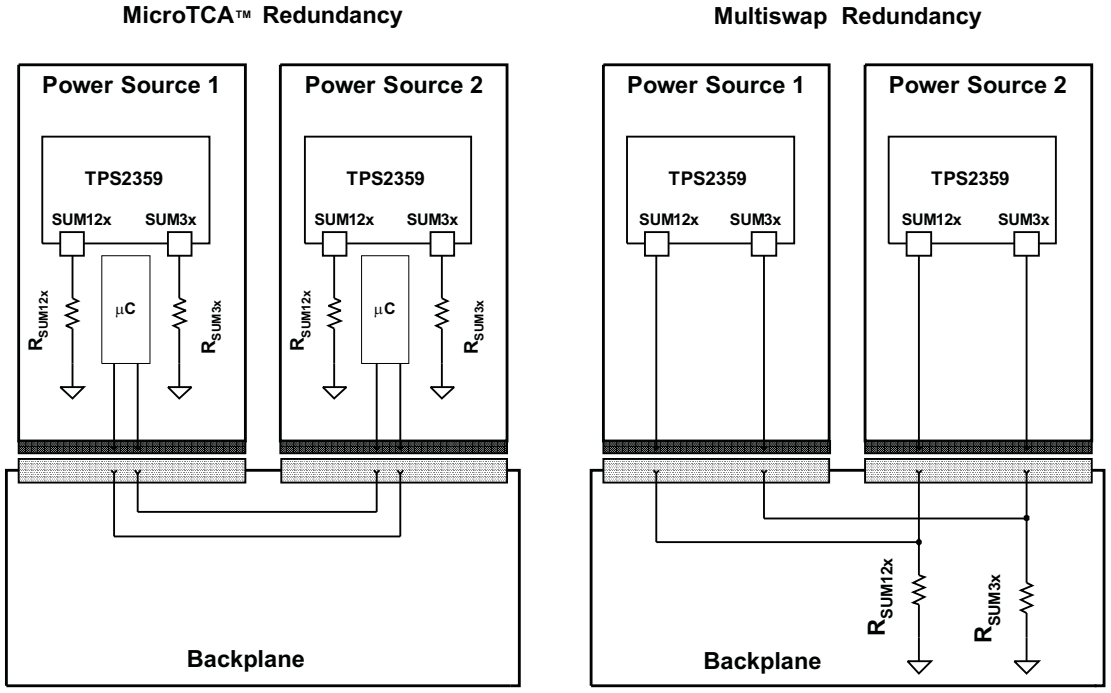


Figure 27. MicroTCA Redundancy vs. Multiswap Redundancy

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12-V Inrush Slew Rate Control

As normally configured, the turn-on slew rate of the 12-V channel output voltage V_{OUT12x} equals:

$$\frac{dV_{out}}{dt} \cong \frac{I_{src}}{C_g} \tag{7}$$

where I_{SRC} equals the current sourced by the PASSx pin (nominally 30 µA) and C_g equals the effective gate capacitance. For purposes of this computation, one can assume that the effective gate capacitance approximately equals the reverse transfer capacitance, C_{RSS}. To reduce the slew rate, increase C_g by connecting additional capacitance from PASSx to ground. Place a resistor of at least 1000 Ω in series with the additional capacitance to prevent it from interfering with the fast turn off of the FET. Since gate charge current is 30 µA and the TPS2359 current limits at start up it is unlikely that this RC is required.

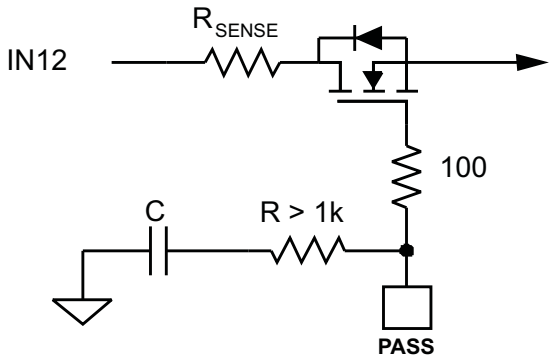


Figure 28. RC Slew Rate Control

12-V ORing Operation for Redundant Systems

The 12-V channels use external pass FETs to provide reverse current blocking. The TPS2359 pulls the BLKx pin high when the input-to-output differential voltage IN12x-OUT12x exceeds a nominal value of 10 mV, and it pulls the pin low when this differential falls below a nominal value of -3 mV. These thresholds provide a nominal 13 mV of hysteresis to help prevent false triggering.

The source of the blocking FET connects to the source of the pass FET, and the drain of the blocking FET connects to the load. This orients the body diode of the blocking FET such that it conducts forward current and blocks reverse current. The body diode of the blocking FET does not normally conduct current because the FET turns on when the voltage differential across it exceeds 10 mV.

Applications that do not use the blocking FET should clear the associated 12xOR bit to turn off the internal circuitry that drives the BLKx pin.

12-V ORing for High-Power Loads

The 12AHP and 12BHP bits adjust the ORing turn-off thresholds of the 12A and 12B channels, respectively. Clearing these bits sets the ORing turn-off thresholds to the default nominal value of -3 mV. Setting these bits shifts the thresholds up by 6 mV to a nominal value of +3 mV (Figure 29). Shifting the turn-off threshold to a postive value ensures that the blocking FET shuts off before any reverse current flows.

A light load may not draw sufficient current to keep the input-to-output differential VIN12x–OUT12x above 3 mV. When this happens, the blocking FET shuts off and then the differential voltage increases until it turns back on. This process endlessly repeats, wasting power and generating noise. Therefore 12AHP or 12BHP should only be set for high-power loads that satisfy the relationship

$$I_{LOAD} > \frac{10mV}{R_{SENSE} + R_{DSonPASS} + R_{DSonBLK}} \tag{8}$$

where I_{LOAD} equals the current drawn by the load, R_{SENSE} equals the value of the sense resistor, $R_{DS(on)PASS}$ equals the maximum on-resistance of the pass FET, and $R_{DSo(n)BLK}$ equals the maximum on-resistance of the blocking FET.

Example: If $R_{SENSE} = R_{HSFET} = R_{ORFET} = 5\ m\Omega$ then a high-power load must always draw at least 667 mA. Most, although not all, AdvancedMC™ loads can benefit from using the high-power bits 12AHP and 12BHP.

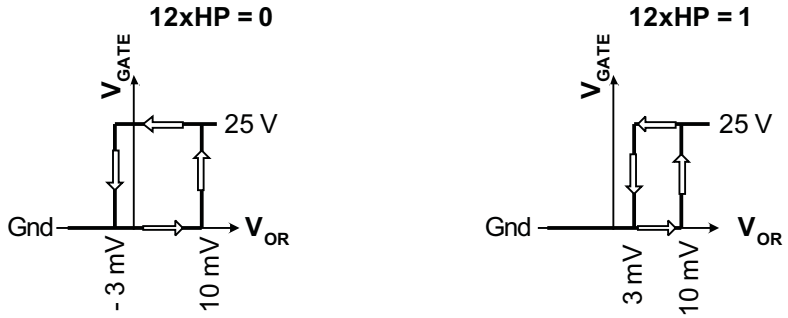


Figure 29. 12-V ORing Thresholds - High Power vs. Low Power

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Internal Bleed-Down Resistors and Bleed-Down Thresholds

The TPS2359 includes two features intended to support downstream loads that require removal and reapplication of power to properly reset their internal circuitry. Disabling and re-enabling a channel of the TPS2359 will not necessarily reset such a load because the capacitance attached to the output bus may not fully discharge.

The TPS2359 includes four bleed down comparators that monitor the output rails through pins OUT12A, OUT12B, OUT3A, and OUT3B. The I^2C interface includes four bits that enable these comparators — 3ADS, 3BDS, 12ADS, and 12BDS. Enabling a bleed down comparator prevents its corresponding channel from turning on until the output voltage drops below about 100 mV. This precaution ensures that the output rail drops so low that all downstream loads properly reset.

In case the downstream load cannot quickly bleed off charge from the output capacitance, the TPS2359 also includes bleed down resistors connected to each output rail through pins OUT12A, OUT12B, OUT3A, and OUT3B. Internal switches connect these resistors from their corresponding rails to ground when the channels are disabled, providing that one sets the appropriate bits in the I2C interface. These bits are named 12AUV, 12BUV, 3AUV, and 3BUV. Clearing these bits ensures that the corresponding resistors never connect to their buses.

If redundant supplies connect to an output, then one should clear the corresponding bleed-down threshold and bleed-down resistor bits. Failing to clear the bleed-down threshold bit will prevent the channel from enabling so long as the redundant supply continues to hold up the output rail. Failing to clear the bleed-down resistor bit will cause current to continually flow through the resistor when the TPS2359 is disabled and the redundant supply holds up the output bus.

Fault Timer Programming

Each of the TPS2359's four channels includes a fault timer. This timer is counting whenever V_{GS} of the FET is less than 6 ±1 V. If the channel remains in current limit so long that the fault timer runs out, then the channel turns off the pass FET and reports a fault condition by means of the xFLT bit in the I^2C interface.

The four fault timers are independently programmable from 0.45 to 13.95 ms in steps of 0.45 ms using the appropriate xFT bits. A code of xFT = 00001B corresponds to a time of 0.45 ms. The code xFT = 00000B should not be used.

The locations of the fault timer programming bits are:

Table 16. Fault Time Control Bits

CHANNEL	REGISTER [bit]				
	7.2 ms	3.6 ms	1.8 ms	0.9 ms	0.45 ms
12A	R1[4]	R1[3]	R1[2]	R1[1]	R1[0]
12B	R4[4]	R4[3]	R4[2]	R4[1]	R4[0]
3A	R2[4]	R2[3]	R2[2]	R2[1]	R2[0]
3B	R5[4]	R5[3]	R5[2]	R5[1]	R5[0]

The user should select the shortest fault times sufficient to allow down-stream loads and bulk capacitors to charge. Shorter fault times reduce the stresses imposed on the pass FETs under fault conditions. This consideration may allow the use of smaller and less expensive pass FETs for the 12-V channels.

The TPS2359 supports two modes of fault timer operation. Clearing the FLTMODE bit causes a channel to latch off whenever its fault timer runs out. The channel remains off until it has been disabled and re-enabled (see Enable Functions section). The TPS2359 operates in this manner by default. Setting the FLTMODE bit causes a faulted channel to automatically attempt to turn back on after a delay roughly one hundred times the fault time. This process repeats until either the fault disappears or the user disables the channel. The pass FET for a 12-V channel with a shorted output must therefore continuously dissipate

$$P_{fault} \approx 0.01 \cdot V_{IN12x} I_{CL} \tag{9}$$

where VIN12x equals the voltage present at the input of the 12-V channel and I_{CL} equals the current limit setting for this channel (the inrush current if 12VNRS is set).

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TPS2359 I²C Interface

The TPS2359 digital interface meets the specifications for an I²C bus operating in the high-speed mode. One can configure the interface to recognize any one of 27 separate I²C addresses using the A0, A1, and A2 pins (Table 17 I²C Addressing). These pins accept any of three distinct voltage levels. Connecting a pin to ground generates a low level (L). Connecting a pin to VINT generates a high level (H). Leaving a pin floating generates a no-connect level (NC).

Table 17. I²C Addressing

EXTERNAL PINS			I²C (Device) ADDRESS		
A2	A1	A0	Dec	Hex	Binary
L	L	L	8	8	1000
L	L	NC	9	9	1001
L	L	H	10	0A	1010
L	NC	L	11	0B	1011
L	NC	NC	12	0C	1100
L	NC	H	13	0D	1101
L	H	L	14	0E	1110
L	H	NC	15	0F	1111
L	H	H	16	10	10000
NC	L	L	17	11	10001
NC	L	NC	18	12	10010
NC	L	H	19	13	10011
NC	NC	L	20	14	10100
NC	NC	NC	21	15	10101
NC	NC	H	22	16	10110
NC	H	L	23	17	10111
NC	H	NC	24	18	11000
NC	H	H	25	19	11001
H	L	L	26	1A	11010
H	L	NC	27	1B	11011
H	L	H	28	1C	11100
H	NC	L	29	1D	11101
H	NC	NC	30	1E	11110
H	NC	H	31	1F	11111
H	H	L	32	20	100000
H	H	NC	33	21	100001
H	H	H	34	22	100010

The I²C hardware interface consists of two wires known as serial data (SDA) and serial clock (SCL). The interface is designed to operate from a nominal 3.3-V supply. SDA is a bidirectional wired-OR bus that requires an external pullup resistor, typically a 2.2-kΩ resistor connected from SDA to the 3.3-V supply.

The I²C protocol assumes one device on the bus acts as a master and another device acts as a slave. The TPS2359 supports only slave operation with two basic functions called register write and register read.

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Register Write: Figure 30 Format of a Register Writeshows the format of a register write. First the master issues a start condition, followed by a seven-bit I^2C address. Next the master writes a zero to signify that it wishes to conduct a write operation. Upon receiving an acknowledge from the slave, the master writes the eight-bit register number across the bus. Following a second acknowledge, the master writes the eight-bit data value for the register across the bus. Upon receiving a third acknowledge, the master issues a stop condition. This action concludes the register write.

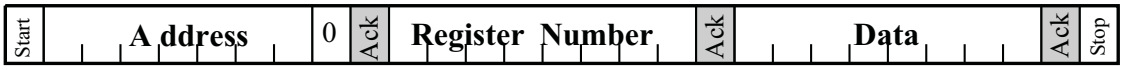


Figure 30. Format of a Register Write. Shaded Regions Denote Bus Control by TPS2358/9

Register Read: Figure 31 Format of a Register Read shows the format of a register read. First the master issues a start condition followed by a seven-bit I^2C address. Next, the master writes a zero to signify that it will conduct a write operation. Upon receiving an acknowledge from the slave, the master writes the eight-bit register number across the bus. Following a second acknowledge, the master issues a repeat start condition. Then the master issues a seven-bit I^2C address followed by a one to signify that it will conduct a read operation. Upon receiving a third acknowledge, the master releases the bus to the TPS2359. The TPS2359 then writes the eight-bit data value from the register across the bus. The master acknowledges receiving this byte and issues a stop condition. This action concludes the register read.



Figure 31. Format of a Register Read. Shaded Regions Denote Bus Control by TPS2358/9

Using the TPS2359 to Control Two AdvancedMC™ Slots

The TPS2359 has been designed for use in systems under I^2C control. Figure 32 shows the TPS2359 in a typical system implementing redundant power sources. A non-redundant application would omit the blocking FETs and leave the BLKx pins unconnected.

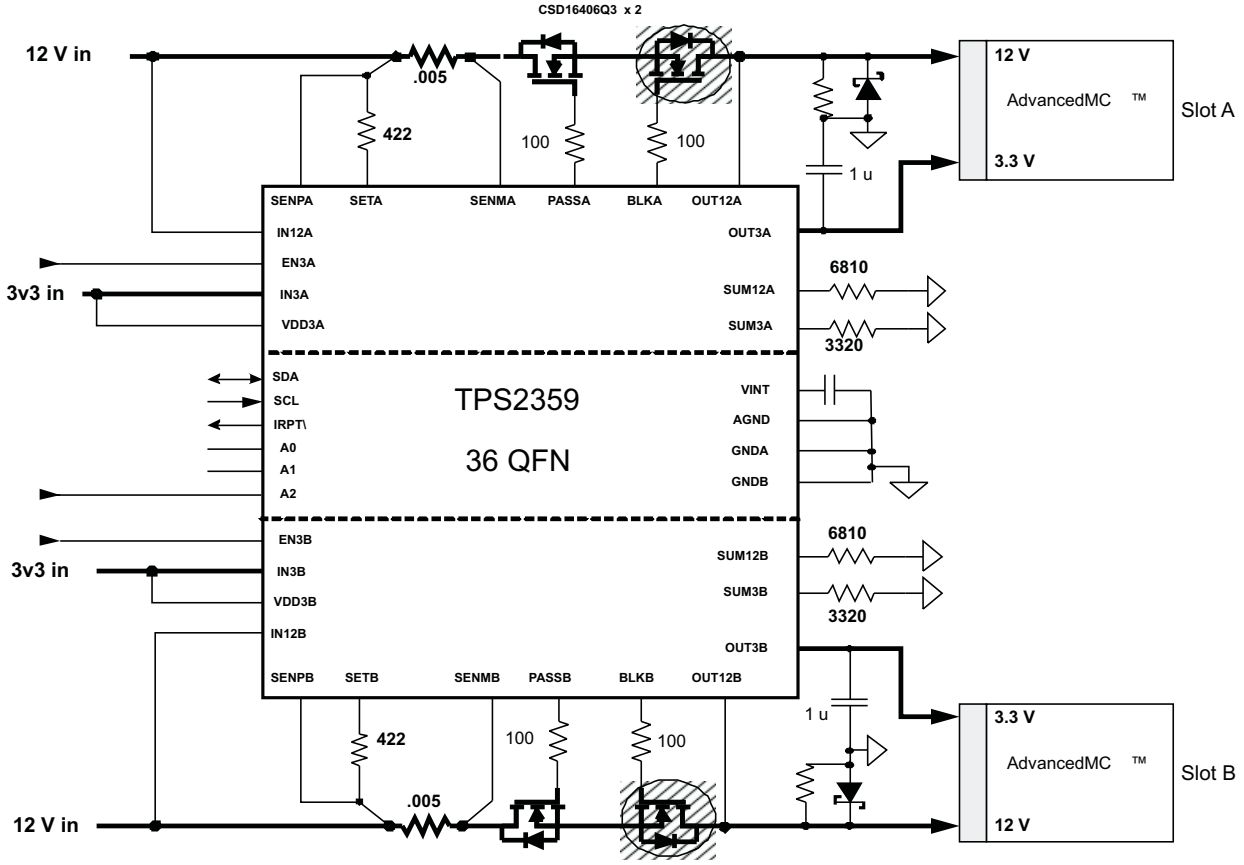


Figure 32. Block Diagram of TPS2359 In a Redundant System

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Layout Consideration

TPS2359 applications require careful attention to layout in order to ensure proper performance and minimize susceptibility to transients and noise. Important points to consider include:

1. Connect AGND, GNDA, and GNDB to a ground plane.
2. Place 0.01-µF or larger ceramic bypass capacitors on IN12A, IN12B, VDD3A, and VDD3B. Minimize the loop area created by the leads running to these devices.
3. Minimize the loop area between the SENMx and SENPx leads by running them side-by-side. Use Kelvin connections at the points of contact with R_{SENSE} (Figure 33).
4. Minimize the loop area between the SETx and SENPx leads. Connect the SETx leads to the same Kelvin points as the SENPx leads, or as close to these points as possible.
5. Size the following runs to carry at least 20 Amps:
   – Runs on both sides of R_{SENSE}
   – Runs from the drains and sources of the external FETs
6. Minimize the loop area between the OUT12x and SENPx leads.
7. Size the runs to IN3x and OUT3x to carry at least 1 Amp.
8. Soldering the powerpad of the TPS2359 to the board will improve thermal performance.

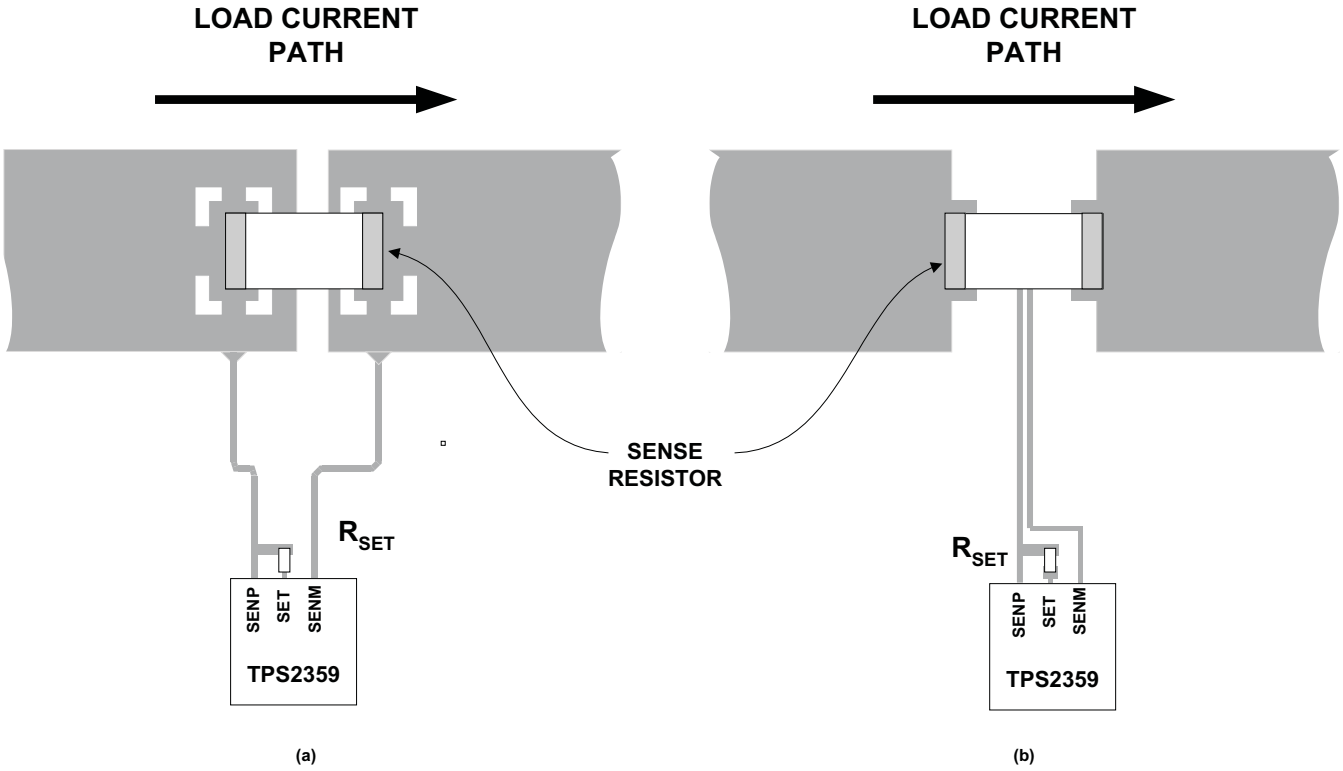


Figure 33. SENMx and SENPx Runs Side-by-Side to Maximize Common Mode Rejection

NOTE

Additional details omitted for clarity.

Transient Protection

The need for transient protection in conjunction with hot-swap controllers should always be considered. When the TPS2359 interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The following equation estimates the magnitude of these voltage spikes:

$$V_{SPIKE} = V_{NOM} + I_{LOAD}\sqrt{L/C} \quad (10)$$

where V_{NOM} equals the nominal supply voltage, I_{LOAD} equals the load current, C equals the capacitance present at the input or output of the TPS2359, and L equals the effective inductance seen looking into the source or the load. The inductance due to a straight length of wire equals approximately

$$L_{StraightWire} \approx 0.2 \times L \times ln\left(\frac{4L}{D} - 0.75\right) \quad nH \quad (11)$$

where L equals the length of the wire and D equals its diameter.

If sufficient capacitance to prevent transients from exceeding the absolute ratings of the TPS2359 cannot be included the application will require the addition of transient protectors.

Output Protection Considerations for MicroTCA Power Systems

MicroTCA power systems have particular transient protection requirements because of the basic power architecture. Traditional protection methods must be adjusted to accommodate these systems where the supplies are OR'ed together after the inrush control and current limit circuits. However, minor changes to some standard techniques will yield very good results.

Unlike systems which have hotswap/inrush control at the load, uTCA power modules and their hot swap circuitry are often a significant distance (up to 1 m of trace length, two way) from the load module. Even with the best designed backplanes this distance results in stray inductance which will store energy while current is being delivered to the load. The inductive energy can cause large negative voltage spikes at the power module output when the current is switched off under load. The spikes become especially severe when the channel shuts off due to a short circuit, which drives the current well above normal levels just before shut off.

The lowest voltage allowed on the device pins is -0.3 V. If a transient makes a pin more negative than -0.3 V the internal ESD Zener diode attached to the pin will become forward biased and current will be conducted across the substrate to the ground pins. This current may disrupt normal operation or, if large enough, damage the silicon. Typical protection solutions involve capacitors, TVSs (Transient Voltage Suppressors) and/or a Schottky diode to absorb the energy which appears at the power module output in the form of a large negative voltage spike.

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The Risk With Output Capacitors

Putting transient filter capacitors at the output of a uTCA power module can cause nuisance trips when that power module is plugged into an active bus. If there is no series resistance with the capacitor and the bus is low impedance an inrush surge can cause the active supply to “detect” a short circuit and shut down. One possible solution is to put a few Ohms of resistance in series with the cap to limit inrush below the fast trip level. A better solution is to put a Schottky diode across the output to clamp the transient energy and shunt it to ground as shown in Figure 34. Although the Schottky diode will absorb most of the energy, the extremely fast di/dt at shutoff allows some of the leading edge energy to couple through the parasitic capacitances of the hotswap FET and the ORing FET, (C_{DS}, C_{GS}, C_{GD}) and into the BLK and GATE pins. Protection for these pins is provided by 100-Ω GATE resistors which have little effect on normal operation but provide good isolation during transient events.

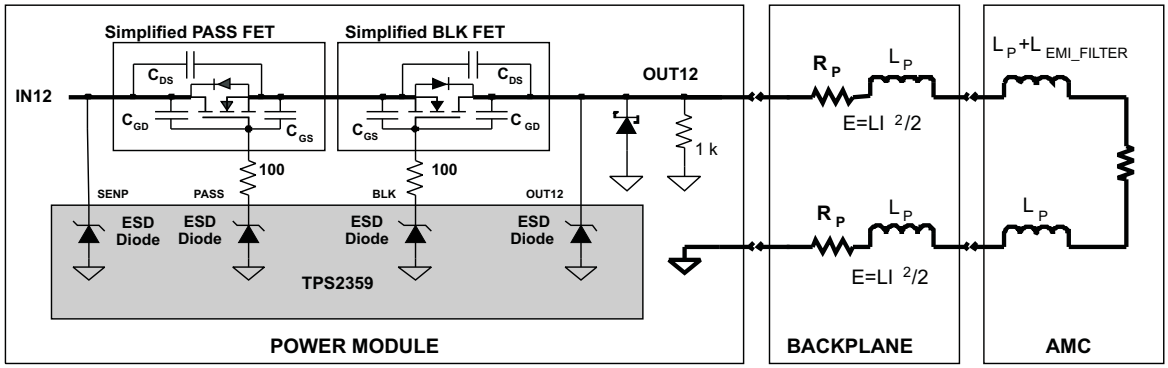


Figure 34. Parasitic Inductance and Transient Protection

Output Bleed Down Resistance

When the TPS2359 commands the 12-V channel off there is a small leakage current sourced by the OUT12 pin. If this leakage is ignored it can eventually charge any external capacitance to approximately 6 V. In some systems this may be acceptable but, if not, the leakage can be bled to GND by commanding the internal bleed down resistor on by setting 12xDS high.

- 12ADS = R1[7]
- 12DSB = R4[7]

If a hardware solution is preferred then a 1-kΩ resistor from OUT12 to GND will suffice. Maximum leakage is around 23 µA and can be modeled as a 6-V source in series with a 280-kΩ resistor.

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REVISION HISTORY

Changes from Revision E (November 2009) to Revision F **Page**

- Changed leakage typo in the EC table from mA to µA 5

Changes from Revision F (August 2010) to Revision G **Page**

- Changed Fault Timer TYP values from 1 ms, and 0.5 ms to 0.5 and 0.41. 3
- Changed Table 2 Register 1, Register 2, Register 4, and Register 5 From: fault time by 0.5, 1, 2, 4, and 8 ms To: 0.41, 0.82, 1.64, 3.28 and 6.56 ms. 17
- Changed Table 4 fault time by From: 0.5, 1, 2, 4, and 8 ms To: 0.41, 0.82, 1.64, 3.28 and 6.56 ms. 20
- Changed 12AFT[4:0] values from 0.5 ms to 0.41 in two places and 15.5 ms to 12.7 ms. 20
- Changed Table 5 falut time by From 0.5, 1, 2, 4, and 8 ms To: 0.41, 0.82, 1.64, 3.28 and 6.56 ms 21
- Changed 3AFT[4:0] values from 0.5 ms to 0.41 in two places and 15.5 ms to 12.7 ms. 21
- Changed Table 7 fault time by From: 0.5, 1, 2, 4, and 8 ms To: 0.41, 0.82, 1.64, 3.28 and 6.56 ms 23
- Changed 12BFT[4:0] values from 0.5 ms to 0.41 ms in two places and 15.5 ms to 12.7 ms. 23
- Changed Table 8 fault time by From: 0.5, 1, 2, 4, and 8 ms To: 0.41, 0.82, 1.64, 3.28 and 6.56 ms 24
- Changed 3BFT[4:0] values from 0.5 ms to 0.41 in two places and 15.5 ms to 12.7 ms. 24
- Changed Table 10 default values from 0 to 1 in four places. 26
- Changed 12APG text from "This bit is set if the voltage on OUT12A drops below the power-good threshold set by the 12APG[1:0] bits, and it remains set until Register 7 is read." to "This bit is set at startup and each time OUT12A drops below the PG threshold set by the 12APG[1:0] bits. It is cleared on read if OUT12A is above the PG threshold." 26
- Changed 3APG text from "This bit is set if the voltage on OUT3A drops below the power-good threshold, and it remains set until Register 7 is read." to "This bit is set at startup and each time OUT3A drops below the PG threshold.It is cleared on read if OUT3A is above the PG threshold." 26
- Changed 12BPG text from "This bit is set if the voltage on OUT12B drops below the power-good threshold set by the 12BPG[1:0] bits, and it remains set until Register 7 is read." to "This bit is set at startup and each time OUT12B drops below the PG threshold set by the 12BAPG[1:0] bits. It is cleared on read if OUT12B is above the PG threshold." 26
- Changed 3BPG text from "This bit is set if the voltage on OUT3B drops below the power-good threshold, and it remains set until Register 7 is read." to "This bit is set at startup and each time OUT3B drops below the PG threshold.It is cleared on read if OUT3B is above the PG threshold." 26
- Changed amplifier to TPS2359. 32
- Changed values in the Fault Timer Programming section: 0.5 ms to 0.41 in two places and 16 ms to 12.7 ms. 39
- Changed Table 16 values From: 8, 4, 2, 1 and 0.5 ms To: 6.56, 3.28, 1.64, 0.82 and 0.41 ms. 39
- Changed From: If a hardware solution is preferred then a -kΩ To: If a hardware solution is preferred then a 1-kΩ 45

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Changes from Revision G (November 2011) to Revision H **Page**

- Changed the Fault Timer section section of the ELECTRICAL CHARACTERISTICS table 3
- Changed Table 2 Register 1, Register 2, Register 4, and Register 5 From: fault time by 0.41, 0.82, 1.64, 3.28, and 6.56 ms To: 0.45, 0.9, 1.8, 3.6 and 7.2 ms. 17
- Changed Table 4 fault time by From: 0.41, 0.82, 1.68, 3.28, and 6.56 ms To: 0.45, 0.9, 1.8, 3.6 and 7.2 ms. 20
- Changed the 12AFT[4:0] description 20
- Changed Table 5 fault time by From: 0.41, 0.82, 1.68, 3.28, and 6.56 ms To: 0.45, 0.9, 1.8, 3.6 and 7.2 ms. 21
- Changed the 3AFT[4:0] description 21
- Changed Table 7 fault time by From: 0.41, 0.82, 1.68, 3.28, and 6.56 ms To: 0.45, 0.9, 1.8, 3.6 and 7.2 ms. 23
- Changed the 12BFT[4:0] description 23
- Changed Table 8 fault time by From: 0.41, 0.82, 1.68, 3.28, and 6.56 ms To: 0.45, 0.9, 1.8, 3.6 and 7.2 ms. 24
- Changed the 3BFT[4:0] description 24
- Changed the Fault Timer Programming section and Table 16 39

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2359RHHR	ACTIVE	VQFN	RHH	36	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS2359	Samples
TPS2359RHHT	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS2359	Samples
TPS2359RHHTG4	ACTIVE	VQFN	RHH	36	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPS2359	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

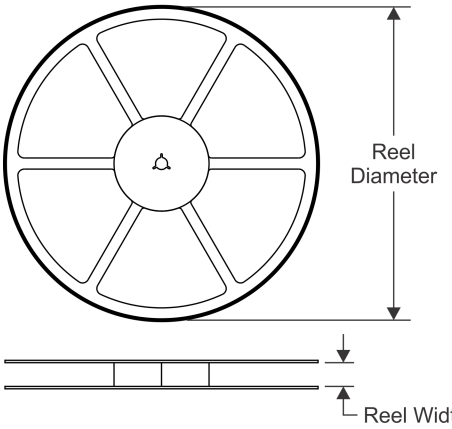
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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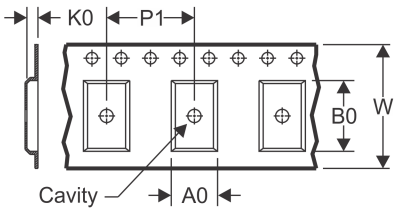
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

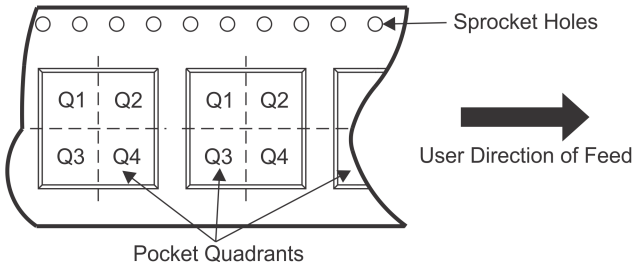


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

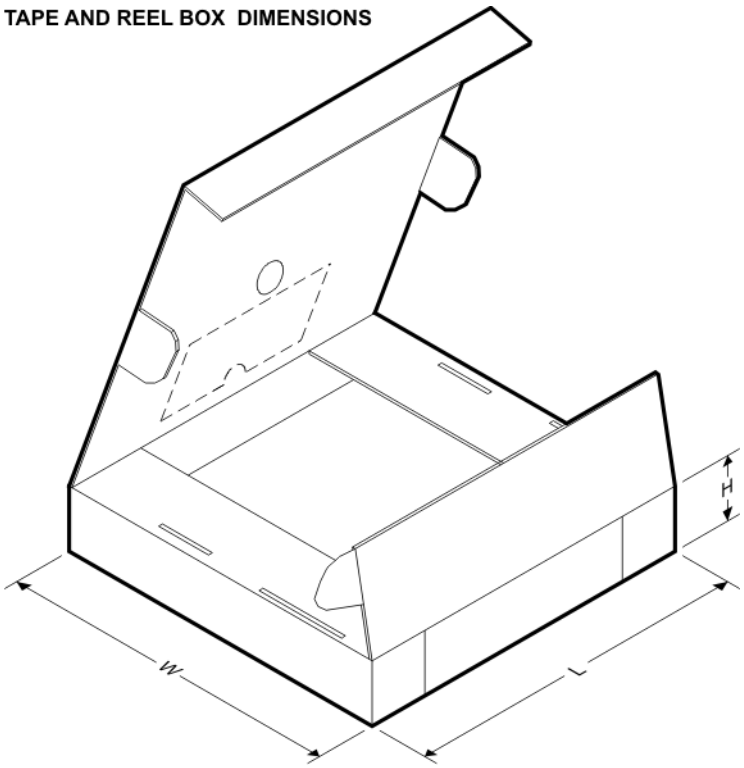
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2359RHHR	VQFN	RHH	36	2500	330.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2
TPS2359RHHT	VQFN	RHH	36	250	180.0	16.4	6.3	6.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2359RHHR	VQFN	RHH	36	2500	367.0	367.0	38.0
TPS2359RHHT	VQFN	RHH	36	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

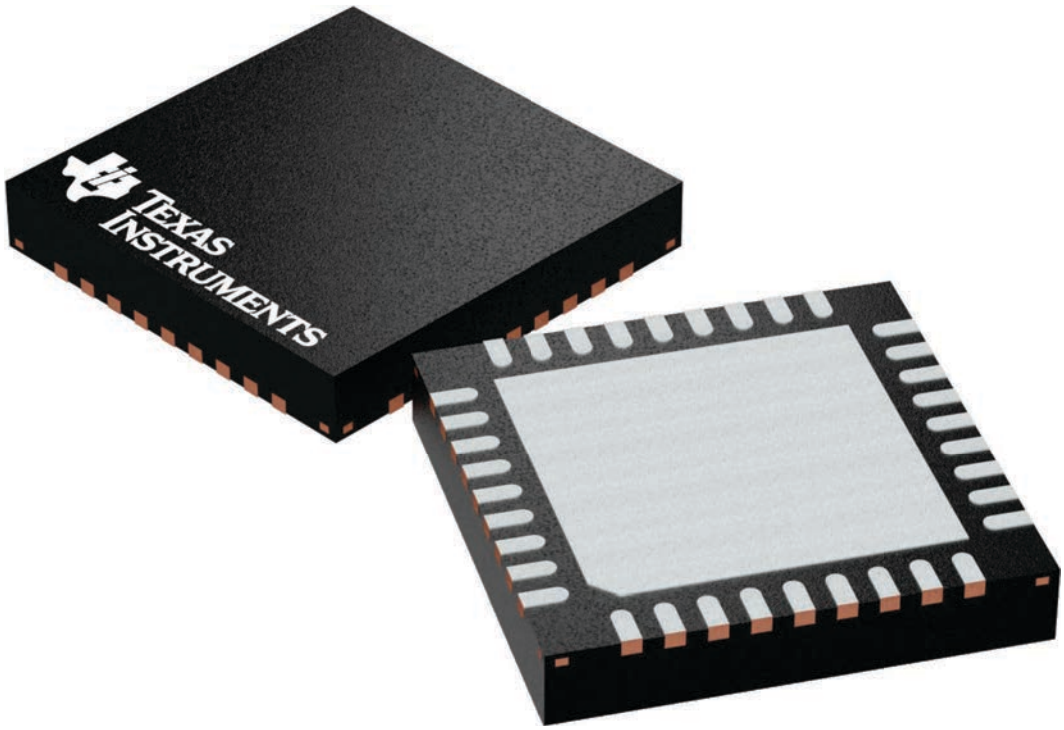
RHH 36

VQFN - 1 mm max height

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



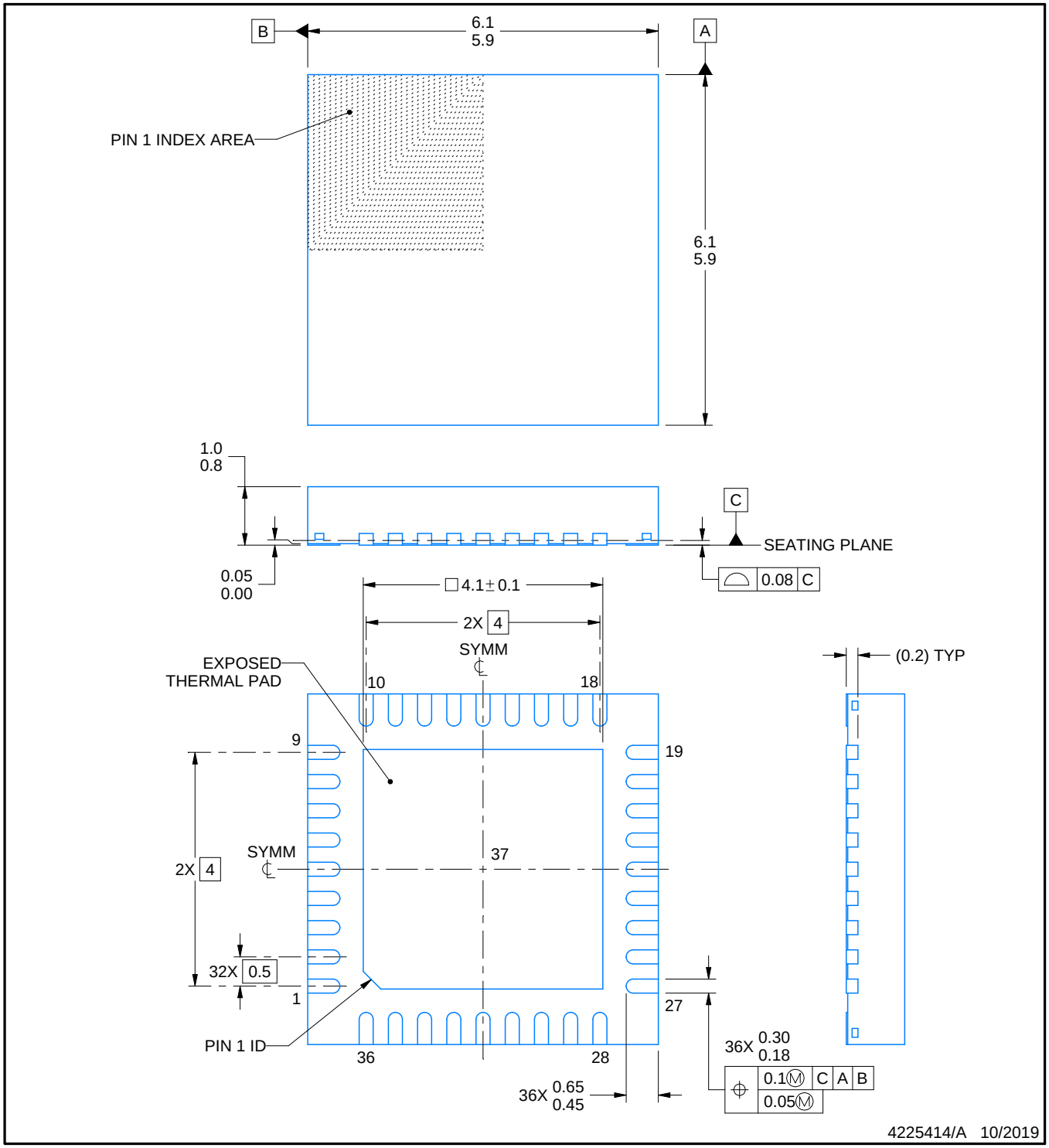
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RHH0036B

PACKAGE OUTLINE

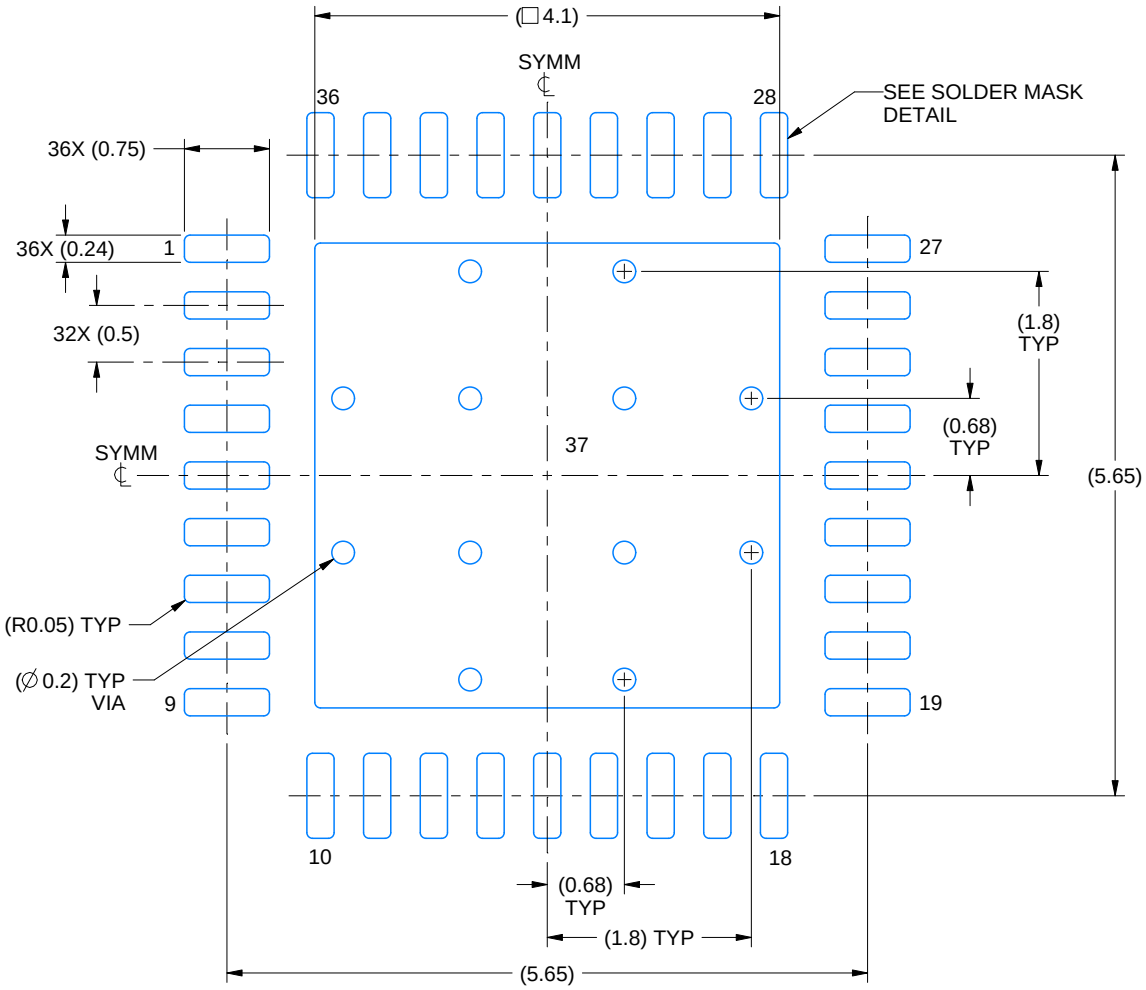
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

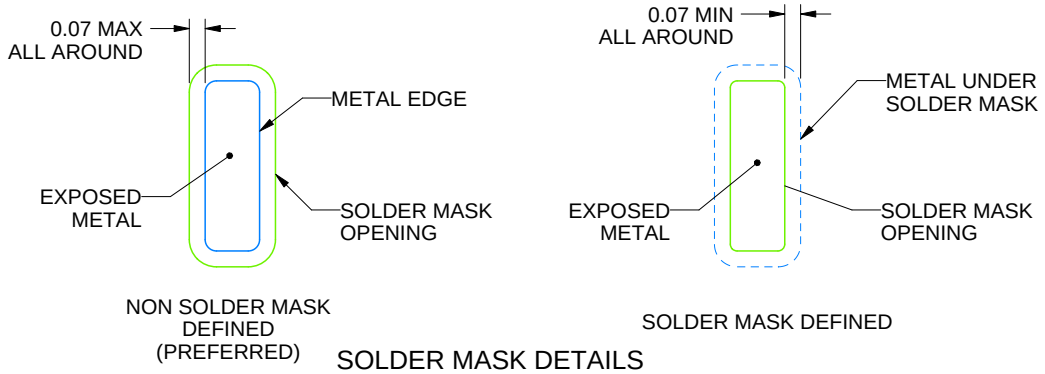


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

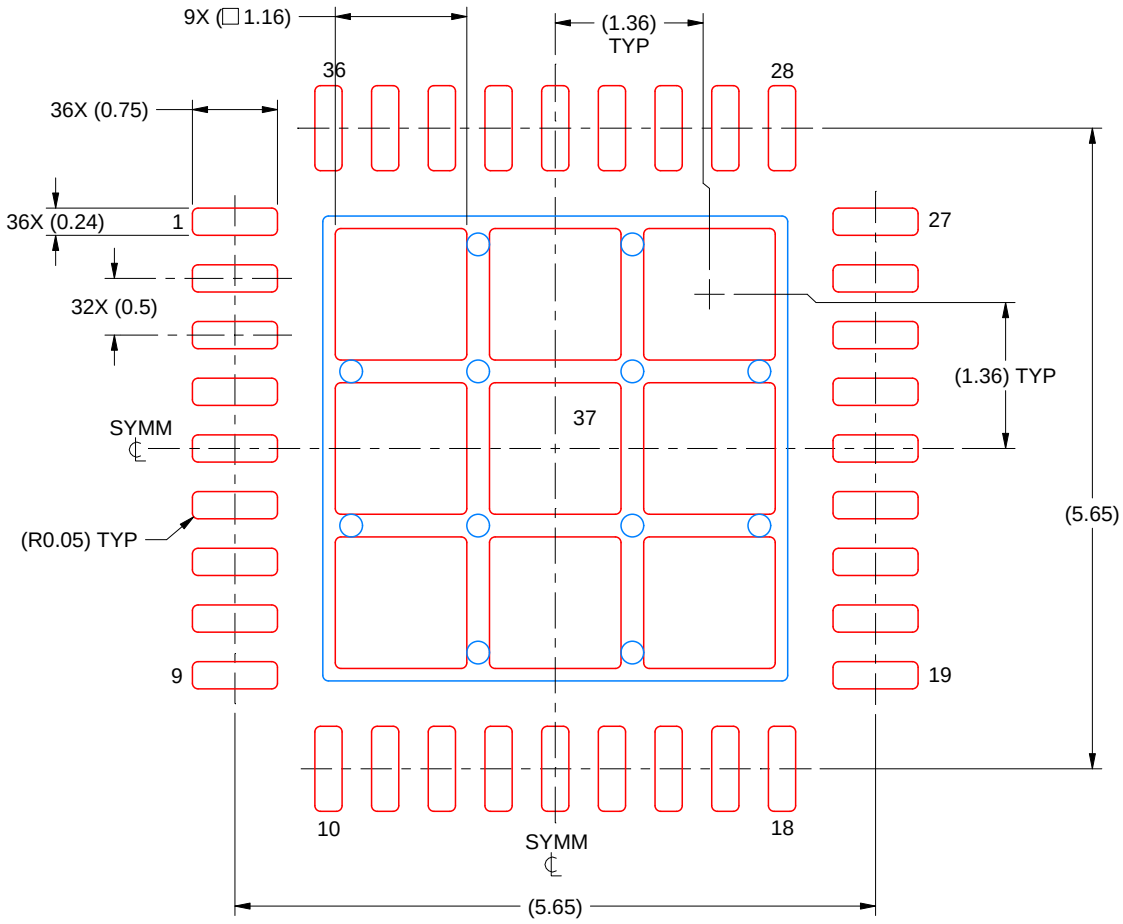


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 15X

EXPOSED PAD 37
72% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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