MPM3632S

High-Frequency 18V/3A DC/DC Regulator with Integrated Inductor

DESCRIPTION

The MPM3632S is a synchronous, rectified, step-down, mini-module regulator with built-in power MOSFETs, an inductor, and two capacitors. It offers a compact solution with only input and output capacitors to achieve a 3A continuous output current with excellent load and line regulation over a wide input supply range. The MPM3632S operates in a fixed 2.2MHz switching frequency with constant on-time (COT) control to provide fast load transient response.

Full protection features include output over-voltage protection, over-current protection, and thermal shut down.

The device eliminates design and manufacturing risks while dramatically improving time to market.

The MPM3632S is available in a space-saving EC LGA-10 (3mmx3mmx1.45mm) package.

FEATURES

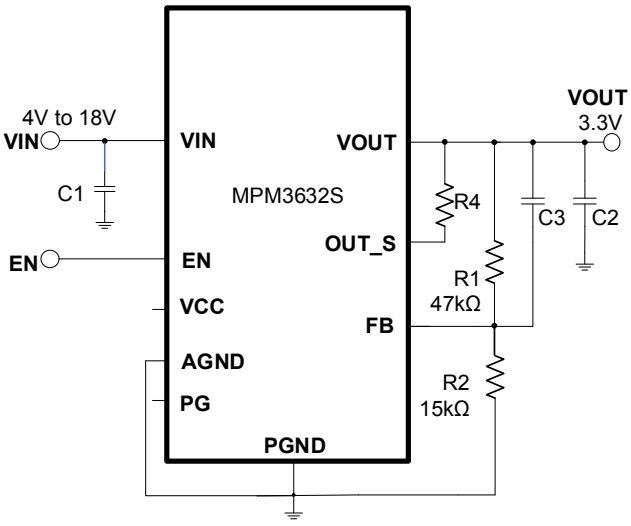
- Wide 4V to 18V Operation Input Range
- Internally Fixed Soft Start Time
- 0.5% Accuracy Output Voltage
- 3A Continuous Output Current
- 2.2MHz Switching Frequency
- Forced CCM Mode
- Power Good Indicator
- Hiccup OCP Protection
- Output Over-Voltage Protection
- Fast Transient Response
- Available in an EC LGA-10 (3mmx3mmx1.45mm) Package

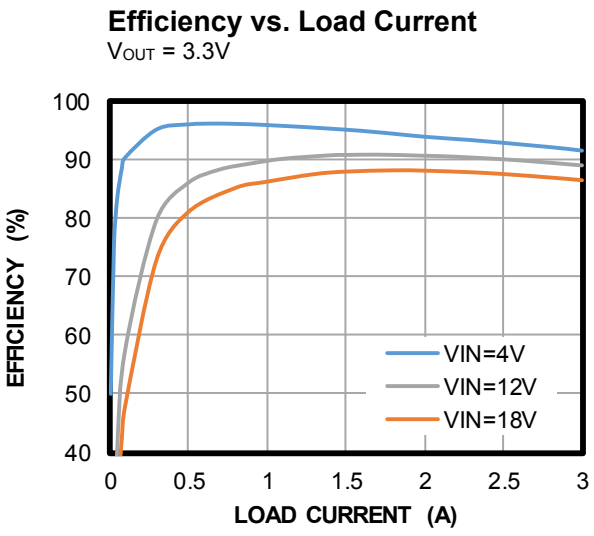
APPLICATIONS

- Server Systems
- Medical and Imaging Equipment
- Distributed Power Systems

All MPS parts are lead-free, halogen free, and adhere to the RoHS directive. For MPS green status, visit the MPS website under Quality Assurance. “MPS”, the MPS logo, and “Simple, Easy Solutions” are registered trademarks of Monolithic Power Systems, Inc. or its subsidiaries.

TYPICAL APPLICATION





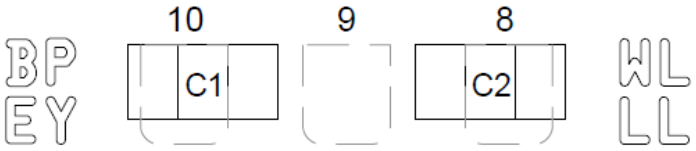
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MPM3632SGPQ	EC LGA-10 (3mmx3mmx1.45mm)	*See Below*	3

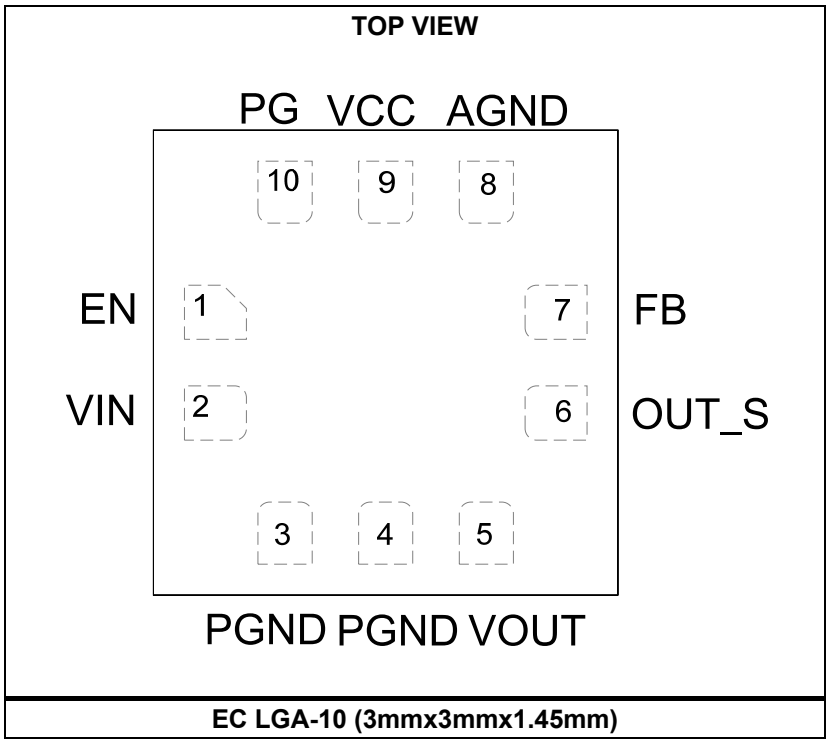
* For Tape & Reel, add suffix –Z (e.g. MPM3632SGPQ–Z). For tray, –Z is not required.

TOP MARKING



Y: Year code
W: Week code
BPE: part number code
LLL: Lot number

PACKAGE REFERENCE



EC LGA-10 (3mmx3mmx1.45mm)

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PIN FUNCTIONS

Pin #	Name	Description
1	EN	**Enable.** Drive EN high to enable the MPM3632S.
2	VIN	**Supply voltage.** The MPM3632S operates from a 4V to 18V input rail. Requires a ceramic capacitor to decouple the input rail. Connect using a wide PCB trace.
3, 4	PGND	**System ground.** Reference ground of the regulated output voltage. Requires special consideration during PCB layout. Connect to GND with copper traces and vias.
5	VOUT	**Power output pin.**
6	OUT_S	**Output voltage sense pin.**
7	FB	**Feedback pin.** Set the output voltage with divider resistors.
8	AGND	**Analog ground.**
9	VCC	**Internal 3.3V LDO regulator output.** The MPM3632S does not require external connections due to its internal decoupling capacitor .
10	PG	**Power good output.** Open-drain structure. PG switches to an open-drain state when FB is greater than 90%. It switches to low if FB is below 80% of V_{REF}.

ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} .....-0.3V to +20V
V_{SW}.....-0.3V (-5V for < 10ns)
to V_{IN} + 0.7V (22V for < 10ns)
V_{BST}..... V_{SW} + 4V
V_{EN}.....18V
V_{OUT} 6.5V
V_{PG}.....5.5V
All other pins.....-0.3V to +4V
Continuous power dissipation (T_A = +25°C) (2)
.....2.08W
Junction temperature.....150°C
Lead temperature.....260°C
Storage temperature .....-65°C to +150°C

ESD Rating

Human-body model (HBM)..... 2kV
Charged-device model (CDM) 1kV

Recommended Operating Conditions (3)

Supply voltage V_{IN} .....4V to 18V
Output voltage V_{OUT} .....0.8V to 5.2V
Operating junction temp. (T_J)....-40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

EVM3632S-PQ-00A	60	30	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on EVM3632S-PQ-00A, 4-layer PCB.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = -40°C to +125°C (5), unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	VEN = 0V			15	µA
Supply current (quiescent)	I_q	No switching, FB = 0.85V		1200		µA
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V			1	µA
Switching frequency		V_{OUT} = 3.3V	-15%	2200	+15%	kHz
		V_{OUT} = 1.2V	-15%	2200	+15%	kHz
Low-side valley current limit (6)	I_{LIMIT1}		3	3.3	3.9	A
Low-side negative current limit	I_{LIMIT2}	Force PWM mode or OVP, need force PWM option		-2.5		A
Minimum on time (6)	t_{ON_MIN}	Reach min t_{ON}, then decrease f_{SW}. Avoid unstable pulse. Simulate 18V to 1V spec.		25		ns
Minimum off time (6)	t_{OFF_MIN}	Reach min t_{OFF} then decrease f_{SW}, simulate 4.2V to 3.3V spec.		80		ns
Reference accuracy	V_{REF}	T_J = -40°C to +125°C	788	800	812	mV
Output load regulation (6)	V_{OLDREG}	V_{OUT} = 3.3V, I_{OUT} = 0A to 3A	-0.5		+0.5	%
Output line regulation (6)	V_{OLNREG}	V_{OUT} = 3.3V, I_O = 0.1A/1.5A/3A	-0.5		+0.5	%
Output over-voltage threshold	V_{OVP}	FB pin OV threshold, monitor Vin OV then hiccup	110%	115%	120%	V_{REF}
OVP hysteresis		OVP is disabled during SS		5%		V_{REF}
OVP delay	t_{OVP}			2		µs
Output pin absolute OV	V_{OVP2}	Same behavior with FB > 115%	5.7	6	6.3	V
Absolute OV hysteresis				50		mV
PG OV threshold rising	$PGOV_{Hi}$	Fault	110%	115%	120%	V_{REF}
PG OV threshold falling	$PGOV_{Lo}$	Good		110%		V_{REF}
PG UV threshold rising	$PGUV_{Hi}$	Good	85%	90%	95%	V_{REF}
PG UV threshold falling	$PGUV_{Lo}$	Fault		80%		V_{REF}
Power good deglitch time	PGDeg			50		µs

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_A = -40°C to +125°C [5], unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PG sink current capability	VPG	Sink 4mA		0.4	0.6	V
EN rising threshold	VEN_RISING		1.1	1.20	1.3	V
EN falling threshold	VEN_FALL		0.96	1.00	1.04	V
VIN UVLO rising	$INUV_{Vth}$		3.2	3.6	3.9	V
VIN UVLO hysteresis	INUVHYS	Take care V_{CC} LDO dropout		500		mV
VCC regulator	VCC			3.3		V
VCC load regulation		I_{CC} = 20mA		3		%
Soft start time [6]	t_{SS}	V_{OUT} from 10% to 90%		1.65		ms
Thermal shutdown [6]				150		°C
Thermal hysteresis [6]				20		°C

Notes:

5) Not tested in production and guaranteed by over-temperature correlation.

6) Guaranteed by characterization, not production tested.

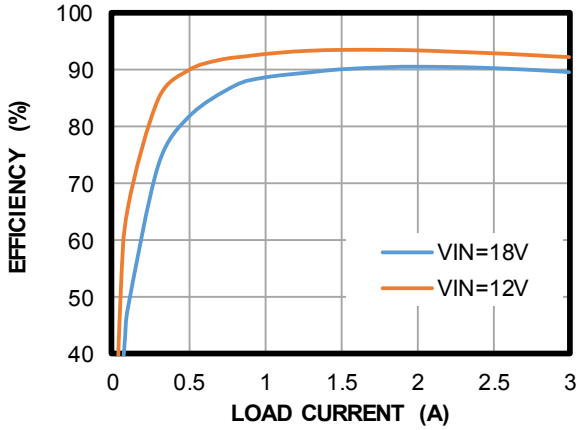
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

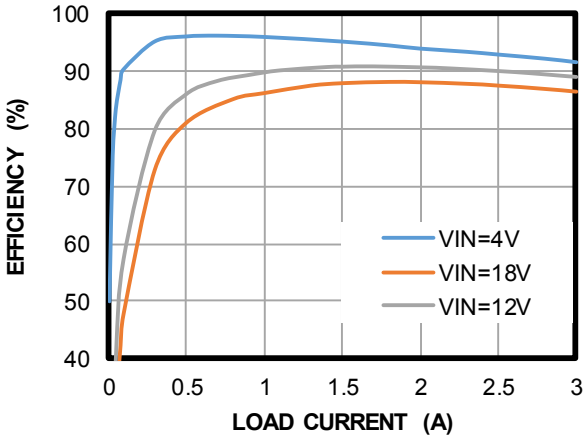
Efficiency vs. Load Current

V_{OUT} = 5V



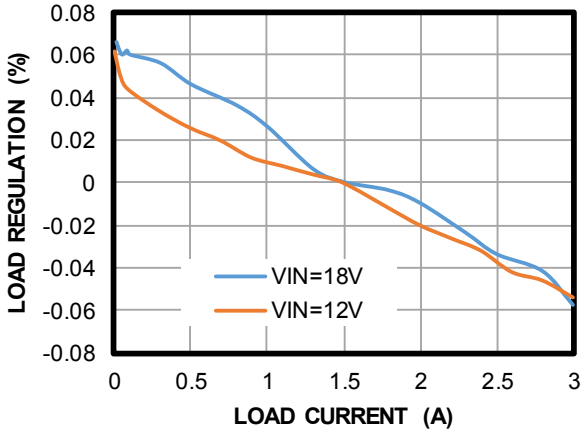
Efficiency vs. Load Current

V_{OUT} = 3.3V



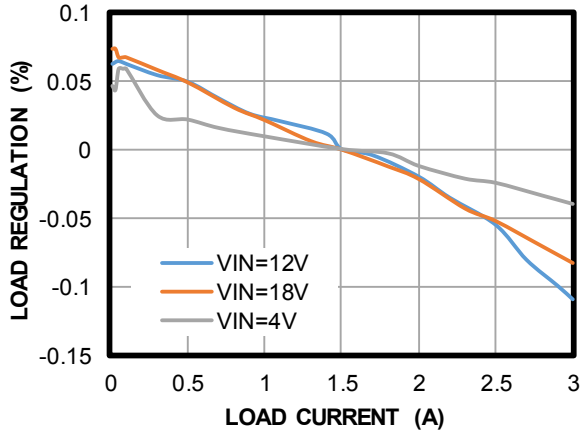
Load Regulation vs. Load Current

V_{OUT} = 5V



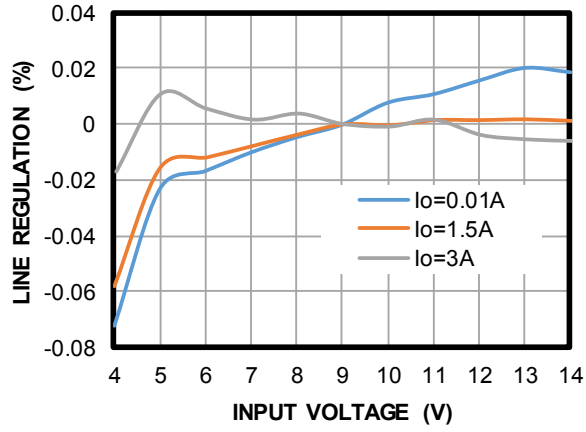
Load Regulation vs. Load Current

V_{OUT} = 3.3V



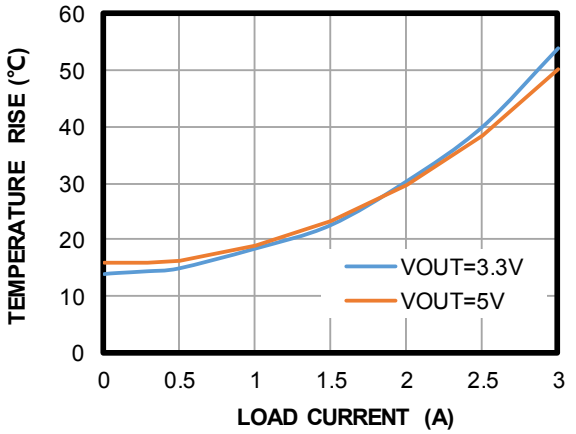
Line Regulation vs. Input Voltage

V_{IN} = 12V, V_{OUT} = 3.3V



Temperature Rise vs. Load Current

V_{IN} = 12V



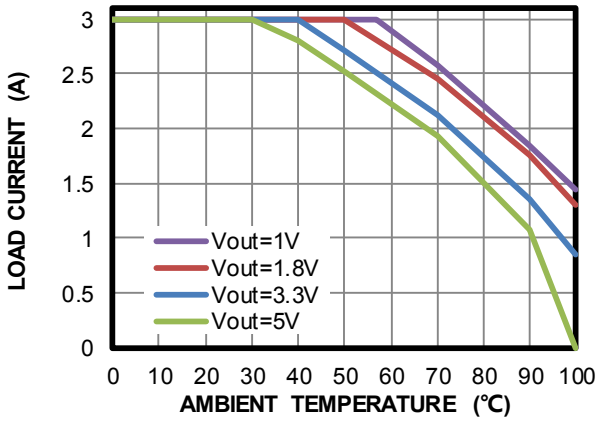
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

Thermal Derating

V_{IN} = 12V



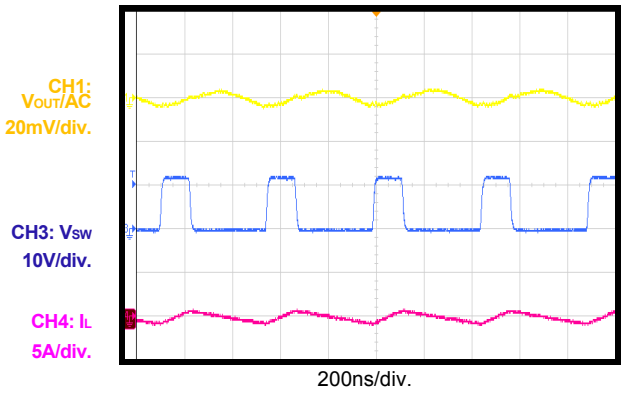
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

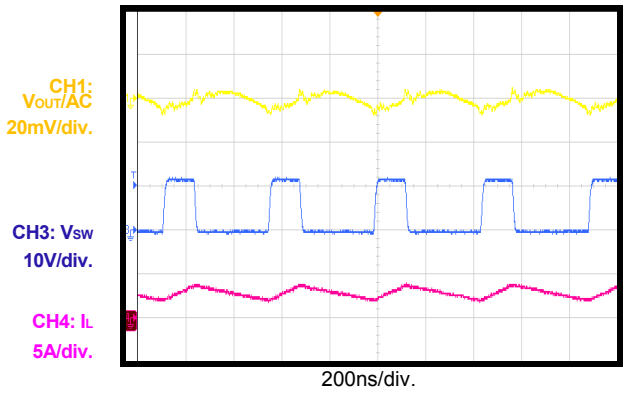
V_O Ripple

I_{OUT} = 0A



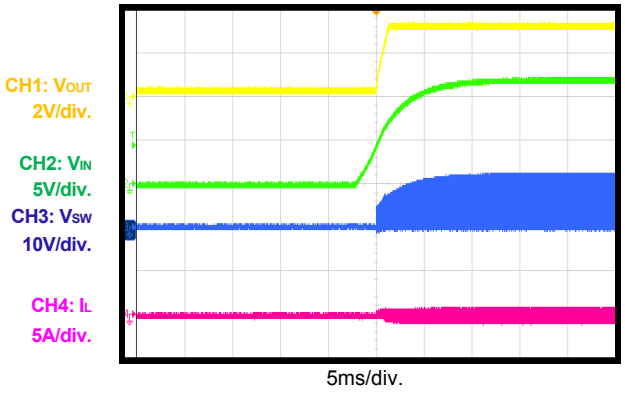
V_O Ripple

I_{OUT} = 3A



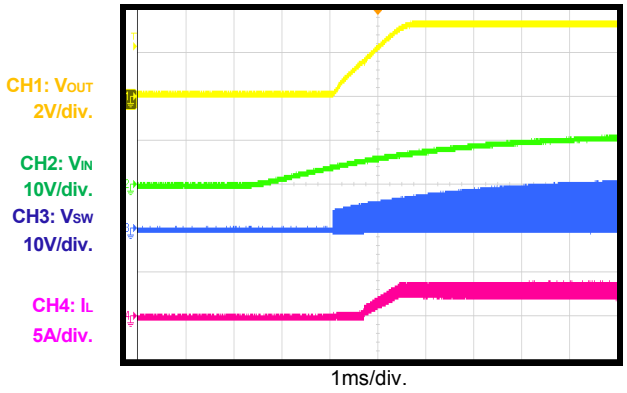
VIN Start-Up through Input Voltage

I_{OUT} = 0A



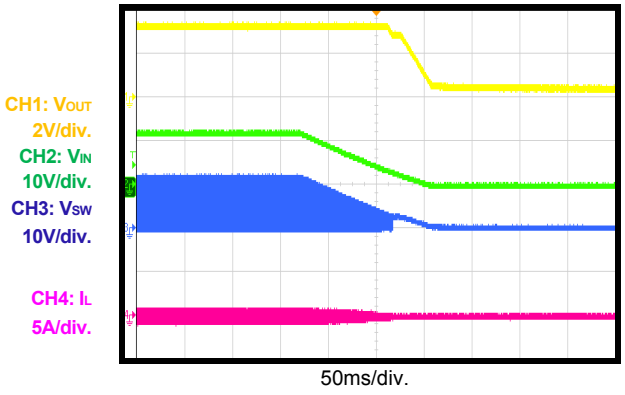
VIN Start-Up through Input Voltage

I_{OUT} = 3A



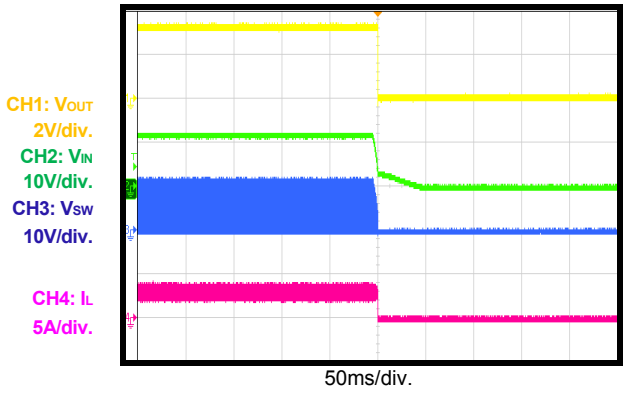
Shutdown through Input Voltage

I_{OUT} = 0A



Shutdown through Input Voltage

I_{OUT} = 3A

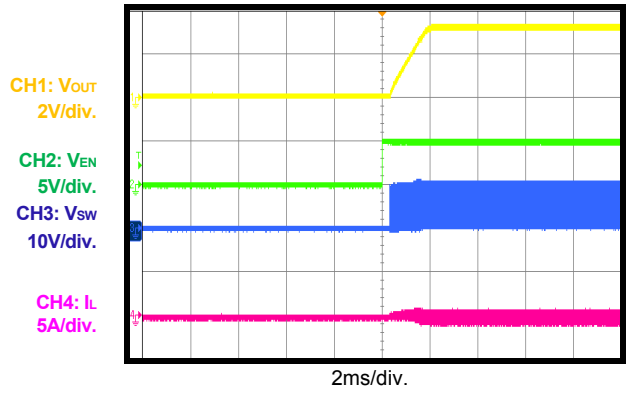


MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

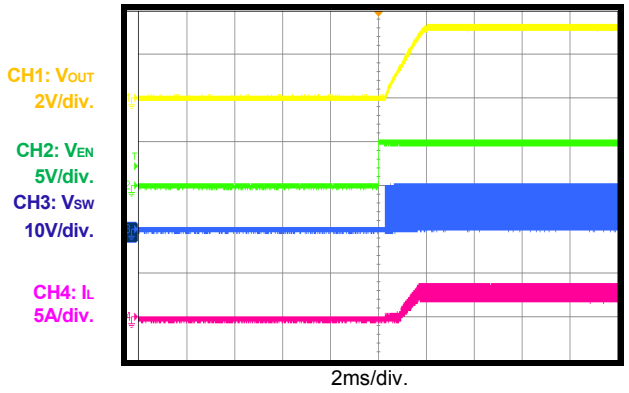
Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

Start-Up through Enable
I_{OUT} = 0A



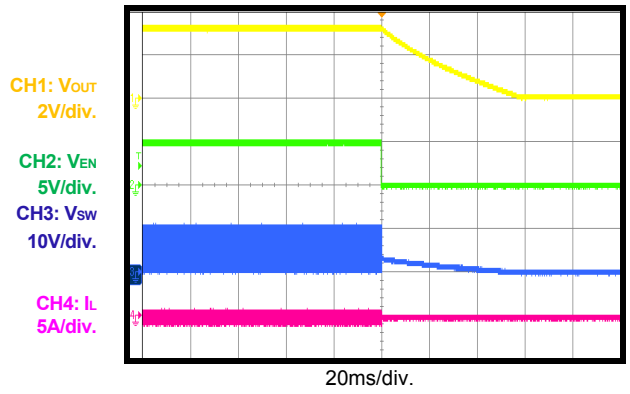
2ms/div.

Start-Up through Enable
I_{OUT} = 3A



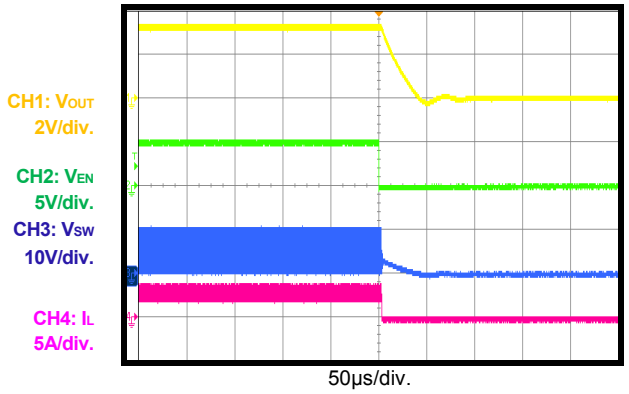
2ms/div.

Shutdown through Enable
I_{OUT} = 0A



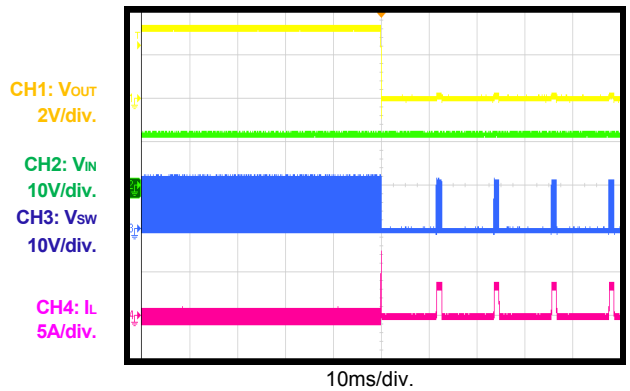
20ms/div.

Shutdown through Enable
I_{OUT} = 3A



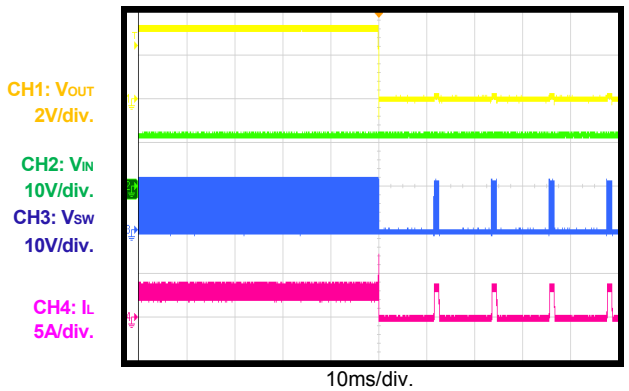
50µs/div.

Short Circuit Entry
I_{OUT} = 0A



10ms/div.

Short Circuit Entry
I_{OUT} = 3A



10ms/div.

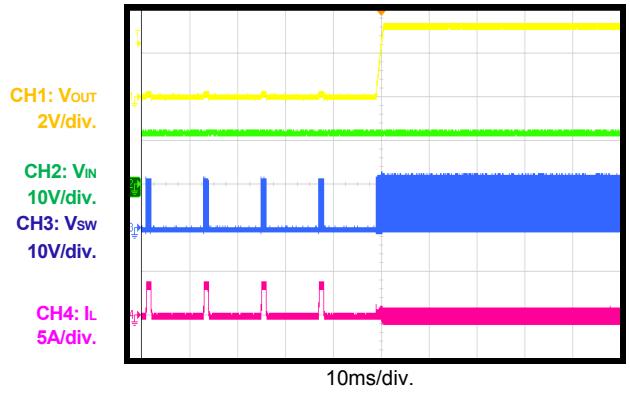
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

Performance waveforms are tested on the evaluation board of the Design Example section.
V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

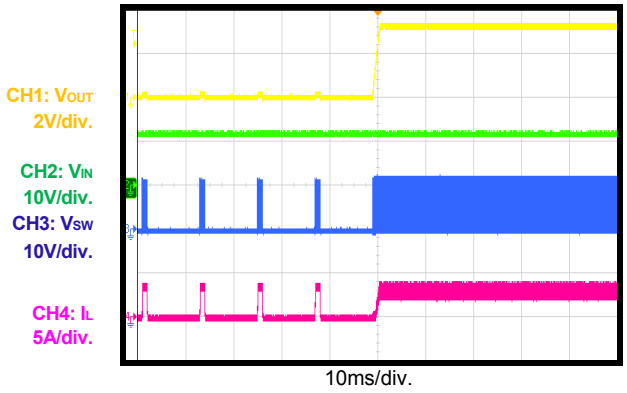
Short Circuit Recovery

I_{OUT} = 0A

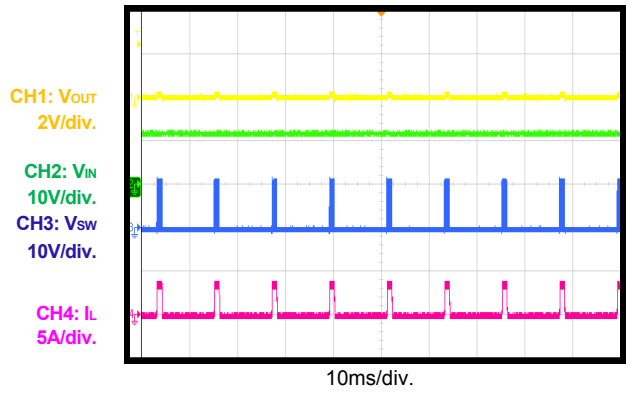


Short Circuit Recovery

I_{OUT} = 3A

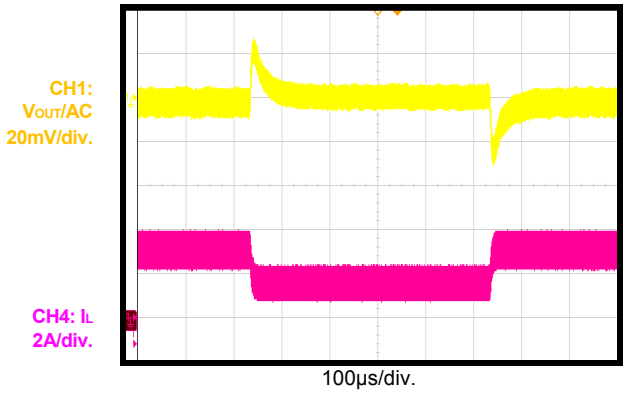


Short Circuit Steady State



Transient Response

I_{OUT} = 1.5A to 3A, 800mA/µs



MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

FUNCTIONAL BLOCK DIAGRAM

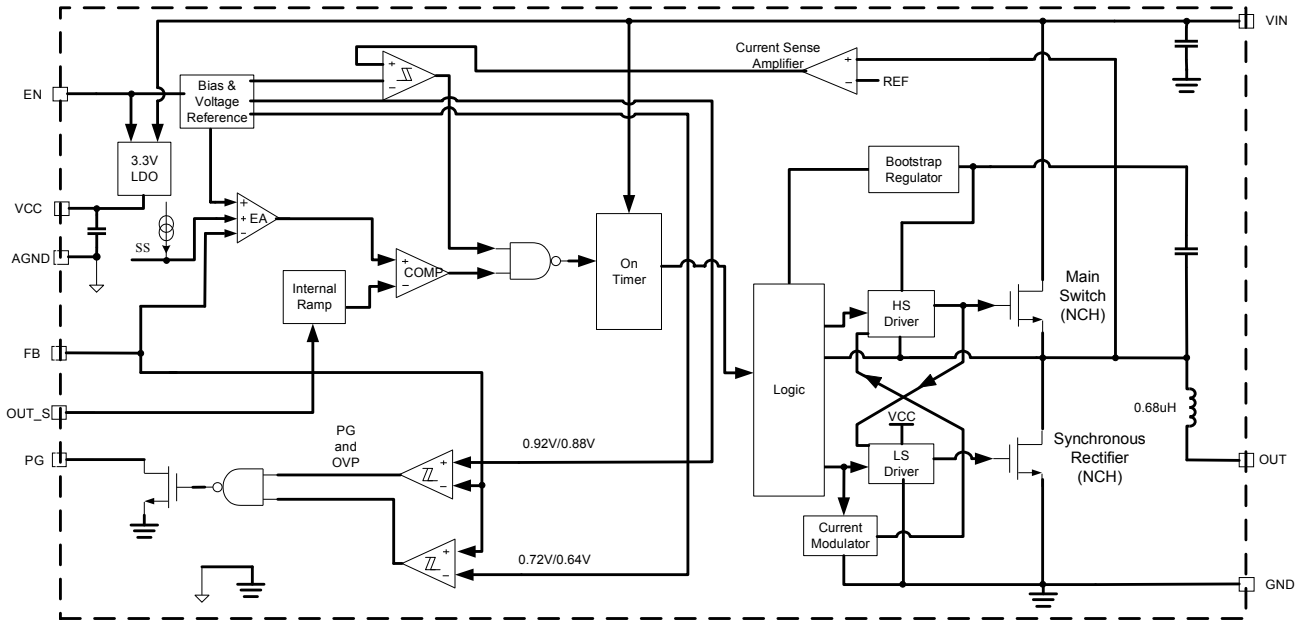


Figure 1: Functional Block Diagram

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

OPERATION

PWM Operation

The MPM3632S is a fully-integrated, synchronous, rectified, forced CCM mode, step-down switch mode converter. Constant-on-time (COT) control provides fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) turns on if the feedback voltage (V_{FB}) drops below the reference voltage (V_{REF}) due to insufficient output voltage. The output voltage and input voltage determine the on period to ensure the switching frequency stays constant over the input voltage range.

After the on period elapses, the HS-FET turns off. It turns on again when V_{FB} drops below V_{REF}. This repetitive operation regulates the output voltage. The integrated low-side MOSFET (LS-FET) turns on when the HS-FET off to minimize the conduction loss. There is a dead short between input and GND if the HS-FET and LS-FET turn on simultaneously This is called shoot-through. To avoid shoot-through, a dead time (DT) is internally generated when the HS-FET is off and the LS-FET is on, or when the LS-FET is off and the HS-FET is on.

An internal compensation is applied for COT control to further stabilize the device. When ceramic capacitors are used as output capacitors, this internal compensation then improves the jitter performance without affecting the line or load regulation.

Regular-Load Operation

Continuous-conduction mode (CCM) is when the output current is high and the inductor current is above 0A. Figure 2 shows CCM operation. When V_{FB} is below V_{REF} - V_{DC_ERROR}, the HS-FET turns on for a fixed interval that is set by an internal one-shot on-timer. When the HS-FET turns off, the LS-FET turns on until the next period.

In CCM, the switching frequency is constant and it is also called PWM operation.

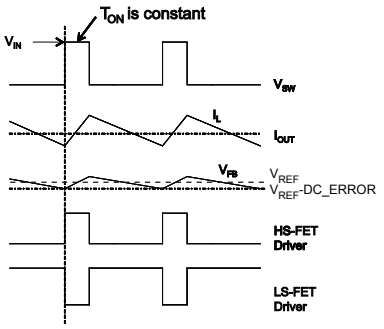


Figure 2: Heavy Load Operation

DC Auto Tune Loop

The MPM3632S applies a DC auto-tune loop to balance the DC error between V_{FB} and V_{REF}. It adjusts the comparator input-REF to make V_{FB} follow V_{REF}. This is a slow loop that improves load and line regulation without affecting the transient performance. Figure 3 shows the relationship between V_{FB}, V_{REF}, and REF.

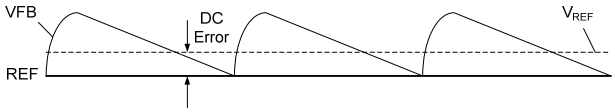


Figure 3: DC Auto-Tune Loop Operation

Internal Regulator

A 3.3V internal regulator powers most of the internal circuitries. When EN is high, this regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} exceeds 3.3V, the output of the regulator is in full regulation. When V_{IN} is below 3.3V, the output voltage decreases and follows the input voltage.

Enable Control

EN is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn it off. The EN pin is a high-voltage input node, so connect the EN pin to the input to set auto startup. The EN pin can support an 18V input voltage.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The device's UVLO comparator monitors the voltage of VIN pin. The UVLO rising threshold is about 3.6V, and its falling threshold is 3.1V.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

Soft Start

Soft start prevents the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage (V_{SS}) that ramps up from 0V to 3.3V. When V_{SS} is lower than V_{REF}, the error amplifier uses V_{SS} as the reference. When V_{SS} is higher than V_{REF}, the error amplifier uses V_{REF} as the reference.

Over-Current Protection and Hiccup

The device has cycle-by-cycle over-current limiting control. The current-limit circuit employs a "valley" current-sensing algorithm. The part uses the $R_{DS(ON)}$ of the low-side MOSFET to sense the current. If the current-sense signal exceeds the current-limit threshold, the PWM does not initiate a new cycle.

The trip level is fixed internally. The inductor current is monitored by the voltage between the GND pin and the SW pin. GND is used as the positive current sensing node, so connect GND to the source terminal of the bottom MOSFET.

Since this value is monitored while the high-side MOSFET is off and the low-side MOSFET is on, the over-current (OC) trip level sets the valley level of the inductor current. The load current at over-current threshold (I_{OC}) can be calculated with Equation (1):

$$I_{OC} = I_limit + \frac{\Delta I_{inductor}}{2} \quad (1)$$

In an over-current condition, the current to the load exceeds the current to the output capacitor, and the output voltage falls off. The output voltage drops until V_{FB} falls below the under-voltage (UV) threshold, which is typically below 50% of V_{REF}. Once UV triggers, the device enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground, and it greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator. The device exits the hiccup mode when the over-current condition is removed.

Over Voltage Protection (OVP)

The MPM3632S monitors the feedback voltage (V_{FB}) to detect an over-voltage condition. When V_{FB} exceeds 115% of the reference voltage (V_{REF}), the controller enters a dynamic regulation period. During this period, the IC turns the low-side MOSFET on until a -2.5A negative current limit triggers and turns off the low-side MOSFET for a fixed delay time if the OV conditions persists. This discharges the output and maintains it within the normal range. The part exits dynamic regulation when V_{FB} falls below 110% of V_{REF}.

If the VOUT pin's absolute voltage exceeds the 6V threshold, the part enters dynamic regulation mode to discharge the output voltage.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperatures exceeds 150°C, it shuts down the whole chip. When the temperature falls below its lower threshold, (about 130°C), the chip enables again.

PG Indicator

The PG pin is an open-drain output. When V_{FB} is above the UV threshold and below the OV threshold, EN is high, VIN is OK, and there is no over-temperature condition, this pin is set to high impedance. Otherwise this pin is pulled down to GND. When an external resistor pulls it up to a reliable voltage, this pin can be used for the digital interface.

Floating Driver and Bootstrap Charging

Figure 4 shows an internal bootstrap charging circuit. An internal bootstrap capacitor powers the floating power of the MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.3V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1 and C2. If V_{IN} - V_{SW} exceeds 3.3V, U1 regulates M1 to maintain a 3.3V BST voltage across C4.

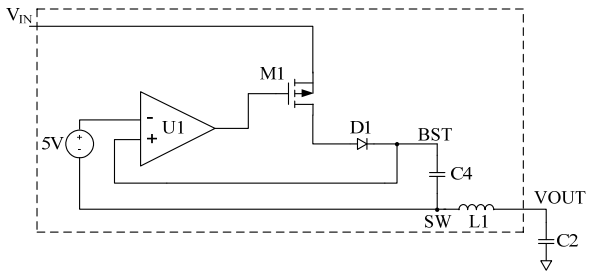


Figure 4: Internal Bootstrap Charging Circuit

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage. Choose the R1 resistance. R2 can be estimated with Equation (2):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1} \quad (2)$$

Figure 5 shows the feedback circuit.

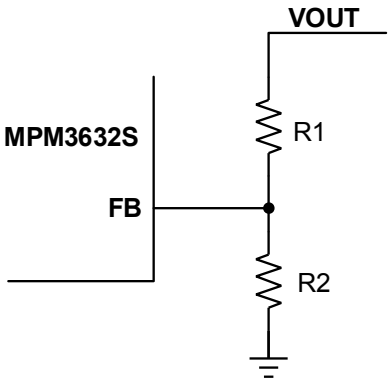


Figure 5: Feedback Network

where V_o is the output voltage. The output voltage feedback gain is determined by:

$$G_{FB} = \frac{R_2}{R_1 + R_2} \quad (3)$$

To stabilize the system and optimize the load transient response, place a feed-forward capacitor (C_{FF}) in parallel with R1. Table 1 shows the values of feedback resistors and feedforward capacitors for common output voltages.

Table 1: Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	C_{FF} (pF)	C_{OUT} (µF)
5	47	8.87	39	22
3.3	47	15	39	22
2.5	47	22	39	22
1.8	47	37.4	22	22
1.5	47	53.6	22	22
1.2	47	93.1	22	22
1	47	187	22	22

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous and requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 10µF capacitor suffices.

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be calculated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT} shown in Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, place a small, high-quality ceramic capacitor (e.g. 0.1µF) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent an excessive voltage ripple at the input. The input voltage ripple caused by the capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_{SW} \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Output Capacitor

An output capacitor (C2) is required to maintain the DC output voltage. Low ESR ceramic capacitors can be used with the device to maintain a low output ripple. A 22µF output ceramic capacitor is sufficient for most cases.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is caused mainly by the capacitance. For simplification, the output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_{SW}^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

With tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be calculated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (8)$$

Where L_1 is a 0.68μH, integrated inductor.

The characteristics of the output capacitor also affect the stability of the regulation system.

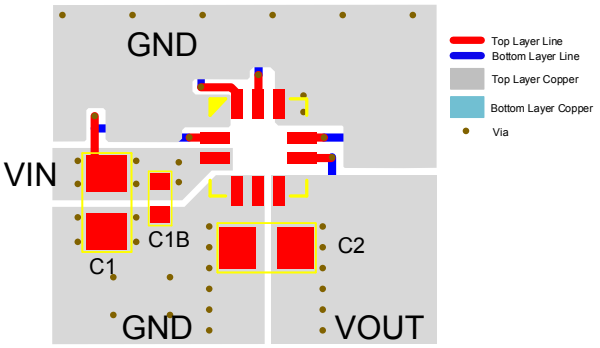
PCB Layout Guidelines (7)

Efficient PCB layout is critical for stable operation. For the best results, see Figure 6 and follow the guidelines below:

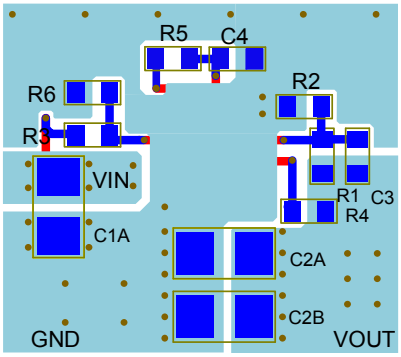
1. Keep the connection of the input ground and GND as short and wide as possible.
2. Ensure that all feedback connections are short and direct.
3. Place the feedback resistors as close as to the chip as possible.
4. Route sensitive analog areas such as FB away from SW.
5. Place enough vias around the chip to improve thermal performance.

Notes:

7) The recommended layout is based on Figure 6.



Top Layer



Bottom Layer

Figure 6: Recommended Layout

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

TYPICAL APPLICATION CIRCUIT

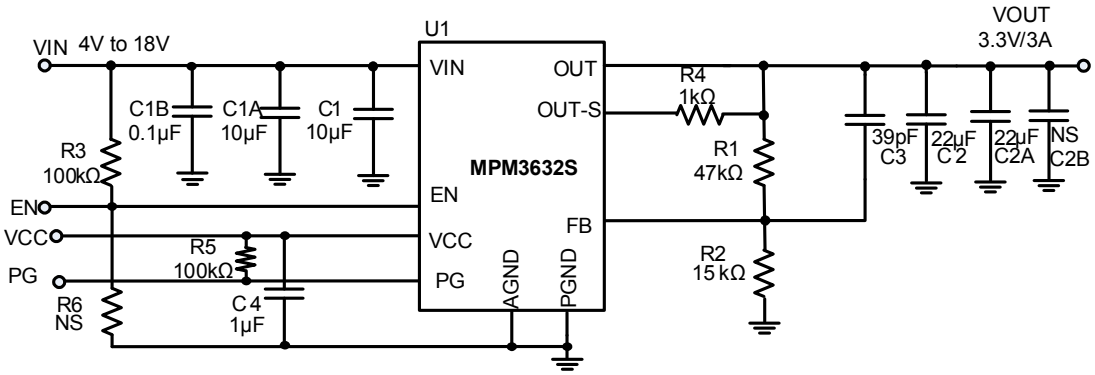
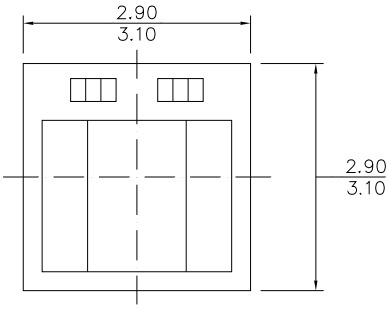


Figure 8: Typical Application Circuit

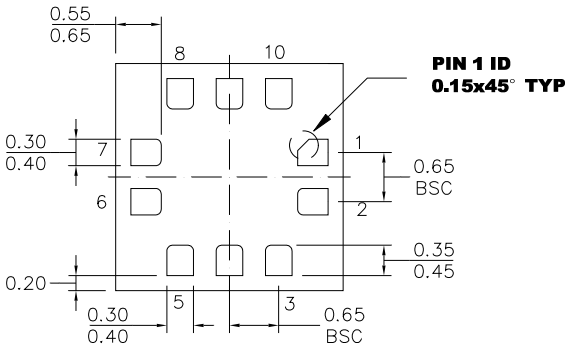
MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

PACKAGE INFORMATION

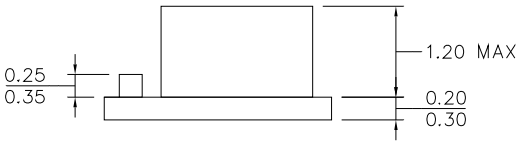
EC LGA-10 (3mmx3mmx1.45mm)



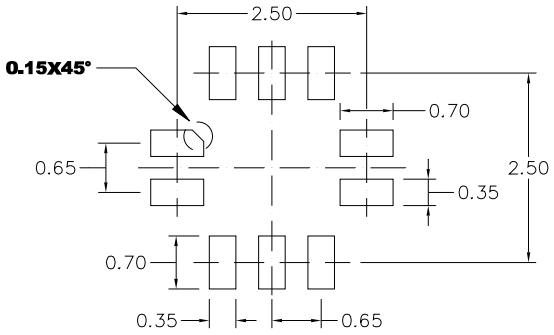
TOP VIEW



BOTTOM VIEW



SIDE VIEW



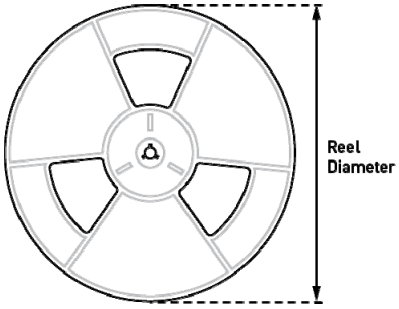
RECOMMENDED LAND PATTERN

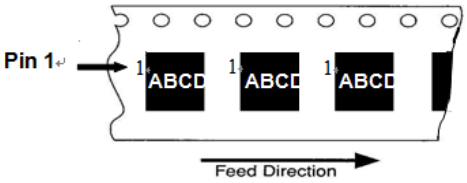
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE x.xx MILLIMETERS MAX.
3) JEDEC REFERENCE IS xxx.
4) DRAWING IS NOT TO SCALE.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.

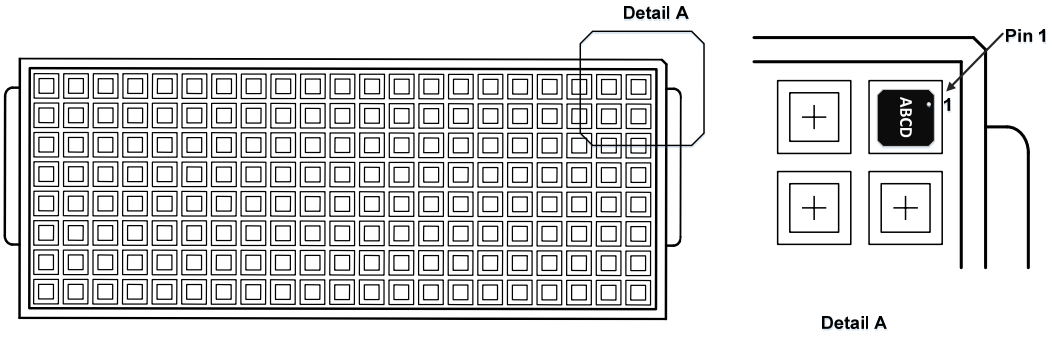
CARRIER INFORMATION 1





Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3632SGPQ-Z	EC LGA (3mmx3mmx1.45mm)	2500	N/A	N/A	13in.	12mm	8mm

CARRIER INFORMATION 2



Note:

This is a schematic diagram of Tray. Different packages correspond to different trays with different length, width and height

Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MPM3632SGPQ	EC LGA (3mmx3mmx1.45mm)	N/A	N/A	490	N/A	N/A	N/A

Notice: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating MPS products into any application. MPS will not assume any legal responsibility for any said applications.

MPS Proprietary Information. Patent Protected. Unauthorized Photocopy and Duplication Prohibited.
© 2020 MPS. All Rights Reserved.