

Utility-band BPSK 6.0 kbps PLM PICtail™ Plus Daughter Board User's Guide

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Table of Contents

Chapter 1. Introduction
1.1 Overview 9
1.2 Board Setup 10
Chapter 2. Hardware
2.1 Functional Overview 15
2.2 Hardware Components 17
Chapter 3. Demonstration
3.1 Software and Tools 19
3.2 Demonstration Applications 25
Appendix A. Board Layout and Schematics
A.1 HV Adapter Board Layout and Schematic 29
A.2 Daughter Board Layout and Schematics 30
Appendix B. Bill of Materials (BOM)
Appendix C. Troubleshooting Guide
C.1 Frequently asked questions 35

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NOTES:

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This preface contains general information that will be useful to know before using the Utility-band BPSK 6.0 kbps PLM PICtail™ Plus Daughter Board. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Recommended Reading
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

- **Chapter 1. "Introduction"** provides a brief overview of the daughter board, highlighting its features and uses.
- **Chapter 2. "Hardware"** provides the hardware descriptions of the daughter board.
- **Chapter 3. "Demonstration"** describes simple applications that demonstrate the capabilities of the Utility-band BPSK 6.0 kbps PLM PICtail™ Plus Daughter Board.
- **Appendix A. "Board Layout and Schematics"** provides a block diagram, board layouts, and detailed schematics of the daughter board and the HV adapter.
- **Appendix B. "Bill of Materials (BOM)"** provides a Bill of Materials for the daughter board and the HV adapter.
- **Appendix C. "Troubleshooting Guide"** discusses common operational issues and methods to resolve them.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
`Plain Courier New`	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`C:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants (in source code)	`0xFF, 'A'`
`Italic Courier New`	A variable argument	*`file.o`*, where `file` can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options] file [options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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RECOMMENDED READING

This user's guide describes how to use the Utility-band BPSK 6.0 kbps PLM PICtail™ Plus Daughter Board. The following Microchip documents are available from the Microchip web site (www.microchip.com), and are recommended as supplemental reference resources.

Explorer 16 Development Board User's Guide (DS51589)

This development board provides a low-cost, modular development system for Microchip's line of 16-bit dsPIC33F Digital Signal Controller (DSC) families, and 16-bit Microcontrollers (MCU) including the PIC24F and PIC24H.

MPLAB® C Compiler for PIC24 MCUs and dsPIC® DSCs User's Guide (DS51288)

This document describes the features of the optimizing C compiler, including how it works with the assembler and linker. The assembler and linker are discussed in detail in the *"MPLAB® Assembler, Linker and Utilities for PIC24 MCUs and dsPIC® DSCs User's Guide"* (DS51317).

dsPIC33F/PIC24H Family Reference Manual and dsPIC33F Family Data Sheets

For information on dsPIC33F DSC device functionality, refer to the applicable family reference manual section and product data sheets.

MPLAB® IDE User's Guide (DS51519)

Consult this document for more information pertaining to the installation and implementation of the MPLAB IDE software, as well as the MPLAB Editor and MPLAB SIM Simulator software that are included with it.

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listings
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The Development Systems product group categories are:

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- **Emulators** – The latest information on the Microchip MPLAB REAL ICE™ in-circuit emulator.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debugger, MPLAB ICD 3.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB SIM simulator, MPLAB IDE Project Manager and general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include the MPLAB PM3 device programmer and the PICkit™ 3 development programmers.

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- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the web site at:

http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revision A (August 2011)

This is the initial release of the Utility-band BPSK 6.0 kbps PLM PICtail™ Plus Daughter Board User's Guide.

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Chapter 1. Introduction

Thank you for purchasing Microchip Technology's Utility-band BPSK 6.0 kbps PLM PICtail™ Plus Daughter Board. This daughter board provides a low-cost solution for implementing a Power Line Modem (PLM) using the Microchip Explorer 16 Development Board.

The daughter board is used with the Explorer 16 Development Board to demonstrate a software-based PLM implementing the Binary Phase Shift Keying (BPSK) modulation technique.

This chapter introduces the daughter board and provides an overview of its features. Topics covered include:

- Overview
- Board Setup

1.1 OVERVIEW

A PLM, also referred to as a Power Line Communication (PLC) modem, uses the existing power lines to provide a cost-effective communication medium. This technology can be used for a wide range of applications including, but not limited to, Automated Meter Reading (AMR), energy consumption monitoring of individual appliances, and lighting, heating, and solar applications. Data rate and robustness of a power line communication link are the main parameters that decide its application spectrum.

The Utility-band BPSK 6.0 kbps PLM PICtail™ Plus Daughter Board incorporates Analog Front End (AFE) circuitry, which is required to implement a software-based modem, using the dsPIC33F Digital Signal Controller (DSC) device on the Explorer 16 Development Board. The daughter board fits into the expansion slot on the Explorer 16 Development Board. A HV adapter cable (included in the package) interfaces the daughter board to the power line. The HV adapter cable incorporates the circuitry required to provide noise-filtering and isolation from the power line. The daughter board and the HV adapter cable are designed to operate at a carrier frequency of 72 kHz (CENELEC-A band).

WARNING

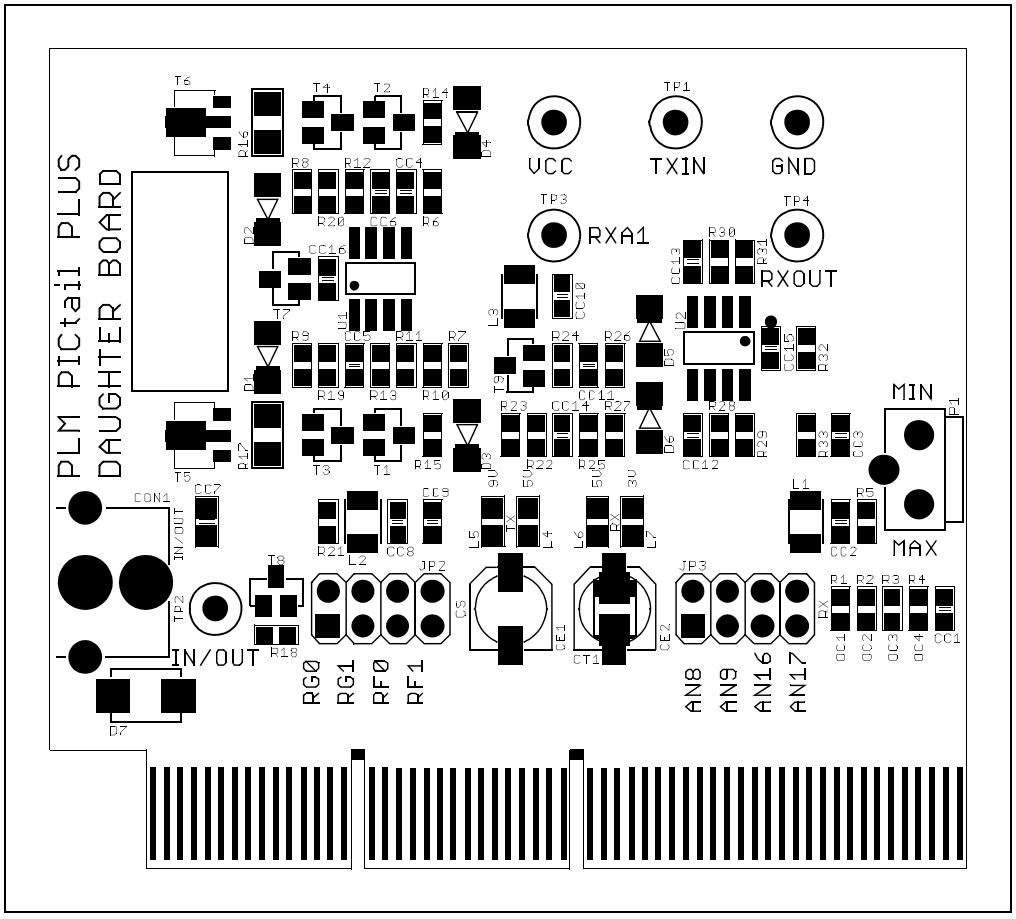
SHOCK HAZARD – Do not open the HV adapter cable enclosure.
Failure to heed this warning could result in bodily harm.

The daughter board does not implement any particular modulation technique. Software on the dsPIC33F DSC device generates 4-channel PWM output, which when summed-up and filtered suitably by the daughter board circuitry, forms an approximated sine wave. This approximated sine wave is modulated in the software using the BPSK modulation technique by controlling the PWM channels. On the receive path, the modulated signal on the power line is filtered and amplified by the daughter board before being fed to the ADC input of the dsPIC33F DSC device. The ADC module on the dsPIC33F DSC device converts this received signal into the digital domain where further filtering and demodulation is performed in software to recover the data.

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The Utility-band BPSK 6.0 kbps PLM PICtail™ Plus Daughter Board is shown in Figure 1-1. Refer to **2.2 "Hardware Components"** for detailed information on the board components.

FIGURE 1-1: UTILITY-BAND BPSK 6.0 kbps PLM PICtail™ PLUS DAUGHTER BOARD



1.2 BOARD SETUP

Figure 1-2 illustrates the setup of the daughter board with the Explorer 16 Development Board. The dsPIC33F Plug-in Module (PIM) and the 9V power supply are plugged into the Explorer 16 Development Board.

Note: If you want to debug or program the software on the dsPIC33F DSC device, the MPLAB® REAL ICE™ in-circuit emulator or ICD3 or PICkit3 should be connected to the Explorer 16 Development Board.

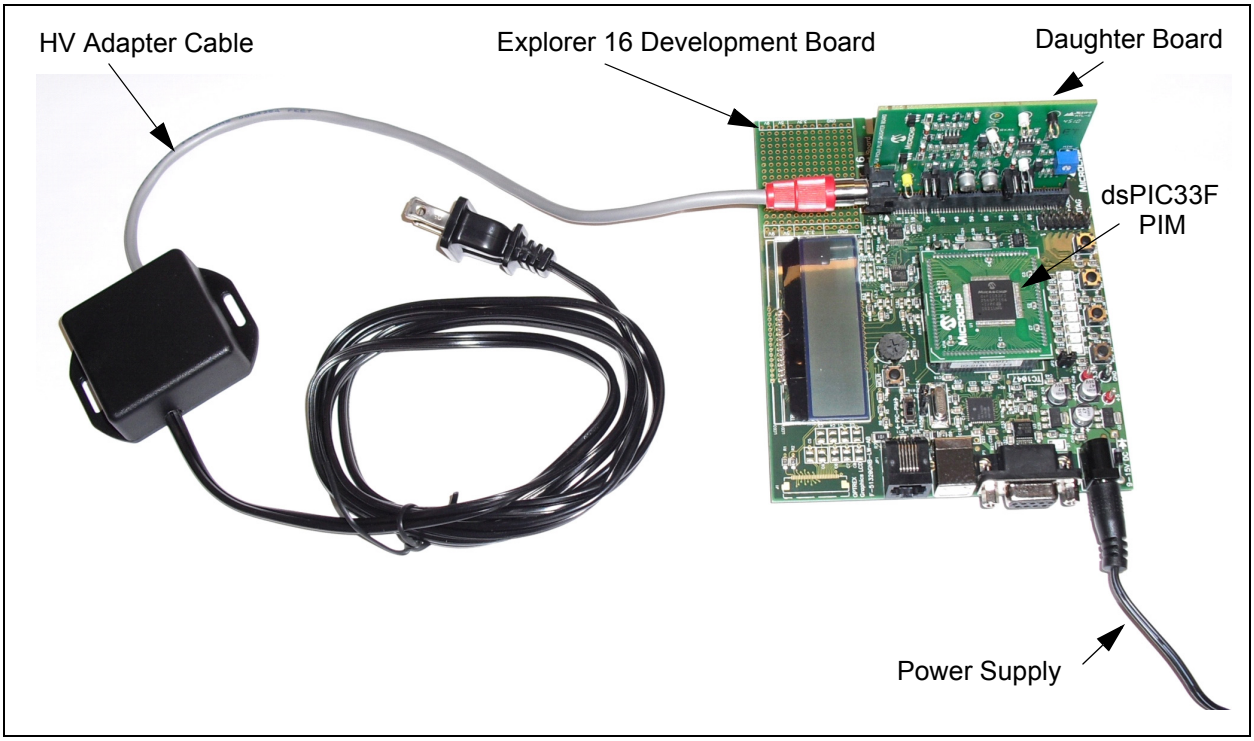
The daughter board is plugged into the PICtail slot of the Explorer 16 Development Board. The RCA jack of the HV adapter cable is connected to the daughter board. The AC end of the HV adapter cable is plugged into a mains power outlet. The daughter board is compatible with 110V/60 Hz mains supply and the 220V/50 Hz mains supply.

WARNING

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FIGURE 1-2: BOARD SETUP

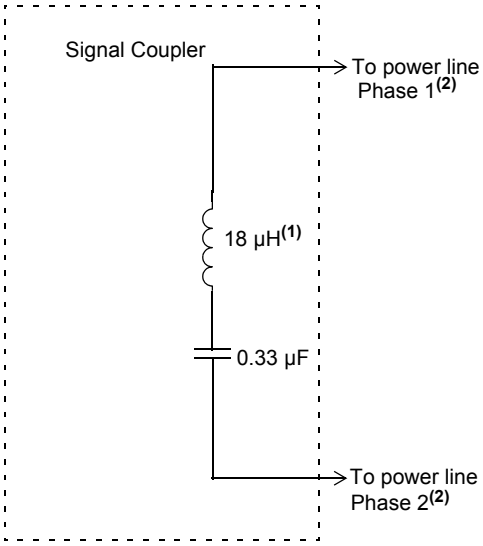


To summarize, following are the items that will be required to evaluate the two daughter boards included in the box:

- Two Explorer 16 Development boards (DM240001)
- Two 9V Power Supplies (AC002014)
- One REAL ICE (DV244005)/ICD3 (DV164035)/PICkit 3 (PG164130)

It is important to understand that some countries have multi-phase power supplies within buildings. In this case, connecting daughter boards to power outlets on different phases may result in partial or total loss of the communication link. A signal coupler device will be required to communicate across different phases of the power supply. A typical signal coupler device consists of a high voltage rated capacitor, optionally in series with an inductor, connected across the two phases of the power supply as shown in Figure 1-4. The capacitor used in the coupler should be rated to handle the instantaneous voltage between the two phases. Using an X-2 or X-1 rating capacitor is highly recommended.

FIGURE 1-3: SIGNAL COUPLER DEVICE



Note 1: Optional.

2: Phases can be interchanged.

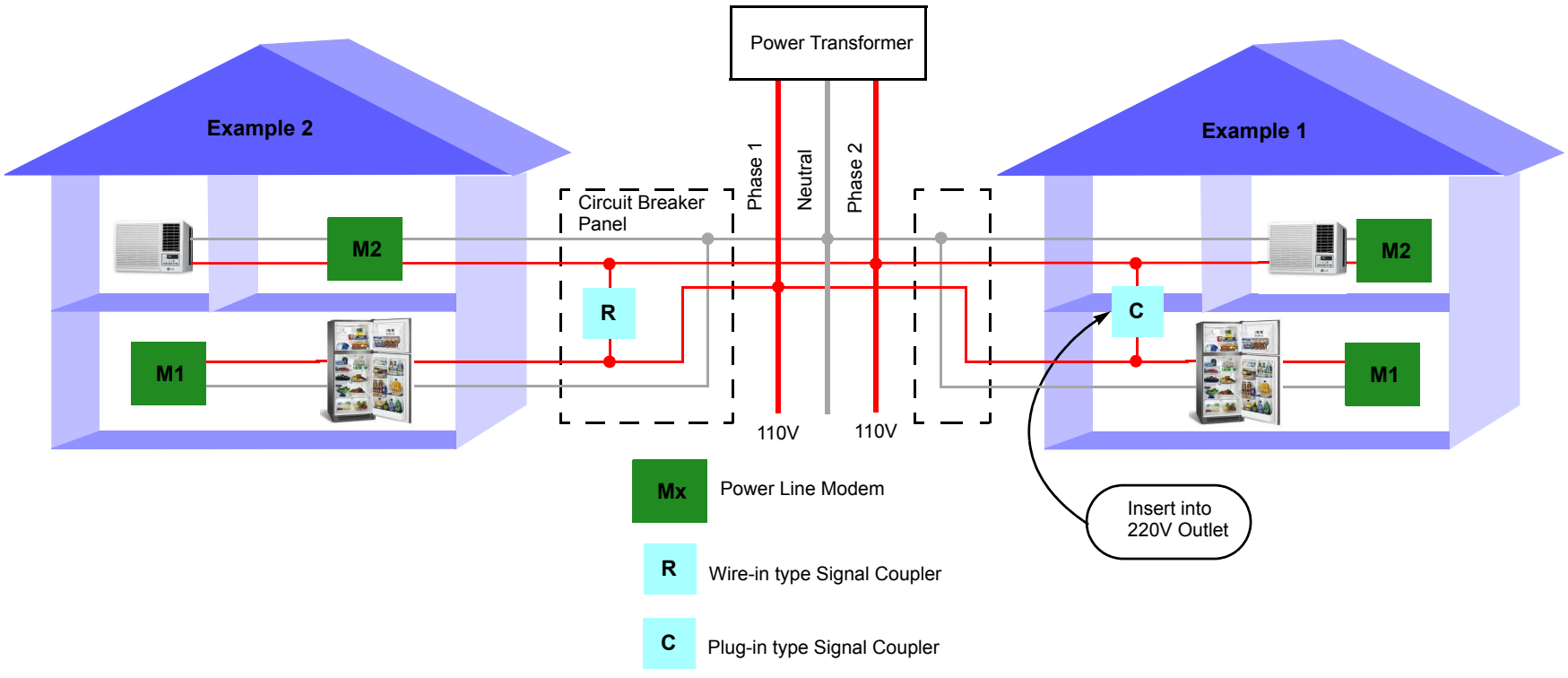
For domestic applications a signal coupler, such as Smarthome™ SignaLinc Model-4816B2, can be plugged into the nearest 220V outlet (typically used for heaters and dryers) as illustrated by Example 1 in Figure 1-4. For application scenarios where a cross-phase 220V outlet is not available, a wire-in type of phase coupler device, such as Smarthome™ SignaLinc V2 Passive Coupler, will have to be used at the circuit breaker panel as illustrated by Example 2 in Figure 1-4.

WARNING

SHOCK HAZARD – The signal coupler might be charged to the line voltage even after it is disconnected from the power line. Please discharge the capacitor by shorting the signal coupler terminals before handling or disassembling the signal coupler.

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FIGURE 1-4: DUAL-PHASE POWER SUPPLY EXAMPLES



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NOTES:

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Chapter 2. Hardware

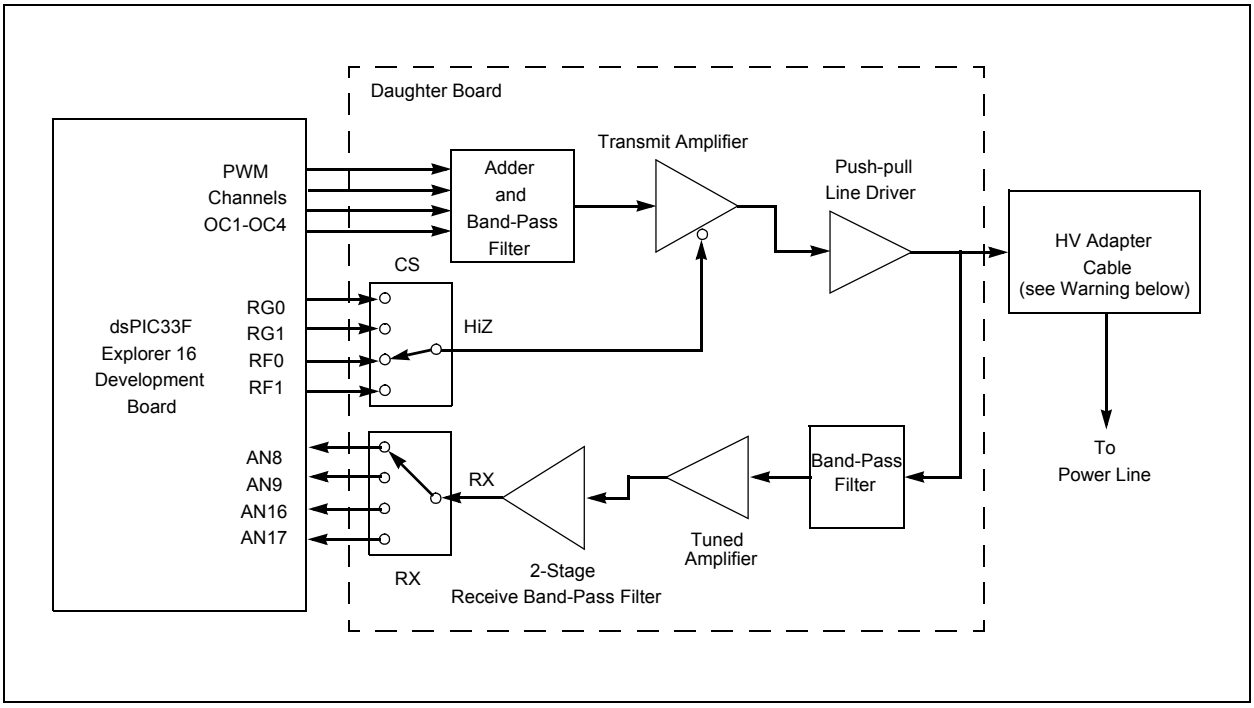
This chapter provides a functional overview of the daughter board and identifies its major hardware components. Topics covered include:

- Functional Overview
- Hardware Components

2.1 FUNCTIONAL OVERVIEW

A block diagram illustrating the functional operation of the daughter board is shown in Figure 2-1.

FIGURE 2-1: UTILITY-BAND BPSK 6.0 kbps PLM PICtail™ PLUS DAUGHTER BOARD BLOCK DIAGRAM



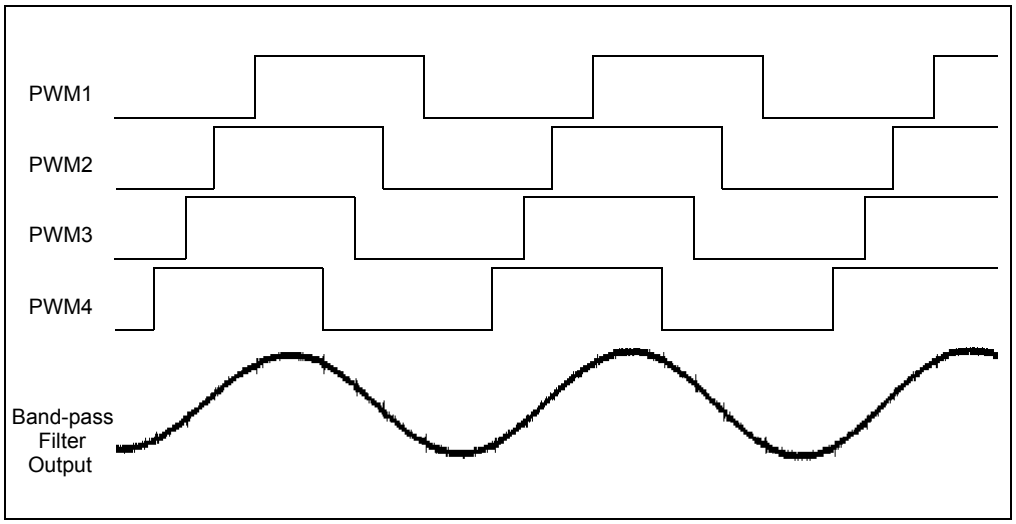
WARNING

SHOCK HAZARD – Do not open the HV adapter cable enclosure.
Failure to heed this warning could result in bodily harm.

2.1.1 Transmit Path

The daughter board utilizes four PWM channels to generate an approximated sine wave. The PWM channels are shifted in phase such that a sum of their instantaneous amplitude resembles a stepped sine wave. By filtering this stepped sine wave using a band-pass filter, a relatively clean sine wave is obtained, as shown in Figure 2-2. The amount of filtering required is dependent on the number of PWM channels. Using higher number of PWM channels will require less filtering.

FIGURE 2-2: PWM-BASED ANALOG SIGNAL GENERATION



After the approximated sine wave is obtained, it is amplified by the MCP6283 Op amp. The Chip Select pin of this Op amp is used to implement flow-control. By asserting the HiZ pin, the transmit amplifier is enabled, thus enabling the transmission path. This HiZ pin can be configured on RG0/ RG1/RF0/RF1 using the jumper, JP2.

The output of this transmit amplifier is fed to the line driver circuit implemented using transistors in a push-pull configuration. The line driver output is then coupled into the power line through the HV adapter cable.

2.1.2 Receive Path

The modulated signal on the power line is received by the HV adapter cable and is passed through an LC band-pass filter to filter out the noise and interference. This filtered signal is then fed to the tuned amplifier, which is implemented using a transistor amplifier in a common-emitter configuration. This amplified signal is then filtered using a high-gain 2-stage active band-pass filter designed around the MCP6282 Op amp. The output of this filter is then fed to the Analog-to-Digital Converter (ADC) input of the dsPIC33F DSC device on the Explorer 16 Development Board. The ADC input pins, AN8/AN9/AN16/AN17, can be selected by appropriately setting the jumper, JP3.

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2.2 HARDWARE COMPONENTS

Figure 2-3 identifies the key hardware components of the daughter board. Table 2-1 lists the descriptions for each hardware component.

FIGURE 2-3: UTILITY-BAND BPSK 6.0 kbps PLM PICtail™ PLUS DAUGHTER BOARD HARDWARE COMPONENTS

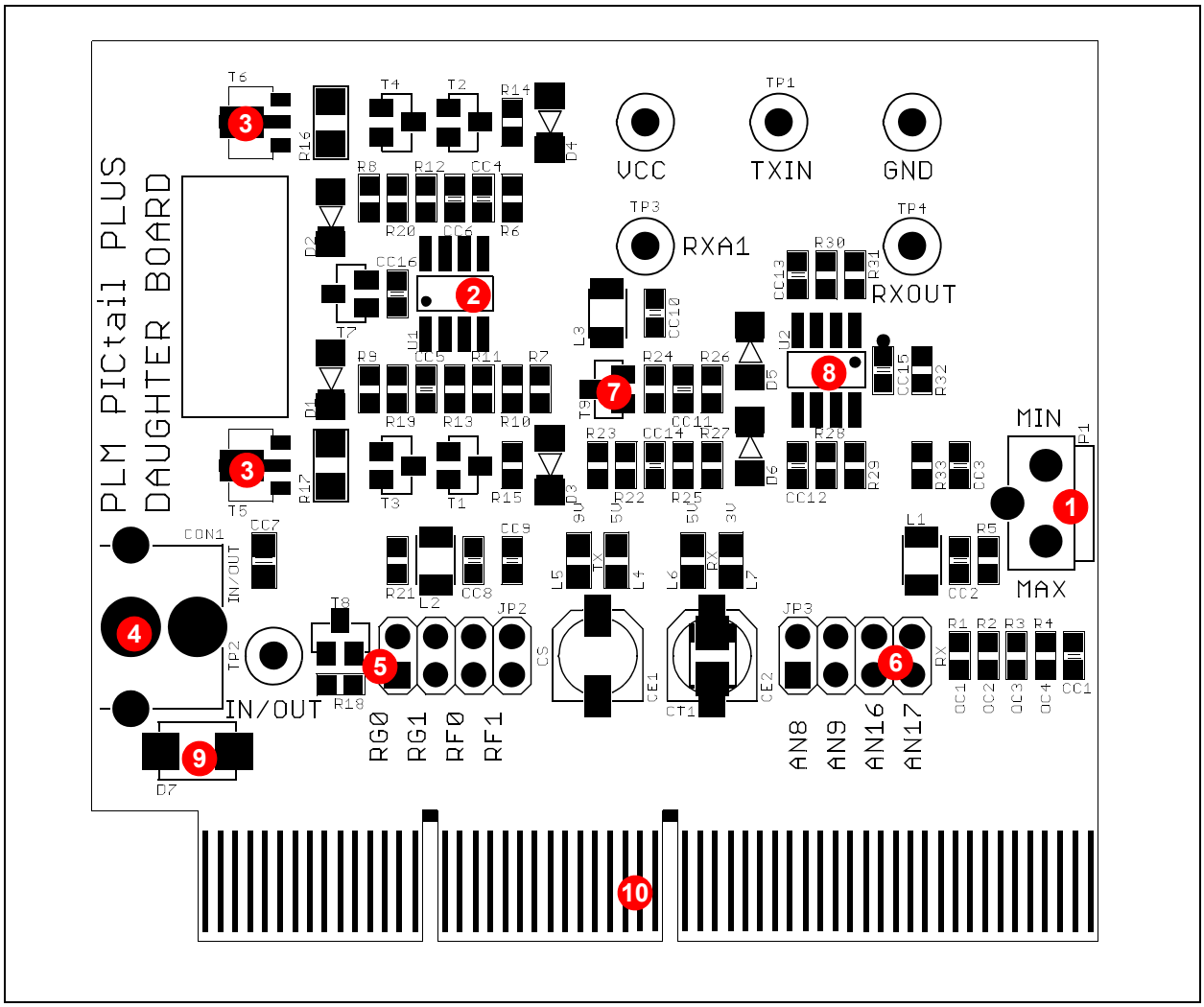


TABLE 2-1: UTILITY-BAND BPSK 6.0 kbps PLM PICtail™ PLUS DAUGHTER BOARD HARDWARE COMPONENTS

Item No.	Description	Item No.	Description
1	Transmit-level set potentiometer (P1)	6	ADC input select jumper (JP3)
2	Transmit amplifier (U1A)	7	Tuned amplifier transistor (T9)
3	Output transistors (T5, T6)	8	Receive Band-pass filter (U2A, U2B)
4	RCA connector (CON1)	9	Transient Voltage Suppressor (D7)
5	HiZ select jumper (JP2)	10	Explorer 16 PICtail™ connector (CON2)

2.2.1 Transmit-level Set Potentiometer (P1)

This 100 kΩ potentiometer sets the average signal output amplitude transmitted from the daughter board. Refer to **A.2 "Daughter Board Layout and Schematics"** for the daughter board schematics.

2.2.2 Transmit Amplifier (U1A)

The transmit amplifier is used to implement flow control on the transmit path.

2.2.3 Output Transistors (T5, T6)

Output transistors are implemented in the push-pull configuration to amplify the transmit signal before coupling the signal into the HV adapter cable.

Note: The output transistors should have good thermal contact with a large copper plane on the PCB to dissipate heat.

2.2.4 RCA Connector (CON1)

The RCA connector is used to connect the daughter board to the HV adapter cable.

2.2.5 HiZ Select Jumper (JP2)

This jumper is used to select the dsPIC33F DSC device pin used for switching the transmit amplifier. Changing this jumper setting will require appropriate changes in the software. See Figure A-5 for the schematic of the jumper connections.

2.2.6 ADC Input Select Jumper (JP3)

This jumper is used to select the dsPIC33F DSC device analog pin required to sample the received signal from the power line. Changing this jumper setting will require appropriate changes in the software. See Figure A-5 for the schematic of the jumper connections.

2.2.7 Tuned Amplifier Transistor (T9)

This transistor configured in the common-emitter configuration is used to implement a tuned amplifier on the receive path.

2.2.8 Receive Band-pass Filter (U2A, U2B)

This 2-stage band-pass filter provides high gain to the received signal while filtering out power line noises and interference signals. The circuit is essentially a high-pass filter with a very high gain. The gain bandwidth product limits the higher frequencies (low-pass response), thereby resulting in a band-pass filter.

2.2.9 Transient Voltage Suppressor (D7)

The transient voltage suppressor is used to protect the daughter board from high voltage transients on the power line.

2.2.10 Explorer 16 Development Board PICtail™ Connector (CON2)

The daughter board connects to the Explorer 16 Development Board using edge connector J3. The daughter board uses the following signals on the Explorer 16 Development Board PICtail Plus connector:

- +3.3V power
- +5V power
- +9V power
- Ground
- dsPIC33F DSC device Output Compare module signals (OC1-OC4)
- dsPIC33F DSC device ADC module input signals (AN8/AN9/AN16/AN17)
- One GPIO for HiZ signal (RG0/RG1/RF0/RF1).

Note: The source code provided on the Microchip web site uses the AN8 pin for ADC input and the RF0 pin for the HiZ signal. Please ensure that jumpers JP2 and JP3 are populated according to this configuration. Using other jumper configurations will require suitable modifications in the source code.

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Chapter 3. Demonstration

This chapter describes simple applications that demonstrate the capabilities of the Utility-band BPSK 6.0 kbps PLM PICtail™ Plus Daughter Board. Topics covered include:

- Software and Tools
- Demonstration Applications

3.1 SOFTWARE AND TOOLS

For free demonstration source code and more information, please visit the related web page at www.microchip.com/powerline. From the landing page, select **Utility-band BPSK 6.0 kbps PLM PICtail™ Plus Daughter Board**. In the downloads section, select a demonstration application to download an archive file that contains the related demonstration source files.

The MPLAB® Integrated Development Environment (IDE) should be installed prior to using the daughter board for application development. While MPLAB IDE provides the assembler tools for development, demonstration applications are written in the C language and require a C compiler to be installed.

Both the MPLAB IDE and C Compiler are available for download from www.microchip.com/MPLAB and www.microchip.com/compilers, respectively.

3.1.1 Running the Demonstration Applications

After downloading the desired demonstration application from the web site, use the following steps to compile and run the demonstration application:

1. Connect the hardware as described in **1.2 "Board Setup"**. For detailed instructions on setting up the Explorer 16 Development Board, refer to the *"Explorer 16 Development Board User's Guide"* (DS51589).
2. Connect the device programmer to a development computer.
3. Open the demonstration project in MPLAB IDE.
4. Verify and optionally edit the configuration files of the demonstration project. Refer to **3.1.3 "Configuration Settings"** for information regarding configuration options.
5. Build the project and program the target Explorer 16 Development Board.

Note 1:	Some demonstration applications may use different project files for successive Explorer 16 Development Boards. Please refer to **3.2 "Demonstration Applications"** for details on these applications.
2:	For detailed instructions, please refer to the readme file included in the project directory.

3.1.2 Configuration Files

Modem and application configuration has been split into several header files, each responsible for a logically separated portion of the code. Each demonstration application defines a `config.h` file that serves as a master configuration file and should include, directly or indirectly, all other configuration files. The modem and framework modules have their own main configuration files (`modem.h` and `framework.h`), normally included by the master `config.h` file. These files can be found in the `config` subdirectory of the relevant project directory.

The entire configuration of the low-level modem code has been placed into three configuration files, which can be found in the modem configuration subdirectory `modem\conf`. These configuration files are:

- `config_plm.h`: Contains options common to all modulation algorithms implemented and allows modulation scheme selection
- `config_bpsk.h`: Contains all BPSK configuration options
- `config_fec.h`: Contains the forward error correction configuration

All configuration options are extensively documented in the source code comments.

3.1.3 Configuration Settings

The following are the important configuration settings.

PLM_OE

This setting selects how the Output Enable (HiZ signal) for the transmit amplifier is asserted. This option is hardware-dependent and must be left at its default value for the daughter board provided in the kit. Possible options are:

- Drive low to enable, high impedance to disable (default)
- Drive low to enable, drive high to disable
- Drive high to enable, drive low to disable

PLM_OE_LAT

The LAT register bit of the Output Enable signal (assembler syntax). This setting must be changed only if a non-default JP2 jumper configuration is used. This setting must match the jumper setting on the daughter board.

PLM_OE_TRIS

The TRIS register bit of the Output Enable signal (assembler syntax). This must match the setting for PLM_OE_LAT.

PLM_ADC_CHNL

This setting selects the ADC input number (i.e., ANx pin). The ADC configuration is adjusted automatically. This setting must be changed only if a non-default JP3 jumper configuration is used. This setting must match jumper setting on the daughter board.

PLM_ADC_TRIS

The TRIS register bit where the selected ANx channel is located.

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PLM_FRAMING

This setting enables the low-level framing and is disabled by default. If enabled, the demodulator will seek frames with following:

- Preamble (length depends on the PLM_PRE_SIZE configuration setting)
- Start Of Frame (as set in the PLM_SOF configuration setting)
- Length (1 to 253, length, SOF and data inclusive)
- Data bytes

PLM_SOF

The Start of Frame (SOF) character. This setting is used only if low-level framing is enabled.

PLM_FEC

This setting enables the Forward Error Correction (FEC) feature. Please note that the Viterbi algorithm used for the FEC feature requires significant processing power, especially at higher code constraint lengths.

PLM_QUALITY_MEASURE

This setting enables received signal quality estimation and determines a 16-bit quality metric calculated during the initial bytes after the last byte synchronization has been found. The metric is an average value of absolute values of demodulated signal samples, taken in the instance of bit decisions during the first 16 bytes after byte synchronization has been found. A value greater then 0x7F00 means perfect quality.

PLM_LOCAL_ECHO

This setting, if enabled, allows the modem to receive its own transmissions.

PLM_DEBUG_MODE

This setting enables various debugging modes and normally should be off (set to DEBUG OFF). The other modes supported are:

- Signal Logging mode, where signal samples on various demodulation stages can be saved in a circular buffer
- Performance Measurement mode in which a GPIO pin (RG0) is set high whenever the processor is executing low-level modem code

PLM_RAM_SAVING

If enabled, this setting causes the modem code to use less RAM (reduced by a third) at a cost of consuming more processing power (2 to 4 MIPS). In case this option is enabled, a processing buffer size must also be selected by manually setting PLM_DEM_BLOCK_LEN. The smaller the buffer, the smaller the amount of RAM used; however, the performance hit is more significant.

PLM_ADC

This setting allows the selection of the ADC, in case the dsPIC33F DSC device used has more than one ADC module.

PLM_USE_DMA

This setting, if set to '1', causes the code to be compiled with DMA support. Unless there are good reasons not to (e.g., no DMA support in the selected CPU model), DMA should be used for best performance.

PLM_FC

This setting sets the carrier frequency and must not be changed while using the daughter board.

PLM_BAUD

This setting sets the modem baud rate. Available options are: 1200, 2400, 4800, and 6000 (default).

PLM_MOD_IMP

This setting selects the number of OC channels dedicated for PWM-based signal generation. Available options are:

- MOD_DDS: Directly calculates sine samples. No real-world output (for demodulator testing with internal loopback)
- MOD_PWM: Uses single OC channel (not recommended)
- MOD_2PWM: Uses two OC channels
- MOD_4PWM: Uses four OC channels (default)

PLM_SOFT_AGC

This setting enables software automatic gain control. In most cases it should be enabled. It may be disabled if the hardware gain guarantees that the working signal will always touch power supply rails. If the input signal is small and the software AGC is disabled, the Costas loop will not get enough feedback and the digital PLL may fall out of synchronization.

PLM_COSTAS_FB

This setting allows the selection of a Costas loop feedback filter implementation. The filter is actually implemented as a regulator. Three options are available:

- direct (equivalent to a P controller)
- PI
- PID

Tests show that the PI implementation brings the best performance. The proportional term is responsible for the phase synchronization, while the integral term allows tracking in the event of a constant frequency offset.

3.1.4 API Functions

The modem API allows for very low level access to the modulator and demodulator code. The application communicates with the modem on a buffer level and the modem itself does not impose any buffer sizes, frames or protocols. All of these features can be freely implemented in the higher layers. All low-level API functions are declared in the header file (`...modem\common\plm.h`) and are C-callable. The following functions are available:

`plm_mod_start()`

This function starts the modulator and configures the Output Compare channel(s), starts Timer2 and enables the Timer2 interrupt. It is mandatory to call this function before any calls to `plm_xmit()` are made.

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`plm_demod_start()`

This function starts the demodulator and configures the selected ADC channel, starts the timer that triggers ADC conversions and optionally enables a DMA channel to service the selected ADC input. Either DMA or ADC and timer interrupts get enabled. It is mandatory to call this function before any calls to `plm_recv()` are made.

`plm_demod_sync()`

This function forces a demodulator resynchronization and may be called in cases when the demodulator keeps indicating bit and byte synchronization, but higher protocol layers decide that the patterns received do not form valid frames, thus suggesting that the byte synchronization is misaligned.

`plm_xmit()`

This function transmits a buffer and is a zero copy operation, meaning the pointer passed is used to access payload bytes directly when needed. The operation is double buffered, meaning the transmission of a previous buffer may already be in progress. In all cases, the buffer passed is added to a single-entry wait queue and a TX_buffer_full (PLM_TX_BF) flag is set. As soon as transmission becomes possible, the pointer is copied to a working register and the TX_buffer_full flag is cleared. The application must not write to the buffer that was passed until the modem code has finished sending. It is possible to determine whether the buffer is still in use by examining the PLM_TX_BF and PLM_TX_ACTIVE status flags. This function must not be called unless the PLM_TX_BF flag is clear.

In addition, the application must generate a minimum of two preamble bytes before sending any data bytes. This is required to synchronize the receiver with the data transmission.

`plm_recv()`

This function fetches a received buffer. The two parameters passed are the address and the size of a new buffer to fill in. The function returns an address within a previously passed buffer, pointing to the first free location in that buffer. If the address returned is equal to the previously passed buffer start address, no data has been received between the calls. If the address returned points outside the buffer (at previous buf+size), the buffer has been fully filled and could possibly overflow, if it was allowed. A NULL pointer is returned on the very first call.

`plm_get_status()`

This function returns the following modem status flags:

- PLM_TX_ACTIVE – transmission is in progress
- PLM_TX_BF – transmit buffer is full
- PLM_BIT_SYNC – the receiver has found bit synchronization
- PLM_BYTE_SYNC – the receiver has found byte synchronization
- PLM_RESYNC – resynchronization has been requested

3.1.5 Resource Requirements

Any dsPIC33F DSC device with at least 2 Kbytes RAM, 16 Kbytes of Flash memory, four Output Compare channels (PWM), one DMA channel, and one 10/12-bit ADC input (500 ksps), can be used with the daughter board. Using dsPIC33F DSC devices without the DMA feature will result in a higher processing power requirement for the modem software, potentially starving the application of execution time. Also, using less than four Output Compare channels will result in reduced operational range and performance.

When called, the modem API functions will claim and start to use the following processor resources:

- One ADC module (default: ADC1)
- One ADC input (default: AN8)
- One optional DMA channel for the ADC servicing (default: DMA0)
- One timer to trigger the ADC conversion:
  - Timer3 when ADC1 is selected
  - Timer5 when ADC2 is selected
- One DMA interrupt vector/ADC and its triggering timer interrupt vector
- One to four Output Compare channels. Default:
  - OC1 and OC2 when PWM2 modulator is selected
  - OC1 through OC4 when PWM4 modulator is selected
- Timer2 and its interrupt vector as PWM time base
- The GPIO pin selected in the configuration for CS control (default: RF0)

The memory and MIPS requirements for the modem software for different baud rates (with DMA and RAM-saving options enabled) are listed in Table 3-1.

TABLE 3-1: MEMORY AND MIPS REQUIREMENTS FOR THE MODEM

Baud Rate	RAM (Bytes)	Flash (Bytes)	MIPS
1200	444	2709	18.4
2400	284	2709	18.4
4800	204	2709	18.6
6000	188	2709	18.7

3.1.6 Developing Custom Applications

An application template has been provided to ease the development of customized PLM applications. The application template can be downloaded from the Utility-band BPSK 6.0 kbps PLM PICtail™ Plus Daughter Board web site at: www.microchip.com/powerline.

By default, the software for the daughter board is designed to operate on a carrier frequency of 72 kHz. However, if required, the software can be modified to operate at a different carrier frequency. In this case, the following need to be taken into consideration:

- The hardware provided in the kit is designed to operate at a carrier frequency of 72 kHz. Changing the carrier frequency in software will require modifications to the hardware components, specifically the components that decide the filter cutoff frequencies
- It is necessary for the carrier frequency to be an integral multiple of the baud rate: Carrier frequency, $F_C = k * baud,\ k \in Integer$
- Lower carrier frequencies result in lower maximum possible data rates
- Carrier frequency or baud rate changes outside the combinations provided in the include file (`...\modem\bpsk\bpsk_filter.inc`) will require recalculation of digital filter coefficients
- Increasing carrier frequency increases the MIPS requirement for the modem software. For this reason, the carrier frequency must be well within the CPU's useful performance limit. The modem software requires approximately 0.234 to 0.303 MIPS/kHz of carrier frequency

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3.2 DEMONSTRATION APPLICATIONS

The five demonstration applications developed for the daughter board are described in this section. Peripherals on the Explorer 16 Development Board, such as the LCD screen, push buttons and LEDs, are used by the demonstration applications to interact with the user. In general, LED D3 indicates the transmission status, LED D5 indicates the receiver bit synchronization status, and LED D4 indicates the receiver byte synchronization status.

Table 3-2 lists the approximate memory requirements for the individual projects of each of the demo applications. The listed memory requirements are valid only when the default configuration settings are used (source codes provided on the web site are configured with default configuration settings). Changing the configuration settings may cause significant changes in the memory requirements.

TABLE 3-2: MEMORY REQUIREMENTS FOR DEMO APPLICATIONS

Demo Application	Project Name	Flash (Bytes)	RAM (Bytes)	Description
Ping Pong Demo	pingpong	6408	688	Point to point two-way communication link tester
Stream Demo	rxstream	6510	672	One-way communication link tester
	txstream	5571	396	
Sensors Demo	node	14058	1348	Single station - multiple node (sensors) demo
	station	13905	1316	
Talk Demo	talk	3408	410	Character level communication link demo
Pipe Demo	pipe	4590	1134	UART-to-UART data link
Template	template	2919	210	Template

3.2.1 Ping Pong Demonstration

This demonstration evaluates the two-way power line communication link between two development boards.

1. Program two Explorer 16 Development Boards with the same demonstration software.
2. Connect the development boards to a power line and power up the Explorer 16 Development Boards.
3. Press the S5 button on one of the Explorer 16 Development Boards, for example, board 1.

   This will cause board 1 to transmit a predetermined frame on the power line. The other board, board 2, connected to the same power line will receive this frame and check it for errors. If no errors are found, board 2 will transmit another predetermined frame on the power line. Again, board 1 will receive this frame and check it for errors. If no errors are found, board 1 will transmit another predetermined frame on the power line. This process continues as an infinite loop, pinging data frames back and forth over the power line. Meanwhile, the LCDs on the two Explorer 16 Development Boards display the following frame statistics information:

   - TX: Number of frames transmitted
   - RX: Number of frames received in total
   - ERR: Number of frames received with errors

Each frame (of 128 byte length) is composed of 16 bytes of preamble, 110 bytes of data and 2 bytes of CRC. The demonstration application has two LCD views, which can be toggled using switch S3 on the Explorer 16 Development Board:

- Frame statistics
- Application configuration (carrier frequency, modulation and baud rate)

3.2.2 Sensor Monitoring Demonstration

This demonstration implements a network protocol with framing, CRC and a network stack framework. The demonstration consists of a base station and a number of nodes. Each node measures its potentiometer state (R6 on the Explorer 16 Development Board) and sends the result to the station. The station displays the received values on the LCD screen.

1. Program one Explorer 16 Development Board with the Station software.
2. Program one or more Explorer 16 Development boards with the Node software (each node must have a unique MAC address and must know the station MAC address).
3. Connect all boards to the power line and they will automatically start to communicate.
4. Turn the potentiometer, R6, on a node board. Observe how the value is updated on the node and station LCD screens.
5. Use the S3 button to change the LCD screen contents. The LCD can display the current potentiometer state and packet statistics (frames transmitted, frames received and errors).

Debug information is sent via the serial port. The output can be observed by connecting a serial port emulator (such as HyperTerminal) to the RS-232 port of the Explorer 16 Development Board. The UART configuration for this demonstration is:

- 115200 bps
- 8-N-1
- No flow control

3.2.3 Pipe Demonstration

This demonstration implements a raw data pipe for UART-to-UART connection over the power line.

1. Connect a sender application (a PC or an embedded device) to the RS-232 port of an Explorer 16 Development Board and a receiver application to the RS-232 port of the other Explorer 16 Development Board.
2. The sender application may start transmitting data.

Data is immediately transferred over the power line and received by the receiver. Sender and receiver may change roles at runtime. One-to-many configurations are also valid.

The link is designed to appear raw and unframed to both RS-232 devices. Internally, however, simple framing is used. Its purpose is to ensure that the receiver maintains byte synchronization. Without framing it would not be practically feasible to guarantee that the receiver and transmitter are byte-aligned. A frame consists of 10 preamble characters (PRE = 0x2A), one Start of Frame character (SOF = 0x1B), a length byte, up to 64 payload bytes, and a 16-bit ITUT CRC checksum. In total there is a 14 byte overhead for each frame.

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The transmitter starts sending when there is at least one byte to send. A frame is terminated when there is no more data in the input buffer or when the 64th payload byte has been transmitted. As long as the application keeps providing data to send, the transmitter will transmit 64 byte frames. If a frame checksum is invalid, the receiver will try to resynchronize, but the frame contents will be transferred to the UART interface.

The UART configuration for this demonstration is:

- 19200 bps
- 8-N-1
- RTS/CTS flow control (hardware)

3.2.4 Stream Demonstration

This demonstration implements a unidirectional link tester to test the power line communication link.

There are two applications in this demonstration: a transmitter and a receiver. The transmitter sends a stream of frames with a constant length and payload. The receiver checks the received frames and displays statistics on the LCD and via the UART. The following statistics are available:

- TX: Number of frames transmitted in total
- RX: Number of frames received in total
- OK: Number of frames received correctly
- ERR: Number of frames received with errors
- CRC: Number of frames that had CRC errors
- PAY: Number of frames with at least one payload error
- TRU: Number of truncated frames. A frame is truncated if bit synchronization was lost before the expected number of octets were received.

Each frame (of 128 byte length) is composed of 16 bytes of preamble, 110 bytes of data and 2 bytes of CRC. The following push buttons can be used to control the demonstration application:

- S3: Next LCD view
- S6: Previous LCD view
- S4: Clear all counters

The transmitter application has two LCD views:

- Frame statistics: TX count
- Application configuration (carrier frequency, modulation and baud rate)

On reset, the transmitter sends the application configuration summary over the UART and prints an asterisk (*) symbol on every transmitted frame. After each 16 frames it prints the total number of frames transmitted so far.

The receiver application has three LCD views:

- Frame statistics: RX, OK and ERR count
- Error statistics: CRC, PAY and TRU count
- Application configuration (carrier frequency, modulation and baud rate)

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On reset, the receiver sends the application configuration summary over the UART. Then, every 5 seconds, it prints all packet statistics in a human-readable form. By increasing the debug level upon compilation, it is also possible to send detailed reports about each frame. This option is disabled by default. The detailed reports have the following format:

- −: Preamble character received
- _: Non-preamble character received out of frame
- <: Frame has started
- ?: Bad payload byte received
- #: The frame has reached the CRC fields
- !: Invalid CRC
- >: Frame has ended
- /: Frame was truncated

The UART configuration for this demonstration is:

- 115200 bps
- 8-N-1
- No flow control

3.2.5 Talk Demonstration

This demonstration implements character level communication.

1. Connect two serial port terminal emulators (such as HyperTerminal) to the RS-232 ports of a pair of Explorer 16 Development Boards.
2. Type your message in one of the terminal windows.

As soon as the Enter key is pressed (i.e., a CR character is sent), the message will be transmitted via the modem interface, preceded by an 8-byte synchronization preamble, and should be received by the second device and printed in the other terminal window. The message buffer size is 80 characters. If the CR character does not appear, the message will be transmitted after the 80th character has been received. Except for the CR character, no other characters have any special meaning and everything that appears at the serial port input, will eventually get transmitted via the modem output.

As there is a difference in transmitting speeds, the serial port being much faster than the modem interface, care must be taken not to overflow the input. When the modem is transmitting its current buffer, it silently ignores everything that it receives via the serial port. The UART configuration for this demonstration is:

- 19200 bps
- 8-N-1
- No flow control

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Appendix A. Board Layout and Schematics

A.1 HV ADAPTER BOARD LAYOUT AND SCHEMATIC

WARNING

SHOCK HAZARD – Do not open the HV adapter cable enclosure.
Failure to heed this warning could result in bodily harm.

FIGURE A-1: HV ADAPTER BOARD LAYOUT

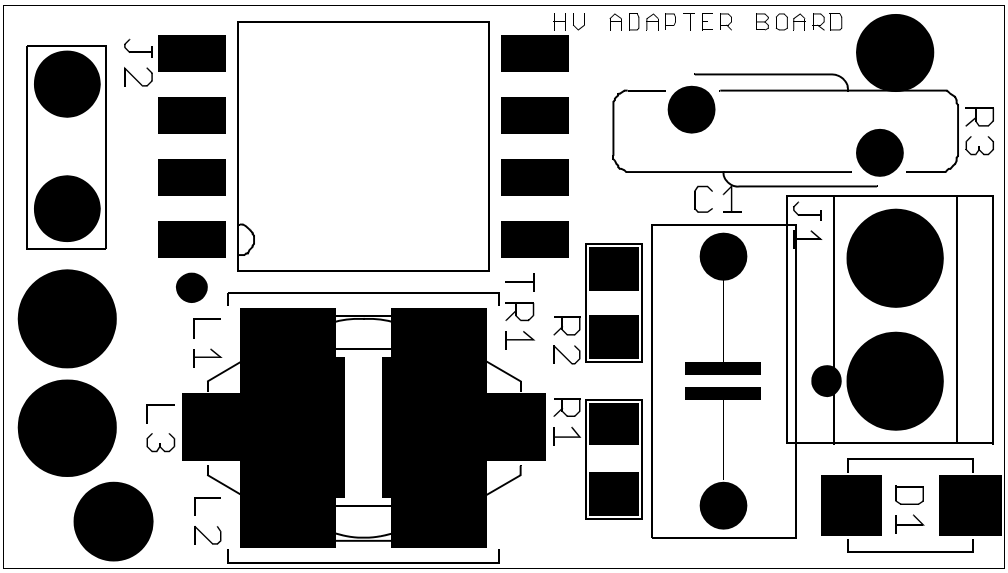
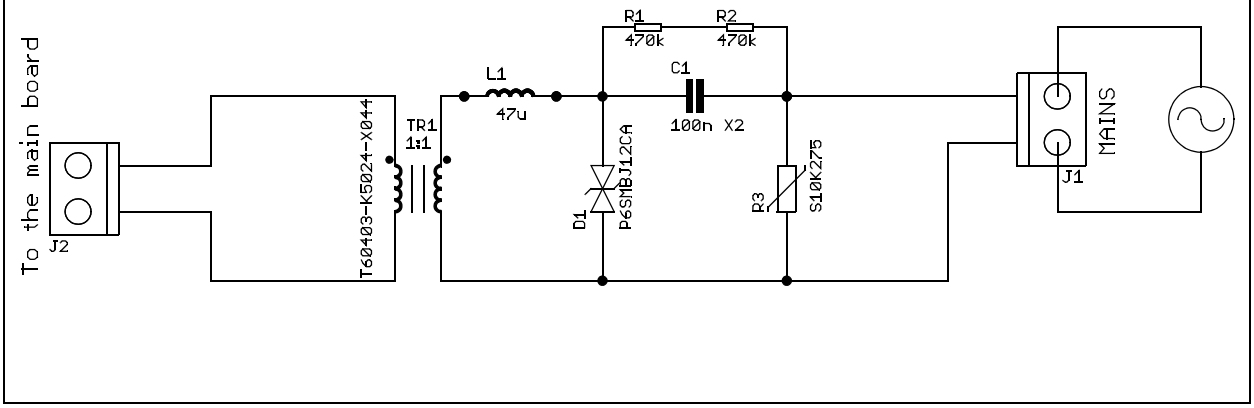
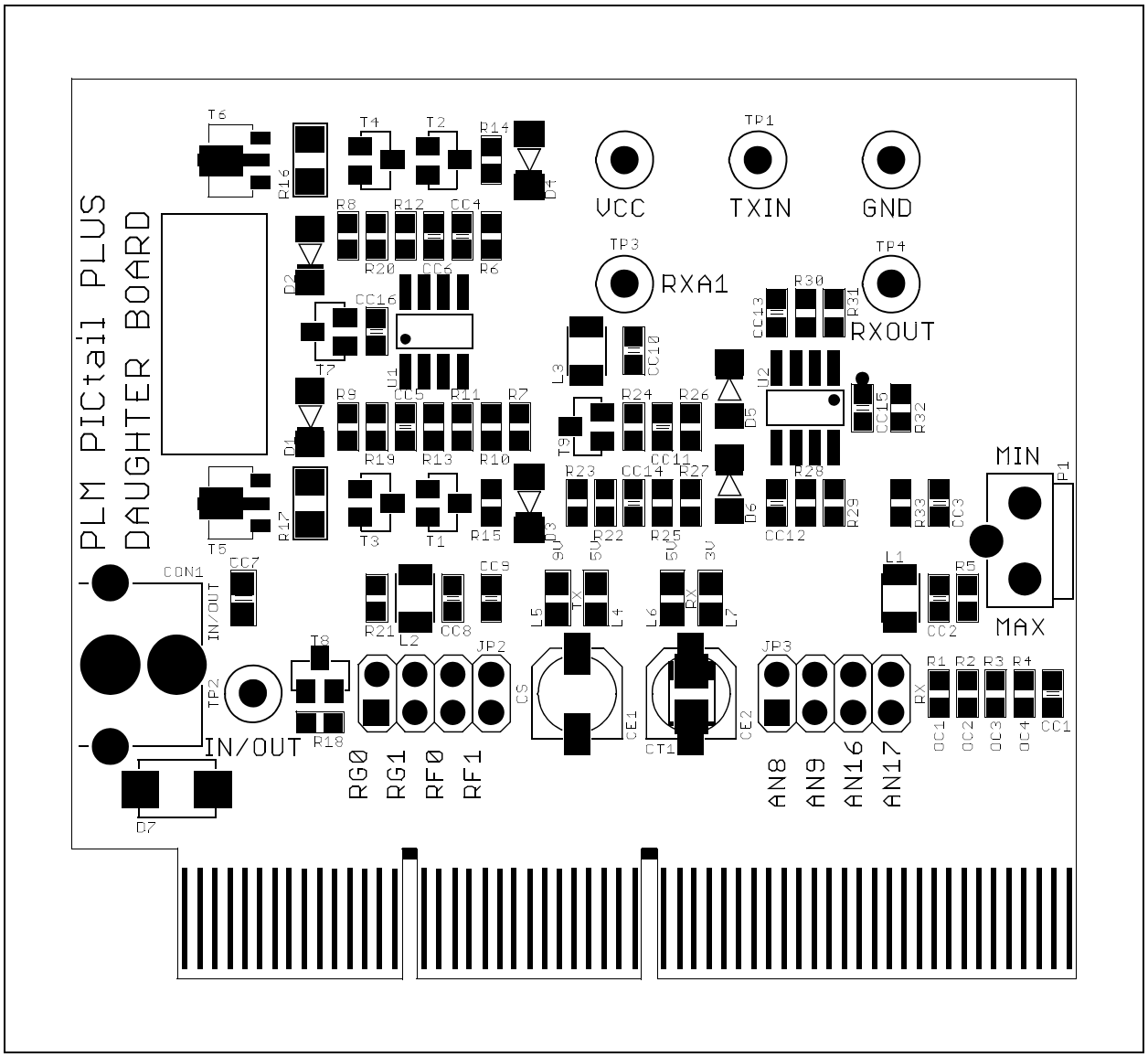


FIGURE A-2: HV ADAPTER BOARD SCHEMATIC



A.2 DAUGHTER BOARD LAYOUT AND SCHEMATICS

FIGURE A-3: DAUGHTER BOARD LAYOUT



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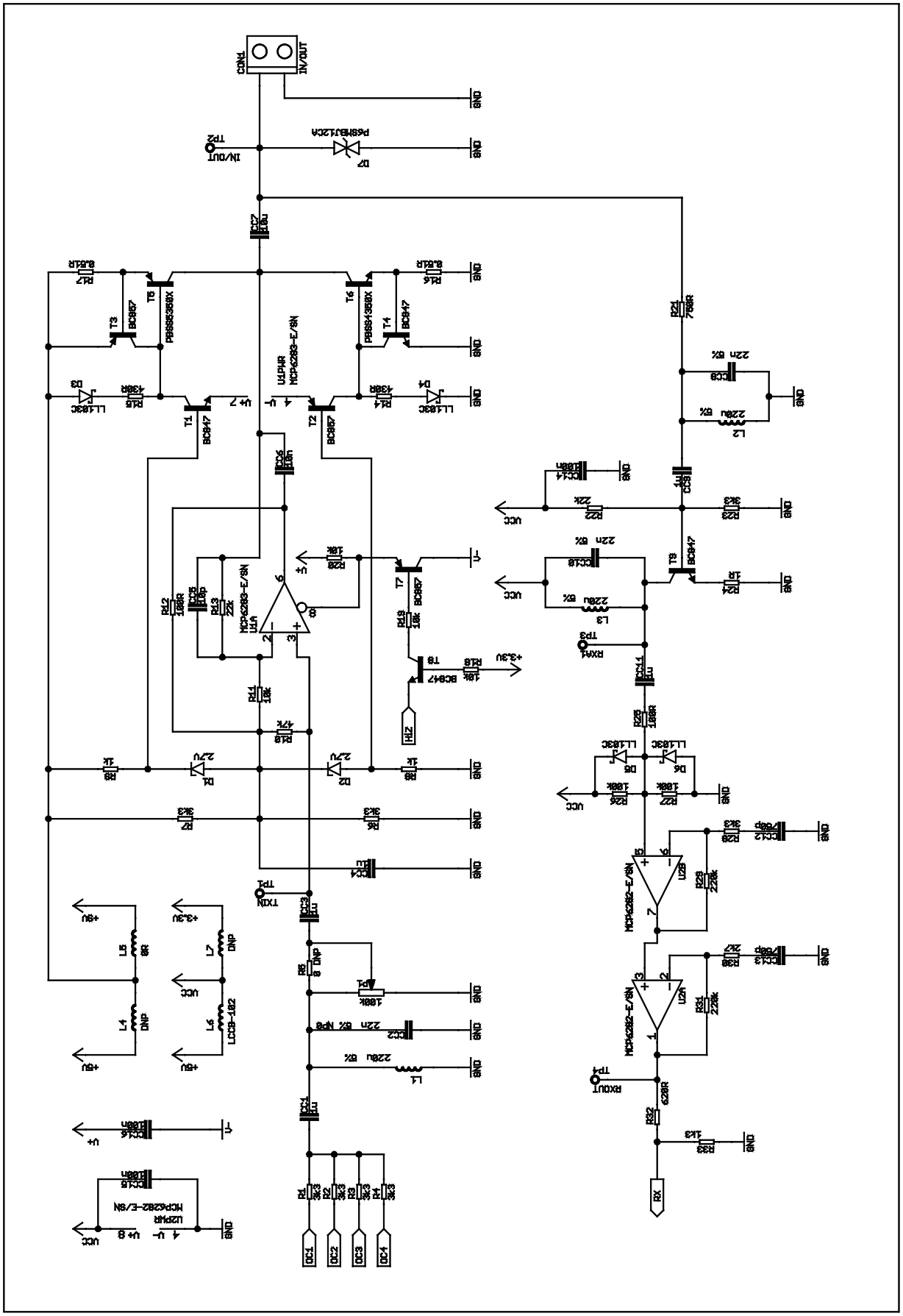


FIGURE A-4: DAUGHTER BOARD SCHEMATIC SHEET 1 OF 2

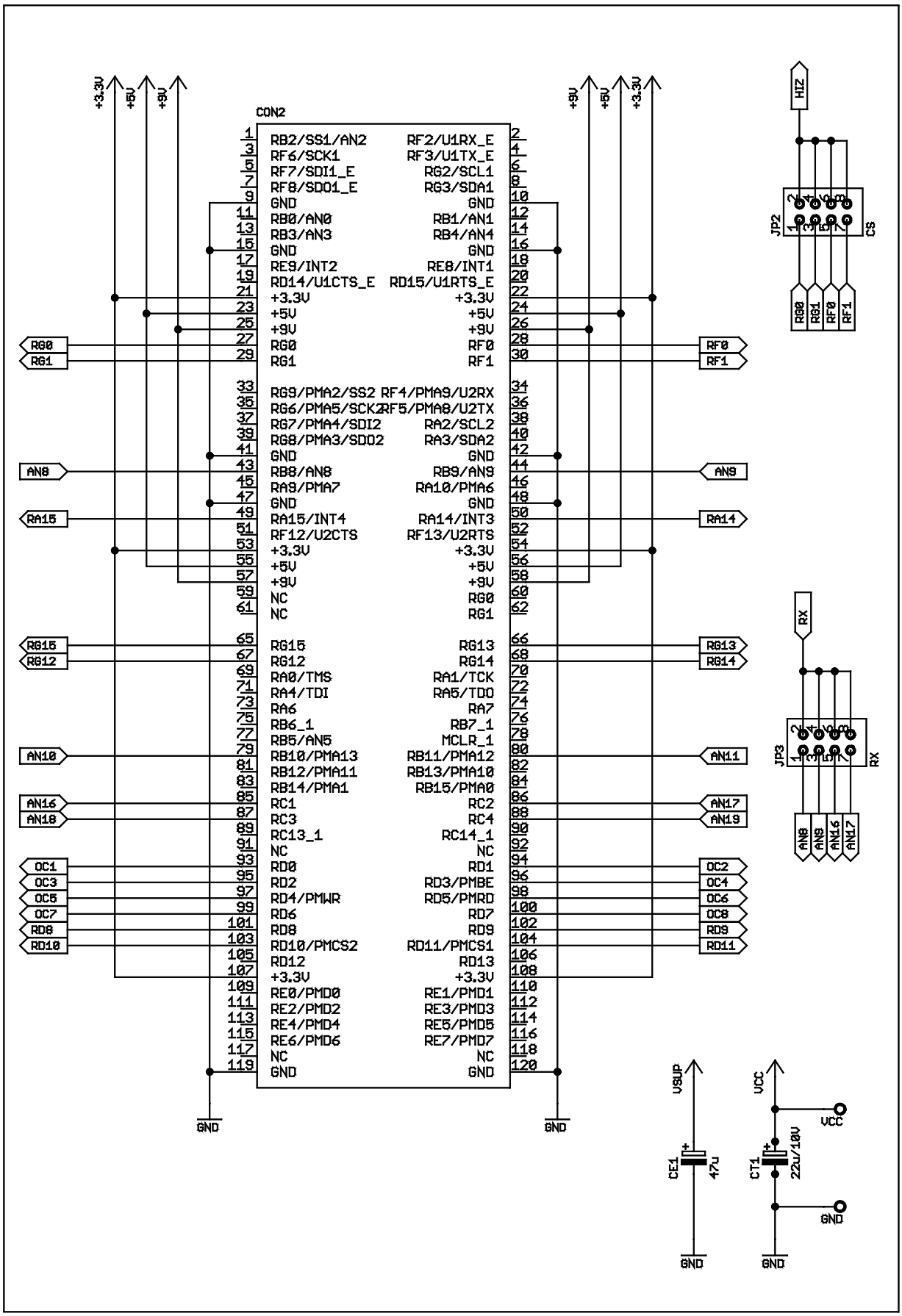


FIGURE A-5: DAUGHTER BOARD SCHEMATIC SHEET 2 OF 2

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Appendix B. Bill of Materials (BOM)

TABLE B-1: DAUGHTER BOARD BILL OF MATERIALS (BOM)

Quantity	Reference	Description	Manufacturer	Manufacturer Part Number
1	D7	12V Bidirectional Transil	Littelfuse Inc.	P6SMB12CA
1	U2	Dual Op amp	Microchip Technology Inc.	MCP6282-E/SN
1	U1	Op amp with CS	Microchip Technology Inc.	MCP6283-E/SN
3	L1, L2, L3	220 µH 5% inductor	TDK	NLV32T-101J-PF
1	T5	PNP Transistor	NXP	PBSS5350X,135
1	T6	NPN Transistor	NXP	PBSS4350X,115
3	T2, T3, T7	PNP Transistor	NXP	BC857BW,115
4	T1, T4, T8, T9	NPN Transistor	NXP	BC847BW,135
2	D1, D2	2v7 Zener Diode	NXP	BZV55-C2V7,115
4	D3, D4, D5, D6	Schottky Diode	Vishay	LL103C-GS08
1	CE1	Electrolytic Cap 47µ 16V C Case	Panasonic - ECG	EEE-1CA470WAR
1	CT1	Tantalum Cap 22µ 10V B Case	Nichicon	F931A226MBA
1	CC7	Ceramic Cap 10µ 0805	Murata	GRM21BR61C106KE15L
5	CC1, CC3, CC4, CC9, CC11	Ceramic Cap 1µ 0603	TDK	C1608Y5V1C105Z
3	CC14, CC15, CC16	Ceramic Cap 100n 0603	Yageo	CC0603ZRY5V7BB104
3	CC2, CC8, CC10	Ceramic Cap 22n 5% 0603	AVX Corp	06035C153JAT2A
1	CC6	Ceramic Cap 10n 0603	Yageo	CC0603KRX7R8BB103
2	CC12, CC13	Ceramic Cap 750p 0603	Murata	GRM1885C1H751JA01D
1	CC5	Ceramic Cap 10p 0603	TDK	C1608C0G1H100D
2	R29, R31	Resistor 220k 0603	Susumu	RR0816P-224-D
2	R26, R27	Resistor 100k 0603	Susumu	RR0816P-104-D
1	R10	Resistor 47k 0603	Susumu	RR0816P-473-D
2	R13, R22	Resistor 22k 0603	Susumu	RR0816P-223-D
4	R11, R18, R19, R20	Resistor 10k 0603	Susumu	RR0816P-103-D
8	R1, R2, R3, R4, R6, R7, R23, R28	Resistor 3k3 0603	Susumu	RR0816P-332-D
1	R30	Resistor 2k7 0603	Susumu	RR0816P-272-D
1	R33	Resistor 1k3 0603	Susumu	RR0816P-132-D
2	R8, R9	Resistor 1k 0603	Susumu	RR0816P-102-D
1	R21	Resistor 750R 0603	Susumu	RR0816P-751-D

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TABLE B-1: DAUGHTER BOARD BILL OF MATERIALS (BOM) (CONTINUED)

Quantity	Reference	Description	Manufacturer	Manufacturer Part Number
1	R32	Resistor 620R 0603	Susumu	RR0816P-621-D
2	R14, R15	Resistor 430R 0603	Susumu	RR0816P-431-D
2	R12, R25	Resistor 100R 0603	Susumu	RR0816P-101-D
1	R24	Resistor 1R 0603	Stackpole Electronics. Inc.	RMCF0603FT1R00
2	R16, R17	Resistor 510m 1206	Rohm Semiconductor	MCR18EZHFLR510
1	L5	Resistor 0R 0603	Stackpole Electronics, Inc.	RMCF0603ZT0R00
1	P1	100k Trimmer Potentiometer	Bourns Inc	3362P-1-104LF
1	CON1	RCA jack - PCB mount right angle	Kycon	KLPX-0848A-2-B
4	JP2, JP3	Jumper 2*2 - Rectangular - Headers, Male Pins	Omron Electronics Inc. (ECB Div)	XG8T-0441
2	J1, J2	Jumper plugs - Place at AN8 and RF0 positions	3M	969102-0000-DA
1	GND	Test point - Blue	Multicomp	Test-1BU
1	TP2 (IN/OUT)	Test point - Red	Multicomp	Test-1R
3	TP1, TP3, TP4 (TXIN, RXA1, RXOUT)	Test point - White	Multicomp	Test-1W
1	L6	Interference suppression bead 120 Ohm 0.2R 0.2A	Ferrocore	LCCB-102

TABLE B-2: HV ADAPTER BILL OF MATERIALS (BOM)

Quantity	Reference	Description	Manufacturer	Manufacturer Part Number
1	TR1	Transformer (HV)	Vacuumschmelze	T60403-K5024-X044
1	D1	12V Bidirectional Transil (HV)	Littelfuse Inc	P6SMB12CA
1	C1	Cap 100 nF X2 630VDC/300VAC(HV)	Kemet	463F310000M1M
1	L1	47 µH inductor (1.28A) (HV)	Murata P S	26470C
2	R1, R2	Resistor 470k 1206 (HV)	Stackpole Electronics Inc.	RMCF1206JT470K
1	Power Cord	Two-Core 18AWG power cord (HV)	Qualtek	221001-01
1	RCA connector	RCA plug - Red (HV)	CUI Inc.	RCP-012
1	Enclosure	Enclosure (HV)	Hammond Manufacturing	1551RFLBK
1	Twisted pair cable, 100 ft	Cable UNSHLD 2C 22AWG 100' (HV)	Belden Wire & Cable	8442 060100
1	R3	Varistor - 275Vrms 10mm Radial (HV)	Epcos Inc.	S10K275

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Appendix C. Troubleshooting Guide

C.1 FREQUENTLY ASKED QUESTIONS

This appendix discusses common operational issues and methods to resolve them.

C.1.1 The daughter boards are not able to communicate on the power line. What can I do to fix the problem?

Possible reasons for the daughter boards to lose the communication link are:

C.1.1.1 DAUGHTER BOARDS CONNECTED ON TWO DIFFERENT POWER SUPPLY PHASES

Connecting daughter boards to power outlets on different phases may result in partial or total loss of the communication link. If you observe that the daughter boards are not able to communicate, try relocating the daughter boards to other power outlets or use a signal coupler device to couple the communication signals across the phases, as described in **1.2 "Board Setup"**.

C.1.1.2 SOFTWARE CONFIGURATION NOT COMPATIBLE WITH HARDWARE DESIGN

Some of the configuration settings are hardware dependent and these settings should match the hardware being used. Following configuration settings are hardware dependent:

- Hi-Z signal polarity (PLM_OE, default: PLM_OE_ACTIVE_LOW_HIZ)
- Hi-Z signal pin (PLM_OE_LAT, default: LATF, #0)
- ADC input channel (PLM_ADC_CHNL, default: 8)
- Carrier frequency (PLM_FC, default: 72000)

C.1.1.3 POTENTIOMETER (P1) SET AT A LOW VALUE

The potentiometer (P1) is used to adjust the average output amplitude transmitted from the daughter board. If the potentiometer is set too low the transmitted signal power may not to be reliably detected by the other daughter board. It is preferable to set the potentiometer value close to the MAX position (turn counter clockwise).

C.1.1.4 DISSIMILAR CONFIGURATION SETTINGS

Daughter boards will not be able to communicate if they are programmed with dissimilar settings for certain configuration options like carrier frequency, Forward Error Correction (FEC), framing and baud rate.

C.1.1.5 IMPROPER JUMPER CONFIGURATION

Ensure that the jumpers at CS (JP2) and RX (JP3) are in place (default: JP2 - RF0, JP3 - AN8). Improper jumper settings can disable the transmitter or receiver sections of the daughter board.

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C.1.1.6 DAUGHTER BOARDS PLUGGED INTO A POWER STRIP WITH EMI FILTERING / SURGE PROTECT FEATURE

Some power strips have Electromagnetic Interference (EMI) filtering or surge protection devices. These devices filter out the power line noises at frequencies much higher than the power line frequency (which is 50 Hz or 60 Hz). Since the daughter board uses a carrier frequency (72 kHz) much higher than the power line frequency, these devices may attenuate the signal and result in unreliable or sometimes non-functional communication link between daughter boards. Also, daughter boards will not be able to communicate if they are connected through isolation power transformers.

C.1.1.7 DAUGHTER BOARDS PLUGGED INTO OUTLETS CLOSE TO NOISE SOURCES

Power lines can pick up and conduct noise from various noise sources like lamp dimmers, electric motors and switching power supplies. Power line noise from these noise sources can cause degradation in the performance of the power line communication link. If you notice reduced performance in communication between daughter boards, try moving them to outlets further away from these noise sources.

C.1.1.8 INTERFERENCE FROM OTHER POWER LINE COMMUNICATION DEVICES

Other Power Line Communication devices on the power line can cause interference and performance degradation if they are operating in the same frequency band as this daughter board. If the interfering device needs to be used simultaneously on the same power line with the daughter board, please change the operating frequency band of the interfering device and move it to a power outlet further away from the daughter board.

C.1.2 What is the maximum operational range of these daughter boards?

Since wall power outlets are connected using wires embedded into the walls, length of wiring between power outlets is generally greater than the physical distance between them. It is hard to quote the maximum operational range of the daughter boards since it depends on many other factors like:

- Structure / architecture of the wiring:

  Branches and rings can cause signal reflections and multi-path signals, which can interfere constructively or destructively with the original signal.
- Age of the wiring:

  As wiring deteriorates over time, loose connections can attenuate or reflect signals.
- Appliances connected on the wiring:

  Number, type and distance of appliances from the daughter boards are also important factors since the appliances can attenuate the signals from the daughter board and create noise on the power line.
- Quality of components used in the wiring (like copper wires, connectors, switches, etc).

  Despite the Automatic Gain Control (AGC) feature incorporated in the modem software, changes in the above mentioned factors may change the maximum possible operational range of the daughter boards.

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C.1.3 What are the important points to keep in mind while designing a custom hardware solution using the schematics provided by Microchip?

Following are the important points to keep in mind while designing a custom hardware solution:

C.1.3.1 POWER SUPPLY RATING

It is important to have a power supply with sufficient rating to power the daughter board. The daughter board can draw up to 600 mA from the power supply. Do not use a programming/debugging tool to power up the daughter board.

C.1.3.2 VENTILATION

Sufficient ventilation must be provided to avoid thermal runaway issues with the output transistors. The output transistors have to be mounted on a large copper plane to dissipate heat efficiently.

C.1.3.3 PCB DESIGN

Due to the very high gain of the receive path, it is very important to carefully design the PCB layout. Output signals should not be routed near the inputs of preceding stages. Ground return paths should be planned to run in straight lines to the common ground reference point and return paths from the last stages should not run under preceding stages.

C.1.4 What are the implications of using less than four Output Compare (OC) channels for the daughter board?

Using less than four Output Compare (OC) channels will reduce the signal power transmitted by the daughter board. Consequently, this can reduce the operating range and performance.

NOTES:

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NOTES:

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