Multiformat 216 MHz Video Encoder with Six NSV® 12-Bit DACs

ADV7320/ADV7321

FEATURES

High definition (HD) input formats
- 16-/20-, 24-/30-bit (4:2:2, 4:4:4) parallel YCrCb

Fully compliant with
- SMPTE 274M (1080i, 1080p @ 74.25 MHz)
- SMPTE 296M (720p)
- SMPTE 240M (1035i)
- RGB in 3-bit × 10-bit 4:4:4 input format

HDTV RGB supported
- RGB, RGBHV
- Other HD formats using async timing mode

Enhanced definition (ED) input formats
- 8-/10-, 16-/20-, 24-/30-bit (4:2:2, 4:4:4) parallel YCrCb
- SMPTE 293M (525p)
- BTA T-1004 EDTV2 (525p)
- ITU-R BT.1358 (625p/525p)
- ITU-R BT.1362 (625p/525p)
- RGB in 3-bit × 10-bit 4:4:4 input format

Standard definition (SD) input formats
- CCIR-656 4:2:2 8-/10-bit or 16-/20-bit parallel input

HD output formats
- YPrPb HDTV (EIA 770.3)
- RGB, RGBHV
- CGMS-A (720p/1080i)

ED output formats
- Macrovision® Rev 1.2 (525p/625p) (ADV7320 only)
- CGMS-A (525p/625p)
- YPrPb progressive scan (PS) (EIA-770.1, EIA-770.2)
- RGB, RGBHV

SD output formats
- Composite NTSC M/N
- Composite PAL M/N/B/D/G/H/I, PAL-60
- SMPTE 170M NTSC-compatible composite video
- ITU-R BT.470 PAL-compatible composite video
- S-video (Y/C)
- EuroScart RGB
- Component YPrPb (Betacam, MII, SMPTE/EBU N10)
- Macrovision Rev 7.1.L1 (ADV7320 only)
  - CGMS/WSS
  - Closed captioning

GENERAL FEATURES

Simultaneous SD/HD or PS/SD inputs and outputs
Oversampling up to 216 MHz
Programmable DAC gain control
Sync outputs in all modes
On-board voltage reference
Six 12-bit NSV (noise shaped video) precision video DACs
2-wire serial I²C® interface, open-drain configuration
Dual I/O supply 2.5 V/3.3 V operation
Analog and digital supply 2.5 V
On-board PLL
64-lead LQFP package
Lead (Pb) free product

APPLICATIONS

EVD (enhanced versatile disk) players
High-end SD/PS DVD recorders/players
SD/PS/HDTV display devices
SD/HDTV set top boxes
Professional video systems

FUNCTIONAL BLOCK DIAGRAM

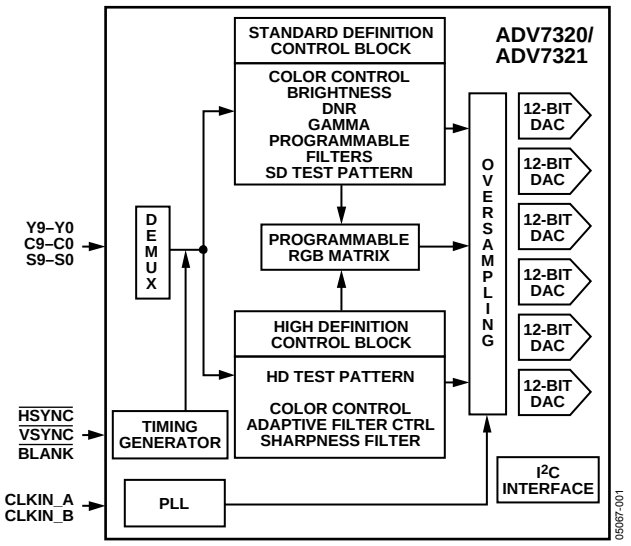


Figure 1.

GENERAL DESCRIPTION

The ADV®7320/ADV7321 are high speed, digital-to-analog encoders on single monolithic chips. They include six high speed NSV video DACs with TTL-compatible inputs. They have separate 8-/10-, 16-/20-, and 24-/30-bit input ports that accept data in high definition (HD) and/or standard definition (SD) video format. For all standards, external horizontal, vertical, and blanking signals, or EAV/SAV timing codes, control the insertion of appropriate synchronization signals into the digital data stream and, therefore, the output signal.

Rev. A
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REVISION HISTORY

5/06—Rev. 0 to Rev. A

Replaced Figure 11....12
Changes to Table 25....41

10/04—Revision 0: Initial Version

DETAILED FEATURES

HD programmable features (720p/1080i/1035i)
- **2× oversampling (148.5 MHz)**
- **Internal test pattern generator**
- **Color hatch, black bar, flat field/frame**
- **Fully programmable YCrCb to RGB matrix**
- **Gamma correction**
- **Programmable adaptive filter control**
- **Programmable sharpness filter control**
- **CGMS-A (720p/1080i)**

ED programmable features (525p/625p)
- **8× oversampling (216 MHz output)**
- **Internal test pattern generator**
- **Color hatch, black bar, flat frame**
- **Individual Y and PrPb output delay**
- **Gamma correction**
- **Programmable adaptive filter control**
- **Fully programmable YCrCb to RGB matrix**
- **Undershoot limiter**
- **Macrovision Rev 1.2 (525p/625p) (ADV7320 only)**
- **CGMS-A (525p/625p)**

SD programmable features
- **16× oversampling (216 MHz)**
- **Internal test pattern generator**
  - **Color bars, black bar**
- **Controlled edge rates for start and end of active video**
- **Individual Y and PrPb output delay**
- **Undershoot limiter**
- **Gamma correction**
- **Digital noise reduction (DNR)**
- **Multiple chroma and luma filters**
- **Luma-SSAF™ filter with programmable gain/attenuation**
- **PrPb SSAF™**
- **Separate pedestal control on component and composite/S-video output**
- **VCR FF/RW sync mode**
- **Macrovision Rev 7.1.L1 (ADV7320 only)**
  - **CGMS/WSS**
  - **Closed captioning**

Table 1. Standards Directly Supported[1]

Resolution	Interlace/PS	Frame Rate (Hz)	Clock Input (MHz)	Standard
720 × 480	I	29.97	27	ITU-R BT.656
720 × 576	I	25	27	ITU-R BT.656
720 × 480	I	29.97	24.54	NTSC Square Pixel
720 × 576	I	25	29.5	PAL Square Pixel
720 × 483	P	59.94	27	SMPTE 293M
720 × 483	P	59.94	27	BTA T-1004
720 × 483	P	59.94	27	ITU-R BT.1358
720 × 576	P	50	27	ITU-R BT.1358
720 × 483	P	59.94	27	ITU-R BT.1362
720 × 576	P	50	27	ITU-R BT.1362
1920 × 1035	I	30	74.25	SMPTE 240M
		29.97	74.1758	
1280 × 720	P	60, 50, 30, 25, 24	74.25	SMPTE 296M
		23.97, 59.94, 29.97	74.1758	
1920 × 1080	I	30, 25	74.25	SMPTE 274M
		29.97	74.1758	
1920 × 1080	P	30, 25, 24	74.25	SMPTE 274M
		23.98, 29.97	74.1758	

[1] Other standards are supported in async timing mode.

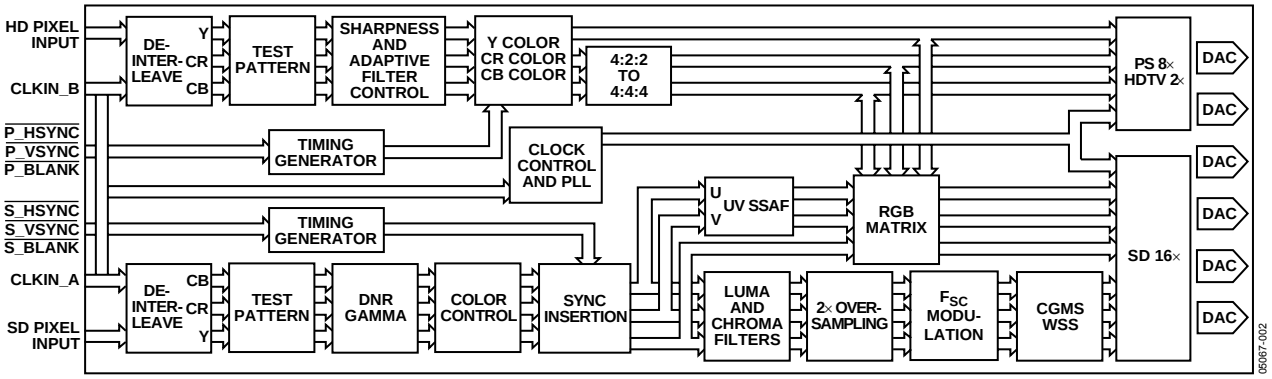


Figure 2. Detailed Functional Block Diagram

TERMINOLOGY

SD: standard definition video, conforming to ITU-R BT.601/ITU-R BT.656.

HD: high definition video, that is, 720p/1080i/1035i.

EDTV: enhanced definition television (525p/625p).

PS: progressive scan video, conforming to SMPTE 293M, ITU-R BT.1358, BTA T-1004 EDTV2, or ITU-R BT.13621362.

HDTV: high definition television video, conforming to SMPTE 274M, or SMPTE 296M and SMPTE 240M.

YCrCb SD, PS, or HD component: digital video.

YPrPb SD, PS, or HD component: analog video.

SPECIFICATIONS

V_{AA} = 2.375 V to 2.625 V, V_{DD} = 2.375 V to 2.625 V, V_{DD_IO} = 2.375 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 3040 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions
STATIC PERFORMANCE[1]					
Resolution		12		Bits	
Integral Nonlinearity		1.5		LSB	
Differential Nonlinearity,[2] +ve		0.25		LSB	
Differential Nonlinearity,[2] –ve		1.5		LSB	
DIGITAL OUTPUTS					
Output Low Voltage, V_{OL}			0.4 [0.4][3]	V	I_{SINK} = 3.2 mA
Output High Voltage, V_{OH}	2.4 [2.0][3]			V	I_{SOURCE} = 400 µA
Three-State Leakage Current		±1.0		µA	V_{IN} = 0.4 V, 2.4 V
Three-State Output Capacitance		2		pF	
DIGITAL AND CONTROL INPUTS					
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}			0.8	V	
Input Leakage Current		10		µA	V_{IN} = 2.4 V
Input Capacitance, C_{IN}		2		pF	
ANALOG OUTPUTS					
Full-Scale Output Current	4.1	4.33	4.6	mA	
Output Current Range	4.1	4.33	4.6	mA	
DAC-to-DAC Matching		1.0		%	
Output Compliance Range, V_{OC}	0	1.0	1.4	V	
Output Capacitance, C_{OUT}		7		pF	
VOLTAGE REFERENCE					
Internal Reference Range, V_{REF}	1.15	1.235	1.3	V	
External Reference Range, V_{REF}	1.15	1.235	1.3	V	
V_{REF} Current[4]		±10		µA	
POWER REQUIREMENTS					
Normal Power Mode					
I_{DD}[5]		137		mA	SD only (16×)
		78		mA	PS only (8×)
		73		mA	HDTV only (2×)
		140	190[6]	mA	SD (16×, 10 bit) + PS (8×, 20 bit)
I_{DD_IO}		1.0		mA	
I_{AA}[7, 8]		37	45	mA	
Sleep Mode					
I_{DD}		80		µA	
I_{AA}		7		µA	
I_{DD_IO}		250		µA	
POWER SUPPLY REJECTION RATIO		0.01		%/%	

[1] Oversampling disabled. Static DAC performance improves with increased oversampling ratios.
[2] DNL measures the deviation of the actual DAC output voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value; for –ve DNL, the actual step value lies below the ideal step value.
[3] For values in brackets, V_{DD_IO} = 2.375 V to 2.75 V.
[4] External current required to overdrive internal V_{REF}.
[5] I_{DD}, the circuit current, is the continuous current required to drive the digital core.
[6] Guaranteed maximum by characterization.
[7] All DACs on.
[8] I_{AA} is the total current required to supply all DACs, including the V_{REF} circuitry and the PLL circuitry.

DYNAMIC SPECIFICATIONS

V_{AA} = 2.375 V to 2.625 V, V_{DD} = 2.375 V to 2.625 V, V_{DD_IO} = 2.375 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 3040 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions
PS MODE					
Luma Bandwidth		12.5		MHz	
Chroma Bandwidth		5.8		MHz	
SNR		65.6		dB	Luma ramp unweighted
		72		dB	Flat field full bandwidth
HDTV MODE					
Luma Bandwidth		30		MHz	
Chroma Bandwidth		13.75		MHz	
SD MODE					
Hue Accuracy		0.2		Degrees	
Color Saturation Accuracy		0.20		%	
Chroma Nonlinear Gain		0.84		±%	Referenced to 40 IRE
Chroma Nonlinear Phase		−0.2		±Degrees	
Chroma/Luma Intermodulation		0		±%	
Chroma/Luma Gain Inequality		96.7		±%	
Chroma/Luma Delay Inequality		−1.0		ns	
Luminance Nonlinearity		0.2		±%	
Chroma AM Noise		84		dB	
Chroma PM Noise		75.3		dB	
Differential Gain		0.25		%	NTSC
Differential Phase		0.2		Degrees	NTSC
SNR		63.5		dB	Luma ramp
		77.7		dB	Flat field full bandwidth

TIMING SPECIFICATIONS

V_{AA} = 2.375 V to 2.625 V, V_{DD} = 2.375 V to 2.625 V, V_{DD_IO} = 2.375 V to 3.6 V, V_{REF} = 1.235 V, R_{SET} = 3040 Ω, R_{LOAD} = 300 Ω. All specifications T_{MIN} to T_{MAX} (0°C to 70°C), unless otherwise noted.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions
MPU PORT[1]					
SCLOCK Frequency	0		400	kHz	
SCLOCK High Pulse Width, t_1	0.6			µs	
SCLOCK Low Pulse Width, t_2	1.3			µs	
Hold Time (Start Condition), t_3	0.6			µs	First clock generated after this period relevant for repeated start condition
Setup Time (Start Condition), t_4	0.6			µs	
Data Setup Time, t_5	100			ns	
SDATA, SCLOCK Rise Time, t_6			300	ns	
SDATA, SCLOCK Fall Time, t_7			300	ns	
Setup Time (Stop Condition), t_8	0.6			µs	
$\overline{\text{RESET}}$ Low Time	100			ns	
ANALOG OUTPUTS					
Analog Output Delay[2]		7		ns	
Output Skew		1		ns	
CLOCK CONTROL AND PIXEL PORT[3]					
f_{CLK}			29.5	MHz	SD PAL square pixel mode
f_{CLK}		81		MHz	PS/HD async mode
Clock High Time, t_9	40			% of one clock cycle	
Clock Low Time, t_{10}	40			% of one clock cycle	
Data Setup Time, t_{11}[1]	2.0			ns	
Data Hold Time, t_{12}[1]	2.0			ns	
SD Output Access Time, t_{13}			15	ns	
SD Output Hold Time, t_{14}	5.0			ns	
HD Output Access Time, t_{13}			14	ns	
HD Output Hold Time, t_{14}	5.0			ns	
PIPELINE DELAY[4]		63		Clock cycles	SD (2×, 16×)
		76		Clock cycles	SD component mode (16×)
		35		Clock cycles	PS (1×)
		41		Clock cycles	PS (8×)
		36		Clock cycles	HD (2×, 1×)

[1] Guaranteed by characterization.
[2] Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of DAC output full-scale transition.
[3] Data: C[9:0], Y[9:0], S[9:0]; Control: P_HSYNC, P_VSYNC, P_BLANK, S_HSYNC, S_VSYNC, S_BLANK.
[4] SD, PS = 27 MHz; HD = 74.25 MHz.

TIMING DIAGRAMS

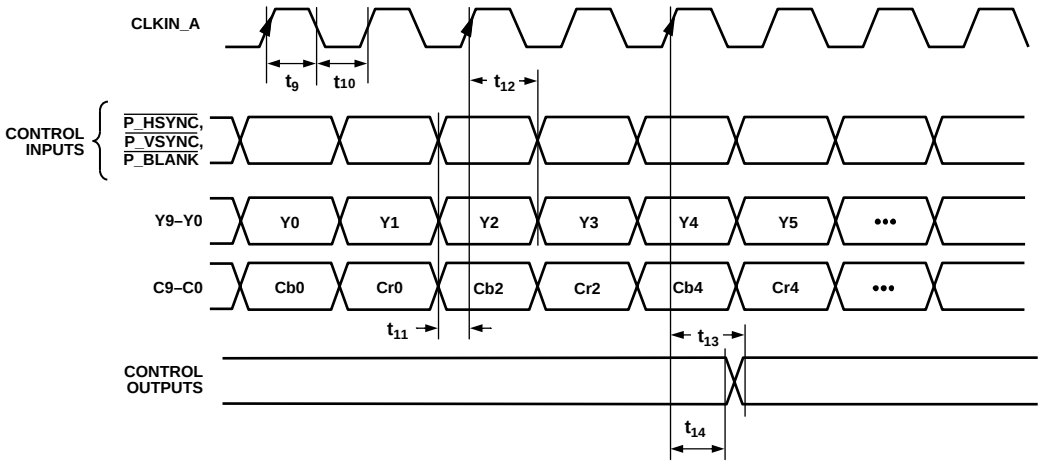


Figure 3. HD Only 4:2:2 Input Mode (Input Mode 010); PS Only 4:2:2 Input Mode (Input Mode 001)

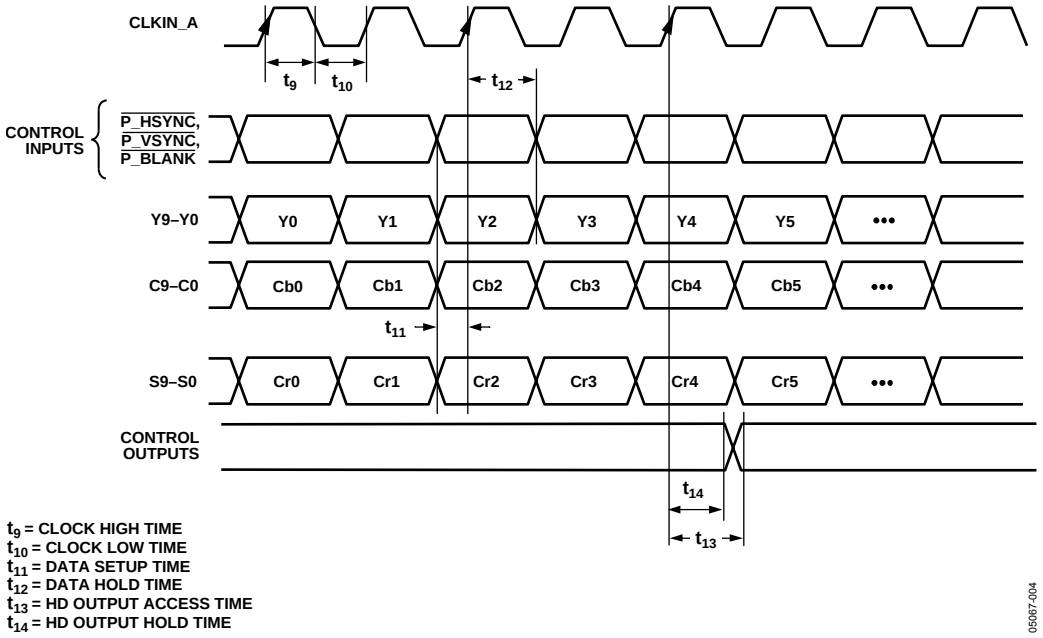


Figure 4. HD Only 4:4:4 Input Mode (Input Mode 010); PS Only 4:4:4 Input Mode (Input Mode 001)

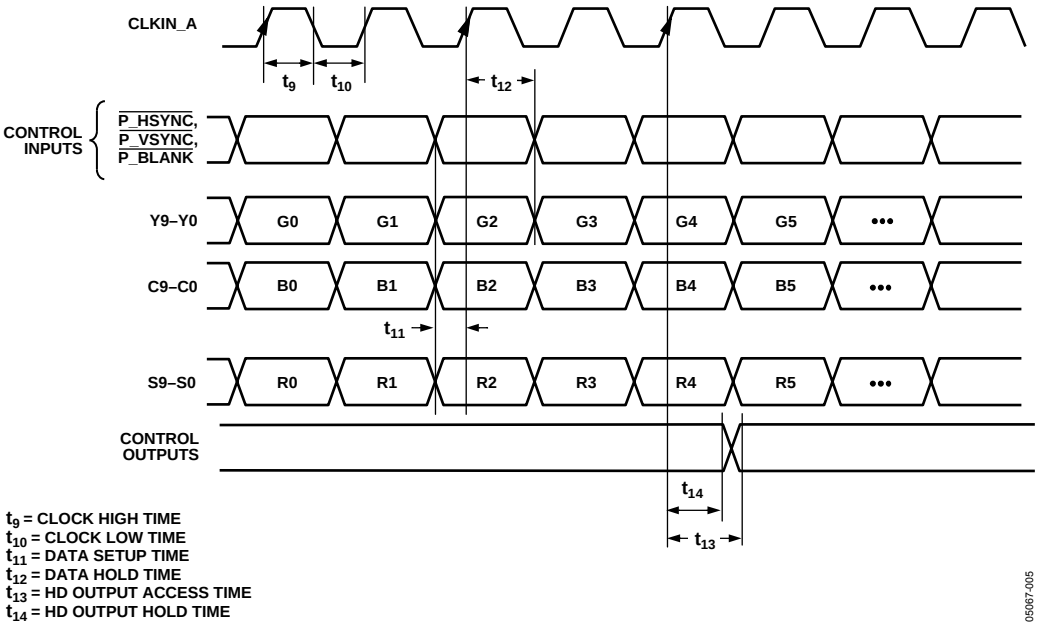


Figure 5. HD RGB 4:4:4 Input Mode (Input Mode 010)

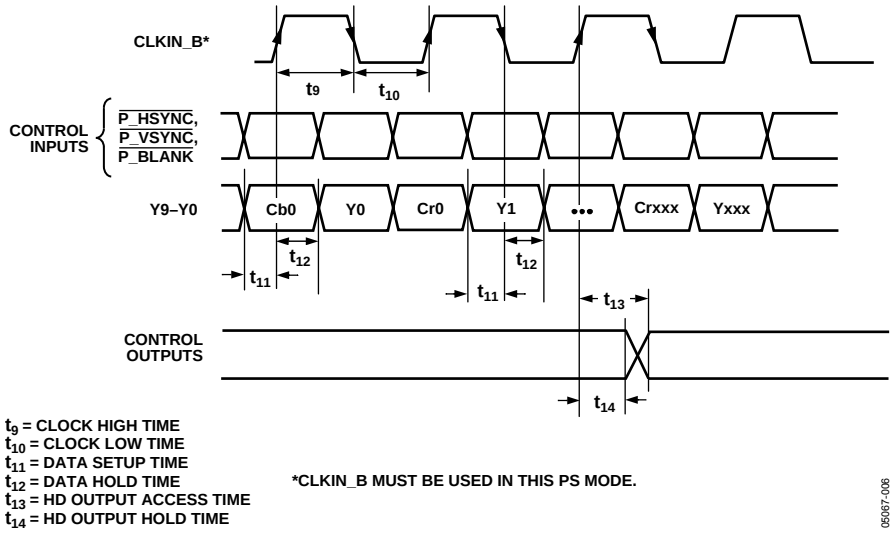


Figure 6. PS 4:2:2 10-Bit Interleaved at 27 MHz $\overline{HSYNC}$/$\overline{VSYNC}$ Input Mode (Input Mode 100)

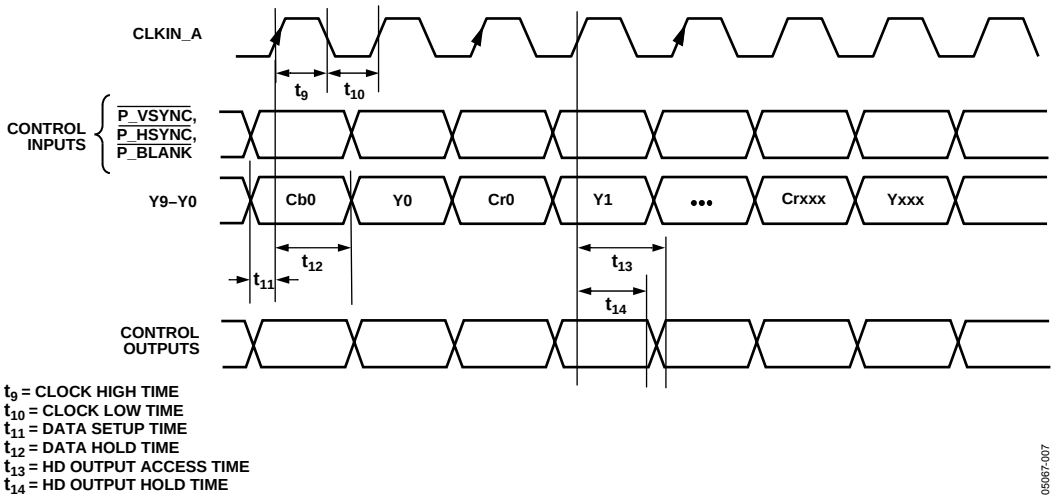


Figure 7. PS 4:2:2 10-Bit Interleaved at 54 MHz $\overline{HSYNC}$ /$\overline{VSYNC}$ Input Mode (Input Mode 111)

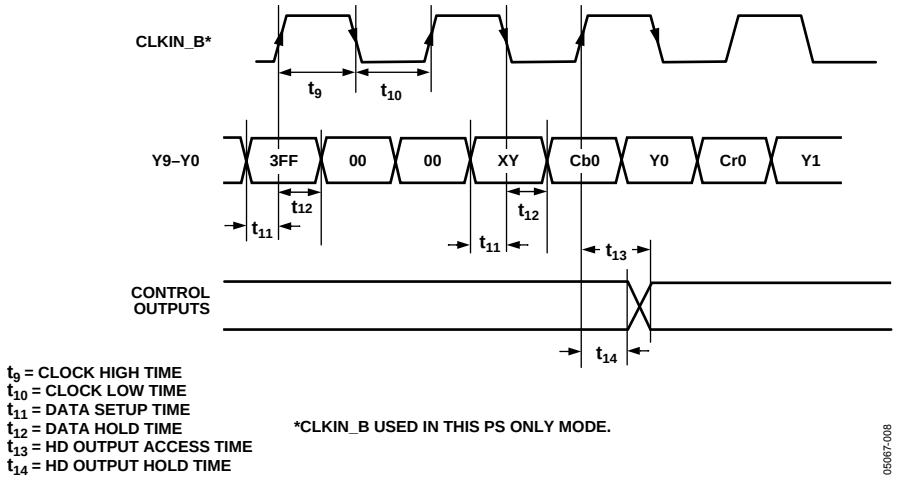


Figure 8. PS Only 4:2:2 10-Bit Interleaved at 27 MHz EAV/SAV Input Mode (Input Mode 100)

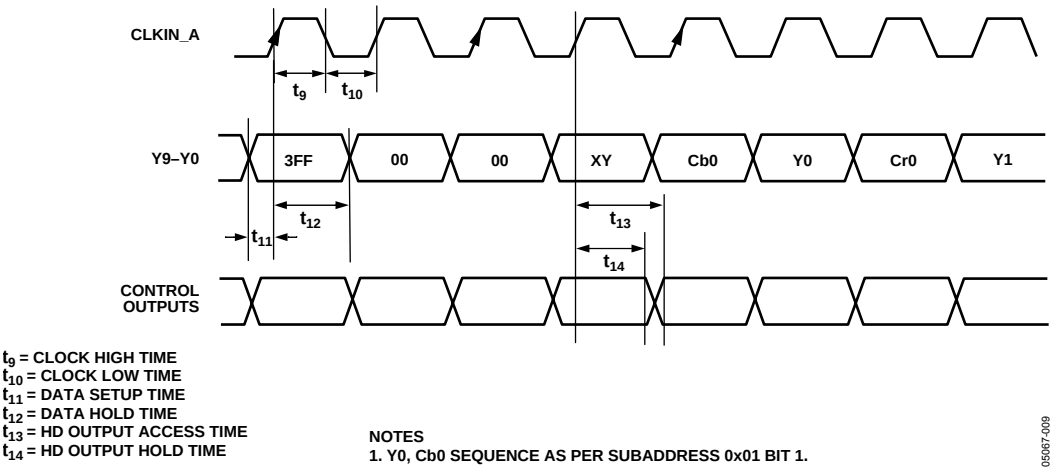


Figure 9. PS Only 4:2:2 10-Bit Interleaved at 54 MHz EAV/SAV Input Mode (Input Mode 111)

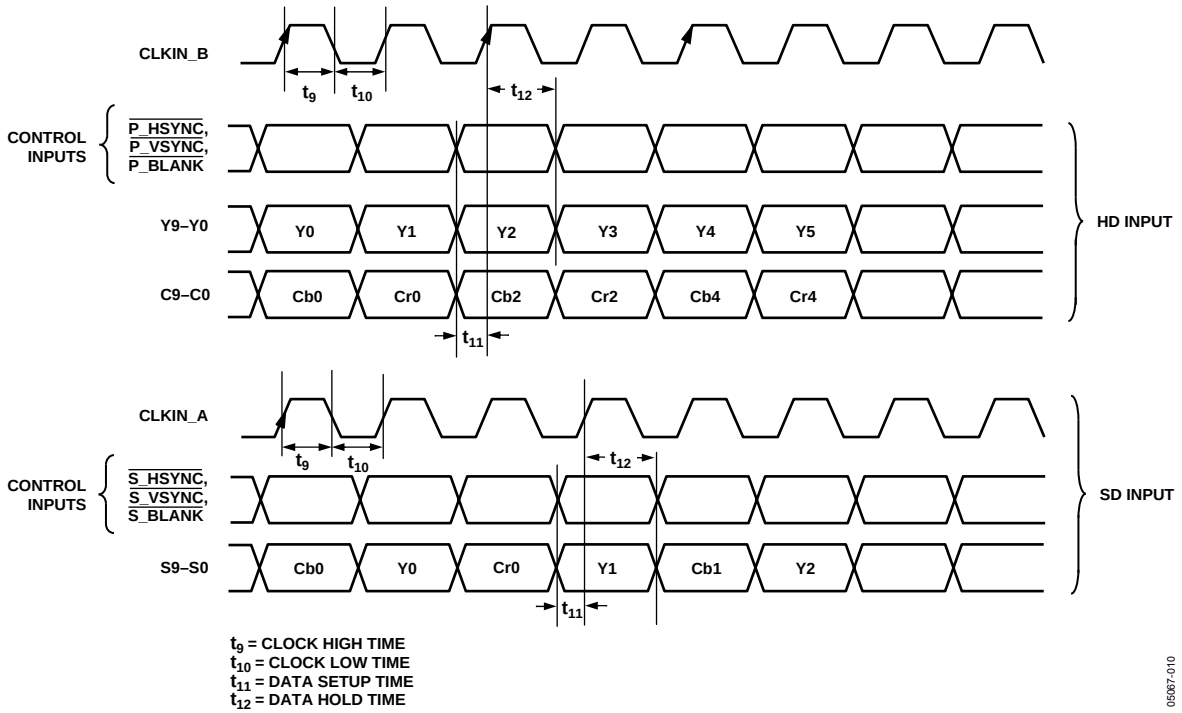


Figure 10. HD 4:2:2 and SD 10-Bit Simultaneous Input Mode (Input Mode 101: SD Oversampled) (Input Mode 110: HD Oversampled)

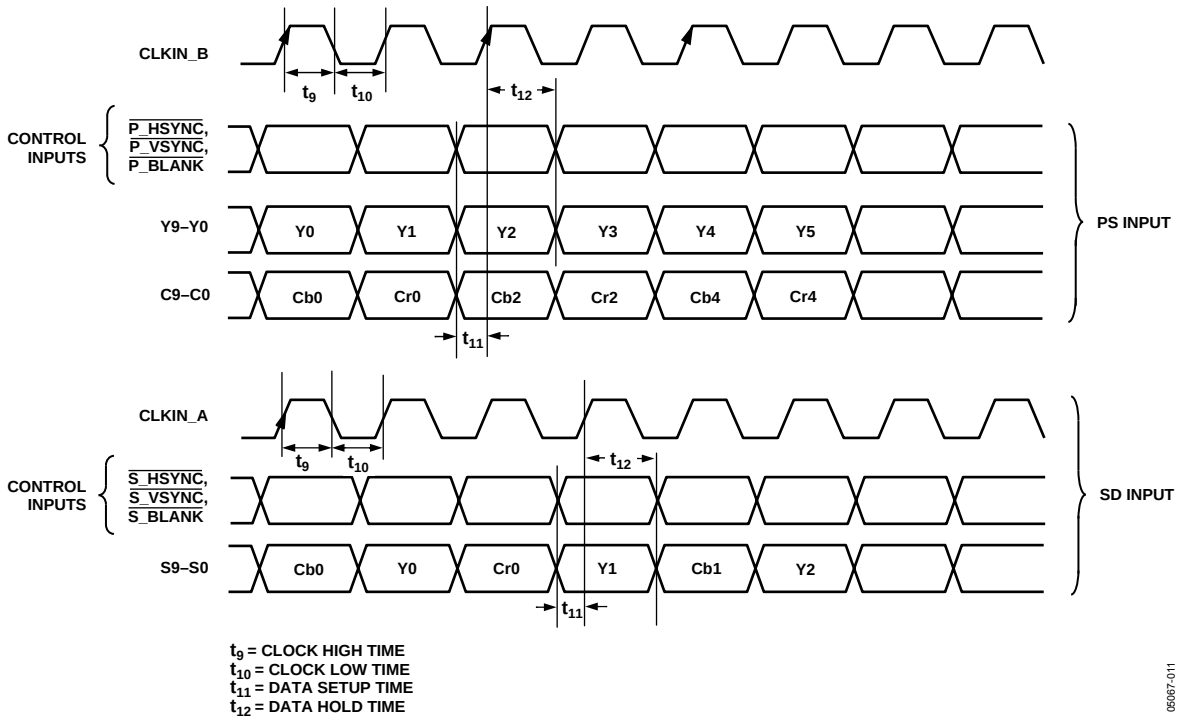


Figure 11. PS 4:2:2 and SD 10-Bit Simultaneous Input Mode (Input Mode 011)

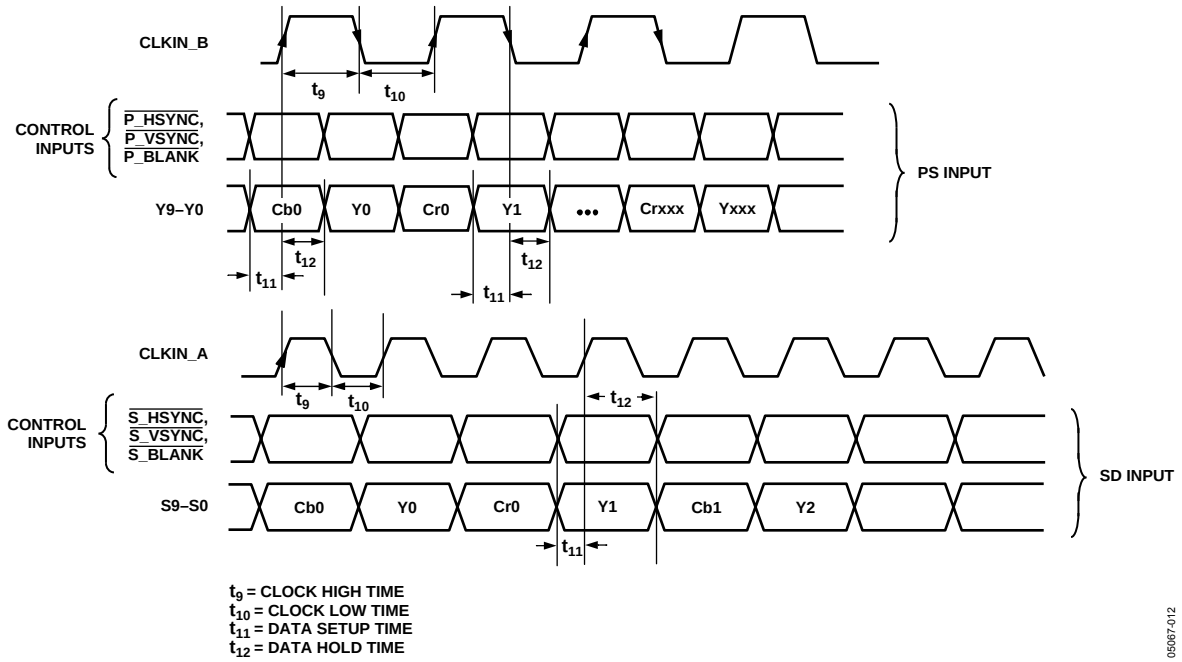


Figure 12. PS 10-Bit and SD 10-Bit Simultaneous Input Mode (Input Mode 100)

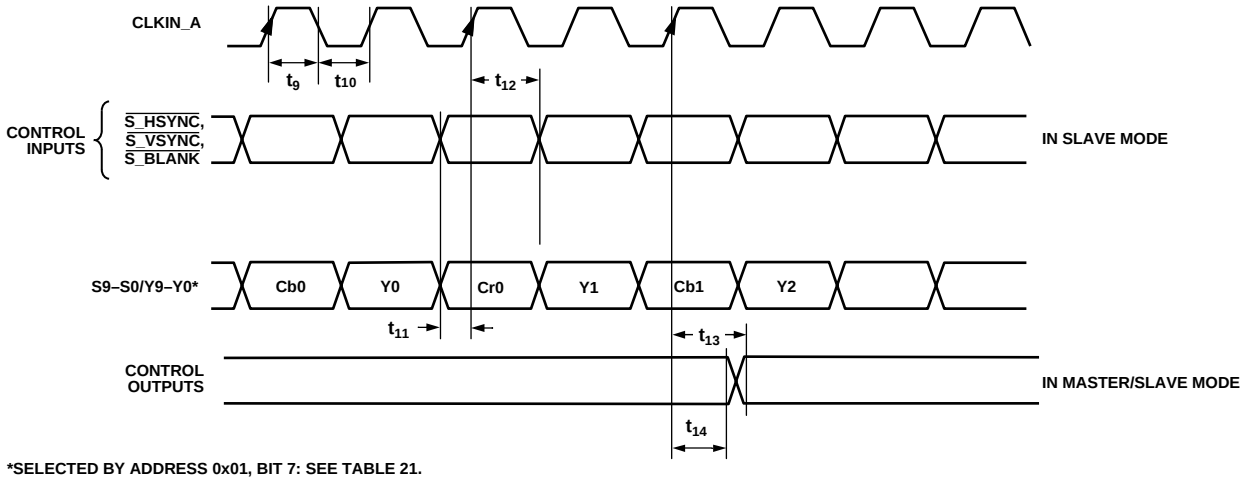
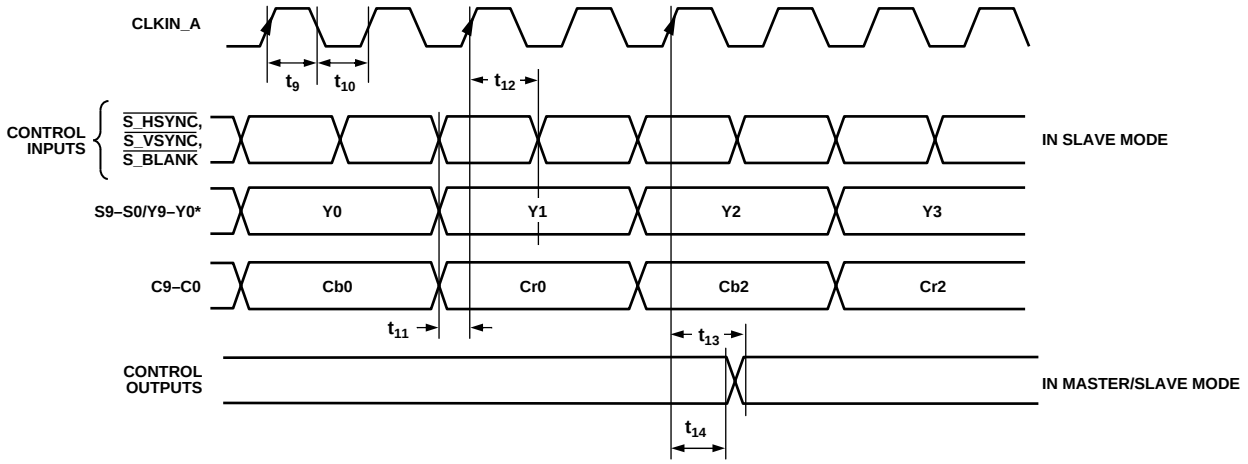


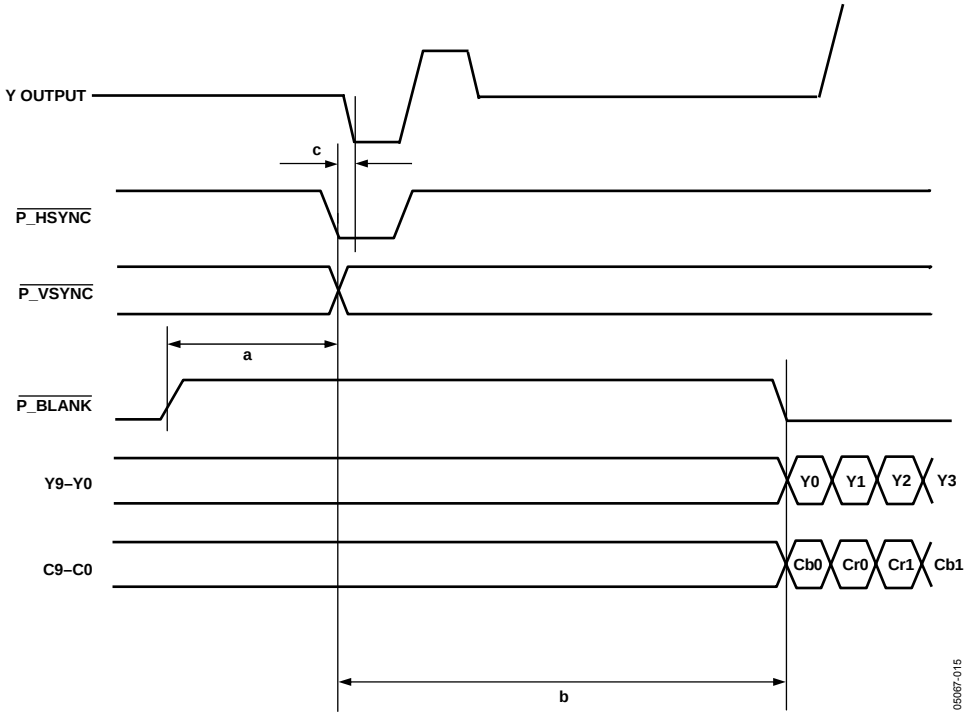
Figure 13. 8-/10-Bit SD Only Pixel Input Mode (Input Mode 000)



*SELECTED BY ADDRESS 0x01, BIT 7: SEE TABLE 21.

t_9 = CLOCK HIGH TIME
t_{10} = CLOCK LOW TIME
t_{11} = DATA SETUP TIME
t_{12} = DATA HOLD TIME
t_{13} = HD OUTPUT ACCESS TIME
t_{14} = HD OUTPUT HOLD TIME

Figure 14. 16-/20-Bit SD Only Pixel Input Mode (Input Mode 000)



a AND b AS PER RELEVANT STANDARD.

c = PIPELINE DELAY. PLEASE REFER TO RELEVANT PIPELINE DELAY. THIS CAN BE FOUND IN THE TIMING SPECIFICATION SECTION OF THE DATA SHEET.

A FALLING EDGE OF HSYNC INTO THE ENCODER GENERATES A FALLING EDGE OF TRI-LEVEL SYNC ON THE OUTPUT AFTER A TIME EQUAL TO THE PIPELINE DELAY.

Figure 15. HD 4:2:2 Input Timing Diagram

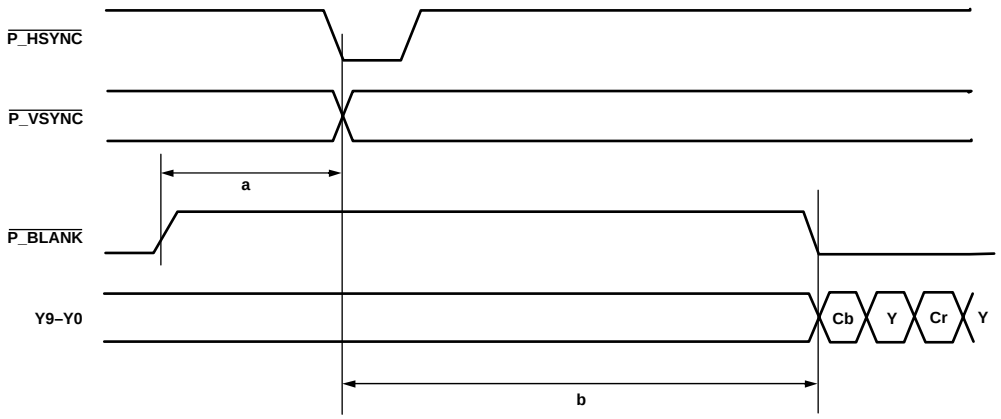


Figure 16. PS 4:2:2 10-Bit Interleaved Input Timing Diagram

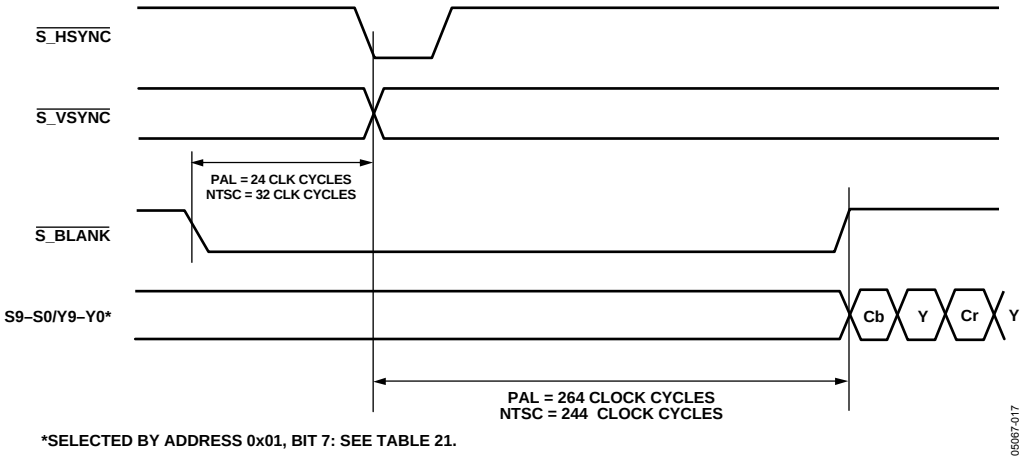


Figure 17. SD Timing Input for Timing Mode 1

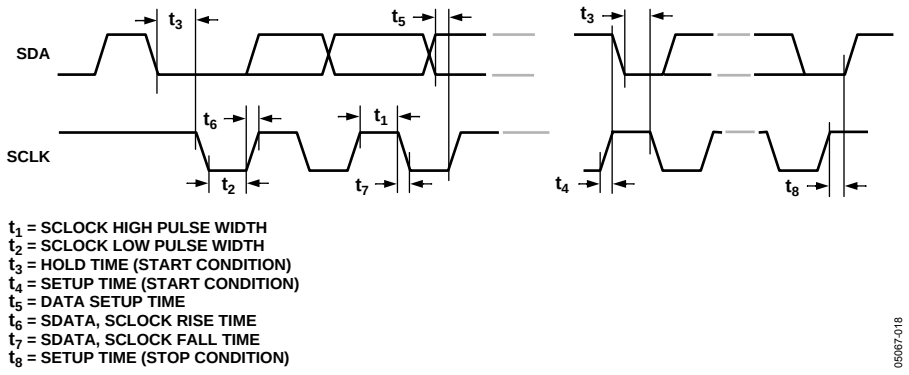


Figure 18. MPU Port Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter[1]	Value
V_{AA} to AGND	−0.3 V to +3.0 V
V_{DD} to DGND	−0.3 V to +3.0 V
V_{DD_IO} to GND_IO	−0.3 V to +4.6 V
Digital Input Voltage to DGND	−0.3 V to V_{DD_IO} +0.3 V
V_{AA} to V_{DD}	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
DGND to GND_IO	−0.3 V to +0.3 V
AGND to GND_IO	−0.3 V to +0.3 V
Ambient Operating Temperature (T_A)	0°C to 70°C
Storage Temperature (T_S)	−65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

[1] Analog output short circuit to any power supply or common can be of an indefinite duration.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JC} = 11°C/W

θ_{JA} = 47°C/W

The ADV7320/ADV7321 are Pb-free, environmentally friendly products. They are manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The devices are suitable for Pb-free applications and are able to withstand surface-mount soldering up to 255°C (±5°C).

In addition, they are backward-compatible with conventional SnPb soldering processes. This means that the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

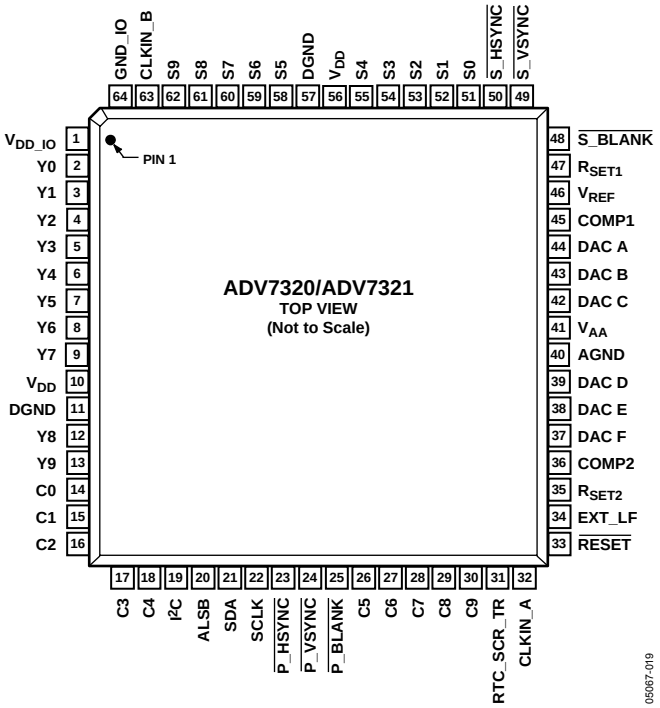


Figure 19. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Input/Output	Description
11, 57	DGND	G	Digital Ground.
40	AGND	G	Analog Ground.
32	CLKIN_A	I	Pixel Clock Input for HD Only (74.25 MHz), PS Only (27 MHz), and SD Only (27 MHz).
63	CLKIN_B	I	Pixel Clock Input. Requires a 27 MHz reference clock for PS mode or a 74.25 MHz (74.1758 MHz) reference clock in HDTV mode. This clock is only used in dual modes.
45, 36	COMP1, COMP2	O	Compensation Pin for DACs. Connect 0.1 µF capacitor from COMP pin to V_{AA}.
44	DAC A	O	CVBS/Green/Y/Y Analog Output.
43	DAC B	O	Chroma/Blue/U/Pb Analog Output.
42	DAC C	O	Luma/Red/V/Pr Analog Output.
39	DAC D	O	In SD Only Mode: CVBS/Green/Y Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Y/Green [HD] Analog Output.
38	DAC E	O	In SD Only Mode: Luma/Blue/U Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Pr/Red Analog Output.
37	DAC F	O	In SD Only Mode: Chroma/Red/V Analog Output; in HD Only Mode and Simultaneous HD/SD Mode: Pb/Blue [HD] Analog Output.
23	$\overline{\text{P_HSYNC}}$	I	Video Horizontal Sync Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
24	$\overline{\text{P_VSYNC}}$	I	Video Vertical Sync Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
25	$\overline{\text{P_BLANK}}$	I	Video Blanking Control Signal for HD in Simultaneous SD/HD Mode and HD Only Mode.
48	$\overline{\text{S_BLANK}}$	I/O	Video Blanking Control Signal for SD Only.
49	$\overline{\text{S_VSYNC}}$	I/O	Video Vertical Sync Control Signal for SD Only.
50	$\overline{\text{S_HSYNC}}$	I/O	Video Horizontal Sync Control Signal for SD Only.
13, 12, 9 to 2	Y9 to Y0	I	SD or PS/HDTV Input Port for Y Data. Input port for interleaved progressive scan data. The LSB is set up on Pin Y0. For 8-bit data input, LSB is set up on Pin Y2.
30 to 26, 18 to 14	C9 to C0	I	PS/HDTV Input Port 4:4:4 Input Mode. This port is used for the Cb[Blue/U] data. The LSB is set up on Pin C0. For 8-bit data input, LSB is set up on Pin C2.

Pin No.	Mnemonic	Input/Output	Description
62 to 58, 55 to 51	S9 to S0	I	SD or PS/HDTV Input Port for Cr[Red/V] Data in 4:4:4 Input Mode. LSB is set up on Pin S0. For 8-bit data input, LSB is set up on Pin S2.
33	$\overline{\text{RESET}}$	I	This input resets the on-chip timing generator and sets the ADV7320/ADV7321 into default register setting. $\overline{\text{RESET}}$ is an active low signal.
47, 35	R_{SET1}, R_{SET2}	I	A 3040 Ω resistor must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs.
22	SCLK	I	I^2C Port Serial Interface Clock Input.
21	SDA	I/O	I^2C Port Serial Data Input/Output.
20	ALSB	I	TTL Address Input. This signal sets up the LSB of the I^2C address. When this pin is tied low, the I^2C filter is activated, which reduces noise on the I^2C interface.
1	V_{DD_IO}	P	Power Supply for Digital Inputs and Outputs.
10, 56	V_{DD}	P	Digital Power Supply.
41	V_{AA}	P	Analog Power Supply.
46	V_{REF}	I/O	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235 V).
34	EXT_LF	I	External Loop Filter for the Internal PLL.
31	RTC_SCR_TR	I	Multifunctional Input. Real-time control (RTC) input, timing reset input, subcarrier reset input.
19	I^2C	I	This input pin must be tied high (V_{DD_IO}) for the ADV7320/ADV7321 to interface over the I^2C port.
64	GND_IO		Digital Input/Output Ground.

TYPICAL PERFORMANCE CHARACTERISTICS

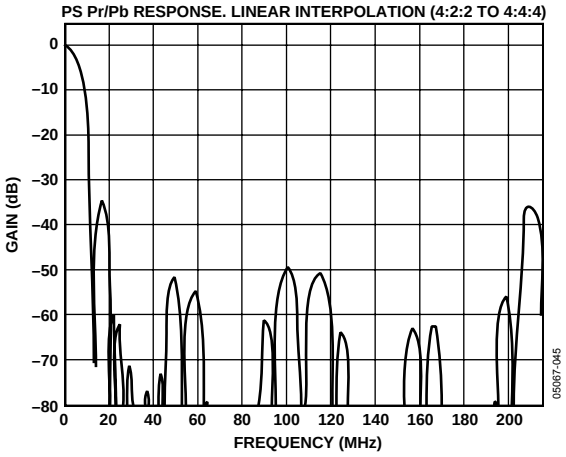


Figure 20. PS—UV 8× Oversampling Filter (Linear)

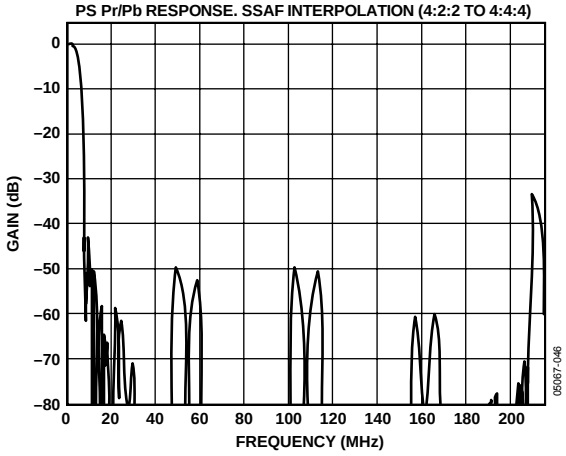


Figure 21. PS—UV 8× Oversampling Filter (SSAF)

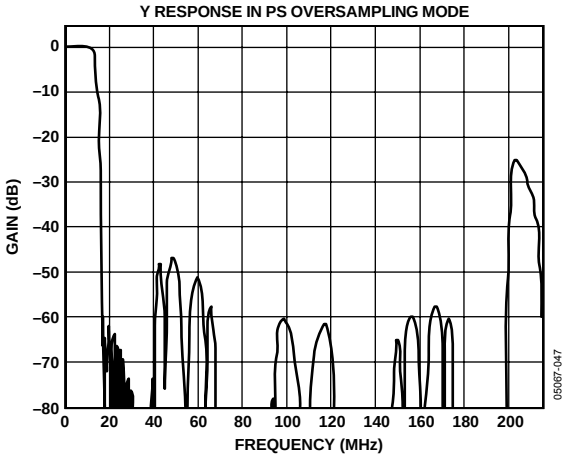


Figure 22. PS—Y 8× Oversampling Filter

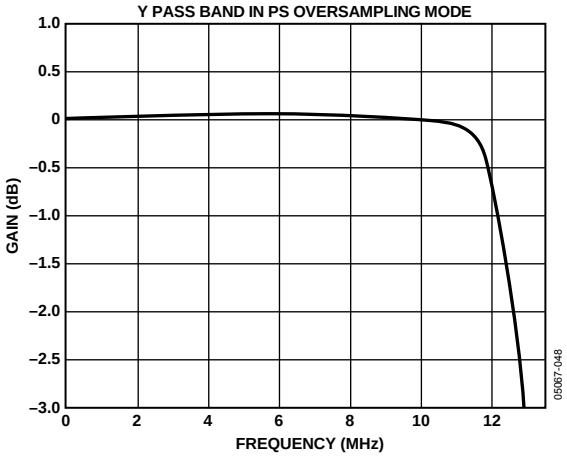


Figure 23. PS—Y 8× Oversampling Filter (Pass Band)

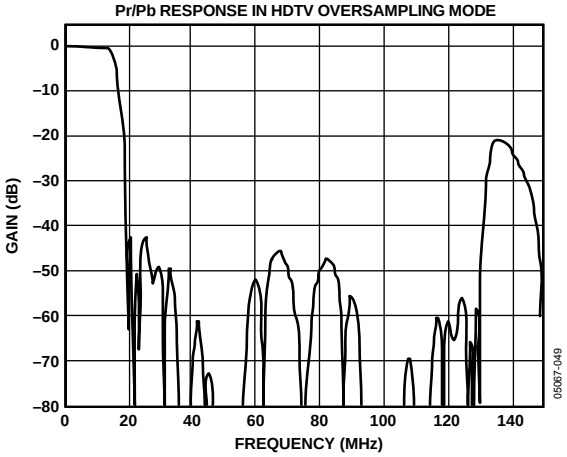


Figure 24. HDTV—UV 2× Oversampling Filter

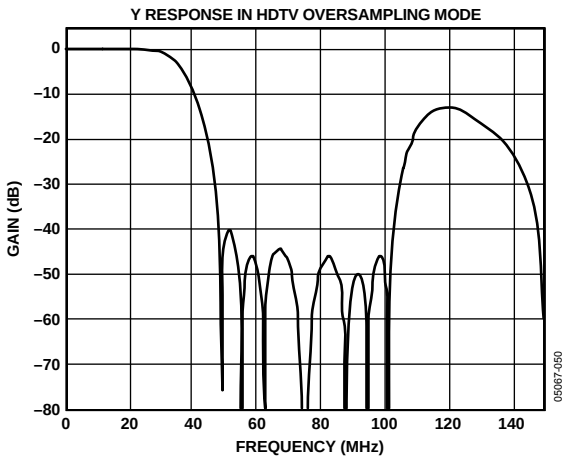


Figure 25. HDTV—Y 2× Oversampling Filter

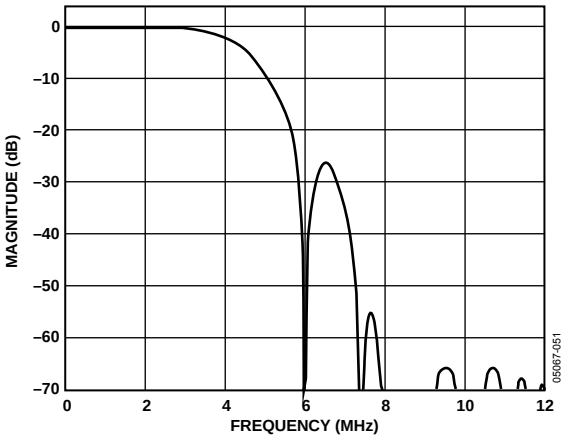


Figure 26. Luma NTSC Low-Pass Filter

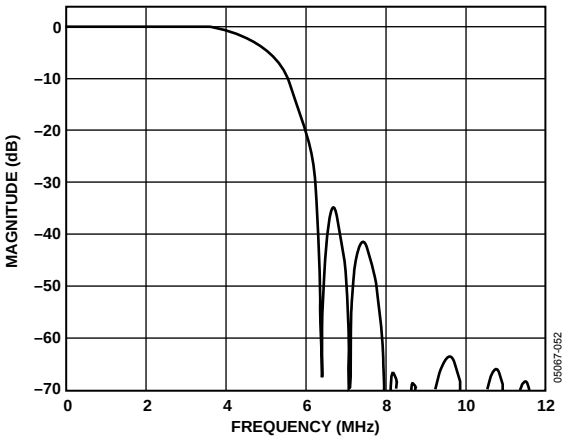


Figure 27. Luma PAL Low-Pass Filter

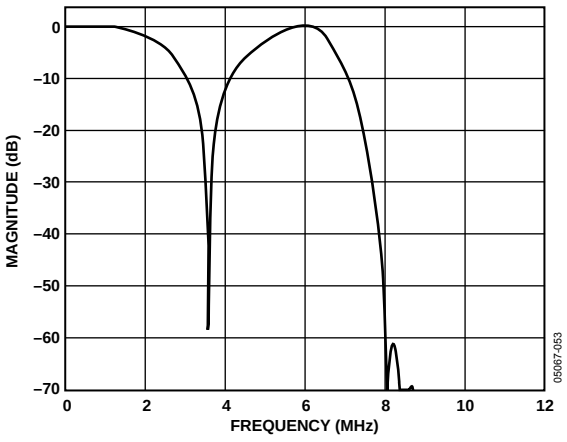


Figure 28. Luma NTSC Notch Filter

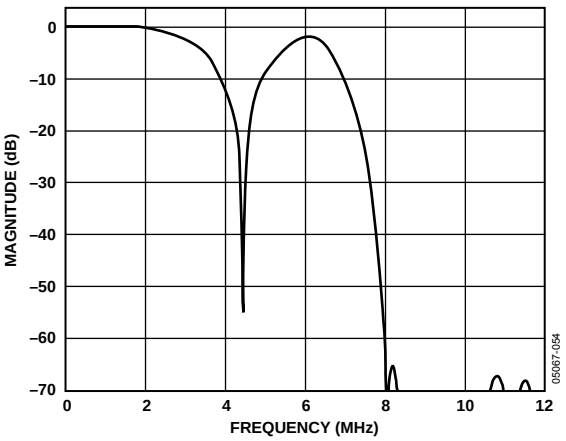


Figure 29. Luma PAL Notch Filter

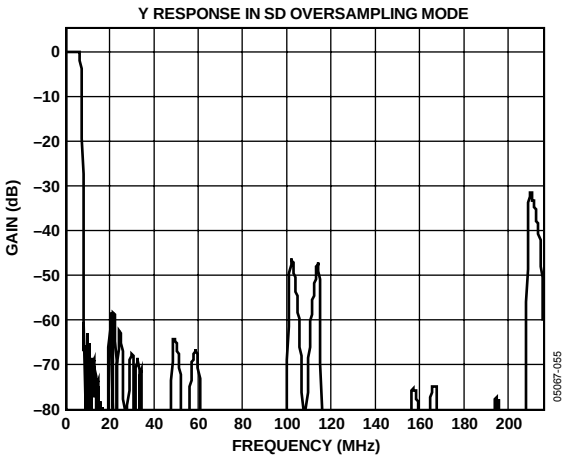


Figure 30. Y—16× Oversampling Filter

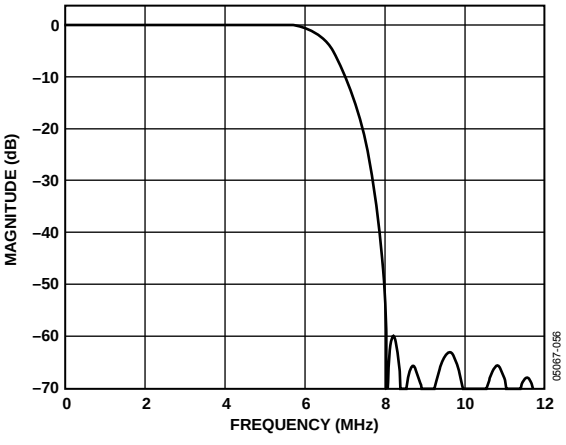


Figure 31. Luma SSAF Filter up to 12 MHz

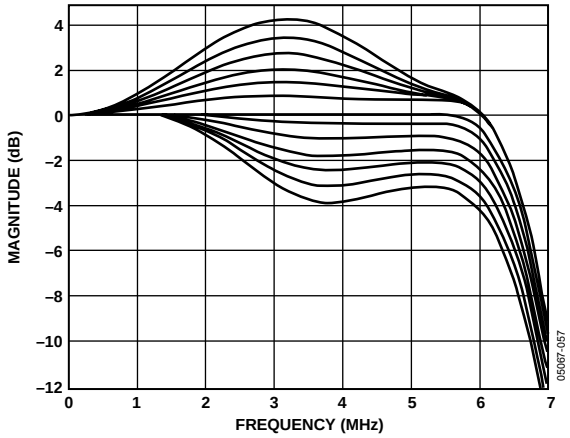


Figure 32. Luma SSAF Filter—Programmable Responses

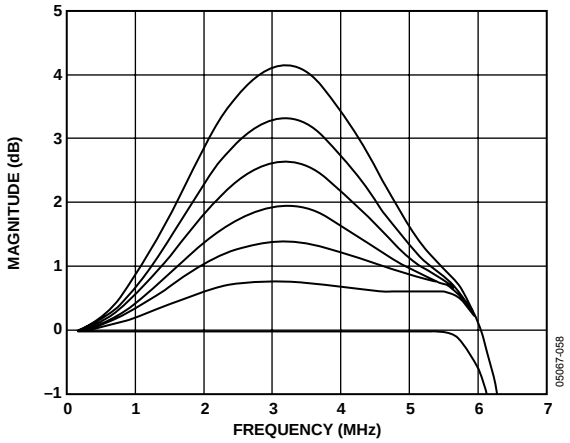


Figure 33. Luma SSAF Filter—Programmable Gain

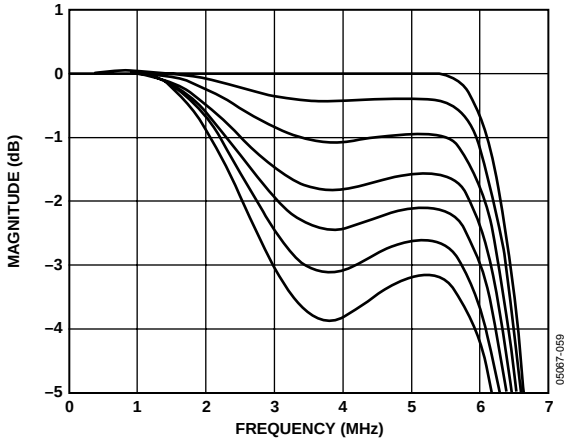


Figure 34. Luma SSAF Filter—Programmable Attenuation

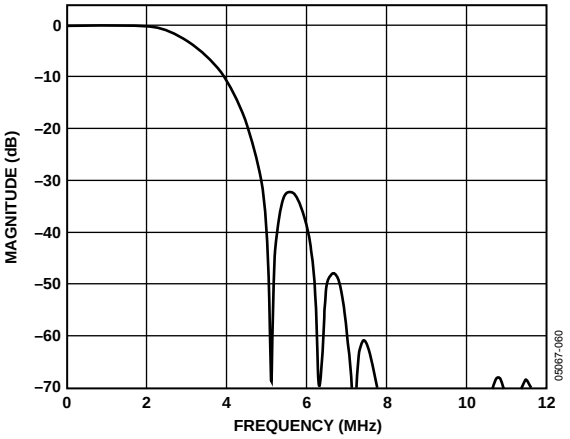


Figure 35. Luma CIF Low-Pass Filter

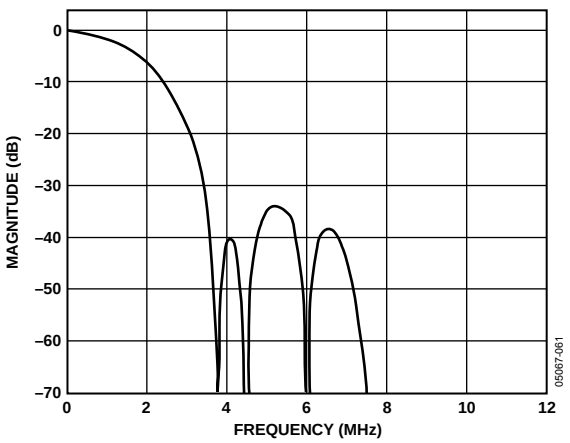


Figure 36. Luma QCIF Low-Pass Filter

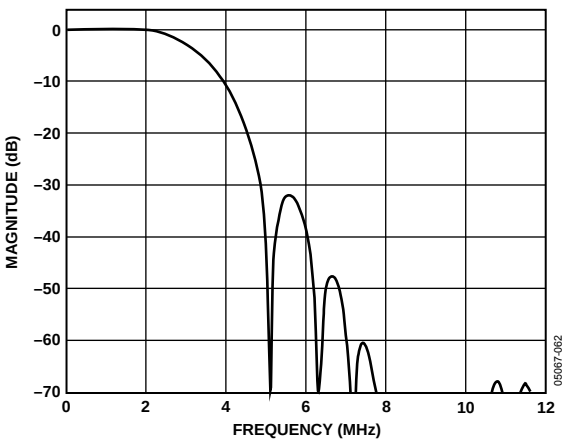


Figure 37. Chroma 3.0 MHz Low-Pass Filter

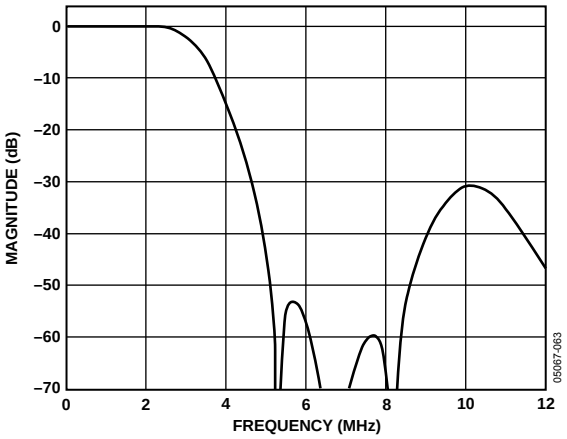


Figure 38. Chroma 2.0 MHz Low-Pass Filter

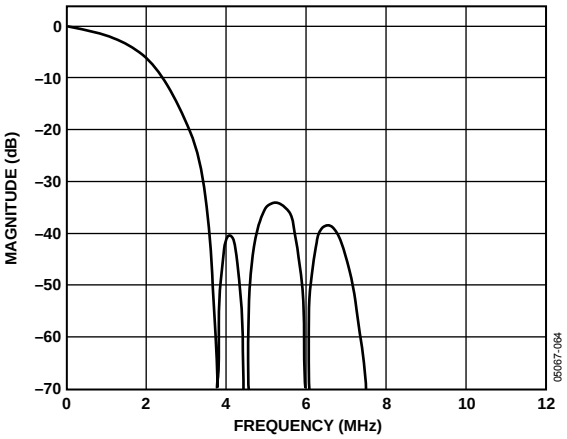


Figure 39. Chroma 1.3 MHz Low-Pass Filter

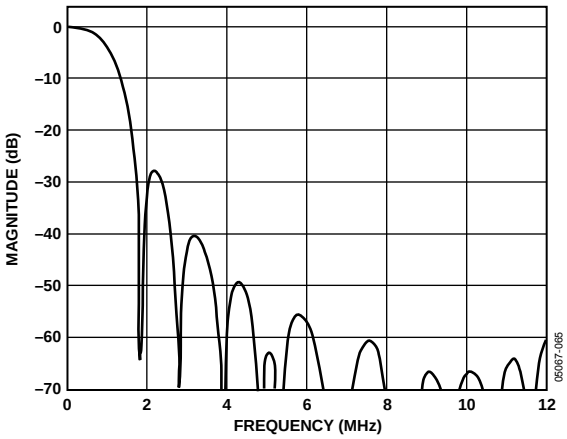


Figure 40. Chroma 1.0 MHz Low-Pass Filter

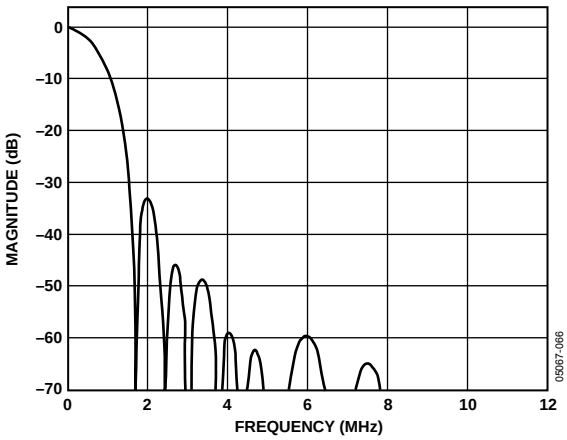


Figure 41. Chroma 0.65 MHz Low-Pass Filter

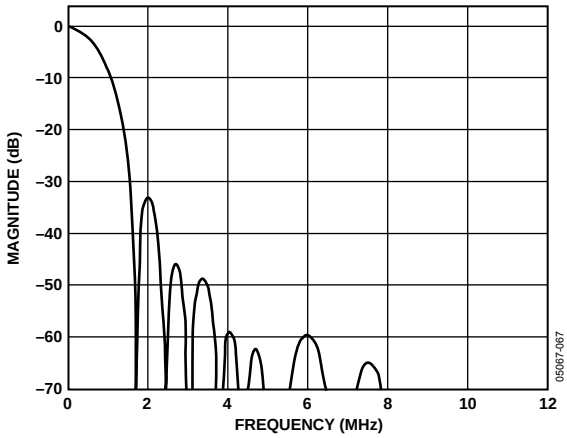


Figure 42. Chroma CIF Low-Pass Filter

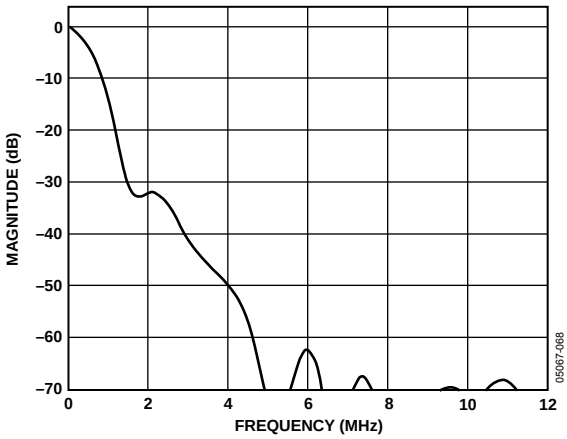


Figure 43. Chroma QCIF Low-Pass Filter

MPU PORT DESCRIPTION

The ADV7320/ADV7321 support a 2-wire serial (I^2C-compatible) microprocessor bus driving multiple peripherals. This port operates in an open-drain configuration. Two inputs, serial data (SDA) and serial clock (SCL), carry information between any device connected to the bus and the ADV7320/ADV7321. Each slave device is recognized by a unique address. The ADV7320/ADV7321 have four possible slave addresses for both read and write operations. These are unique addresses for each device and are illustrated in Figure 44 and Figure 45. The LSB sets either a read or write operation. Logic 1 corresponds to a read operation, while Logic 0 corresponds to a write operation. A1 is enabled by setting the ALSB pin of the ADV7320/ADV7321 to Logic 0 or Logic 1. When ALSB is set to 1, there is greater input bandwidth on the I^2C lines, which allows high speed data transfers on this bus. When ALSB is set to 0, there is reduced input bandwidth on the I^2C lines, which means that pulses of less than 50 ns do not pass into the I^2C internal controller. This mode is recommended for noisy systems.

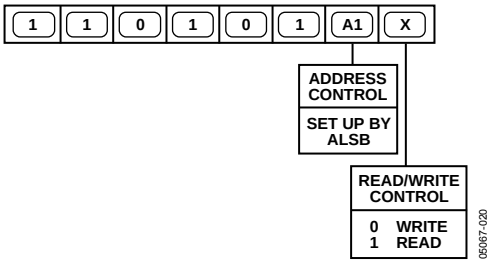


Figure 44. ADV7320 Slave Address = 0xD4

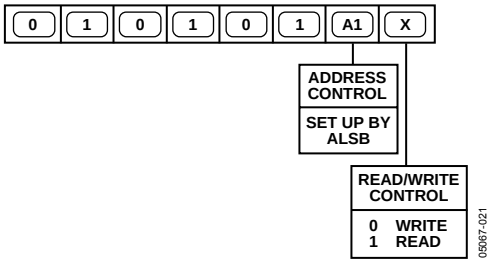


Figure 45. ADV7321 Slave Address = 0x54

To control the various devices on the bus, the following protocol must be followed. First, the master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA while SCL remains high. This indicates that an address/data stream will follow. All peripherals respond to the start condition and shift the next eight bits (7-bit address + R/$\overline{W}$ bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCL lines waiting for the start condition and the correct transmitted address. The R/$\overline{W}$ bit determines the direction of the data.

Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The ADV7320/ADV7321 act as standard slave devices on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit address plus the R/$\overline{W}$ bit. It interprets the first byte as the device address and the second byte as the starting subaddress. There is a subaddress auto-increment facility. This allows data to be written to or read from registers in ascending subaddress sequence starting at any valid subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all of the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause the device to immediately jump to the idle condition. During a given SCL high period, the user should only issue a start condition, a stop condition, or a stop condition followed by a start condition. If an invalid subaddress is issued by the user, the ADV7320/ADV7321 do not issue an acknowledge and return to the idle condition. If the user utilizes the auto-increment method of addressing the encoder and exceeds the highest subaddress, the following actions are taken:

- In read mode, the highest subaddress register contents are output until the master device issues a no acknowledge. This indicates the end of a read. A no acknowledge condition is when the SDA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADV7320/ADV7321, and the part returns to the idle condition.

Before writing to the subcarrier frequency registers, it is required to reset ADV7320/ADV7321 at least once after power-up.

The four subcarrier frequency registers must be updated, starting with Subcarrier Frequency Register 0 and ending with Subcarrier Frequency Register 3. The subcarrier frequency will only update after the last subcarrier frequency register byte has been received by the ADV7320/ADV7321.

Figure 46 illustrates an example of data transfer for a write sequence and the start and stop conditions. Figure 47 shows bus write and read sequences.

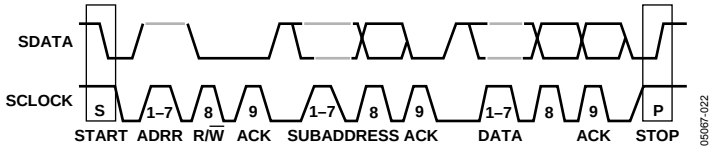


Figure 46. Bus Data Transfer

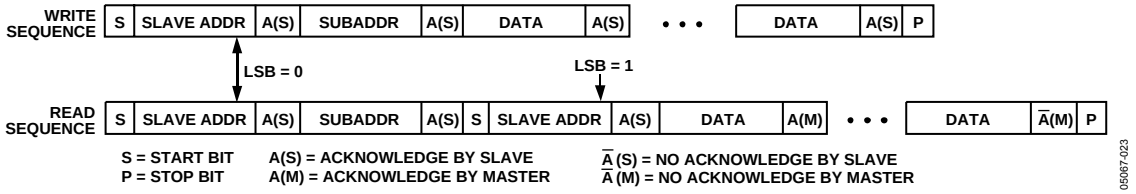


Figure 47. Read and Write Sequences

REGISTER ACCESS

The MPU can write to or read from all registers of the ADV7320/ADV7321 except the subaddress registers, which are write only registers. The subaddress register selected determines which register the next read or write operation will access. All communication with the part through the bus starts with an access to the subaddress register. A read/write operation is then performed from/to the target address, which increments to the next address until a stop command is performed on the bus.

REGISTER PROGRAMMING

The following tables describe the functionality of each register. All registers can be read from and written to, unless otherwise stated.

SUBADDRESS REGISTER (SR7 TO SR0)

Each subaddress register is an 8-bit write only register. After the encoder's bus is accessed and a read or write operation is selected, the subaddress is set up. The subaddress register determines to or from which register the operation takes place.

Table 7. Registers 0x00 to 0x01

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Value (Shaded)
0x00	Power Mode Register	Sleep Mode. With this control enabled, the current consumption is reduced to µA level. All DACs and the internal PLL cct are disabled. I^2C registers can be read from and written to in sleep mode.								0 1	Sleep mode off. Sleep mode on.	0xFC
		PLL and Oversampling Control. This control allows the internal PLL cct to be powered down and the oversampling to be switched off.							0 1		PLL on. PLL off.	
		DAC F: Power On/Off.						0 1			DAC F off. DAC F on.	
		DAC E: Power On/Off.					0 1				DAC E off. DAC E on.	
		DAC D: Power On/Off.				0 1					DAC D off. DAC D on.	
		DAC C: Power On/Off.			0 1						DAC C off. DAC C on.	
		DAC B: Power On/Off.		0 1							DAC B off. DAC B on.	
		DAC A: Power On/Off.	0 1								DAC A off. DAC A on.	
0x01	Mode Select Register	Reserved.								0	Reserved.	
		Clock Edge.							0 1		Cb clocked upon rising edge. Y clocked upon rising edge.	Only for PS interleaved input at 27 MHz.
		Reserved.						0				
		Clock Align.					0 1				Must be set if the phase delay between the two input clocks is <9.25 ns or >27.75 ns.	Only if two input clocks are used.
		Input Mode.		0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1					SD input only. PS input only. HDTV input only. SD and PS (20-bit). SD and PS (10-bit). SD and HDTV (SD oversampled). SD and HDTV (HDTV oversampled). PS only (at 54 MHz).	0x38
		Y/C/S Bus Swap.	0 1								Allows data to be applied to data ports in various configurations (SD feature only).	See Table 21.

Table 8. Registers 0x02 to 0x0F

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
0x02	Mode Register 0	Reserved							0	0	0 must be written to these bits.	0x20
		Test Pattern Black Bar						0 1			Disabled. Enabled.	0x11, Bit 2 must also be enabled.
		Manual RGB Matrix Adjust					0 1				Disable manual RGB matrix adjust. Enable manual RGB matrix adjust.	
		Sync on RGB[1]				0 1					No sync. Sync on all RGB outputs.	
		RGB/YPrPb Output			0 1						RGB component outputs. YPrPb component outputs.	
		SD Sync		0 1							No sync output. Output SD syncs on S_HSYNC, S_VSYNC, S_BLANK pins.	
		HD Sync	0 1								No sync output. Output HD, ED, syncs on S_HSYNC, S_VSYNC.	
0x03	RGB Matrix 0								x	x	LSB for GY.	0x03
0x04	RGB Matrix 1		 x	 x	 x	 x	x	x	x	x	LSB for RV. LSB for BU. LSB for GV. LSB for GU.	0xF0
0x05	RGB Matrix 2		x	x	x	x	x	x	x	x	Bits 9 to 2 for GY.	0x4E
0x06	RGB Matrix 3		x	x	x	x	x	x	x	x	Bits 9 to 2 for GU.	0x0E
0x07	RGB Matrix 4		x	x	x	x	x	x	x	x	Bits 9 to 2 for GV.	0x24
0x08	RGB Matrix 5		x	x	x	x	x	x	x	x	Bits 9 to 2 for BU.	0x92
0x09	RGB Matrix 6		x	x	x	x	x	x	x	x	Bits 9 to 2 for RV.	0x7C
0x0A	DAC A, B, C Output Level[2]	Positive Gain to DAC Output Voltage	0 0 0 0 0	0 0 0 0 1	0 0 0 1 0	0 0 0 1 0	0 0 0 1 0	0 0 0 1 0	0 0 1 1 0	0 1 0 … 1 0	0% +0.018% +0.036% … +7.382% +7.5%	0x00
		Negative Gain to DAC Output Voltage	1 1 1 1	1 1 0 1	0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1	0 0 1 1	0 1 0 … 1	−7.5% −7.382% −7.364% … −0.018%	
0x0B	DAC D, E, F Output Level	Positive Gain to DAC Output Voltage	0 0 0 0 0	0 0 0 0 1	0 0 0 1 0	0 0 0 1 0	0 0 0 1 0	0 0 0 1 0	0 0 1 1 0	0 1 0 … 1 0	0% +0.018% +0.036% … +7.382% +7.5%	0x00
		Negative Gain to DAC Output Voltage	1 1 1 1	1 1 0 1	0 0 0 1	0 0 0 1	0 0 0 1	0 0 0 1	0 0 1 1	0 1 0 … 1	−7.5% −7.382% −7.364% … −0.018%	
0x0C		Reserved										0x00
0x0D		Reserved										0x00
0x0E		Reserved										0x00
0x0F		Reserved										0x00

[1] For more detail, refer to Appendix 7.
[2] For more detail on the programmable output levels, refer to the Programmable DAC Gain Control section.

Table 9. Registers 0x10 to 0x11

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Note	Reset Values
0x10	HD Mode Register 1	HD Output Standard							0	0	EIA770.2 output		0x00
									0	1	EIA770.1 output		
									1	0	Output levels for full input range		
									1	1	Reserved		
		Input Sync Format						0			$\overline{\text{HSYNC}}$, VSYNC, $\overline{\text{BLANK}}$		
								1			EAV/SAV codes		
		HD/ED Input Mode	0	0	0	0	0				SMPTE 293M, ITU-BT. 1358	525p @ 59.94 Hz	
			0	0	0	0	1				Async mode		
			0	0	0	1	0				BTA-1004, ITU-BT. 1362	525p @ 59.94 Hz	
			0	0	0	1	1				ITU-BT. 1358	625p @ 50 Hz	
			0	0	1	0	0				ITU-BT. 1362	625p @ 50 Hz	
			0	0	1	0	1				SMPTE 296M-1, -2	720p @ 60/59.94 Hz	
			0	0	1	1	0				SMPTE 296M-3	720p @ 50 Hz	
			0	0	1	1	1				SMPTE 296M-4, -5	720p @ 30/29.97 Hz	
			0	1	0	0	0				SMPTE 296M-6	720p @ 25 Hz	
			0	1	0	0	1				SMPTE 296M-7, -8	720p @ 24/23.98 Hz	
			0	1	0	1	0				SMPTE 240M	1035i @ 60/59.94 Hz	
			0	1	0	1	1				Reserved		
			0	1	1	0	0				Reserved		
			0	1	1	0	1				SMPTE 274M-4, -5	1080i @ 30/29.97 Hz	
			0	1	1	1	0				SMPTE 274M-6	1080i @ 25 Hz	
			0	1	1	1	1				SMPTE 274M-7, -8	1080p @ 30/29.97 Hz	
			1	0	0	0	0				SMPTE 274M-9	1080p @ 25 Hz	
			1	0	0	0	1				SMPTE 274M-10, -11	1080p @ 24/23.98 Hz	
			10010–11111								Reserved		
0x11	HD Mode Register 2	HD Pixel Data Valid								0	Pixel data valid off		0x00
										1	Pixel data valid on		
									0		Reserved		
		HD Test Pattern Enable						0			HD test pattern off		
								1			HD test pattern on		
		HD Test Pattern Hatch/Field					0				Hatch		
							1				Field/frame		
		HD VBI Open				0					Disabled		
						1					Enabled		
		HD Undershoot Limiter		0	0						Disabled	Only available in EDTV (525p/625p)	
				0	1						–11 IRE		
				1	0						–6 IRE		
				1	1						–1.5 IRE		
		HD Sharpness Filter	0								Disabled		
			1								Enabled		

Table 10. Register 0x12

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
0x12	HD Mode Register 3	HD Y Delay with Respect to Falling Edge of $\overline{\text{HSYNC}}$						0 0 0 0 1	0 0 1 1 0	0 1 0 1 0	0 clock cycles 1 clock cycle 2 clock cycles 3 clock cycles 4 clock cycles	0x00
		HD Color Delay with Respect to Falling Edge of $\overline{\text{HSYNC}}$			0 0 0 0 1	0 0 1 1 0	0 1 0 1 0				0 clock cycles 1 clock cycle 2 clock cycles 3 clock cycles 4 clock cycles	
		HD CGMS		0 1							Disabled Enabled	
		HD CGMS CRC	0 1								Disabled Enabled	

Table 11. Registers 0x13 to 0x14

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
0x13	HD Mode Register 4	HD Cr/Cb Sequence								0 1	Cb after falling edge of $\overline{\text{HSYNC}}$. Cr after falling edge of $\overline{\text{HSYNC}}$.	0x4C
		Reserved							0		0 must be written to this bit.	
		HD Input Format						0 1			8-bit input. 10-bit input.	
		Sinc Filter on DAC D, E, F					0 1				Disabled. Enabled.	
		Reserved				0					0 must be written to this bit.	
		HD Chroma SSAF			0 1						Disabled. Enabled.	
		HD Chroma Input		0 1							4:4:4 4:2:2	
		HD Double Buffering	0 1								Disabled. Enabled.	
0x14	HD Mode Register 5	HD Timing Reset								x	A low-high-low transition resets the internal HD timing counters.	0x00
		HD Hsync Generation[1]							0 1		Refer to the $\overline{\text{HSYNC}}$/$\overline{\text{VSYNC}}$ Output Control section.	
		HD Vsync Generation[1]						0 1				
		HD Blank Polarity					0 1				$\overline{\text{BLANK}}$ active high. $\overline{\text{BLANK}}$ active low.	
		HD Macrovision for 525p and 625p				0 1					Macrovision disabled. Macrovision enabled.	
		Reserved			0						0 must be written to these bits.	
		HD $\overline{\text{VSYNC}}$/Field Input		0 1							0 = field input. 1 = $\overline{\text{VSYNC}}$ input.	
		Horizontal/Vertical Counters[2]	0 1								Update field/line counter. Field/line counter free running.	

[1] Used in conjunction with HD_SYNC in Register 0x02, Bit 7, set to 1.
[2] When set to 0, the horizontal/vertical counters automatically wrap around at the end of the line/field/frame of the standard selected. When set to 1, the horizontal/vertical counters are free running and wrap around when external sync signals indicate to do so.

Table 12. Register 0x15

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
0x15	HD Mode Register 6	Reserved								0	0 must be written to this bit.	0x00
		HD RGB Input							0 1		Disabled. Enabled.	
		HD Sync on PrPb						0 1			Disabled. Enabled.	
		HD Color DAC Swap					0 1				DAC E = Pb; DAC F = Pr. DAC E = Pr; DAC F = Pb.	
		HD Gamma Curve A				0					Gamma Curve A.	
		HD Gamma Curve B				1					Gamma Curve B.	
		HD Gamma Curve Enable			0 1						Disabled. Enabled.	
		HD Adaptive Filter Mode		0 1							Mode A. Mode B.	
		HD Adaptive Filter Enable	0 1								Disabled. Enabled.	

Table 13. Registers 0x16 to 0x37

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
0x16	HD Y Level[1]		x	x	x	x	x	x	x	x	Y level value	0xA0
0x17	HD Cr Level[1]		x	x	x	x	x	x	x	x	Cr level value	0x80
0x18	HD Cb Level[1]		x	x	x	x	x	x	x	x	Cb level value	0x80
0x19		Reserved										0x00
0x1A		Reserved										0x00
0x1B		Reserved										0x00
0x1C		Reserved										0x00
0x1D		Reserved										0x00
0x1E		Reserved										0x00
0x1F		Reserved										0x00
0x20	HD Sharpness Filter Gain	HD Sharpness Filter Gain Value A					0 0 … 0 1 … 1	0 0 … 1 0 … 1	0 0 … 1 0 … 1	0 1 … 1 0 … 1	Gain A = 0 Gain A = +1 … Gain A = +7 Gain A = −8 … Gain A = −1	0x00
		HD Sharpness Filter Gain Value B	0 0 … 0 1 … 1	0 0 … 1 0 … 1	0 0 … 1 0 … 1	0 1 … 1 0 … 1					Gain B = 0 Gain B = +1 … Gain B = +7 Gain B = −8 … Gain B = −1	
0x21	HD CGMS Data 0	HD CGMS Data Bits	0	0	0	0	C19	C18	C17	C16	CGMS 19 to 16	0x00
0x22	HD CGMS Data 1	HD CGMS Data Bits	C15	C14	C13	C12	C11	C10	C9	C8	CGMS 15 to 8	0x00
0x23	HD CGMS Data 2	HD CGMS Data Bits	C7	C6	C5	C4	C3	C2	C1	C0	CGMS 7 to 0	0x00
0x24	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A0	0x00
0x25	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A1	0x00
0x26	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A2	0x00
0x27	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A3	0x00
0x28	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A4	0x00
0x29	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A5	0x00
0x2A	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A6	0x00
0x2B	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A7	0x00
0x2C	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A8	0x00
0x2D	HD Gamma A	HD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A9	0x00
0x2E	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B0	0x00
0x2F	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B1	0x00
0x30	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B2	0x00
0x31	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B3	0x00
0x32	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B4	0x00
0x33	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B5	0x00
0x34	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B6	0x00
0x35	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B7	0x00
0x36	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B8	0x00
0x37	HD Gamma B	HD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B9	0x00

[1] For use with internal test pattern only.

Table 14. Registers 0x38 to 0x3D

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
0x38	HD Adaptive Filter Gain 1	HD Adaptive Filter Gain 1, Value A					0 0 … 0 1 … 1	0 0 … 1 0 … 1	0 0 … 1 0 … 1	0 1 … 1 0 … 1	Gain A = 0 Gain A = +1 … Gain A = +7 Gain A = −8 … Gain A = −1	0x00
		HD Adaptive Filter Gain 1, Value B	0 0 … 0 1 … 1	0 0 … 1 0 … 1	0 0 … 1 0 … 1	0 1 … 1 0 … 1					Gain B = 0 Gain B = +1 … Gain B = +7 Gain B = −8 … Gain B = −1	
0x39	HD Adaptive Filter Gain 2	HD Adaptive Filter Gain 2, Value A					0 0 … 0 1 … 1	0 0 … 1 0 … 1	0 0 … 1 0 … 1	0 1 … 1 0 … 1	Gain A = 0 Gain A = +1 … Gain A = +7 Gain A = −8 … Gain A = −1	0x00
		HD Adaptive Filter Gain 2, Value B	0 0 … 0 1 … 1	0 0 … 1 0 … 1	0 0 … 1 0 … 1	0 1 … 1 0 … 1					Gain B = 0 Gain B = +1 … Gain B = +7 Gain B = −8 … Gain B = −1	
0x3A	HD Adaptive Filter Gain 3	HD Adaptive Filter Gain 3, Value A					0 0 … 0 1 … 1	0 0 … 1 0 … 1	0 0 … 1 0 … 1	0 1 … 1 0 … 1	Gain A = 0 Gain A = +1 … Gain A = +7 Gain A = −8 … Gain A = −1	0x00
		HD Adaptive Filter Gain 3, Value B	0 0 … 0 1 … 1	0 0 … 1 0 … 1	0 0 … 1 0 … 1	0 1 … 1 0 … 1					Gain B = 0 Gain B = +1 … Gain B = +7 Gain B = −8 … Gain B = −1	
0x3B	HD Adaptive Filter Threshold A	HD Adaptive Filter Threshold A	x	x	x	x	x	x	x	x	Threshold A	0x00
0x3C	HD Adaptive Filter Threshold B	HD Adaptive Filter Threshold B	x	x	x	x	x	x	x	x	Threshold B	0x00
0x3D	HD Adaptive Filter Threshold C	HD Adaptive Filter Threshold C	x	x	x	x	x	x	x	x	Threshold C	0x00

Table 15. Registers 0x3E to 0x43

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
0x3E		Reserved										0x00
0x3F		Reserved										0x00
0x40	SD Mode Register 0	SD Standard							0	0	NTSC.	0x00
									0	1	PAL B, D, G, H, I.	
									1	0	PAL M.	
									1	1	PAL N.	
		SD Luma Filter				0	0	0			LPF NTSC.	
						0	0	1			LPF PAL.	
						0	1	0			Notch NTSC.	
						0	1	1			Notch PAL.	
						1	0	0			SSAF luma.	
						1	0	1			Luma CIF.	
						1	1	0			Luma QCIF.	
						1	1	1			Reserved.	
		SD Chroma Filter	0	0	0						1.3 MHz.	
			0	0	1						0.65 MHz.	
			0	1	0						1.0 MHz.	
			0	1	1						2.0 MHz.	
			1	0	0						Reserved.	
			1	0	1						Chroma CIF.	
			1	1	0						Chroma QCIF.	
			1	1	1						3.0 MHz.	
0x41		Reserved										0x00
0x42	SD Mode Register 1	SD PrPb SSAF								0	Disabled.	0x08
										1	Enabled.	
		SD DAC Output 1							0		Refer to the Output Configuration section.	
									1			
		SD DAC Output 2						0			Refer to the Output Configuration section.	
								1				
		SD Pedestal					0				Disabled.	
							1				Enabled.	
		SD Square Pixel				0					Disabled.	
						1					Enabled.	
		SD VCR FF/RW Sync			0						Disabled.	
					1						Enabled.	
		SD Pixel Data Valid		0							Disabled.	
				1							Enabled.	
		SD SAV/EAV Step Edge Control	0								Disabled.	
			1								Enabled.	
0x43	SD Mode Register 2	SD Pedestal YPrPb Output								0	No pedestal on YUV.	0x00
										1	7.5 IRE pedestal on YUV.	
		SD Output Levels Y							0		Y = 700 mV/300 mV.	
									1		Y = 714 mV/286 mV.	
		SD Output Levels PrPb					0	0			700 mV p-p (PAL); 1000 mV p-p (NTSC).	
							0	1			700 mV p-p.	
							1	0			1000 mV p-p.	
							1	1			648 mV p-p.	
		SD VBI Open				0					Disabled.	
						1					Enabled.	
		SD CC Field Control		0	0						CC disabled.	
				0	1						CC on odd field only.	
				1	0						CC on even field only.	
				1	1						CC on both fields.	
		Reserved	0								Reserved.	

Table 16. Registers 0x44 to 0x49

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
0x44	SD Mode Register 3	SD $\overline{\text{VSYNC}}$-3H								0 1	Disabled $\overline{\text{VSYNC}}$ = 2.5 lines (PAL), $\overline{\text{VSYNC}}$ = 3 lines (NTSC)	0x00
		SD RTC/TR/SCR						0 0 1 1	0 1 0 1		Genlock disabled Subcarrier reset Timing reset RTC enabled	
		SD Active Video Length					0 1				720 pixels 710 (NTSC)/702 (PAL)	
		SD Chroma				0 1					Chroma enabled Chroma disabled	
		SD Burst			0 1						Enabled Disabled	
		SD Color Bars		0 1							Disabled Enabled	
		SD DAC Swap	0 1								DAC A = luma, DAC B = chroma DAC A = chroma, DAC B = luma	
0x45	Reserved											0x00
0x46	SD Mode Register 4	NTSC Color Subcarrier Adjust (Falling Edge of HS to Start of Color Burst)[1]							0 0 1 1	0 1 0 1	5.17 µs 5.31 µs (default) 5.59 µs (must be set for Macrovision compliance) Reserved	0x01
0x47	SD Mode Register 5	SD PrPb Scale								0 1	Disabled Enabled	0x00
		SD Y Scale							0 1		Disabled Enabled	
		SD Hue Adjust						0 1			Disabled Enabled	
		SD Brightness					0 1				Disabled Enabled	
		SD Luma SSAF Gain				0 1					Disabled Enabled	
		Reserved			0						0 must be written to this bit	
		Reserved		0							0 must be written to this bit	
		Reserved	0								0 must be written to this bit	
0x48	SD Mode Register 6	Reserved								0		0x00
		Reserved							0		0 must be written to this bit	
		SD Double Buffering						0 1			Disabled Enabled	
		SD Input Format				0 0 1 1	0 1 0 1				8-bit input 16-bit input 10-bit input 20-bit input	
		SD Digital Noise Reduction			0 1						Disabled Enabled	
		SD Gamma Control		0 1							Disabled Enabled	
		SD Gamma Curve	0 1								Gamma Curve A Gamma Curve B	
0x49	SD Mode Register 7	SD Undershoot Limiter							0 0 1 1	0 1 0 1	Disabled −11 IRE −6 IRE −1.5 IRE	0x00
		Reserved						0			0 must be written to this bit	
		SD Black Burst Output on DAC Luma					0 1				Disabled Enabled	
		SD Chroma Delay			0 0 1 1	0 1 0 1					Disabled 4 clock cycles 8 clock cycles Reserved	
		Reserved		0							0 must be written to this bit	
		Reserved	0								0 must be written to this bit	

[1] NTSC color bar adjust should be set to 10 b for Macrovision compliance (ADV7320 only).

Table 17. Registers 0x4A to 0x58

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Value
0x4A	SD Timing Register 0	SD Slave/Master Mode								0 1	Slave mode. Master mode.	0x08
		SD Timing Mode						0 0 1 1	0 1 0 1		Mode 0. Mode 1. Mode 2. Mode 3.	
		SD BLANK Input					0 1				Enabled. Disabled.	
		SD Luma Delay			0 0 1 1	0 1 0 1					No delay. 2 clock cycles. 4 clock cycles. 6 clock cycles.	
		SD Min. Luma Value		0 1							−40 IRE. −7.5 IRE.	
		SD Timing Reset	x	0	0	0	0	0	0	0	A low-high-low transition resets the internal SD timing counters.	
0x4B	SD Timing Register 1	SD $\overline{\text{HSYNC}}$ Width							0 0 1 1	0 1 0 1	T_a = 1 clock cycle. T_a = 4 clock cycles. T_a = 16 clock cycles. T_a = 128 clock cycles.	0x00
		SD $\overline{\text{HSYNC}}$ to $\overline{\text{VSYNC}}$ Delay					0 0 1 1	0 1 0 1			T_b = 0 clock cycle. T_b = 4 clock cycles. T_b = 8 clock cycles. T_b = 18 clock cycles.	
		SD $\overline{\text{HSYNC}}$ to $\overline{\text{VSYNC}}$ Rising Edge Delay (Mode 1 Only)			x x	0 1					$T_c = T_b$. $T_c = T_b$ + 32 µs.	
		$\overline{\text{VSYNC}}$ Width (Mode 2 Only)			0 0 1 1	0 1 0 1					1 clock cycle. 4 clock cycles. 16 clock cycles. 128 clock cycles.	
		$\overline{\text{HSYNC}}$ to Pixel Data Adjust	0 0 1 1	0 1 0 1							0 clock cycles. 1 clock cycle. 2 clock cycles. 3 clock cycles.	
0x4C	SD F_{SC} Register 0[1]		x	x	x	x	x	x	x	x	Subcarrier Frequency Bits 7 to 0.	0x1E[1]
0x4D	SD F_{SC} Register 1		x	x	x	x	x	x	x	x	Subcarrier Frequency Bits 15 to 8.	0x7C
0x4E	SD F_{SC} Register 2		x	x	x	x	x	x	x	x	Subcarrier Frequency Bits 23 to 16.	0xF0
0x4F	SD F_{SC} Register 3		x	x	x	x	x	x	x	x	Subcarrier Frequency Bits 31 to 24.	0x21
0x50	SD F_{SC} Phase		x	x	x	x	x	x	x	x	Subcarrier Phase Bits 9 to 2.	0x00
0x51	SD Closed Captioning	Extended Data on Even Fields	x	x	x	x	x	x	x	x	Extended Data Bits 7 to 0.	0x00
0x52	SD Closed Captioning	Extended Data on Even Fields	x	x	x	x	x	x	x	x	Extended Data Bits 15 to 8.	0x00
0x53	SD Closed Captioning	Data on Odd Fields	x	x	x	x	x	x	x	x	Data Bits 7 to 0.	0x00
0x54	SD Closed Captioning	Data on Odd Fields	x	x	x	x	x	x	x	x	Data Bits 15 to 8.	0x00
0x55	SD Pedestal Register 0	Pedestal on Odd Fields	17	16	15	14	13	12	11	10	Setting any of these bits to 1 disables pedestal on the line number indicated by the bit settings.	0x00
0x56	SD Pedestal Register 1	Pedestal on Odd Fields	25	24	23	22	21	20	19	18		0x00
0x57	SD Pedestal Register 2	Pedestal on Even Fields	17	16	15	14	13	12	11	10		0x00
0x58	SD Pedestal Register 3	Pedestal on Even Fields	25	24	23	22	21	20	19	18		0x00

[1] For precise NTSC F_{SC}, this register should be programmed to 0x1F.

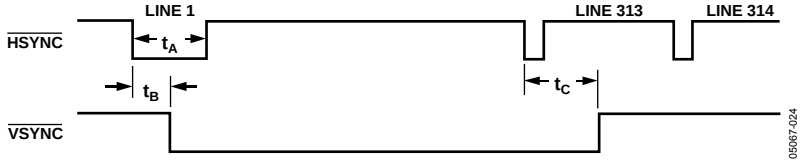


Figure 48. Timing Register 1 in PAL Mode

Table 18. Registers 0x59 to 0x64

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
0x59	SD CGMS/WSS 0	SD CGMS Data					19	18	17	16	CGMS Data Bits C19 to C16	0x00
		SD CGMS CRC				0 1					Disabled Enabled	
		SD CGMS on Odd Fields			0 1						Disabled Enabled	
		SD CGMS on Even Fields		0 1							Disabled Enabled	
		SD WSS	0 1								Disabled Enabled	
0x5A	SD CGMS/WSS 1	SD CGMS/WSS Data	 15	 14	13	12	11	10	9	8	CGMS Data Bits C13 to C8, or WSS Data Bits C13 to C8 CGMS Data Bits C15 to C14	0x00 0x00
0x5B	SD CGMS/WSS 2	SD CGMS/WSS Data	7	6	5	4	3	2	1	0	CGMS/WSS Data Bits C7 to C0	0x00
0x5C	SD LSB Register	SD LSB for Y Scale Value							x	x	SD Y Scale Bits 1 to 0	
		SD LSB for Cb Scale Value					x	x			SD Cb Scale Bits 1 to 0	
		SD LSB for Cr Scale Value			x	x					SD Cr Scale Bits 1 to 0	
		SD LSB for F_{SC} Phase	x	x							Subcarrier Phase Bits 1 to 0	
0x5D	SD Y Scale Register	SD Y Scale Value	x	x	x	x	x	x	x	x	SD Y Scale Bits 7 to 2	0x00
0x5E	SD Cb Scale Register	SD Cb Scale Value	x	x	x	x	x	x	x	x	SD Cb Scale Bits 7 to 2	0x00
0x5F	SD Cr Scale Register	SD Cr Scale Value	x	x	x	x	x	x	x	x	SD Cr Scale Bits 7 to 2	0x00
0x60	SD Hue Register	SD Hue Adjust Value	x	x	x	x	x	x	x	x	SD Hue Adjust Bits 7 to 0	0x00
0x61	SD Brightness/WSS	SD Brightness Value		x	x	x	x	x	x	x	SD Brightness Bits 6 to 0	0x00
		SD Blank WSS Data	0 1								Disabled Enabled	Line 23
0x62	SD Luma SSAF	SD Luma SSAF Gain/Attenuation	0 0 0	0 0 0	0 0 0	0 0 0	0 0 1	0 1 1	0 1 0	0 0 0	−4 dB 0 dB +4 dB	0x00
0x63	SD DNR 0	Coring Gain Border					0 0 0 0 0 0 0 0 1	0 0 0 0 1 1 1 1 0	0 0 1 1 0 0 1 1 0	0 1 0 1 0 1 0 1 0	No gain +1/16 [−1/8] +2/16 [−2/8] +3/16 [−3/8] +4/16 [−4/8] +5/16 [−5/8] +6/16 [−6/8] +7/16 [−7/8] +8/16 [−1]	0x00 In DNR mode, the values in brackets apply.
		Coring Gain Data	0 0 0 0 0 0 0 0 1	0 0 0 0 1 1 1 1 0	0 0 1 1 0 0 1 1 0	0 1 0 1 0 1 0 1 0					No gain +1/16 [−1/8] +2/16 [−2/8] +3/16 [−3/8] +4/16 [−4/8] +5/16 [−5/8] +6/16 [−6/8] +7/16 [−7/8] +8/16 [−1]	
0x64	SD DNR 1	DNR Threshold			0 0 … 1 1	0 0 … 1 1	0 0 … 1 1	0 0 … 1 1	0 0 … 1 1	0 1 … 0 1	0 1 … 62 63	0x00
		Border Area		0 1							2 pixels 4 pixels	
		Block Size Control	0 1								8 pixels 16 pixels	

Table 19. Registers 0x65 to 0x7C

SR7–SR0	Register	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
0x65	SD DNR 2	DNR Input Select						0	0	1	Filter A	0x00
								0	1	0	Filter B	
								0	1	1	Filter C	
								1	0	0	Filter D	
		DNR Mode				0					DNR mode	
						1					DNR sharpness mode	
		DNR Block Offset	0	0	0	0					0 pixel offset	
			0	0	0	1					1 pixel offset	
			…	…	…	…					…	
			1	1	1	0					14 pixel offset	
			1	1	1	1					15 pixel offset	
0x66	SD Gamma A	SD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A0	0x00
0x67	SD Gamma A	SD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A1	0x00
0x68	SD Gamma A	SD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A2	0x00
0x69	SD Gamma A	SD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A3	0x00
0x6A	SD Gamma A	SD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A4	0x00
0x6B	SD Gamma A	SD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A5	0x00
0x6C	SD Gamma A	SD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A6	0x00
0x6D	SD Gamma A	SD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A7	0x00
0x6E	SD Gamma A	SD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A8	0x00
0x6F	SD Gamma A	SD Gamma Curve A Data Points	x	x	x	x	x	x	x	x	A9	0x00
0x70	SD Gamma B	SD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B0	0x00
0x71	SD Gamma B	SD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B1	0x00
0x72	SD Gamma B	SD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B2	0x00
0x73	SD Gamma B	SD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B3	0x00
0x74	SD Gamma B	SD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B4	0x00
0x75	SD Gamma B	SD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B5	0x00
0x76	SD Gamma B	SD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B6	0x00
0x77	SD Gamma B	SD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B7	0x00
0x78	SD Gamma B	SD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B8	0x00
0x79	SD Gamma B	SD Gamma Curve B Data Points	x	x	x	x	x	x	x	x	B9	0x00
0x7A	SD Brightness Detect	SD Brightness Value	x	x	x	x	x	x	x	x	Read only	
0x7B	Field Count Register	Field Count						x	x	x	Read only	0x8x
		Reserved					0				Reserved	
		Reserved				0					Reserved	
		Reserved			0						Reserved	
		Revision Code	1	0							Read only	
0x7C		Reserved									Reserved	0x00

Table 20. Registers 0x7D to 0x91

SR7-SR0	Register[1]	Bit Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Setting	Reset Values
0x7D	Reserved											
0x7E	Reserved											
0x7F	Reserved											
0x80	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x81	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x82	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x83	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x84	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x85	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x86	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x87	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x88	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x89	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x8A	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x8B	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x8C	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x8D	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x8E	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x8F	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x90	Macrovision	MV Control Bits	x	x	x	x	x	x	x	x		0x00
0x91	Macrovision	MV Control Bit	0	0	0	0	0	0	0	x	Bits 1 to 7 must be 0	0x00

[1] Macrovision registers only on the ADV7320.

INPUT CONFIGURATION

When 10-bit input data is applied, the following bits must be set to 1:

Address 0x13, Bit 2 (HD 10-bit enable)
Address 0x48, Bit 4 (SD 10-bit enable)

Note that the ADV7320 defaults to simultaneous SD and PS upon power-up (Address[0x01]: Input Mode = 011).

SD ONLY

Address[0x01]: Input Mode = 000

In 8-/10-bit input mode, multiplexed data is input on Pins S9 to S0 (or Pins Y9 to Y0, depending on Register Address 0x01, Bit 7), with S0 being the LSB in 10-bit input mode (see Table 21). Input standards supported are ITU-R BT.601/656. In 16-/20-bit input mode, the Y pixel data is input on Pins S9 to S2 and CrCb data is input on Pins Y9 to Y2 (see Table 21).

16-/20-Bit Mode Operation

When Register 0x01 Bit 7 = 0, CrCb data is input on the Y bus and Y data is input on the S bus. When Register 0x01 Bit 7 = 1, CrCb data is input on the C bus, and Y data is input on Y bus.

The 27 MHz clock input must be input on Pin CLKIN_A. Input sync signals are input on the $\overline{\text{S_VSYNC}}$, $\overline{\text{S_HSYNC}}$, and $\overline{\text{S_BLANK}}$ pins.

Table 21. SD 8-/10-Bit and 16-/20-Bit Configuration

	Configuration	
Parameter	**8-/10-Bit Mode**	**16-/20-Bit Mode**
Register 0x01, Bit 7 = 0		
Y Bus		CrCb
S Bus	656/601, YCrCb	Y
C Bus		
Register 0x01, Bit 7 = 1		
Y Bus	656/601, YCrCb	Y
S Bus		
C Bus		CrCb

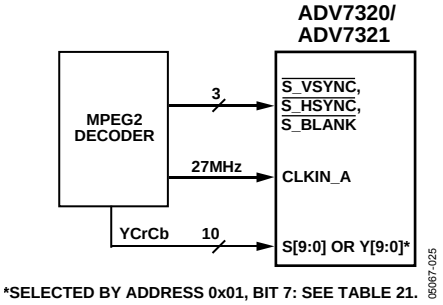


Figure 49. SD Only Input Mode

PS ONLY OR HDTV ONLY

Address[0x01]: Input Mode = 001 or 010, Respectively

YCrCb PS, HDTV, or any other HD YCrCb data can be input in 4:2:2 or 4:4:4. In 4:2:2 input format, the Y data is input on Pins Y9 to Y0 and the CrCb data is input on Pins C9 to C0. In 4:4:4 input mode, Y data is input on Pins Y9 to Y0, Cb data is input on Pins C9 to C0, and Cr data is input on Pins S9 to S0. If the YCrCb data does not conform to SMPTE 293M (525p), ITU-R BT.1358M (625p), SMPTE 274M (1080i), SMPTE 296M (720p), SMPTE 240M (1035i), or BTA-T1004/1362, the async timing mode must be used. RGB data can only be input in 4:4:4 format in PS or HDTV input modes when HD RGB input is enabled. G data is input on Pins Y9 to Y0, R data is input on Pins S9 to S0, and B data is input on Pins C9 to C0. The clock signal must be input on Pin CLKIN_A.

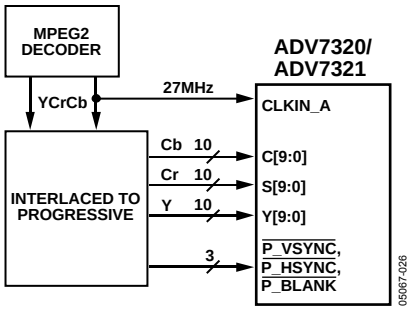


Figure 50. Progressive Scan Input Mode

SIMULTANEOUS SD/PS OR SD/HDTV

Address[0x01]: Input Mode 011 (SD 10-Bit, PS 20-Bit), Input Mode 101 (SD and HD, SD Oversampled), or Input Mode 110 (SD and HD, HD Oversampled)

YCrCb PS and HD data must be input in 4:2:2 format. In 4:2:2 input format, the HD Y data is input on Pins Y9 to Y0 and the HD CrCb data is input on Pins C9 to C0. If PS 4:2:2 data is interleaved onto a single 10-bit bus, Pins Y9 to Y0 are used for the input port. The input data is input at 27 MHz, with the data being clocked upon the rising and falling edges of the input clock. The input mode register at Address 0x01 is set accordingly. If the YCrCb data does not conform to SMPTE 293M (525p), ITU-R BT.1358M (625p), SMPTE 274M (1080i), SMPTE 296M (720p), SMPTE 240M (1035i), or BTA-T1004/1362, the async timing mode must be used.

The 8- or 10-bit SD data must be compliant with ITU-R BT.601/656 in 4:2:2 format. SD data is input on Pins S9 to S0, with S0 being the LSB. Using 8-bit input format, the data is input on Pins S9 to S2. The clock input for SD must be input on CLKIN_A, and the clock input for HD must be input on CLKIN_B. Synchronization signals are optional. SD syncs are input on Pins $\overline{\text{S_VSYNC}}$, $\overline{\text{S_HSYNC}}$, and $\overline{\text{S_BLANK}}$. HD syncs are input on Pins $\overline{\text{P_VSYNC}}$, $\overline{\text{P_HSYNC}}$, and $\overline{\text{P_BLANK}}$.

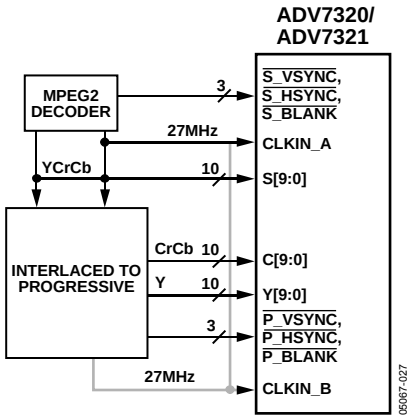


Figure 51. Simultaneous SD and PS Input

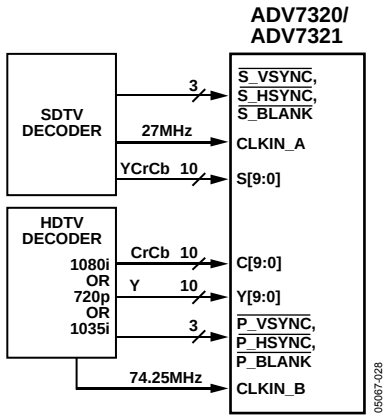


Figure 52. Simultaneous SD and HD Input

In simultaneous SD/HD input mode, if the two clock phases differ by less than 9.25 ns or by more than 27.75 ns, the clock align bit [Address 0x01, Bit 3] must be set accordingly. If the application uses the same clock source for both SD and PS, the clock align bit must be set because the phase difference between both inputs is less than 9.25 ns.

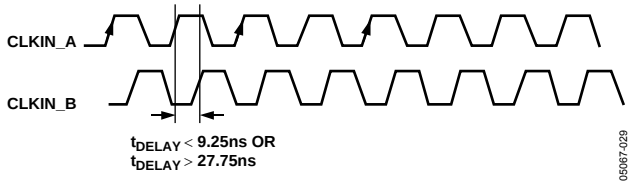


Figure 53. Clock Phase with Two Input Clocks

PS AT 27 MHZ (DUAL EDGE) OR 54 MHZ

Address[0x01]: Input Mode 100 or 111, Respectively

YCrCb PS data can be input at 27 MHz or 54 MHz. The input data is interleaved onto a single 8-/10-bit bus and is input on Pins Y9 to Y0. When a 27 MHz clock is supplied, the data is clocked upon the rising and falling edges of the input clock, and the clock edge bit [Address 0x01, Bit 1] must be set accordingly.

Table 22 provides an overview of all possible input configurations. Figure 54, Figure 55, and Figure 56 show the possible conditions: Cb data on the rising edge, and Y data on the rising edge.

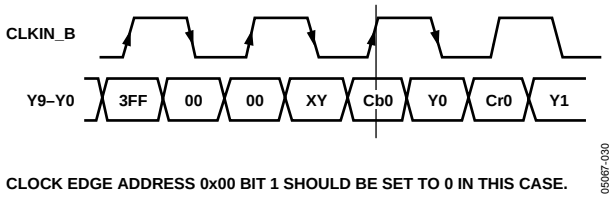


Figure 54. Input Sequence in PS Bit Interleaved Mode (EAV/SAV)

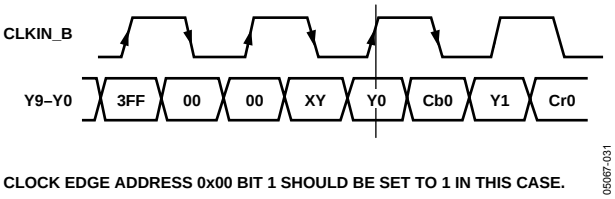


Figure 55. Input Sequence in PS Bit Interleaved Mode (EAV/SAV)

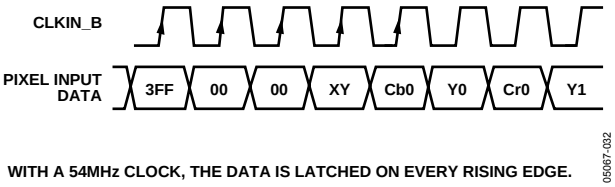


Figure 56. Input Sequence in PS Bit Interleaved Mode (EAV/SAV)

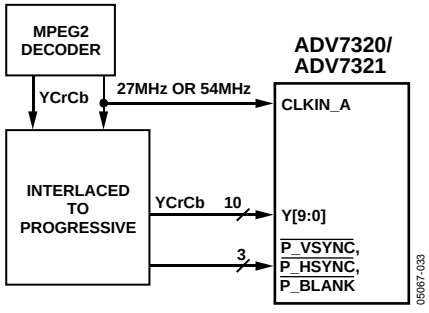


Figure 57. 10-Bit PS at 27 MHz or 54 MHz

Table 22. Input Configurations

Input Format	Total Bits	Data Format	Input Video	Input Pins	Subaddress	Register Setting
ITU-R BT.656 (See Table 21)	8	4:2:2	YCrCb	S9 to S2 (MSB = S9)	0x01 0x48	0x00 0x00
	10	4:2:2	YCrCb	S9 to S0 (MSB = S9)	0x01 0x48	0x00 0x10
	16	4:2:2	Y CrCb	S9 to S2 (MSB = S9) Y9 to Y2 (MSB = Y9)	0x01 0x48	0x00 0x08
	20	4:2:2	Y CrCb	S9 to S0 (MSB = S9) Y9 to Y0 (MSB = Y9)	0x01 0x48	0x00 0x18
	8	4:2:2	YCrCb	Y9 to Y2 (MSB = Y9)	0x01 0x48	0x80 0x00
	10	4:2:2	YCrCb	Y9 to Y0 (MSB = Y9)	0x01 0x48	0x80 0x10
PS Only	8 (27 MHz clock)	4:2:2	YCrCb	Y9 to Y2 (MSB = Y9)	0x01 0x13	0x10 0x40
	10 (27 MHz clock)	4:2:2	YCrCb	Y9 to Y0 (MSB = Y9)	0x01 0x13	0x10 0x44
	8 (54 MHz clock)	4:2:2	YCrCb	Y9 to Y2 (MSB = Y9)	0x01 0x13	0x70 0x40
	10 (54 MHz clock)	4:2:2	YCrCb	Y9 to Y0 (MSB = Y9)	0x01 0x13	0x70 0x44
	16	4:2:2	Y CrCb	Y9 to Y2 (MSB = Y9) C9 to C2 (MSB = C9)	0x01 0x13	0x10 0x40
	20	4:2:2	Y CrCb	Y9 to Y0 (MSB = Y9) C9 to C0 (MSB = C9)	0x01 0x13	0x10 0x44
	24	4:4:4	Y Cb Cr	Y9 to Y2 (MSB = Y9) C9 to C2 (MSB = C9) S9 to S2 (MSB = S9)	0x01 0x13	0x10 0x00
	30	4:4:4	Y Cb Cr	Y9 to Y0 (MSB = Y9) C9 to C0 (MSB = C9) S9 to S0 (MSB = S9)	0x01 0x13	0x10 0x04
HDTV Only	16	4:2:2	Y CrCb	Y9 to Y2 (MSB = Y9) C9 to Y2 (MSB = C9)	0x01 0x13	0x20 0x40
	20	4:2:2	Y CrCb	Y9 to Y0 (MSB = Y9) C9 to C0 (MSB = C9)	0x01 0x13	0x20 0x44
	24	4:4:4	Y Cb Cr	Y9 to Y2 (MSB = Y9) C9 to C2 (MSB = C9) S9 to S2 (MSB = S9)	0x01 0x13	0x20 0x00
	30	4:4:4	Y Cb Cr	Y9 to Y0 (MSB = Y9) C9 to C0 (MSB = C9) S9 to S0 (MSB = S9)	0x01 0x13	0x20 0x04
HD RGB	24	4:4:4	G B R	Y9 to Y2 (MSB = Y9) C9 to C2 (MSB = C9) S9 to S2 (MSB = S9)	0x01 0x13 0x15	0x10 or 0x20 0x00 0x02
	30	4:4:4	G B R	Y9 to Y0 (MSB = Y9) C9 to C0 (MSB = C9) S9 to S0 (MSB = S9)	0x01 0x13 0x15	0x10 or 0x20 0x04 0x02
ITU-R BT.656 and PS	8 (SD)	4:2:2	YCrCb	S9 to S2 (MSB = S9)	0x01	0x40
	8 (PS)	4:2:2	YCrCb	Y9 to Y2 (MSB = Y9)	0x13 0x48	0x40 0x00
ITU-R BT.656 and PS	10 (SD)	4:2:2	YCrCb	S9 to S0 (MSB = S9)	0x01	0x40
	10 (PS)	4:2:2	YCrCb	Y9 to Y0 (MSB = Y9)	0x13 0x48	0x44 0x10
ITU-R BT.656 and PS or HDTV	8	4:2:2	YCrCb	S9 to S2 (MSB = S9)	0x01	0x30, 0x50, or 0x60
	16	4:2:2	Y CrCb	Y9 to Y2 (MSB = Y9) C9 to C2 (MSB = C9)	0x13 0x48	0x40 0x00
ITU-R BT.656 and PS or HDTV	10	4:2:2	YCrCb	S9 to S0 (MSB = S9)	0x01	0x30, 0x50, or 0x60
	20	4:2:2	Y CrCb	Y9 to Y0 (MSB = Y9) C9 to C0 (MSB = C9)	0x13 0x48	0x44 0x10

FEATURES

OUTPUT CONFIGURATION

Table 23, Table 24, and Table 25 demonstrate what output signals are assigned to the DACs when the control bits are set accordingly.

Table 23. Output Configuration in SD Only Mode

RGB/YUV Output 0x02, Bit 5	SD DAC Output 1 0x42, Bit 2	SD DAC Output 2 0x42, Bit 1	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F
0	0	0	CVBS	Luma	Chroma	G	B	R
0	0	1	G	B	R	CVBS	Luma	Chroma
0	1	0	G	Luma	Chroma	CVBS	B	R
0	1	1	CVBS	B	R	G	Luma	Chroma
1	0	0	CVBS	Luma	Chroma	Y	U	V
1	0	1	Y	U	V	CVBS	Luma	Chroma
1	1	0	Y	Luma	Chroma	CVBS	U	V
1	1	1	CVBS	U	V	Y	Luma	Chroma

Luma/Chroma Swap 0x44, Bit 7	
0	Table as above
1	Table as above, but with all luma/chroma instances swapped

Table 24. Output Configuration in HD Only or PS Only Mode

Input Format	RGB Input 0x15, Bit 1	RGB/YPrPb Output 0x02, Bit 5	Color Swap 0x15, Bit 3	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F
YCrCb 4:2:2	0	0	0	N/A	N/A	N/A	G	B	R
YCrCb 4:2:2	0	0	1	N/A	N/A	N/A	G	R	B
YCrCb 4:2:2	0	1	0	N/A	N/A	N/A	Y	Pb	Pr
YCrCb 4:2:2	0	1	1	N/A	N/A	N/A	Y	Pr	Pb
YCrCb 4:4:4	0	0	0	N/A	N/A	N/A	G	B	R
YCrCb 4:4:4	0	0	1	N/A	N/A	N/A	G	R	B
YCrCb 4:4:4	0	1	0	N/A	N/A	N/A	Y	Pb	Pr
YCrCb 4:4:4	0	1	1	N/A	N/A	N/A	Y	Pr	Pb
RGB 4:4:4	1	0	0	N/A	N/A	N/A	G	B	R
RGB 4:4:4	1	0	1	N/A	N/A	N/A	G	R	B
RGB 4:4:4	1	1	0	N/A	N/A	N/A	G	B	R
RGB 4:4:4	1	1	1	N/A	N/A	N/A	G	R	B

Table 25. Output Configuration in Simultaneous SD or SD/HD Only Mode

Input Formats	RGB/YPrPb Output 0x02, Bit 5	HD/PS Color Swap 0x15, Bit 3	DAC A	DAC B	DAC C	DAC D	DAC E	DAC F
ITU-R.BT656 and HD/PS YCrCb in 4:2:2	0	0	CVBS	Luma	Chroma	G	B	R
ITU-R.BT656 and HD/PS YCrCb in 4:2:2	0	1	CVBS	Luma	Chroma	G	R	B
ITU-R.BT656 and HD/PS YCrCb in 4:2:2	1	0	CVBS	Luma	Chroma	Y	Pb	Pr
ITU-R.BT656 and HD/PS YCrCb in 4:2:2	1	1	CVBS	Luma	Chroma	Y	Pr	Pb

HD ASYNC TIMING MODE

[Subaddress 0x10, Bits 3 and 2]

For any input data that does not conform to the standards selectable in input mode (Subaddress 0x10) asynchronous timing mode can be used to interface to the ADV7320/ADV7321. Timing control signals for $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, and $\overline{\text{BLANK}}$ must be programmed by the user. Macrovision and programmable oversampling rates are not available in async timing mode.

In async mode, the PLL must be turned off [Subaddress 0x00, Bit 1 = 1]. Register 0x10 should be programmed to 0x01.

Figure 58 and Figure 59 show examples of how to program the ADV7320/ADV7321 to accept a high definition standard other than SMPTE 293M, SMPTE 274M, SMPTE 296M, or ITU-R BT.1358.

Follow the specifications in Table 26 when programming the control signals in async timing mode. For standards that do not require a trisync level, $\overline{\text{P_BLANK}}$ must be tied low at all times.

Table 26. Async Timing Mode Truth Table

$\overline{\text{P_HSYNC}}$	$\overline{\text{P_VSYNC}}$	$\overline{\text{P_BLANK}}$[1]	Reference	Reference in Figure 58 and Figure 59
1 → 0	0	0 or 1	50% point of falling edge of trilevel horizontal sync signal	a
0	0 → 1	0 or 1	25% point of rising edge of trilevel horizontal sync signal	b
0 → 1	0 or 1	0	50% point of falling edge of trilevel horizontal sync signal	c
1	0 or 1	0 → 1	50% start of active video	d
1	0 or 1	1 → 0	50% end of active video	e

[1] When async timing mode is enabled, $\overline{\text{P_BLANK}}$, Pin 25, becomes an active high input. $\overline{\text{P_BLANK}}$ is set to active low at Address 0x10, Bit 6.

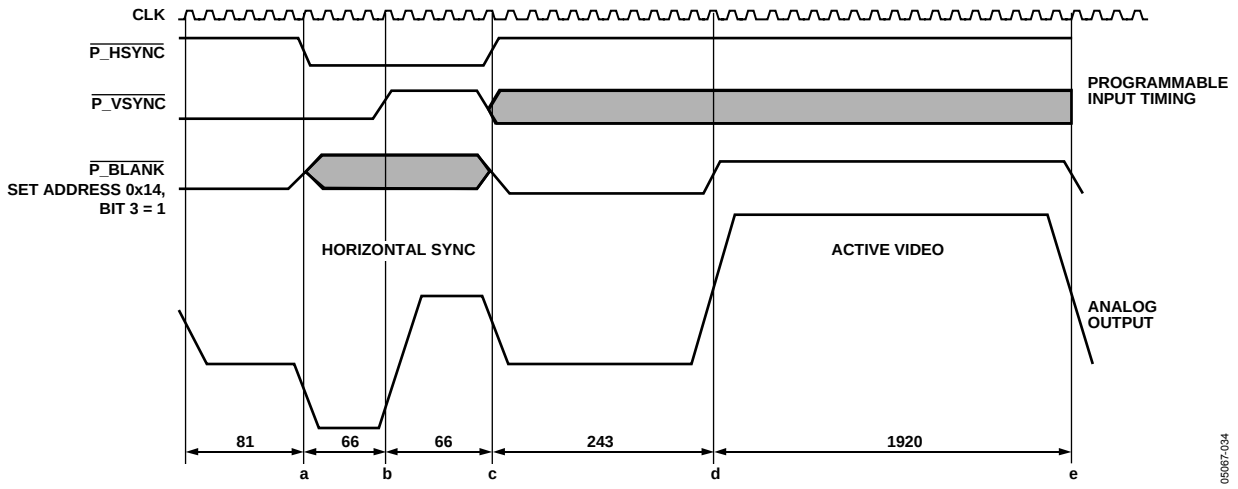


Figure 58. Async Timing Mode—Programming Input Control Signals for SMPTE 295M Compatibility

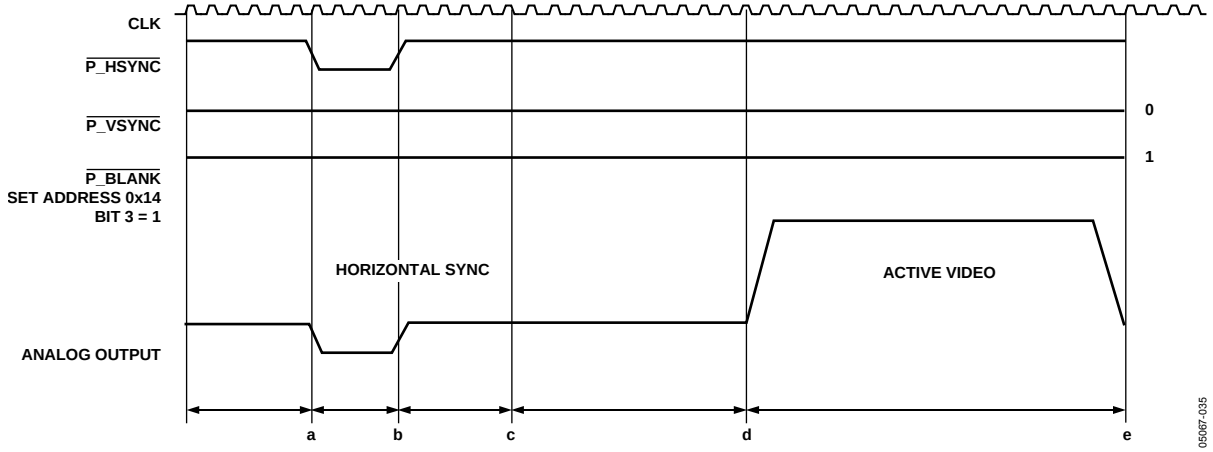


Figure 59. Async Timing Mode—Programming Input Control Signals for Bilevel Sync Signal

HD TIMING RESET

A timing reset is achieved by toggling the HD timing reset control bit [Subaddress 0x14, Bit 0] from 0 to 1. In this state, the horizontal and vertical counters remain reset. When this bit is set back to 0, the internal counters resume counting.

The minimum time the pin must be held high is one clock cycle; otherwise, this reset signal might not be recognized. This timing reset applies to the HD timing counters only.

SD REAL-TIME CONTROL, SUBCARRIER RESET, AND TIMING RESET

[Subaddress 0x44, Bits 2 and 1]

Together with the RTC_SCR_TR pin and SD Mode Register 3 [Address 0x44, Bits 1 and 2], the ADV7320/ADV7321 can be used in (a) timing reset mode, (b) subcarrier phase reset mode, or (c) RTC mode.

a. A timing reset is achieved after a low-to-high transition on the RTC_SCR_TR pin (Pin 31). In this state, the horizontal and vertical counters remain reset. Upon releasing this pin (set to low), the internal counters resume counting, starting with Field 1, and the subcarrier phase is reset.

   The minimum time the pin must be held high is one clock cycle; otherwise, this reset signal might not be recognized. This timing reset applies to the SD timing counters only.

b. In subcarrier phase reset, a low-to-high transition on the RTC_SCR_TR pin (Pin 31) resets the subcarrier phase to 0 on the field following the subcarrier phase reset when the SD RTC/TR/SCR control bits at Address 0x44 are set to 01.

   This reset signal must be held high for a minimum of one clock cycle.

   Because the field counter is not reset, it is recommended that the reset signal is applied in Field 7 (PAL) or Field 3 (NTSC). The reset of the phase then occurs on the next field, that is, Field 1, lined up correctly with the internal counters. The field count register at Address 0x7B can be used to identify the number of the active field.

c. In RTC mode, the ADV7320/ADV7321 can be used to lock to an external video source. The real-time control mode allows the ADV7320/ADV7321 to automatically alter the subcarrier frequency to compensate for line length variations. When the part is connected to a device, such as an ADV7183A video decoder (see Figure 62), that outputs a digital data stream in the RTC format, it automatically changes to the compensated subcarrier frequency on a line-by-line basis. This digital data stream is 67 bits wide and the subcarrier is contained in Bits 0 to 21. Each bit is two clock cycles long. Write 0x00 into all four subcarrier frequency registers when this mode is used.

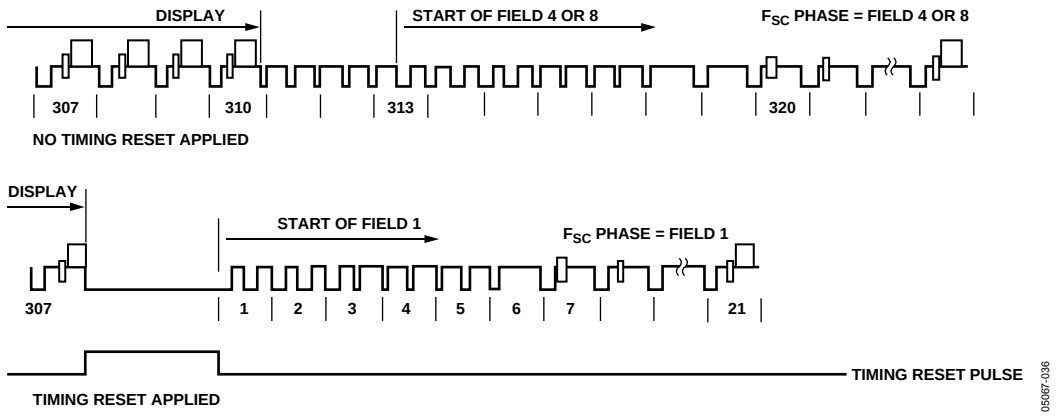


Figure 60. Timing Reset Timing Diagram

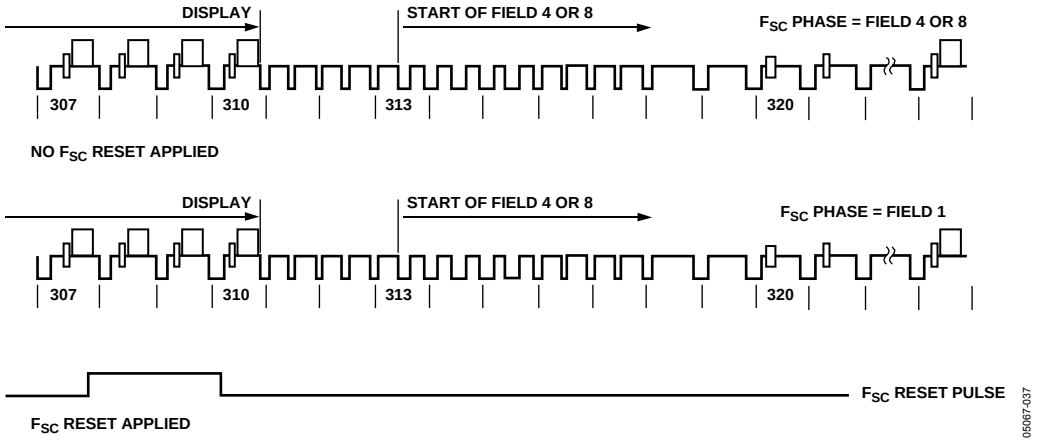
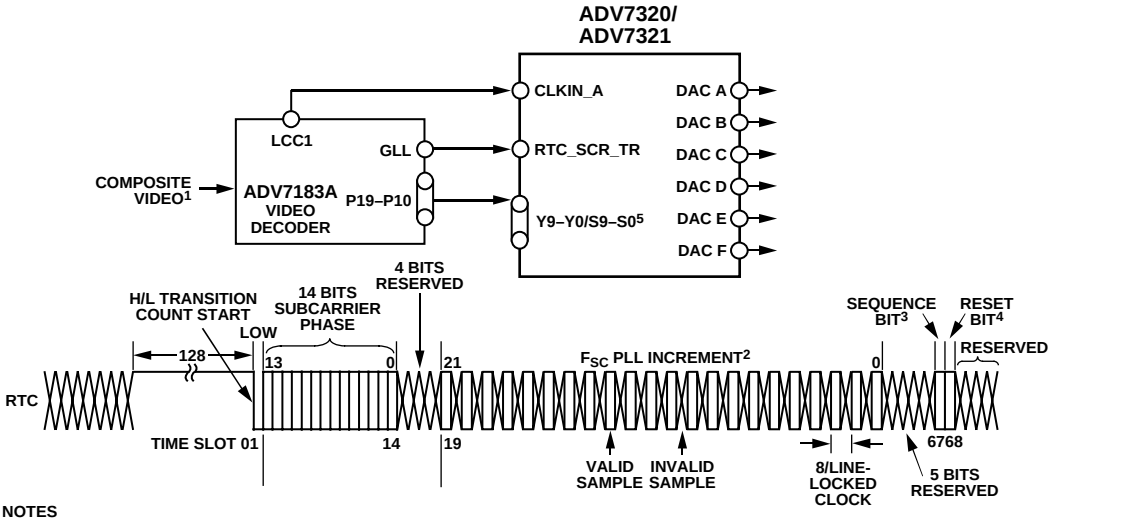


Figure 61. Subcarrier Reset Timing Diagram



NOTES
[1]FOR EXAMPLE, VCR OR CABLE.
[2]F_{SC} PLL INCREMENT IS 22 BITS LONG. VALUE LOADED INTO ADV7320/ADV7321 F_{SC} DDS REGISTER IS F_{SC}. PLL INCREMENTS BITS 21:0 AND BITS 0:9 OF SUBCARRIER FREQUENCY REGISTERS. ALL ZEROS SHOULD BE WRITTEN TO THE SUBCARRIER FREQUENCY REGISTERS OF THE ADV7320/ADV7321.
[3]SEQUENCE BIT PAL: 0 = LINE NORMAL, 1 = LINE INVERTED; NTSC: 0 = NO CHANGE.
[4]RESET ADV7320/ADV7321 DDS.
[5]SELECTED BY REGISTER ADDRESS 0x01, BIT 7.

Figure 62. RTC Timing and Connections

RESET SEQUENCE

A reset is activated with a high-to-low transition on the $\overline{\text{RESET}}$ pin (Pin 33) according to the timing specifications, and the ADV7320/ADV7321 revert to the default output configuration. Figure 63 illustrates the $\overline{\text{RESET}}$ timing sequence.

SD VCR FF/RW SYNC

[Subaddress 0x42, Bit 5]

In DVD record applications where the encoder is used with a decoder, the VCR FF/RW sync control bit [Subaddress 0x42, Bit 5] can be used for nonstandard input video, that is, in fast forward or rewind modes.

In fast forward mode, the sync information at the start of a new field in the incoming video usually occurs before the correct number of lines/fields are reached; in rewind mode, this sync signal usually occurs after the total number of lines/fields are reached. Conventionally this means that the output video will have corrupted field signals because one signal is generated by the incoming video and another is generated when the internal lines/field counters reach the end of a field.

When the VCR FF/RW sync control is enabled, the line/field counters are updated according to the incoming $\overline{\text{VSYNC}}$ signal, and the analog output matches the incoming $\overline{\text{VSYNC}}$ signal.

This control is available in all slave timing modes except Slave Mode 0.

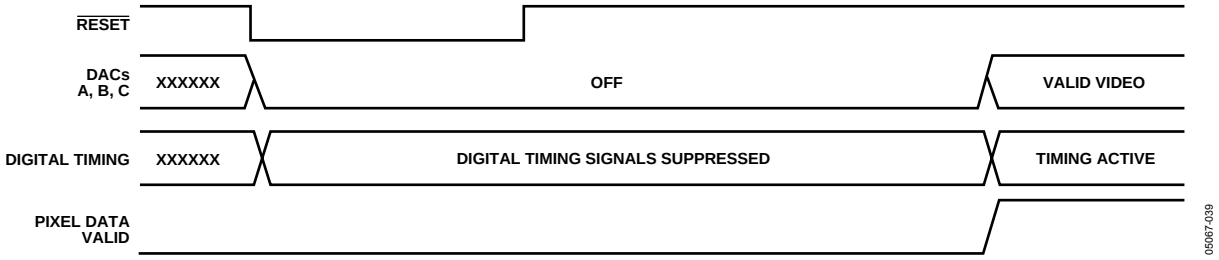


Figure 63. $\overline{\text{RESET}}$ Timing Sequence

VERTICAL BLANKING INTERVAL

The ADV7320/ADV7321 accepts input data that contains VBI data (such as CGMS, WSS, VITS) in SD and HD modes.

For the SMPTE 293M (525p) standard, VBI data can be inserted on Lines 13 to 42 of each frame, or on Lines 6 to 43 for the ITU-R BT.1358 (625p) standard.

This data can be present on Lines 10 to 20 for SD NTSC and on Lines 7 to 22 for PAL.

If VBI is disabled [Address 0x11, Bit 4 for HD; Address 0x43, Bit 4 for SD], VBI data is not present at the output and the entire VBI is blanked. These control bits are valid in all master and slave modes.

In Slave Mode 0, if VBI is enabled, the blanking bit in the EAV/SAV code is overwritten. It is possible to use VBI in this timing mode as well.

In Slave Mode 1 or 2, the $\overline{\text{BLANK}}$ control bit [Address 0x4A, Bit 3] must be enabled to allow VBI data to pass through the ADV7320/ADV7321. Otherwise, the ADV7320/ADV7321 automatically blank the VBI to standard.

If CGMS is enabled and VBI is disabled, the CGMS data will nevertheless be available at the output.

See Appendix 1—Copy Generation Management System.

SUBCARRIER FREQUENCY REGISTERS

[Subaddresses 0x4C to 0x4F]

Four 8-bit registers are used to set up the subcarrier frequency. The value of these registers is calculated using the equation

$$Subcarrier\ Frequency\ Register = \frac{Number\ of\ subcarrier\ periods\ in\ one\ video\ line}{Number\ of\ 27\ MHz\ clk\ cycles\ in\ one\ video\ line} \times 2^{32}$$

where the sum is rounded to the nearest integer.

For example, in NTSC mode

$$Subcarrier\ Register\ Value = \left(\frac{227.5}{1716}\right) \times 2^{32} = 569408543$$

where:
Subcarrier Register Value = 0x21F07C1F.
SD F_{SC} Register 0: 0x1F.
SD F_{SC} Register 1: 0x7C.
SD F_{SC} Register 2: 0xF0.
SD F_{SC} Register 3: 0x21.

See the MPU Port Description section for more details on accessing the subcarrier frequency registers.

Programming the F_{SC}

The subcarrier register value is divided into four F_{SC} registers as shown above. To load the value into the encoder, users must write to the F_{SC} registers in sequence, starting with $F_{SC}0$. The value is not loaded until the $F_{SC}4$ write is complete.

Note that the ADV7320/ADV7321 power-up value for $F_{SC}0$ is 0x1E. For precise NTSC F_{SC}, write 0x1F to this register.

SQUARE PIXEL TIMING MODE

[Address 0x42, Bit 4]

In square pixel mode, the following timing diagrams apply.

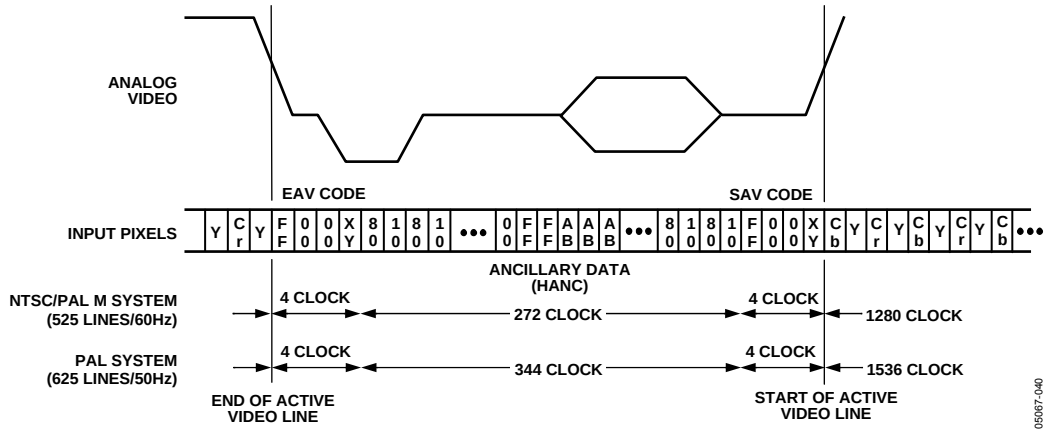


Figure 64. EAV/SAV Embedded Timing

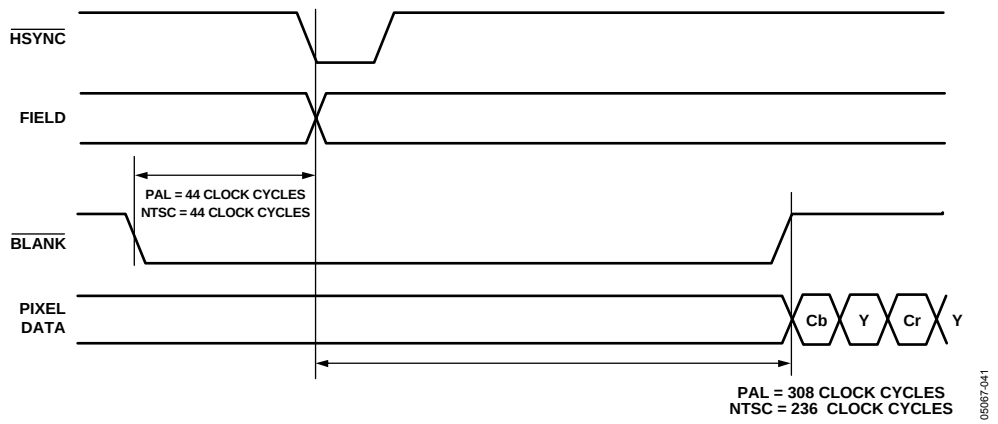


Figure 65. Active Pixel Timing

FILTERS

Table 27 shows an overview of the programmable filters available on the ADV7320/ADV7321.

Table 27. Selectable Filters

Filter	Subaddress
SD Luma LPF NTSC	0x40
SD Luma LPF PAL	0x40
SD Luma Notch NTSC	0x40
SD Luma Notch PAL	0x40
SD Luma SSAF	0x40
SD Luma CIF	0x40
SD Luma QCIF	0x40
SD Chroma 0.65 MHz	0x40
SD Chroma 1.0 MHz	0x40
SD Chroma 1.3 MHz	0x40
SD Chroma 2.0 MHz	0x40
SD Chroma 3.0 MHz	0x40
SD Chroma CIF	0x40
SD Chroma QCIF	0x40
SD UV SSAF	0x42
HD Chroma Input	0x13
HD Sinc Filter	0x13
HD Chroma SSAF	0x13

SD Internal Filter Response

[Subaddress 0x40 [7:2]; Subaddress 0x42, Bit 0]

The Y filter supports several frequency responses, including two low-pass responses, two notch responses, an extended SSAF response with or without gain boost attenuation, a CIF response, and a QCIF response. The UV filter supports several different frequency responses, including six low-pass responses, a CIF response, and a QCIF response, as shown in Figure 35 and Figure 36.

If SD SSAF gain is enabled, there are 12 response options in the range −4 dB to +4 dB [Subaddress 0x47, Bit 4]. Choose the desired response by programming the correct value via the I²C [Subaddress 0x62]. The variation of frequency responses are shown in Figure 32 and Figure 33.

In addition to the chroma filters listed in Table 27, the ADV7320/ADV7321 contain an SSAF filter specifically designed for the color difference component outputs, U and V. This filter has a cutoff frequency of about 2.7 MHz and a gain of −40 dB at 3.8 MHz, as shown in Figure 66. This filter can be controlled with Address 0x42, Bit 0.

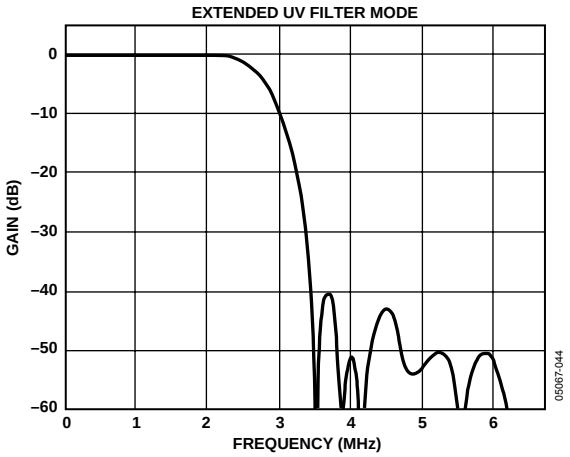


Figure 66. UV SSAF Filter

If this filter is disabled, one of the chroma filters shown in Table 28 can be selected and used for the CVBS or luma/chroma signal.

Table 28. Internal Filter Specifications

Filter	Pass-Band Ripple[1] (dB)	3 dB Bandwidth[2] (MHz)
Luma LPF NTSC	0.16	4.24
Luma LPF PAL	0.1	4.81
Luma Notch NTSC	0.09	2.3/4.9/6.6
Luma Notch PAL	0.1	3.1/5.6/6.4
Luma SSAF	0.04	6.45
Luma CIF	0.127	3.02
Luma QCIF	Monotonic	1.5
Chroma 0.65 MHz	Monotonic	0.65
Chroma 1.0 MHz	Monotonic	1
Chroma 1.3 MHz	0.09	1.395
Chroma 2.0 MHz	0.048	2.2
Chroma 3.0 MHz	Monotonic	3.2
Chroma CIF	Monotonic	0.65
Chroma QCIF	Monotonic	0.5

[1] Pass-band ripple is the maximum fluctuation from the 0 dB response in the pass band. The pass band is defined to have 0 Hz to fc (Hz) frequency limits for a low-pass filter, and 0 Hz to f1 (Hz) and f2 (Hz) to infinity for a notch filter, where fc, f1, and f2 are the −3 dB points.
[2] 3 dB bandwidth refers to the −3 dB cutoff frequency.

PS/HD Sinc Filter

[Subaddress 0x13, Bit 3]

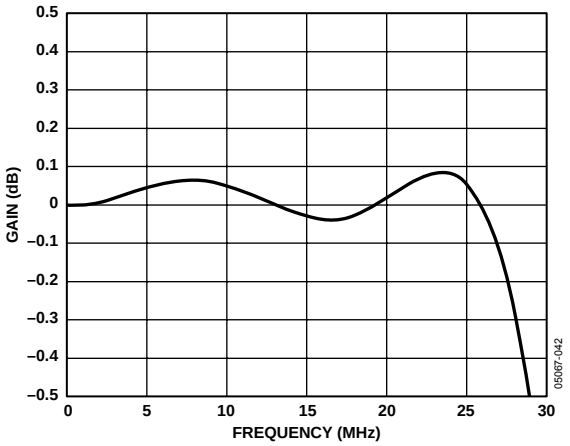


Figure 67. HD Sinc Filter Enabled

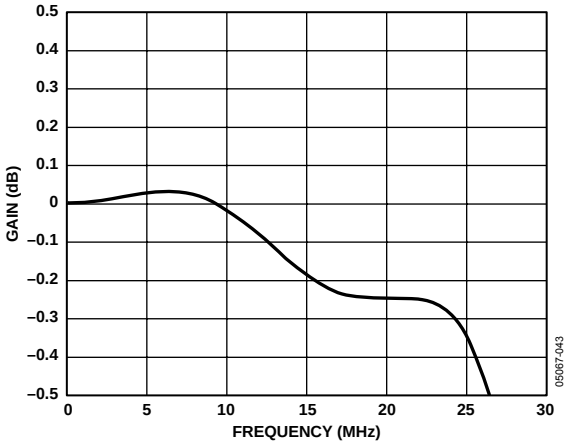


Figure 68. HD Sinc Filter Disabled

COLOR CONTROLS AND RGB MATRIX

HD Y Level, HD Cr Level, HD Cb Level

[Subaddresses 0x16 to 0x18]

Three 8-bit registers at Addresses 0x16, 0x17, and 0x18 are used to program the output color of the internal HD test pattern generator, be it the lines of the cross hatch pattern or the uniform field test pattern. They are not functional as color controls for external pixel data input. For this purpose, the RGB matrix is used.

The values for Y and the color difference signals used to obtain white, black, and saturated primary and complementary colors conform to the ITU-R BT.601-4 standard.

Table 29 shows sample color values that can be programmed into the color registers when the output standard selection is set to EIA 770.2.

Table 29. Sample Color Values for EIA 770.2 Output Standard Selection

Sample Color	Y Value	Cr Value	Cb Value
White	235 (EB)	128 (80)	128 (80)
Black	16 (10)	128 (80)	128 (80)
Red	81 (51)	240 (F0)	90 (5A)
Green	145 (91)	34 (22)	54 (36)
Blue	41 (29)	110 (6E)	240 (F0)
Yellow	210 (D2)	146 (92)	16 (10)
Cyan	170 (AA)	16 (10)	166 (A6)
Magenta	106 (6A)	222 (DE)	202 (CA)

RGB Matrix

[Subaddresses 0x03 to 0x09]

The internal RGB matrix automatically performs all YCrCb to RGB scaling according to the input standard programmed in the device as selected by input mode Register 0x01 [6:4]. Table 30 shows the options available in this matrix.

Note that it is not possible to do a color space conversion from RGB-in to YPrPb-out. Also, it is not possible to input SD RGB.

Table 30. Matrix Conversion Options

HDTV/SD/PS			
Input	Output	Reg. 0x02,Bit 5 (YUV/RGB OUT)	Reg. 0x15, Bit 1 (RGB IN/YCrCb IN, PS/HD Only)
YCrCb	YPrPb	1	0
YCrCb	RGB	0	0
RGB	RGB	0	1

Manual RGB Matrix Adjust Feature

Normally, there is no need to enable this feature in Register 0x02, Bit 3, because the RGB matrix automatically performs color space conversion depending on the input mode chosen (SD/PS, HD) and the polarity of RGB/YPrPb output in Register 0x02, Bit 5 (see Table 30). For this reason, the manual RGB matrix adjust feature is disabled by default. However, For HDTV YCrCb-to-RGB conversion, the RGB matrix must be enabled to invoke the correct coefficients for this color space. The coefficients do not need to be adjusted.

The manual RGB matrix adjust feature provides custom coefficient manipulation and is used in PS and HD modes only.

When the manual RGB matrix adjust feature is enabled, the default values in Registers 0x05 to 0x09 are correct for HDTV color space only. The color components are converted according to the 1080i and 720p standards (SMPTE 274M, SMPTE 296M)

$$R = Y + 1.575Pr$$

$$G = Y - 0.468Pr - 0.187Pb$$

$$B = Y + 1.855Pb$$

This is reflected in the preprogrammed values for GY = 0x13B, GU = 0x3B, GV = 0x93, BU = 0x248, and RV = 0x1F0.

If the RGB matrix is enabled and another input standard (such as SD or PS) is used, the scale values for GY, GU, GV, BU, and RV must be adjusted according to this input standard color space. The user should consider that the color component conversion might use different scale values. For example, SMPTE 293M uses the following equations for conversion:

$$R = Y + 1.402Pr$$

$$G = Y - 0.714Pr - 0.344Pb$$

$$B = Y + 1.773Pb$$

The manual RGB matrix adjust feature can be used to control the HD output levels in cases where the video output does not conform to the standard due to altering the DAC output stages such as termination resistors. The programmable RGB matrix is used for external HD/PS data and is not functional when internal test patterns are enabled. To adjust Registers 0x05 to 0x09, the manual RGB matrix adjust must be enabled [Register 0x02, Bit 3 = 1].

Programming the RGB Matrix

If custom manipulation of coefficients is required, enable the RGB matrix in Address 0x02, Bit 3, set the output to RGB [Address 0x02, Bit 5], and disable sync on PrPb (default) [Address 0x15, Bit 2]. Enabling sync on RGB is optional [Address 0x02, Bit 4].

GY at Addresses 0x03 and 0x05 controls the green signal output levels. BU at Addresses 0x04 and 0x08 controls the blue signal output levels, and RV at Addresses 0x04 and 0x09 control the red signal output levels. To control YPrPb output levels, enable the YUV output [Address 0x02, Bit 5]. In this case GY [Address 0x05; Address 0x03, Bits 0 and 1] is used for the Y output, RV [Address 0x09; Address 0x04, Bits 0 and 1] is used for the Pr output, and BU [Address 0x08; Address 0x04, Bits 2 and 3] is used for the Pb output.

If RGB output is selected, the RGB matrix scaler uses the following equations:

$$G = GY \times Y + GU \times Pb + GV \times Pr$$

$$B = GY \times Y + BU \times Pb$$

$$R = GY \times Y + RV \times Pr$$

If YPrPb output is selected, the following equations are used:

$$Y = GY \times Y$$

$$U = BU \times Pb$$

$$V = RV \times Pr$$

Upon power-up, the RGB matrix is programmed with the default values listed in Table 31.

Table 31. RGB Matrix Default Values

Address	Default
0x03	0x03
0x04	0xF0
0x05	0x4E
0x06	0x0E
0x07	0x24
0x08	0x92
0x09	0x7C

When the manual RGB matrix adjust feature is not enabled, the ADV7320/ADV7321 automatically scale YCrCb inputs to all standards supported by this part as selected by the input mode Register 0x01 [6:4].

SD Luma and Color Control

[Subaddresses 0x5C, 0x5D, 0x5E, 0x5F]

SD Y Scale, SD Cr Scale, and SD Cb Scale are three 10-bit-wide control registers that scale the Y, Cb, and Cr output levels.

Each of these registers represents the value required to scale the Cb or Cr level from 0.0 to 2.0 and the Y level from 0.0 to 1.5 of its initial level. The value of these 10 bits is calculated using the following equation:

$$Y, Cr, or Cb\ Scalar\ Value = Scale\ Factor \times 512$$

For example,

Scale Factor = 1.18

$$Y, Cb, or Cr\ Scale\ Value = 1.18 \times 512 = 665.6$$

Y, Cb, or Cr Scale Value = 665 (*rounded to the nearest integer*)

Y, Cb, or Cr Scale Value = 1010 0110 01b

Address 0x5C, SD LSB Register = 0x15
Address 0x5D, SD Y Scale Register = 0xA6
Address 0x5E, SD Cb Scale Register = 0xA6
Address 0x5F, SD Cr Scale Register = 0xA6

Note that this feature affects all interlaced output signals, that is, CVBS, Y-C, YPrPb, and RGB.

SD Hue Adjust Value

[Subaddress 0x60]

The hue adjust value is used to adjust the hue on the composite and chroma outputs.

These eight bits represent the value required to vary the hue of the video data, that is, the variance in phase of the subcarrier during active video with respect to the phase of the subcarrier during the color burst. The ADV7320/ADV7321 provide a range of ±22.5° increments of 0.17578125°. For normal operation (zero adjustment), this register is set to 0x80. Values 0xFF and 0x00 represent the upper and lower limits, respectively, of attainable adjustment.

Hue Adjust (°) = 0.17578125° (HCR_d − 128) for positive hue adjust value.

For example, to adjust the hue by +4°, write 0x97 to the hue adjust value register:

$$\left(\frac{4}{0.17578125}\right) + 128 = 105d = 0x97 .$$

where the sum is rounded to the nearest integer.

To adjust the hue by −4°, write 0x69 to the hue adjust value register:

$$\left(\frac{-4}{0.17578125}\right) + 128 = 105d = 0x69$$

where the sum is rounded to the nearest integer.

SD Brightness Control

[Subaddress 0x61]

The brightness is controlled by adding a programmable setup level onto the scaled Y data. This brightness level can be added onto the scaled Y data. For NTSC with pedestal, the setup can vary from 0 IRE to 22.5 IRE. For NTSC without pedestal and for PAL, the setup can vary from −7.5 IRE to +15 IRE.

The brightness control register is an 8-bit register. Seven bits of this 8-bit register are used to control the brightness level, which can be a positive or negative value.

For example,

1. To add +20 IRE brightness level to an NTSC signal with pedestal, write 0x28 to Address 0x61, SD brightness.

   0x[*SD Brightness Value*] =

   0x[*IRE Value* × 2.015631] =

   0x[20 × 2.015631] = 0x[40.31262] = 0x28

2. To add −7 IRE brightness level to a PAL signal, write 0x72 to Address 0x61, SD brightness.

   [*IRE Value*| × 2.075631

   [7 × 2.015631] = [14.109417] = 0001110b

   [0001110] *into twos complement* = [1110010]b = 0x72

Table 32. Brightness Control Values[1]

Setup Level in NTSC with Pedestal	Setup Level in NTSC Without Pedestal	Setup Level in PAL	SD Brightness
22.5 IRE	15 IRE	15 IRE	0x1E
15 IRE	7.5 IRE	7.5 IRE	0x0F
7.5 IRE	0 IRE	0 IRE	0x00
0 IRE	−7.5 IRE	−7.5 IRE	0x71

[1] Values in the range of 0x3F to 0x44 might result in an invalid output signal.

SD Brightness Detect

[Subaddress 0x7A]

The ADV7320/ADV7321 allow monitoring the brightness level of the incoming video data. Brightness detect is a read-only register.

Double Buffering

[Subaddress 0x13, Bit 7; Subaddress 0x48, Bit 2]

Double-buffered registers are updated once per field upon the falling edge of the Vsync signal. Double buffering improves the overall performance because modifications to register settings are not made during active video, but take effect upon the start of the active video.

Double buffering can be activated on the following HD registers: HD Gamma Curve A, HD Gamma Curve B, and HD CGMS registers.

Double buffering can be activated on the following SD registers: SD Gamma Curve A and SD Gamma Curve B, SD Y scale, SD U scale, SD V scale, SD brightness, SD closed captioning, and SD Macrovision Bits 5 to 0.

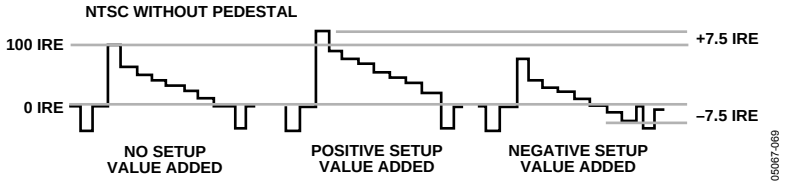


Figure 69. Examples of Brightness Control Values

PROGRAMMABLE DAC GAIN CONTROL

DACs A, B, and C are controlled by Register 0A.

DACs D, E, and F are controlled by Register 0B.

The I²C control registers will adjust the output signal gain up or down from its absolute level.

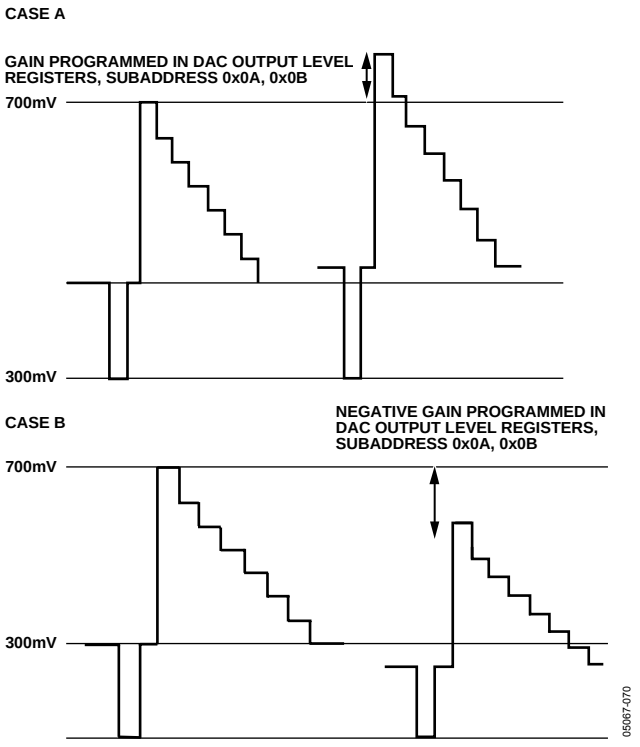


Figure 70. Programmable DAC Gain—Positive and Negative Gain

In Case A, the video output signal is gained. The absolute level of the sync tip and blanking level both increase with respect to the reference video output signal. The overall gain of the signal is increased from the reference signal.

In Case B, the video output signal is reduced. The absolute level of the sync tip and blanking level both decrease with respect to the reference video output signal. The overall gain of the signal is reduced from the reference signal.

The range of this feature is specified for ±7.5% of the nominal output from the DACs. For example, if the output current of the DAC is 4.33 mA, the DAC tune feature can change this output current from 4.008 mA (−7.5%) to 4.658 mA (+7.5%).

The reset value of the vid_out_ctrl registers is 0x00; therefore, nominal DAC current is output. Table 33 is an example of how the output current of the DACs varies for a nominal 4.33 mA output current.

Table 33. DAC Gain Control

Reg 0x0A or 0x0B	DAC Current (mA)	% Gain	Note
0100 0000 (0x40)	4.658	7.5000%	
0011 1111 (0x3F)	4.653	7.3820%	
0011 1110 (0x3E)	4.648	7.3640%	
...	...	...	
...	...	...	
0000 0010 (0x02)	4.43	0.0360%	
0000 0001 (0x01)	4.38	0.0180%	
0000 0000 (0x00)	4.33	0.0000%	(I²C Reset Value, Nominal)
1111 1111 (0xFF)	4.25	−0.0180%	
1111 1110 (0xFE)	4.23	−0.0360%	
...	...	...	
...	...	...	
1100 0010 (0xC2)	4.018	−7.3640%	
1100 0001 (0xC1)	4.013	−7.3820%	
1100 0000 (0xC0)	4.008	−7.5000%	

GAMMA CORRECTION

[Subaddresses 0x24 to 0x37 for HD, Subaddresses 0x66 to 0x79 for SD]

Gamma correction is available for SD and HD video. For each standard, there are twenty 8-bit-wide registers. They are used to program the Gamma Correction Curves A and B. HD Gamma Curve A is programmed at Addresses 0x24 to 0x2D, and HD Gamma Curve B is programmed at 0x2E to 0x7. SD Gamma Curve A is programmed at Addresses 0x66 to 0x6F, and SD Gamma Curve B is programmed at Addresses 0x70 to 0x79.

Generally gamma correction is applied to compensate for the nonlinear relationship between signal input and brightness level output (as perceived on the CRT). It can also be applied wherever nonlinear processing is used.

Gamma correction uses the function

$$Signal_{OUT} = (Signal_{IN})^{\gamma}$$

where γ = gamma power factor.

Gamma correction is performed on the luma data only. The user can choose either of two curves, Curve A or Curve B. At any one time, only one of these curves can be used.

The response of the curve is programmed at 10 predefined locations. In changing the values at these locations, the gamma curve can be modified. Between these points, linear interpolation is used to generate intermediate values. If the curve has a total length of 256 points, the 10 locations are at 24, 32, 48, 64, 80, 96, 128, 160, 192, and 224. Locations 0, 16, 240, and 255 are fixed and cannot be changed.

For lengths of 16 to 240 points, the gamma correction curve is calculated as follows:

$$y = x\gamma$$

where:
y = gamma corrected output.
x = linear input signal.
γ = gamma power factor.

To program the gamma correction registers, calculate the seven values for y using the following formula:

$$y_n = \left[\frac{x_{(n-16)}}{(240-16)}\right]\gamma \times (240-16) + 16$$

where:
$x_{(n-16)}$ = value for x along x-axis at points n.
n = 24, 32, 48, 64, 80, 96, 128, 160, 192, or 224.
y_n = value for y along the y-axis, which must be written into the gamma correction register.

For example,

y_{24} = [(8/224)0.5 × 224] + 16 = 58

y_{32} = [(16/224)0.5 × 224] + 16 = 76

y_{48} = [(32/224)0.5 × 224] + 16 = 101

y_{64} = [(48/224)0.5 × 224] + 16 = 120

y_{80} = [(64/224)0.5 × 224] + 16 = 136

y_{96} = [(80/224)0.5 × 224] + 16 = 150

y_{128} = [(112/224)0.5 × 224] + 16 = 174

y_{160} = [(144/224)0.5 × 224] + 16 = 195

y_{192} = [(176/224)0.5 × 224] + 16 = 214

y_{224} = [(208/224)0.5 × 224] + 16 = 232

where the sum of each equation is rounded to the nearest integer.

The gamma curves in Figure 71 and Figure 72 are only examples; any user-defined curve is acceptable in the range of 16 to 240.

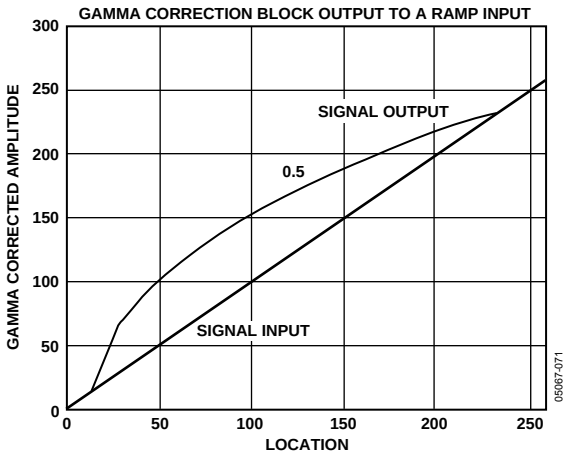


Figure 71. Signal Input (Ramp) and Signal Output for Gamma 0.5

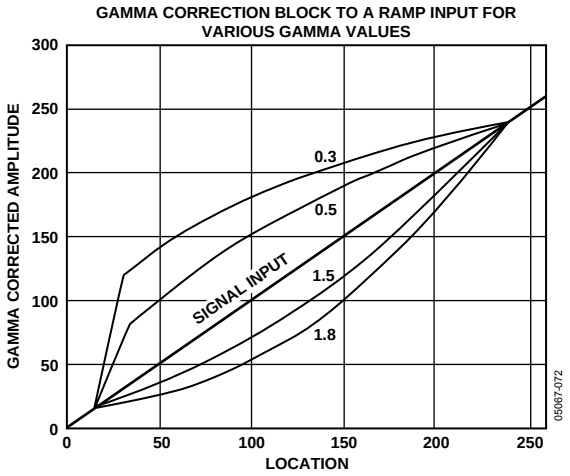


Figure 72. Signal Input (Ramp) and Selectable Output Curves

HD SHARPNESS FILTER AND ADAPTIVE FILTER CONTROLS

[Subaddresses 0x20, 0x38 to 0x3D]

There are three filter modes available on the ADV7320/ADV7321: sharpness filter mode and two adaptive filter modes.

HD Sharpness Filter Mode

To enhance or attenuate the Y signal in the frequency ranges shown in Figure 73, the HD sharpness filter must be enabled and the HD adaptive filter enable must be disabled.

To select one of the 256 individual responses, the corresponding gain values, which range from –8 to +7, for each filter must be programmed into the HD sharpness filter gain register at Address 0x20.

HD Adaptive Filter Mode

The HD Adaptive Filter Threshold A, B, and C registers, the HD Adaptive Filter Gain 1, 2, and 3 registers, and the HD sharpness gain register are used in adaptive filter mode. To activate the adaptive filter control, the HD sharpness filter and the HD adaptive filter must be enabled.

The derivative of the incoming signal is compared to the three programmable threshold values: HD Adaptive Filter Threshold A, B, and C. The recommended threshold range is from 16 to 235, but any value between 0 and 255 can be used.

The edges can then be attenuated with the settings in the HD Adaptive Filter Gain 1, 2, and 3 registers, and HD sharpness filter gain register.

According to the settings of the HD adaptive filter mode control, there are two adaptive filter modes available:

- Mode A is used when adaptive filter mode is set to 0. In this case, Filter B (LPF) is used in the adaptive filter block. Also, only the programmed values for Gain B in the HD sharpness filter gain and HD Adaptive Filter Gain 1, 2, and 3 are applied when needed. The Gain A values are fixed and cannot be changed.
- Mode B is used when adaptive filter mode is set to 1. In this mode, a cascade of Filter A and Filter B is used. Settings for Gain A and Gain B in the HD sharpness filter gain and HD Adaptive Filter Gain 1, 2, and 3 become active when needed.

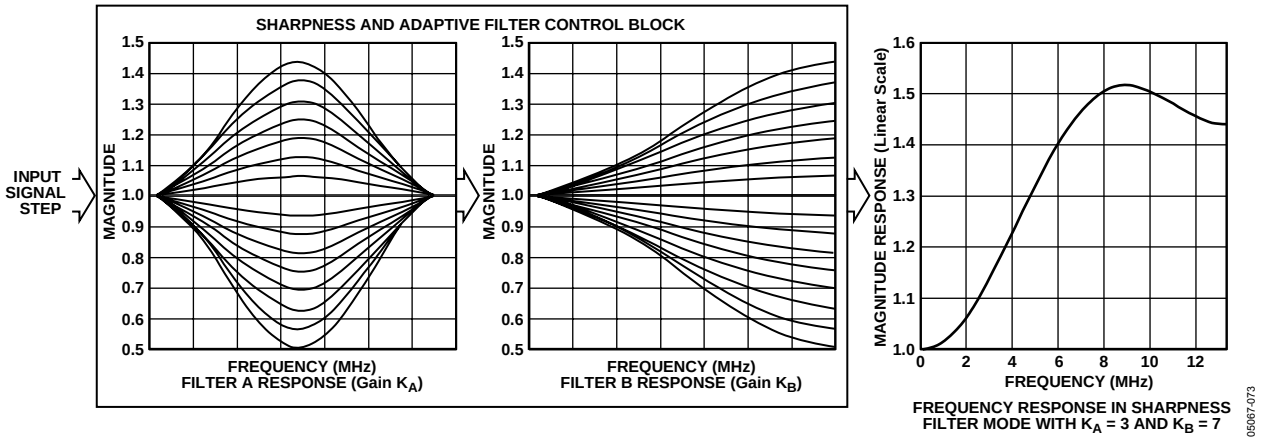


Figure 73. Sharpness and Adaptive Filters Control Block

HD SHARPNESS FILTER AND ADAPTIVE FILTER APPLICATION EXAMPLES

HD Sharpness Filter Application

The HD sharpness filter can be used to enhance or attenuate the Y video output signal. The register settings listed in Table 34 were used to achieve the results shown in Figure 74. Input data was generated by an external signal source.

Table 34. Sharpness Control

Address	Register Setting	Reference[1]
0x00	0xFC	
0x01	0x10	
0x02	0x20	
0x10	0x00	
0x11	0x81	
0x20	0x00	a
0x20	0x08	b
0x20	0x04	c
0x20	0x40	d
0x20	0x80	e
0x20	0x22	f

[1] See Figure 74.

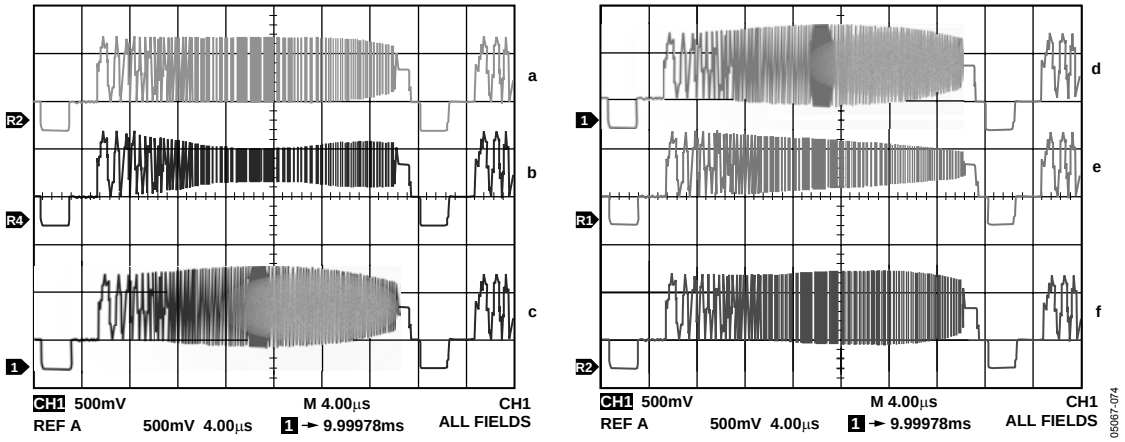


Figure 74. HD Sharpness Filter Control with Different Gain Settings for HD Sharpness Filter Gain Values

Adaptive Filter Control Application

Figure 75 and Figure 76 show how a typical signal is processed by the adaptive filter control block in Mode A.

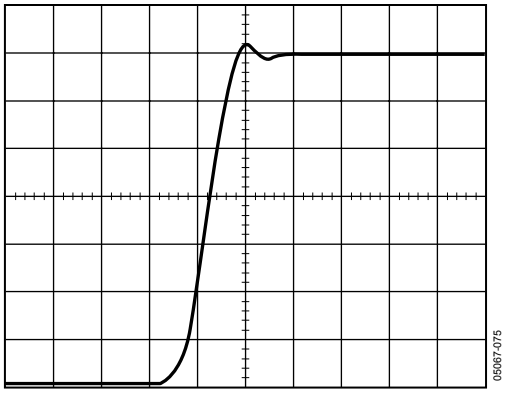


Figure 75. Input Signal to Adaptive Filter Control

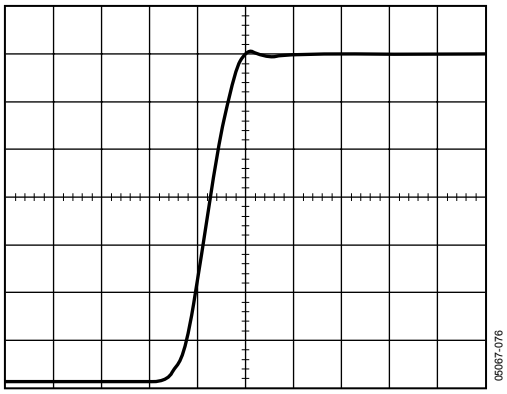


Figure 76. Output Signal with Adaptive Filter Control (Mode A)

The register settings in Table 35 were used to obtain the results shown in Figure 76 (to remove the ringing on the Y signal). Input data was generated by an external signal source.

Table 35. Register Settings for Figure 76

Address	Register Setting
0x00	0xFC
0x01	0x38
0x02	0x20
0x10	0x00
0x11	0x81
0x15	0x80
0x20	0x00
0x38	0xAC
0x39	0x9A
0x3A	0x88
0x3B	0x28
0x3C	0x3F
0x3D	0x64

When changing the adaptive filter mode to Mode B [Address 0x15, Bit 6], the output shown in Figure 77 can be obtained from the input signal shown in Figure 75.

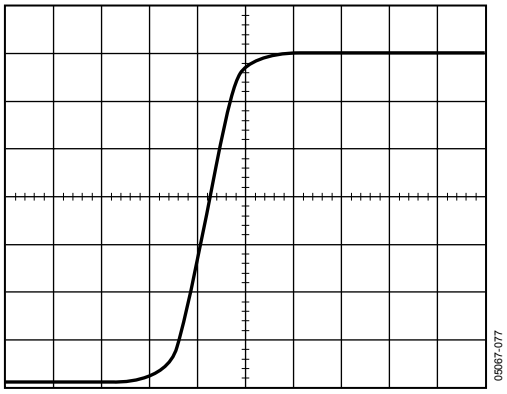


Figure 77. Output Signal with Adaptive Filter Control (Mode B)

SD DIGITAL NOISE REDUCTION

[Subaddresses 0x63, 0x64, 0x65]

DNR is applied to the Y data only. A filter block selects the high frequency, low amplitude components of the incoming signal (DNR input select). The absolute value of the filter output is compared to a programmable threshold value (DNR threshold control). There are two DNR modes available: DNR mode and DNR sharpness mode.

In DNR mode, if the absolute value of the filter output is less than the threshold, it is assumed to be noise. A programmable amount (coring gain border, coring gain data) of this noise signal is subtracted from the original signal. Likewise, in DNR sharpness mode, if the absolute value of the filter output is less than the programmed threshold, it is assumed to be noise. If the level exceeds the threshold and is identified as a valid signal, a fraction of the signal (coring gain border, coring gain data) is added to the original signal to boost high frequency components and sharpen the video image.

In MPEG systems, it is common to process the video information in blocks of 8 pixels × 8 pixels for MPEG2 systems, or 16 pixels × 16 pixels for MPEG1 systems (block size control). DNR can be applied to the resulting block transition areas that are known to contain noise. Generally, the block transition area contains two pixels. It is possible to define this area to contain four pixels (border area).

It is also possible to compensate for variable block positioning or differences in YCrCb pixel timing with the use of the DNR block offset.

The digital noise reduction registers are three 8-bit registers. They are used to control the DNR processing.

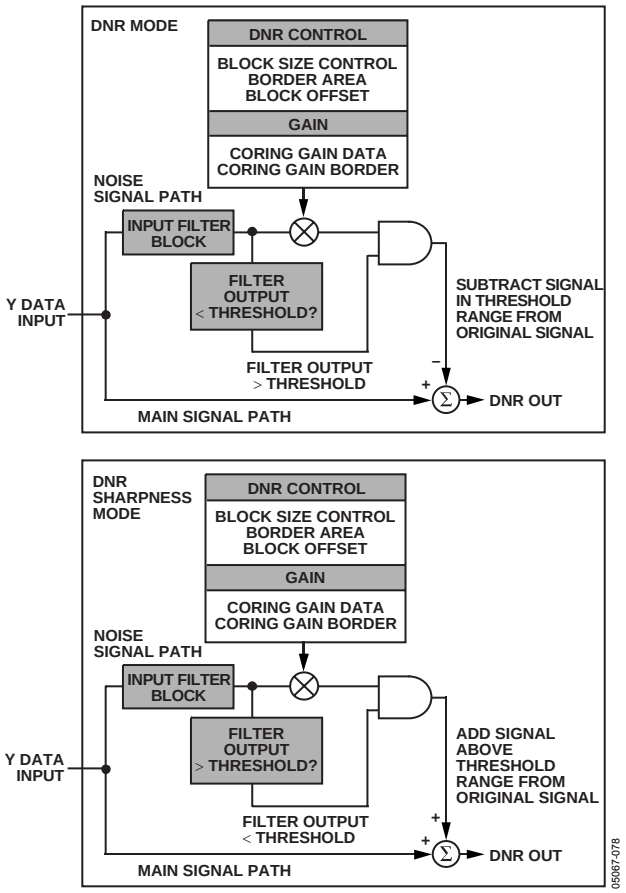


Figure 78. DNR Block Diagram

CORING GAIN BORDER

[Address 0x63, Bits 3 to 0]

These four bits are assigned to the gain factor applied to border areas. In DNR mode, the range of gain values is 0 to 1 in increments of 1/8. This factor is applied to the DNR filter output, which lies below the set threshold range. The result is then subtracted from the original signal.

In DNR sharpness mode, the range of gain values is 0 to 0.5 in increments of 1/16. This factor is applied to the DNR filter output, which lies above the threshold range. The result is added to the original signal.

CORING GAIN DATA

[Address 0x63, Bits 7 to 4]

These four bits are assigned to the gain factor applied to the luma data inside the MPEG pixel block. In DNR mode, the range of gain values is 0 to 1 in increments of 1/8. This factor is applied to the DNR filter output, which lies below the set threshold range. The result is then subtracted from the original signal.

In DNR sharpness mode, the range of gain values is 0 to 0.5 in increments of 1/16. This factor is applied to the DNR filter output, which lies above the threshold range. The result is added to the original signal.

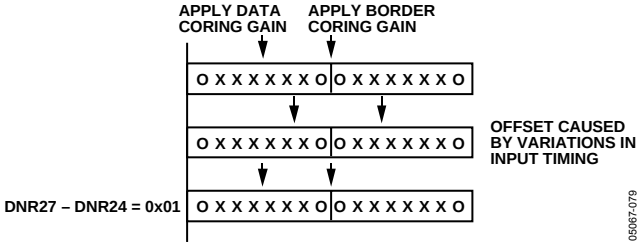


Figure 79. DNR Offset Control

DNR THRESHOLD

[Address 0x64, Bits 5 to 0]

These six bits are used to define the threshold value in the range of 0 to 63. The range is an absolute value.

BORDER AREA

[Address 0x64, Bit 6]

When this bit is set to Logic 1, the block transition area can be defined to consist of four pixels. If this bit is set to Logic 0, the border transition area consists of two pixels, where one pixel refers to two clock cycles at 27 MHz.

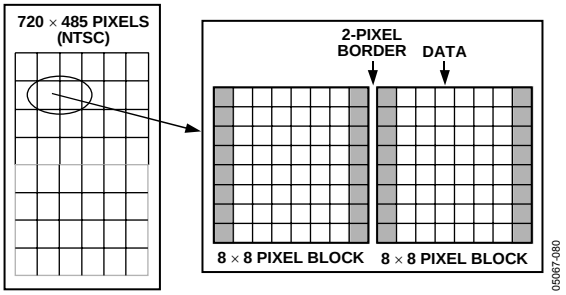


Figure 80. DNR Border Area

BLOCK SIZE CONTROL

[Address 0x64, Bit 7]

This bit is used to select the size of the data blocks to be processed. Setting the block size control function to Logic 1 defines a 16-pixel × 16-pixel data block, and Logic 0 defines an 8-pixel × 8-pixel data block, where one pixel refers to two clock cycles at 27 MHz.

DNR INPUT SELECT CONTROL

[Address 0x65, Bits 2 to 0]

Three bits are assigned to select the filter, which is applied to the incoming Y data. The signal that lies in the pass band of the selected filter is DNR processed. Figure 81 shows the filter responses selectable with this control.

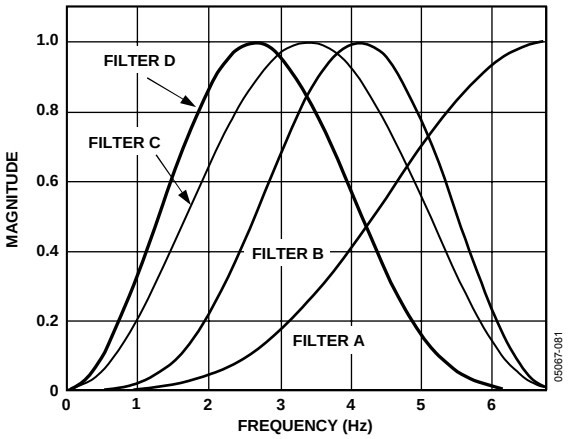


Figure 81. DNR Input Select

DNR MODE CONTROL

[Address 0x65, Bit 4]

This bit is used to select the DNR mode. Logic 0 selects DNR mode; Logic 1 selects DNR sharpness mode.

DNR works on the principle of defining low amplitude, high frequency signals as probable noise and subtracting this noise from the original signal.

In DNR mode, it is possible to subtract a fraction of the signal that lies below the set threshold, assumed to be noise, from the original signal. The threshold is set in DNR Register 1.

When DNR sharpness mode is enabled, it is possible to add a fraction of the signal that lies above the set threshold to the original signal, since this data is assumed to be valid data and not noise. The overall effect is that the signal is boosted (similar to using an extended SSAF filter).

BLOCK OFFSET CONTROL

[Address 0x65, Bits 7 to 4]

Four bits are assigned to this control, which allows a maximum shift of 15 pixels in a data block. Consider the fixed coring gain positions. The block offset shifts the data in steps of one pixel such that the border coring gain factors can be applied at the same position regardless of variations in input timing of the data.

SD ACTIVE VIDEO EDGE

[Subaddress 0x42, Bit 7]

When the active video edge feature is enabled, the first three pixels and the last three pixels of the active video on the luma channel are scaled so that maximum transitions on these pixels are not possible. The scaling factors are ×1/8, ×1/2, and ×7/8. All other active video passes through unprocessed.

SAV/EAV STEP-EDGE CONTROL

The ADV7320/ADV7321 have the capability of controlling fast rising and falling signals at the start and end of active video to minimize ringing.

An algorithm monitors SAV and EAV and determines when the edges are rising or falling too fast. The result is reduced ringing at the start and end of active video for fast transitions. Subaddress 0x42, Bit 7 = 1, enables this feature.

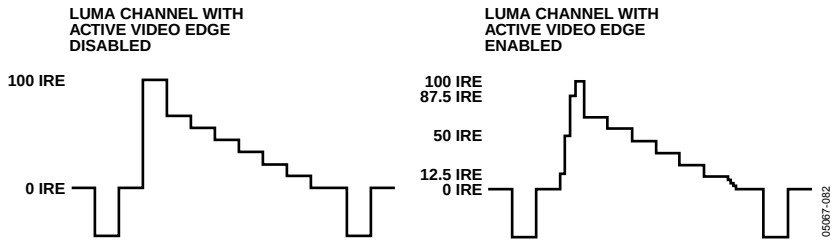


Figure 82. Example of Active Video Edge Functionality

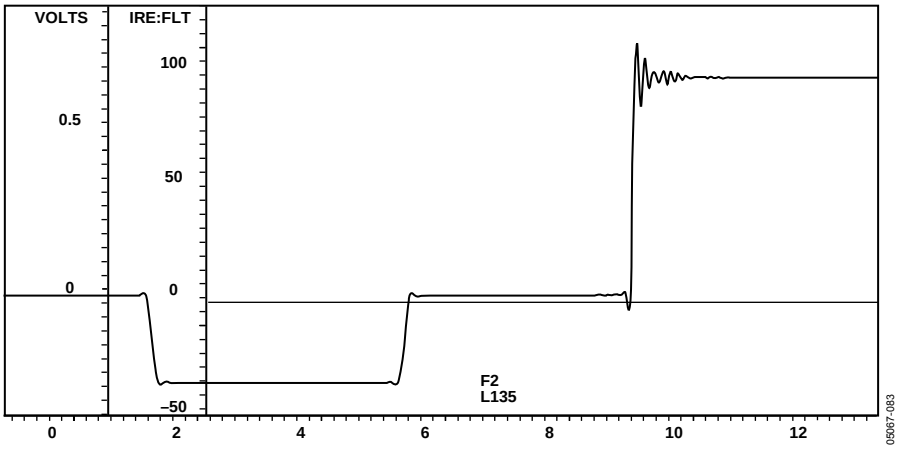


Figure 83. Address 0x42, Bit 7 = 0

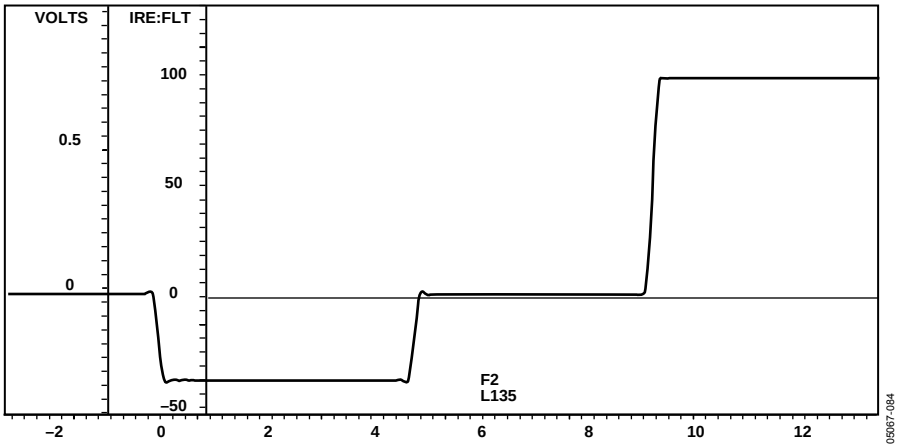


Figure 84. Address 0x42, Bit 7 = 1

HSYNC/VSYNC OUTPUT CONTROL

The ADV7320/ADV7321 have the ability to accept either embedded time codes in the input data, or external Hsync and Vsync signals on P_HSYNC/P_VSYNC, outputting the respective signals on the S_HSYNC and S_VSYNC pins.

Table 36. Hsync Output Control[1]

HD/ED[2] Slave Mode (0x10, Bit 2)	HD/ED Sync Output Enable (0x02, Bit 7)	SD Sync Output Enable (0x02, Bit 6)	I2C_Hsync_gen_sel (0x14, Bit 1)	Signal on S_HSYNC Pin	Duration
x	0	0	x	Tristate	–
x	0	1	x	Pipelined SD Hsync	See Appendix 5—SD Timing Modes
External Hsync and Vsync/Field Mode	1	x	0	External Pipelined HD/ED Hsync	As per Hsync timing
EAV/SAV Mode	1	x	0	Pipelined HD/ED Hsync based on AV Code H bit	Same as line blanking interval
x	1	x	1	Pipelined HD/ED Hsync based on horizontal counter	Same as embedded Hsync

[1] In all HD/ED standards where there is an Hsync o/p, the start of the Hsync pulse is aligned with the falling edge of the embedded Hsync in the output video.
[2] ED = enhanced definition.

Table 37. Vsync Output Control[1]

HD/ED[2] Slave Mode (0x10, Bit 2)	HD/ED Sync Output Enable (0x02, Bit 7)	SD Sync Output Enable (0x02, Bit 6)	I2C_Vsync _gen_sel (0x14, Bit 2)	Video Standard	Signal on S_VSYNC Pin	Duration
x	0	0	x	x	Tristate	–
x	0	1	x	Interlaced	Pipelined SD Vsync/field	See Appendix 5—SD Timing Modes
External Hsync and Vsync/Field Mode	1	x	0	x	External pipelined HD/ED Vsync or field signal	As per external Vsync or field signal
EAV/SAV Mode	1	x	0	All HD interlace standards	External pipelined field signal based on AV Code F bit	Field
EAV/SAV Mode	1	x	0	All HD/ED progressive standards	Pipelined Vsync based on AV Code V bit	Vertical blanking interval
x	1	x	1	All HD/ED standards except 525p	External pipelined HD/ED Vsync based on vertical counter	Aligned with serration lines
x	1	x	1	525p	External pipelined HD/ED VSYNC based on vertical counter	Vertical blanking interval

[1] In all HD/ED standards where there is an Hsync o/p, the start of the Hsync pulse is aligned with the falling edge of the embedded Hsync in the output video.
[2] ED = enhanced definition = progressive scan 525p or 625p.

BOARD DESIGN AND LAYOUT

DAC TERMINATION AND LAYOUT CONSIDERATIONS

The ADV7320/ADV7321 contain an on-board voltage reference. The ADV7320/ADV7321 can be used with an external V_{REF} (AD1580).

The R_{SET} resistors are connected between the R_{SET} pins and AGND and are used to control the full-scale output current and, therefore, the DAC voltage output levels. For full-scale output, R_{SET} must have a value of 3040 Ω. The R_{SET} values should not be changed. R_{LOAD} has a value of 300 Ω for full-scale output.

VIDEO OUTPUT BUFFER AND OPTIONAL OUTPUT FILTER

Output buffering on all six DACs is necessary to drive output devices, such as SD or HD monitors. Analog Devices produces a range of suitable op amps for this application, for example, the AD8061. More information on line-driver buffering circuits is given in the relevant op amps' data sheets.

An optional analog reconstruction low-pass filter (LPF) may be required as an anti-imaging filter if the ADV7320/ADV7321 are connected to a device that requires this filtering.

The filter specifications vary with the application.

Table 38. External Filter Requirements

Application	Oversampling	Cutoff Frequency (MHz)	Attenuation −50 dB @ (MHz)
SD	2×	>6.5	20.5
SD	16×	>6.5	209.5
PS	1×	>12.5	14.5
PS	8×	>12.5	203.5
HDTV	1×	>30	44.25
HDTV	2×	>30	118.5

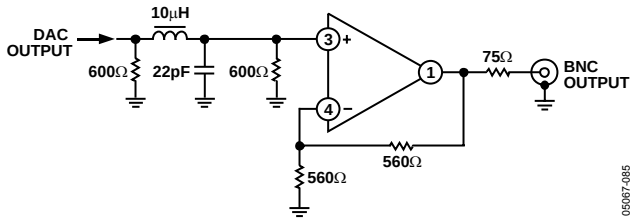


Figure 85. Example of Output Filter for SD, 16× Oversampling

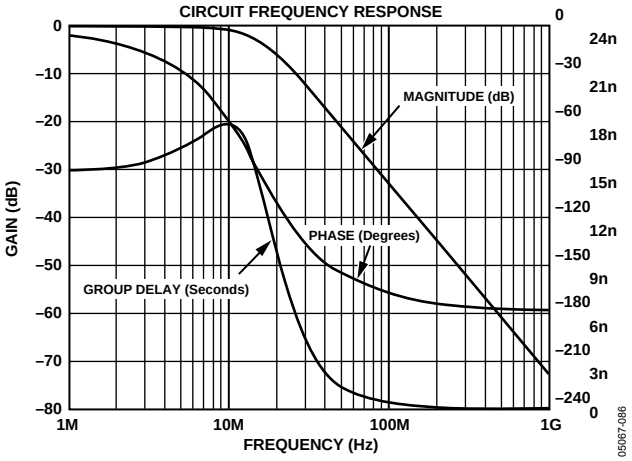


Figure 86. Filter Plot for Output Filter for SD, 16× Oversampling

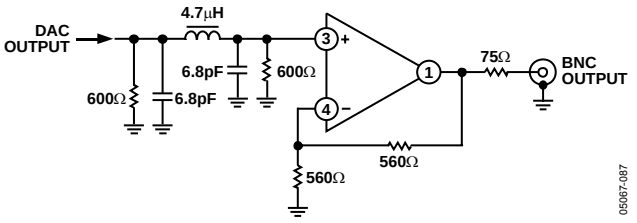


Figure 87. Example of Output Filter for PS, 8× Oversampling

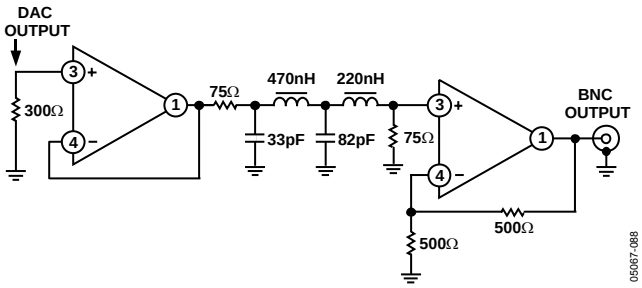


Figure 88. Example of Output Filter for HDTV, 2× Oversampling

Table 39. Possible Output Rates from the ADV7320/ADV7321

Input Mode Address 0x01, Bits 6 to 4	PLL Address 0x00, Bit 1	Output Rate (MHz)
SD Only	Off	27 (2×)
	On	216 (16×)
PS Only	Off	27 (1×)
	On	216 (8×)
HDTV Only	Off	74.25 (1×)
	On	148.5 (2×)

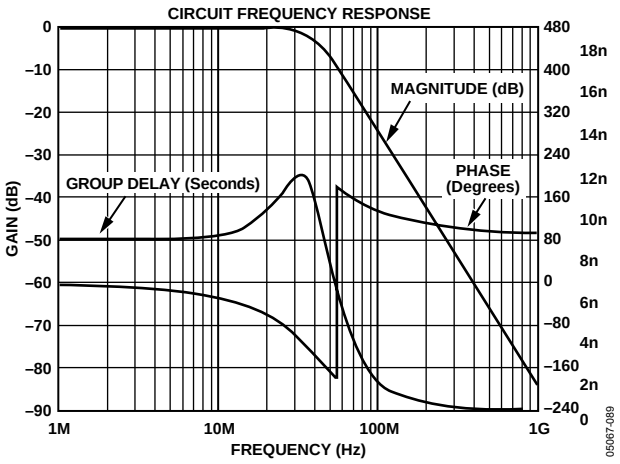


Figure 89. Filter Plot for Output Filter for PS, 8× Oversampling

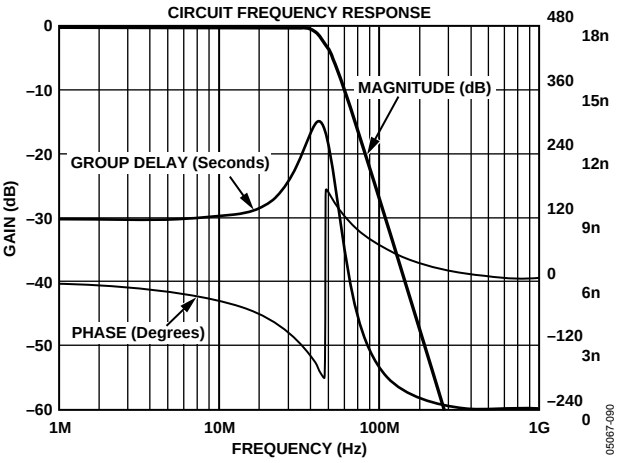


Figure 90. Filter Plot for Output Filter for HDTV, 2× Oversampling

PCB BOARD LAYOUT

The ADV7320/ADV7321 are optimally designed for lowest noise performance of both radiated and conducted noise. To complement the excellent noise performance of the ADV7320/ADV7321, it is imperative that great care be given to the PC board layout.

The layout should be optimized for lowest noise on the ADV7320/ADV7321 power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and AGND, V_{DD} and DGND, and V_{DD_IO} and GND_IO pins should be kept as short as possible to minimized inductive ringing.

It is recommended that a 4-layer printed circuit board is used, with power and ground planes separating the layer of the signal carrying traces of the components and solder side layer. Component placement should be carefully considered in order to separate noisy circuits, such as crystal clocks, high speed logic circuitry, and analog circuitry.

There should be a separate analog ground plane and a separate digital ground plane.

Each power plane should encompass a digital power plane and an analog power plane. The analog power plane should contain the DACs and all associated circuitry, V_{REF} circuitry. The digital power plane should contain all logic circuitry.

The analog and digital power planes should be individually connected to the common power plane at a single point through a suitable filtering device, such as a ferrite bead.

DAC output traces on a PCB should be treated as transmission lines. It is recommended that the DACs be placed as close as possible to the output connector, with the analog output traces being as short as possible (less than 3 inches). The DAC termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB's ground plane. As well as minimizing reflections, short analog output traces reduce noise pickup from neighboring digital circuitry.

To avoid crosstalk between the DAC outputs, it is recommended that as much space as possible be left between the tracks of the individual DAC output pins. The addition of ground tracks between outputs is also recommended.

Supply Decoupling

Noise on the analog power plane can be further reduced by the use of decoupling capacitors.

Optimum performance is achieved by the use of 10 nF and 0.1 µF ceramic capacitors. Each group of V_{AA}, V_{DD}, or V_{DD_IO} pins should be individually decoupled to ground. This should be done by placing the capacitors as close as possible to the device with the capacitor leads as short as possible, thus minimizing lead inductance.

A 1 µF tantalum capacitor is recommended across the V_{AA} supply in addition to 10 nF ceramic. See the circuit layout in Figure 91.

Digital Signal Interconnect

The digital signal lines should be isolated as much as possible from the analog outputs and other analog circuitry. Digital signal lines should not overlay the analog power plane.

Due to the high clock rates, avoid long clock lines to the ADV7320/ADV7321 to minimize noise pickup.

Any active pull-up termination resistors for the digital inputs should be connected to the digital power plane and not the analog power plane.

Analog Signal Interconnect

Locate the ADV7320/ADV7321 as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

For optimum performance, each analog output should be source- and load-terminated, as shown in Figure 91. The termination resistors should be as close as possible to the ADV7320/ADV7321 to minimize reflections.

For optimum performance, it is recommended that all decoupling and external components relating to the ADV7320/ADV7321 are located on the same side of the PCB and as close as possible to the ADV7320/ADV7321. Unused inputs should be tied to ground.

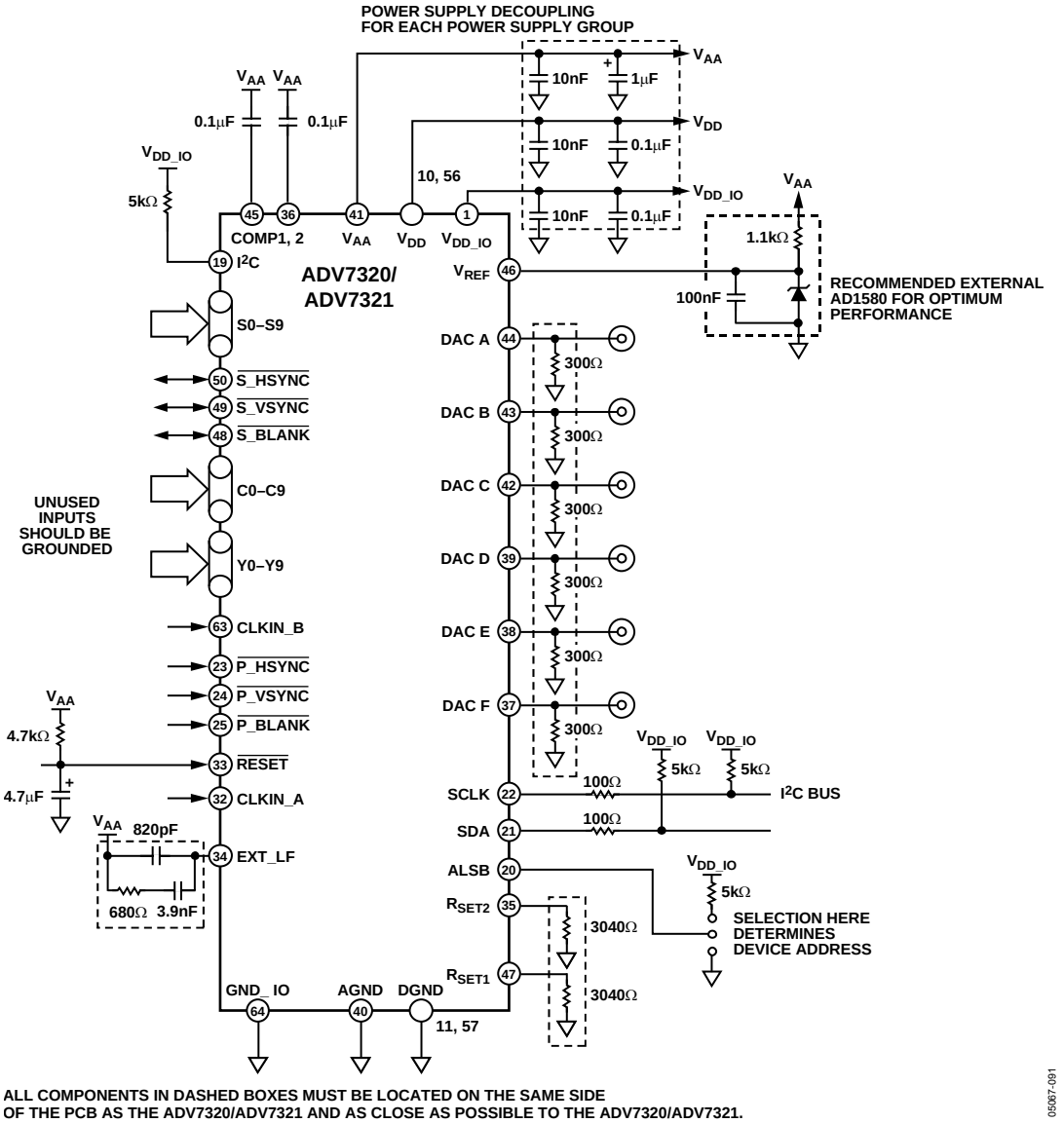


Figure 91. ADV7320/ADV7321 Circuit Layout

APPENDIX 1—COPY GENERATION MANAGEMENT SYSTEM

PS CGMS

Data Registers 2 to 0

[Subaddresses 0x21, 0x22, 0x23]

525p

Using the vertical blanking interval 525p system, 525p CGMS conforms to the CGMS-A EIA-J CPR1204-1 (March 1998) transfer method of video identification information and to the IEC61880 (1998) 525p/60 video system's analog interface for the video and accompanying data.

When PS CGMS is enabled [Subaddress 0x12, Bit 6 = 1], CGMS data is inserted on Line 41. The 525p CGMS data registers are at Addresses 0x21, 0x22, and 0x23.

625p

The 625p CGMS conforms to the IEC62375 (2004) 625p/50 video system's analog interface for the video and accompanying data using the vertical blanking interval.

When PS CGMS is enabled [Subaddress 0x12, Bit 6 = 1], CGMS data is inserted on Line 43. The 625p CGMS data registers are at Addresses 0x22, and 0x23.

HD CGMS

[Address 0x12, Bit 6]

The ADV7320/ADV7321 support copy generation management system (CGMS) in HDTV mode (720p and 1080i) in accordance with EIAJ CPR-1204-2.

The HD CGMS data registers are found at Addresses 0x021, 0x22, and 0x23.

SD CGMS

Data Registers 2 to 0

[Subaddresses 0x59, 0x5A, 0x5B]

The ADV7320/ADV7321 support copy generation management system (CGMS), conforming to the EIAJ CPR-1204 and ARIB TR-B15 standards. CGMS data is transmitted on Line 20 for odd fields and Line 283 for even fields. Bits C/W05 and C/W06 control whether CGMS data is output on odd or even fields. CGMS data can only be transmitted when the ADV7320/ADV7321 are configured in NTSC mode. The CGMS data is 20 bits long. The CGMS data is preceded by a reference pulse of the same amplitude and duration as a CGMS bit (see Figure 94).

720p System

CGMS data is applied to Line 24 of the luminance vertical blanking interval.

1080i System

CGMS data is applied to Line 19 and Line 582 of the luminance vertical blanking interval.

CGMS FUNCTIONALITY

If SD CGMS CRC [Address 0x59, Bit 4] or PS/HD CGMS CRC [Subaddress 0x12, Bit 7] is set to Logic 1, the last six bits, C19 to C14, which compose the 6-bit CRC check sequence, are automatically calculated on the ADV7320/ADV7321. This calculation is based on the lower 14 bits (C0 to C13) of the data in the data registers and output with the remaining 14 bits to form the complete 20 bits of the CGMS data. The calculation of the CRC sequence is based on the polynomial $x^6 + x + 1$ with a preset value of 111111. If SD CGMS CRC [Address 0x59, Bit 4] and PS/HD CGMS CRC [Address 0x12, Bit 7] are set to Logic 0, all 20 bits (C0 to C19) are output directly from the CGMS registers (CRC must be manually calculated by the user).

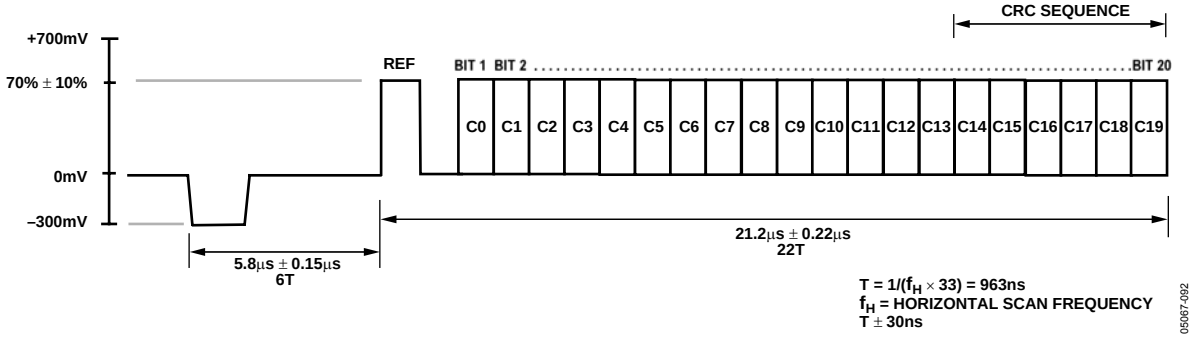


Figure 92. PS 525p CGMS Waveform (Line 41)

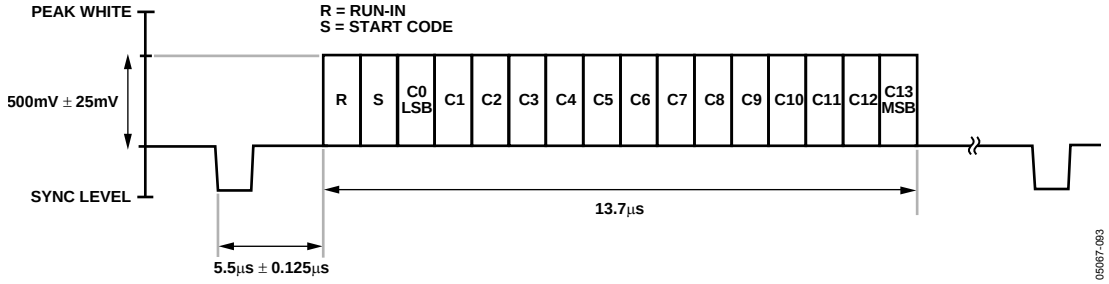


Figure 93. PS 625p CGMS-A Waveform (Line 43)

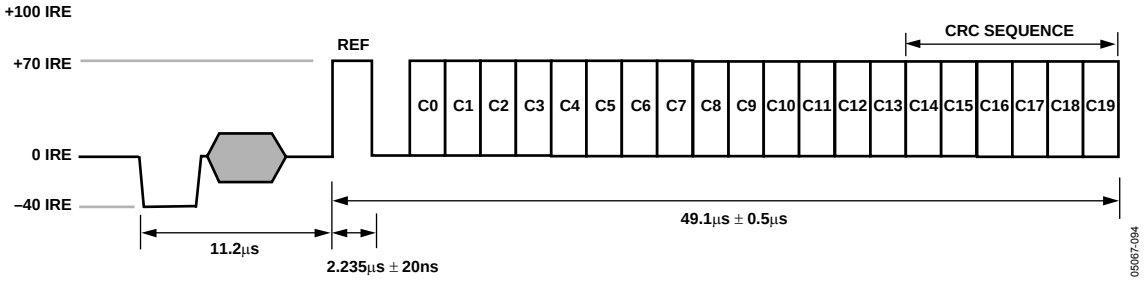


Figure 94. SD CGMS Waveform

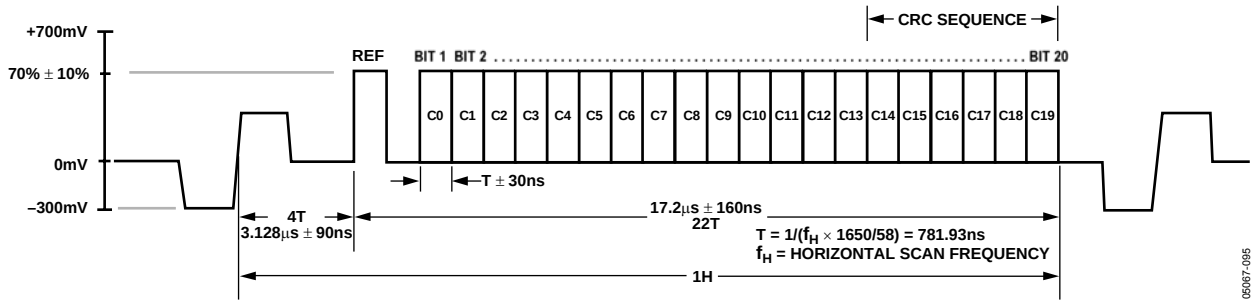


Figure 95. HDTV 720p CGMS Waveform

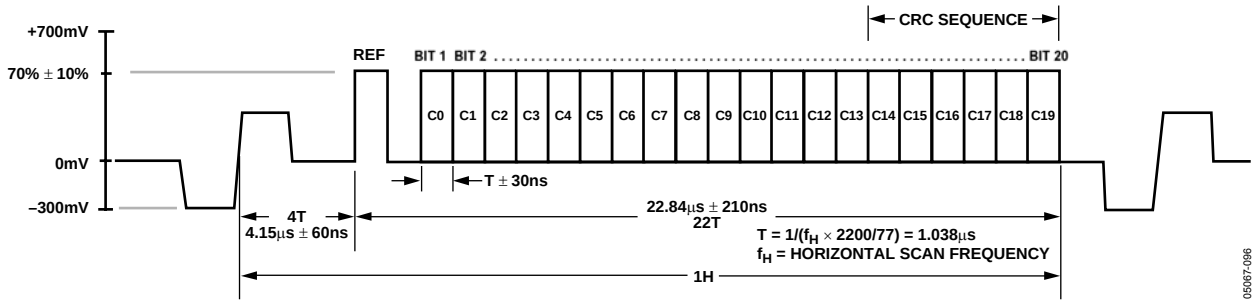


Figure 96. HDTV 1080i CGMS Waveform

APPENDIX 2—SD WIDE SCREEN SIGNALING

[Subaddresses 0x59, 0x5A, 0x5B]

The ADV7320/ADV7321 support wide screen signaling (WSS) conforming to the ETS 300 294 standard. WSS data is transmitted on Line 23. WSS data can be transmitted only when the device is configured in PAL mode. The WSS data is 14 bits long, and the function of each bit is shown in Table 40. The WSS data is preceded by a run-in sequence and a start code (see Figure 97). If SD WSS [Address 0x59, Bit 7] is set to Logic 1, it enables the WSS data to be transmitted on Line 23. The latter portion of Line 23 (42.5 sec after the falling edge of $\overline{\text{HSYNC}}$) is available for the insertion of video. It is possible to blank the WSS portion of Line 23 with Subaddress 0x61, Bit 7.

Table 40. Function of WSS Bits

Bit				**Description**		
Bit 0 to Bit 2				Aspect ratio/format/position		
Bit 3				Odd parity check of Bit 0 to Bit 2		
B0	**B1**	**B2**	**B3**	**Aspect Ratio**	**Format**	**Position**
0	0	0	1	4:3	Full format	N/A
1	0	0	0	14:9	Letterbox	Center
0	1	0	0	14:9	Letterbox	Top
1	1	0	1	16:9	Letterbox	Center
0	0	1	0	16:9	Letterbox	Top
1	0	1	1	>16:9	Letterbox	Center
0	1	1	1	14:9	Full format	Center
1	1	1	0	16:9	N/A	N/A
1	1	1	0	16:9		
B4						
0				Camera mode		
1				Film mode		
B5						
0				Standard coding		
1				Motion adaptive color plus		
B6						
0				No helper		
1				Modulated helper		
B7				Reserved		
B9		**B10**				
0		0		No open subtitles		
1		0		Subtitles in active image area		
0		1		Subtitles out of active image area		
1		1		Reserved		
B11						
0				No surround sound information		
1				Surround sound mode		
B12				Reserved		
B13				Reserved		

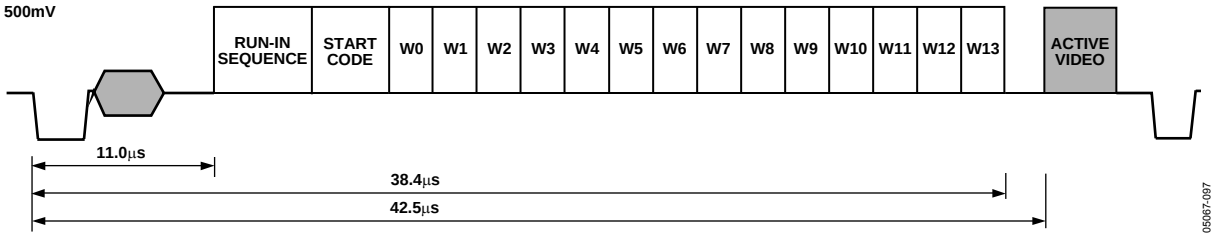


Figure 97. WSS Waveform Diagram

APPENDIX 3—SD CLOSED CAPTIONING

[Subaddresses 0x51 to 0x54]

The ADV7320/ADV7321 support closed captioning conforming to the standard television synchronizing waveform for color transmission. Closed captioning is transmitted during the blanked active line time of Line 21 of the odd fields and Line 284 of the even fields.

Closed captioning consists of a 7-cycle sinusoidal burst that is frequency- and phase-locked to the caption data. After the clock run-in signal, the blanking level is held for two data bits and is followed by a Logic 1 start bit. Sixteen bits of data follow the start bit. These consist of two 8-bit bytes, seven data bits, and one odd parity bit. The data for these bytes is stored in the SD closed captioning registers [Addresses 0x53 to 0x54].

The ADV7320/ADV7321 also support the extended closed captioning operation, which is active during even fields and encoded on Scan Line 284. The data for this operation is stored in the SD closed captioning registers [Addresses 0x51 to 0x52].

All clock run-in signals and timing to support closed captioning on Lines 21 and 284 are generated automatically by the ADV7320/ADV7321. All pixels inputs are ignored during Lines 21 and 284 if closed captioning is enabled.

FCC Code of Federal Regulations (CFR) 47 section 15.119 and EIA608 describe the closed captioning information for Line 21 and Line 284.

The ADV7320/ADV7321 use a single-buffering method. This means that the closed captioning buffer is only 1 byte deep; therefore, there is no frame delay in outputting the closed captioning data, unlike other 2-byte-deep buffering systems. The data must be loaded one line before it is output on Line 21 and Line 284. A typical implementation of this method is to use $\overline{\text{VSYNC}}$ to interrupt a microprocessor, which in turn loads the new data (2 bytes) in every field. If no new data is required for transmission, 0s must be inserted in both data registers; this is called nulling. It is also important to load control codes, all of which are double bytes, on Line 21, or a TV will not recognize them. If there is a message such as "Hello World" that has an odd number of characters, it is important to add a blank character at the end so that the end-of-caption, 2-byte control code lands in the same field.

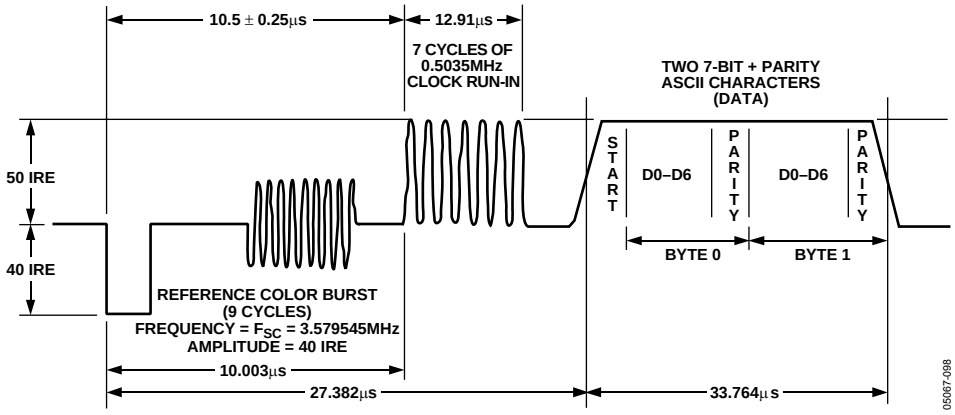


Figure 98. Closed Captioning Waveform, NTSC

APPENDIX 4—TEST PATTERNS

The ADV7320/ADV7321 can generate SD and HD test patterns.

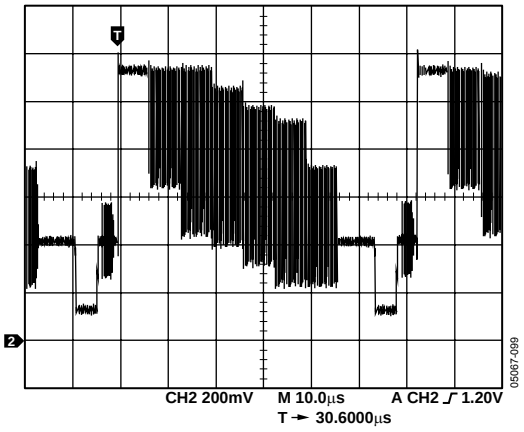


Figure 99. NTSC Color Bars

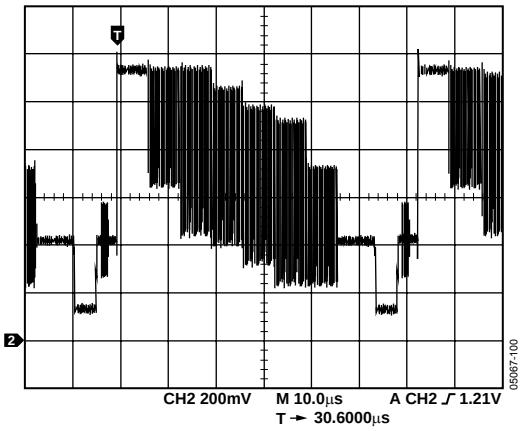


Figure 100. PAL Color Bars

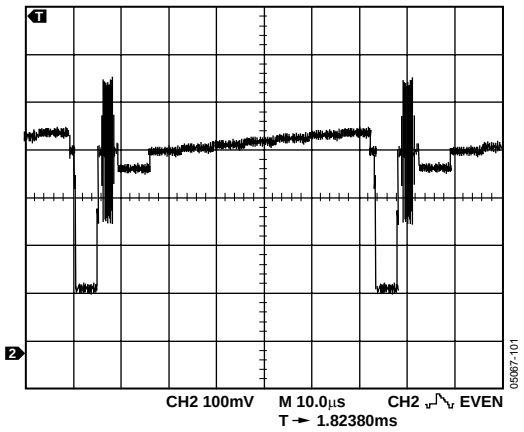


Figure 101. NTSC Black Bar
(–21 mV, 0 mV, 3.5 mV, 7 mV, 10.5 mV, 14 mV,18 mV, 23 mV)

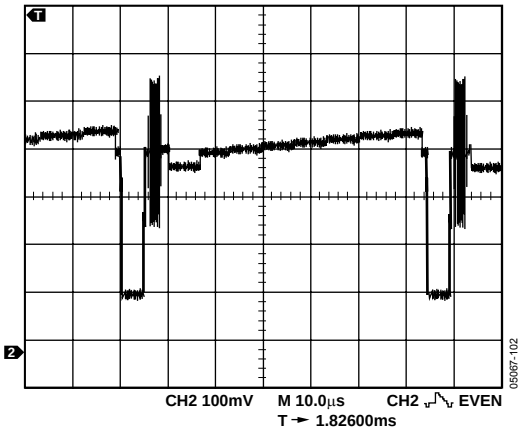


Figure 102. PAL Black Bar
(–21 mV, 0 mV, 3.5 mV, 7 mV, 10.5 mV, 14 mV, 18 mV, 23 mV)

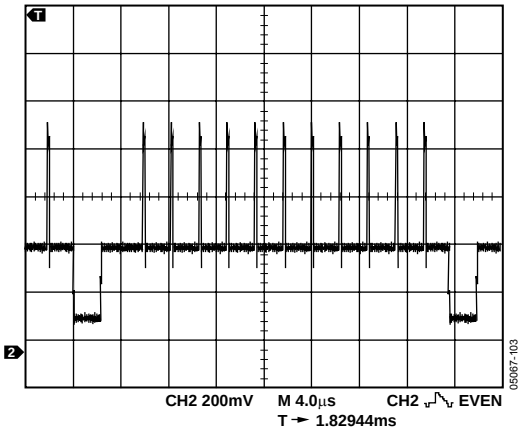


Figure 103. 525p Hatch Pattern

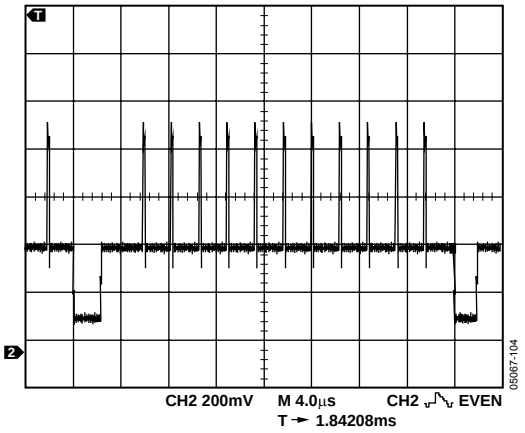


Figure 104. 625p Hatch Pattern

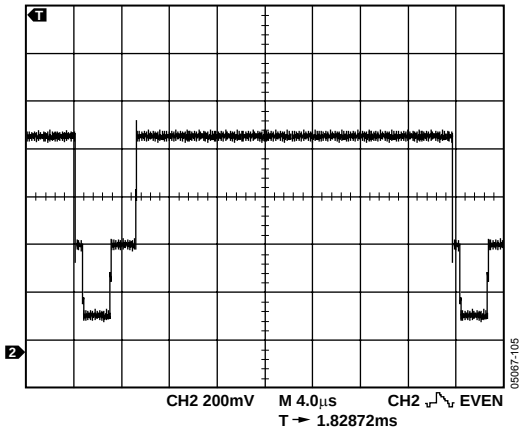


Figure 105. 525p Field Pattern

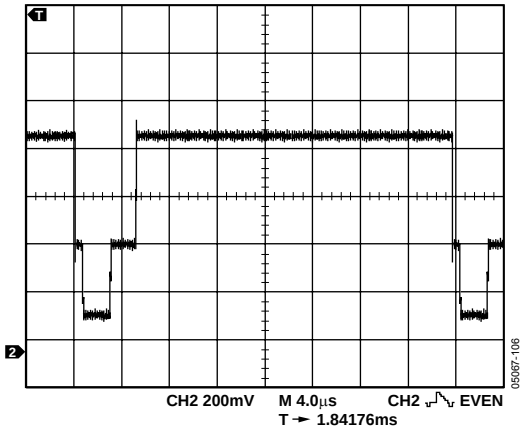


Figure 106. 625p Field Pattern

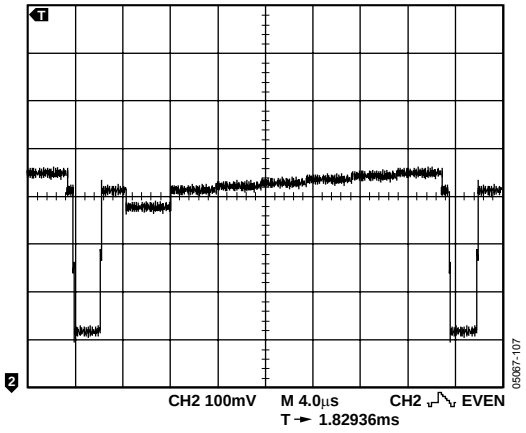


Figure 107. 525p Black Bar
(–35 mV, 0 mV, 7 mV, 14 mV, 21 mV, 28 mV, 35 mV)

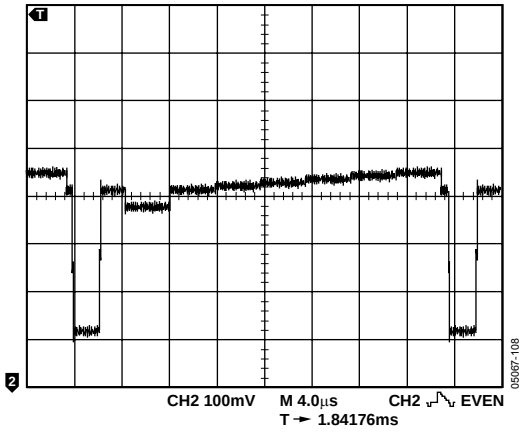


Figure 108. 625p Black Bar
(–35 mV, 0 mV, 7 mV, 14 mV, 21 mV, 28 mV, 5 mV)

The register settings in Table 41 are used to generate an SD NTSC CVBS output on DAC A, S-video on DACs B and C, and YPrPb on DACs D, E, and F. Upon power-up, the subcarrier registers are programmed with the appropriate values for NTSC. All other registers are set as normal/default.

Table 41. NTSC Test Pattern Register Writes

Subaddress	Register Setting
0x00	0xFC
0x40	0x10
0x42	0x40
0x44	0x40 (internal test pattern on)
0x4A	0x08

For PAL CVBS output on DAC A, the same settings are used, except Subaddress 0x40 is programmed to 0x11 and the F_{SC} registers are programmed as shown in Table 42.

Table 42. PAL F_{SC} Register Writes

Subaddress	Description	Register Setting
0x4C	$F_{SC}0$	0xCB
0x4D	$F_{SC}1$	0x8A
0x4E	$F_{SC}2$	0x09
0x4F	$F_{SC}3$	0x2A

Note that when programming the F_{SC} registers, the user must write the values in the sequence $F_{SC}0$, $F_{SC}1$, $F_{SC}2$, $F_{SC}3$. The full F_{SC} value is only accepted after the $F_{SC}3$ write is complete.

The register settings in Table 43 are used to generate a 525p hatch pattern on DAC D, E, and F. All other registers are set as normal/default.

Table 43. 525p Test Pattern Register Writes

Subaddress	Register Setting
Ox00	0xFC
0x01	0x10
0x10	0x00
0x11	0x05
0x16	0xA0
0x17	0x80
0x18	0x80

For 625p hatch pattern on DAC D, the same register settings are used except Subaddress 0x10 = 0x18.

APPENDIX 5—SD TIMING MODES

[Subaddress 0x4A]

MODE 0 (CCIR-656)—SLAVE OPTION (TIMING REGISTER 0 TR0 = X X X X X 0 0 0)

The ADV7320/ADV7321 are controlled by the SAV (start active video) and EAV (end active video) time codes in the pixel data. All timing information is transmitted using a 4-byte synchronization pattern. A synchronization pattern is sent immediately before and after each line during active picture and retrace. If Pins $\overline{\text{S_VSYNC}}$, $\overline{\text{S_HSYNC}}$, and $\overline{\text{S_BLANK}}$ are not used, they should be tied high during this mode. Blank output is available.

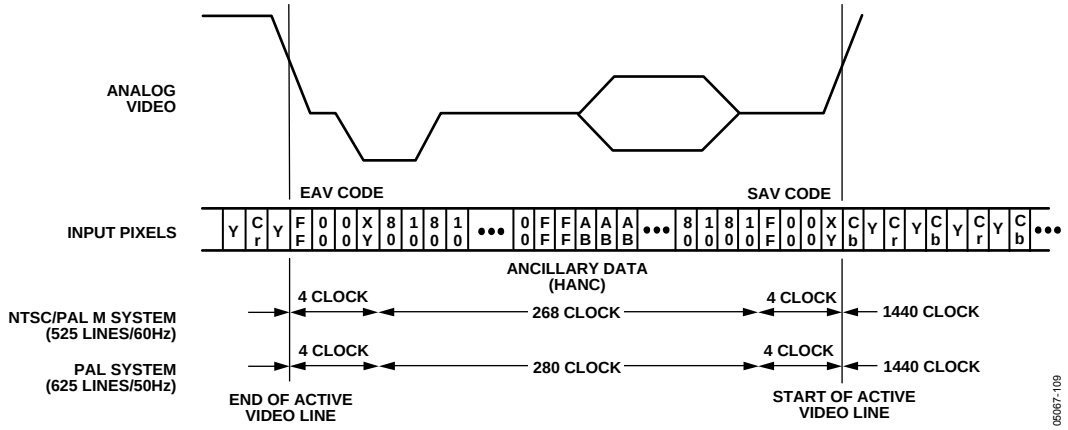


Figure 109. SD Slave Mode 0

MODE 0 (CCIR-656)—MASTER OPTION (TIMING REGISTER 0 TR0 = X X X X X 0 0 1)

The ADV7320/ADV7321 generate H, V, and F signals required for the SAV (start active video) and EAV (end active video) time codes in the CCIR656 standard. The H, V, and F bits are output on $\overline{\text{S_HSYNC}}$, $\overline{\text{S_BLANK}}$, and $\overline{\text{S_VSYNC}}$, respectively.

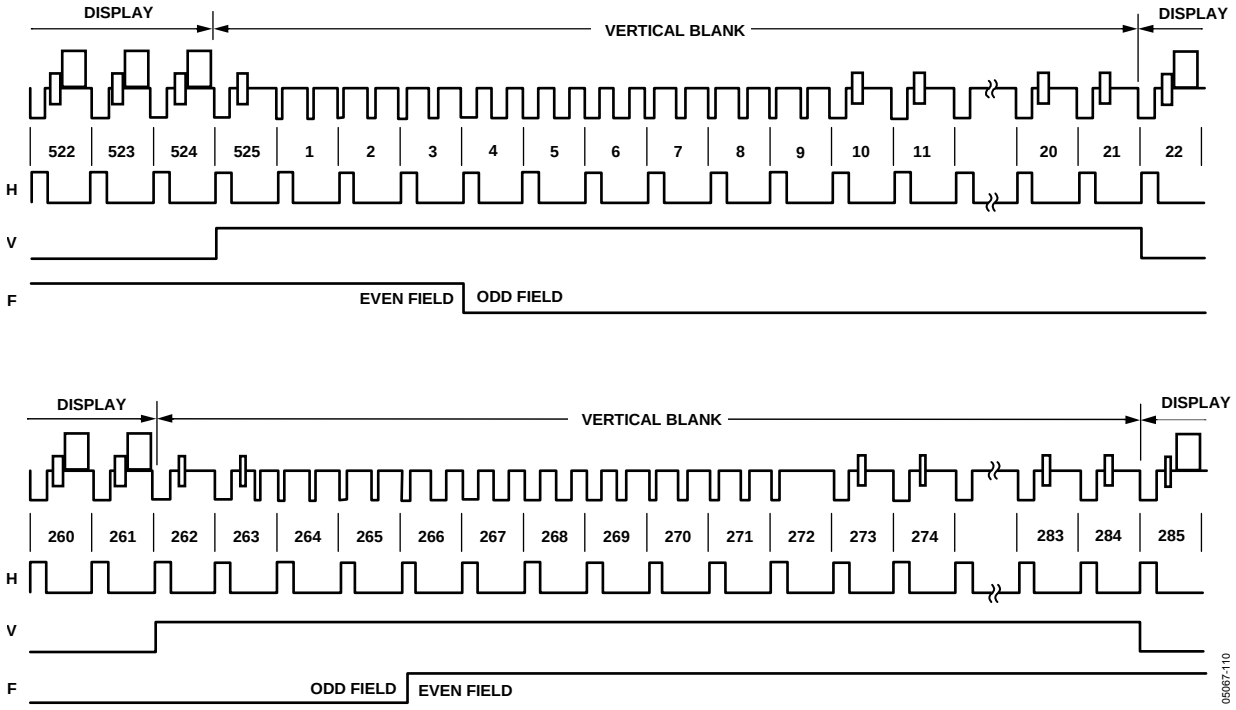


Figure 110. SD Master Mode 0 (NTSC)

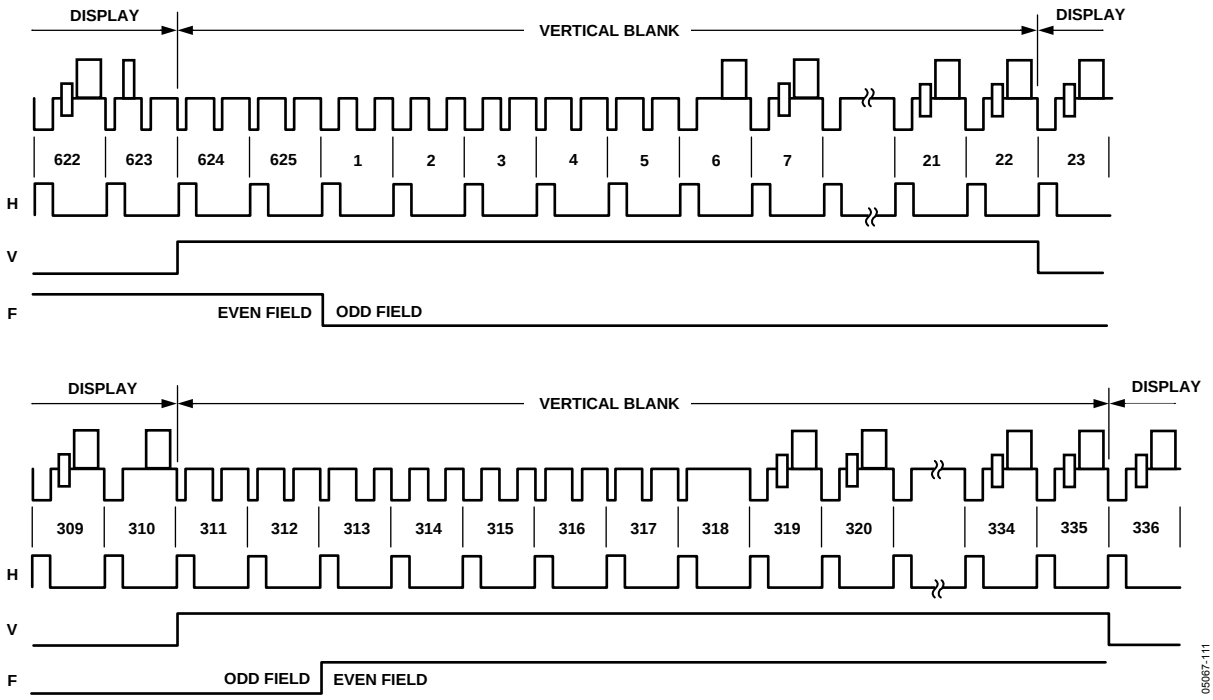


Figure 111. SD Master Mode 0 (PAL)

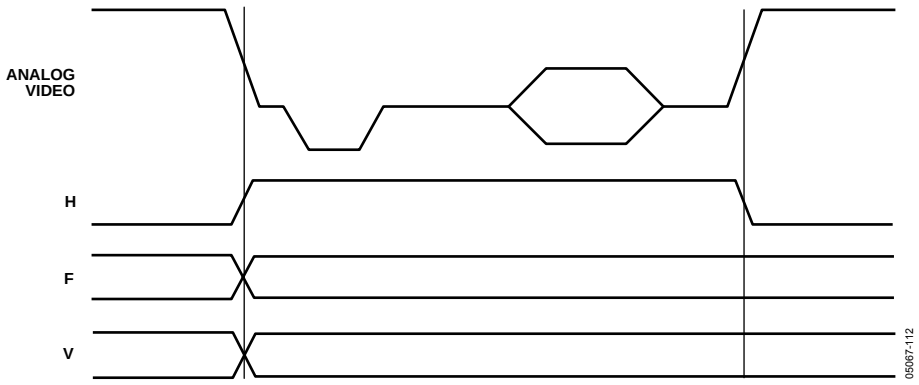


Figure 112. SD Master Mode 0 (Data Transitions)

MODE 1—SLAVE OPTION (TIMING REGISTER 0 TR0 = X X X X X 0 1 0)

In this mode, the ADV7320/ADV7321 accept horizontal sync and odd/even field signals. When $\overline{\text{HSYNC}}$ is low, a transition of the field input indicates a new frame, that is, vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, ADV7320/ADV7321 automatically blank all normally blank lines as per CCIR-624. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and FIELD are input on $\overline{\text{S_HSYNC}}$, $\overline{\text{S_BLANK}}$, and $\overline{\text{S_VSYNC}}$, respectively.

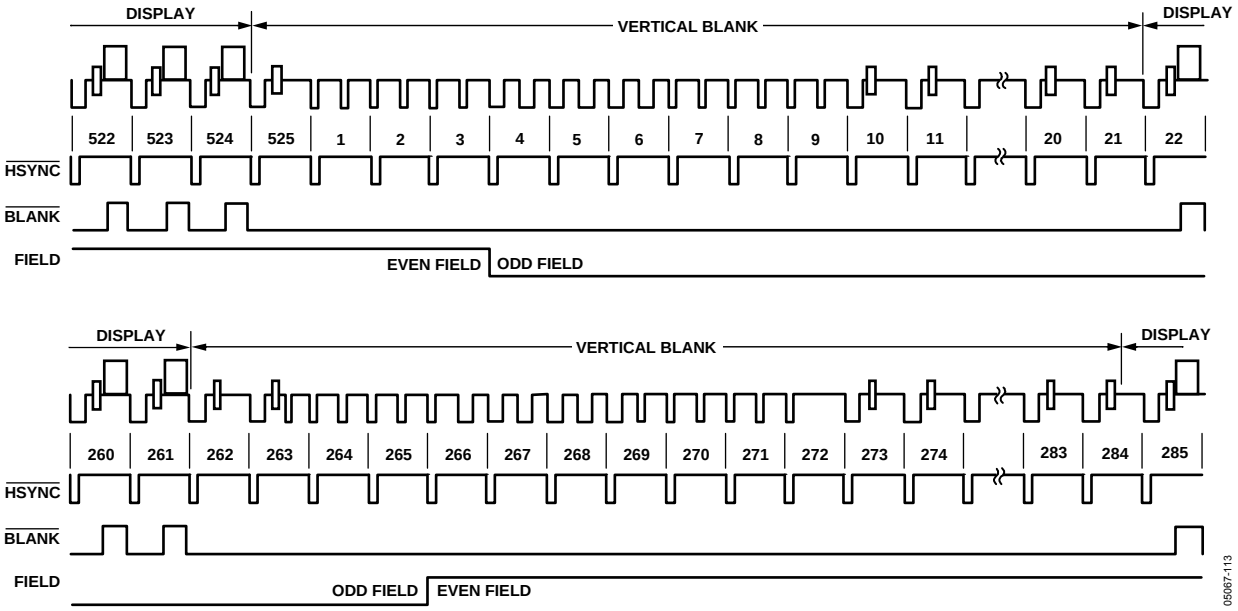


Figure 113. SD Slave Mode 1 (NTSC)

MODE 1—MASTER OPTION (TIMING REGISTER 0 TR0 = X X X X X 0 1 1)

In this mode, the ADV7320/ADV7321 can generate horizontal sync and odd/even field signals. When $\overline{\text{HSYNC}}$ is low, a transition of the field input indicates a new frame, that is, vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, ADV7320/ADV7321 automatically blank all normally blank lines as per CCIR-624. Pixel data is latched on the rising clock edge following the timing signal transitions. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and FIELD are output on $\overline{\text{S_HSYNC}}$, $\overline{\text{S_BLANK}}$, and $\overline{\text{S_VSYNC}}$, respectively.

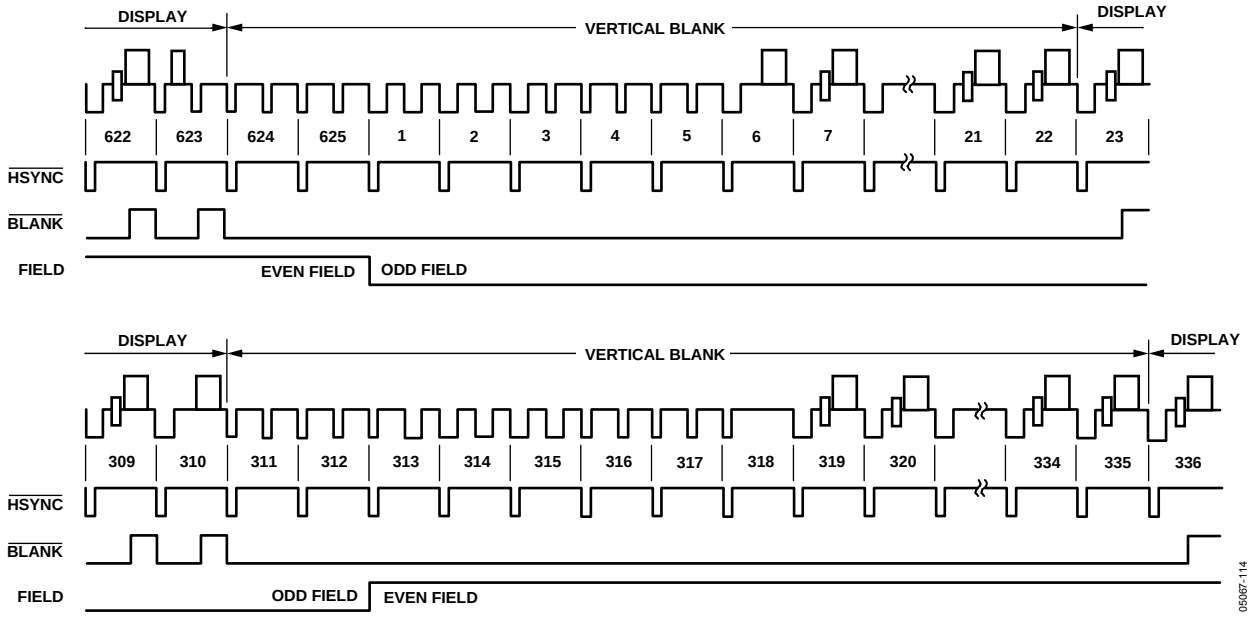


Figure 114. SD Slave Mode 1 (PAL)

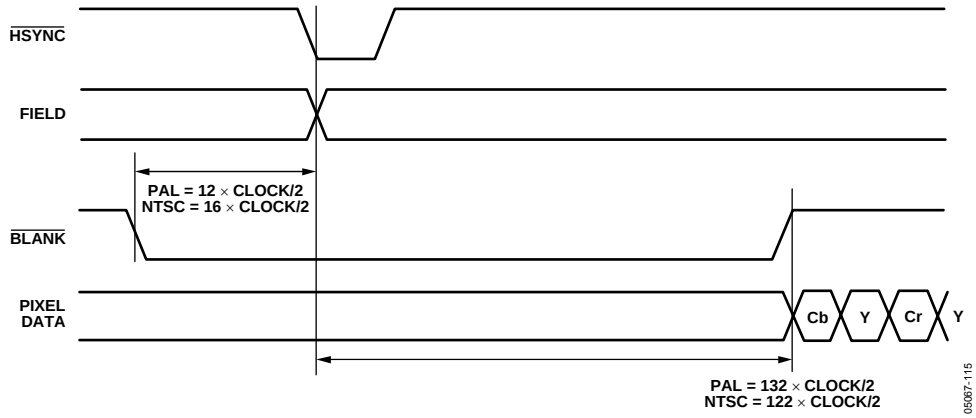


Figure 115. SD Timing Mode 1—Odd/Even Field Transitions Master/Slave

MODE 2— SLAVE OPTION (TIMING REGISTER 0 TR0 = X X X X X 1 0 0)

In this mode, the ADV7320/ADV7321 accept horizontal and vertical sync signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field. A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, ADV7320/ADV7321 automatically blank all normally blank lines as per CCIR-624. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{VSYNC}}$ are input on $\overline{\text{S_HSYNC}}$, $\overline{\text{S_BLANK}}$, and $\overline{\text{S_VSYNC}}$, respectively.

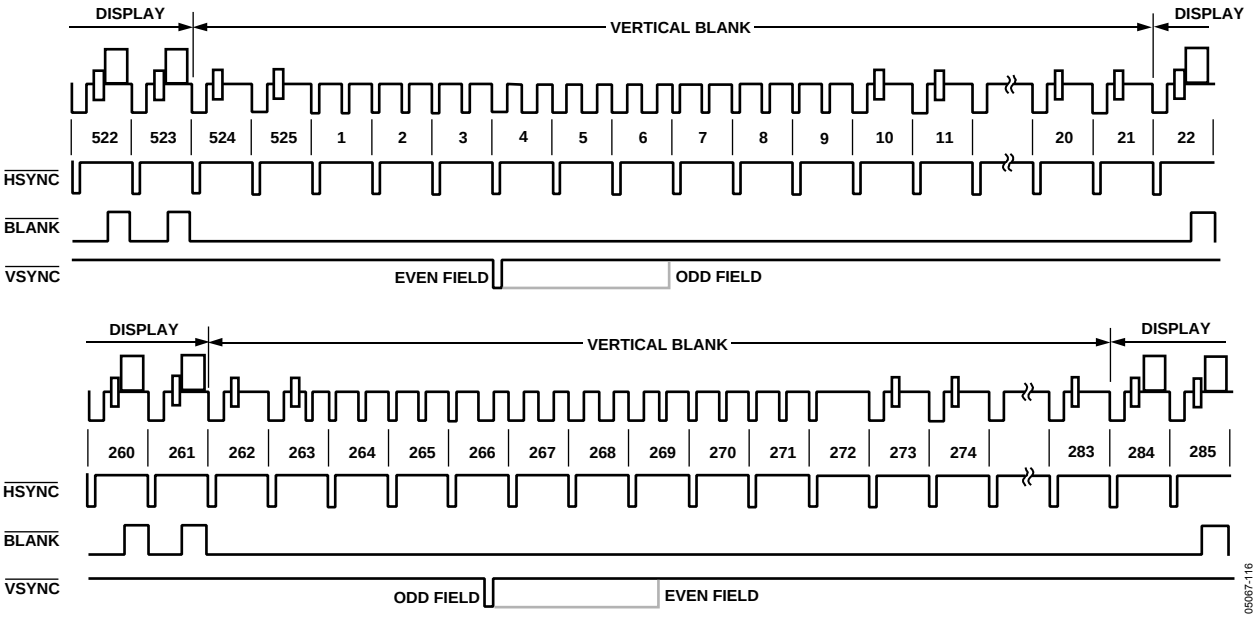


Figure 116. SD Slave Mode 2 (NTSC)

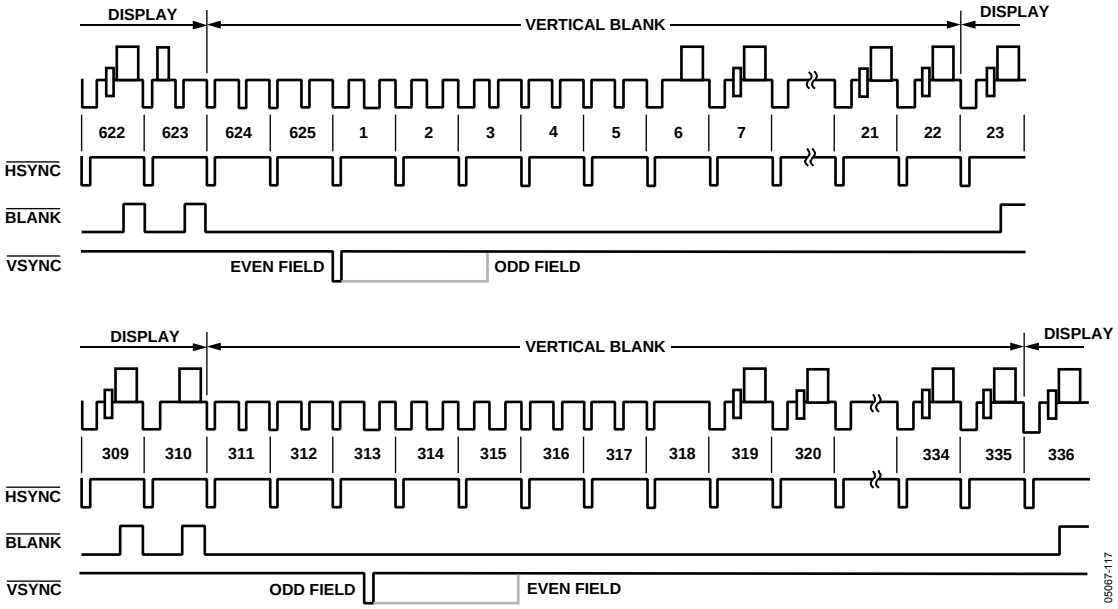


Figure 117. SD Slave Mode 2 (PAL)

MODE 2—MASTER OPTION (TIMING REGISTER 0 TR0 = X X X X X 1 0 1)

In this mode, the ADV7320/ADV7321 can generate horizontal and vertical sync signals. A coincident low transition of both $\overline{\text{HSYNC}}$ and $\overline{\text{VSYNC}}$ inputs indicates the start of an odd field.

A $\overline{\text{VSYNC}}$ low transition when $\overline{\text{HSYNC}}$ is high indicates the start of an even field. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, the ADV7320/ADV7321 automatically blank all normally blank lines as per CCIR-624. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{VSYNC}}$ are output on $\overline{\text{S_HSYNC}}$, $\overline{\text{S_BLANK}}$, and $\overline{\text{S_VSYNC}}$, respectively.

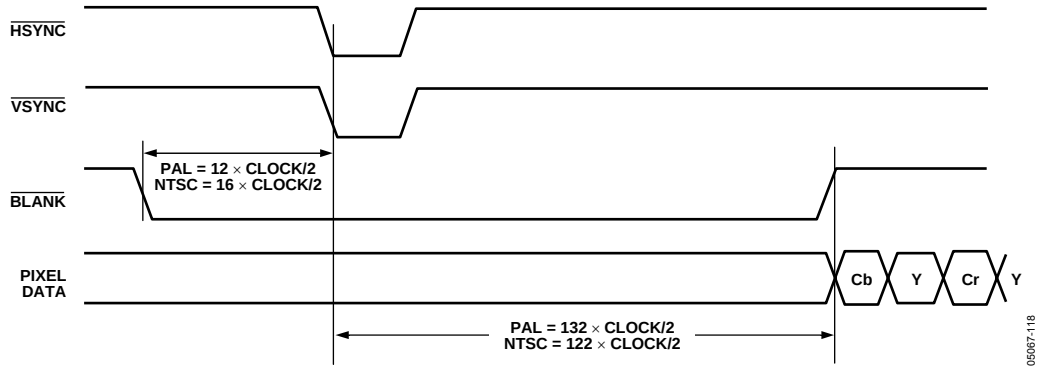


Figure 118. SD Timing Mode 2 Even-to-Odd Field Transition Master/Slave

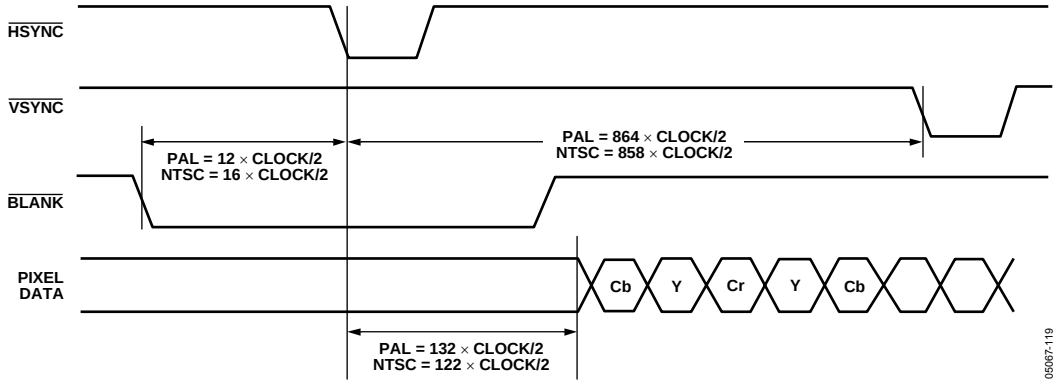


Figure 119. SD Timing Mode 2 Odd-to-Even Field Transition

MODE 3—MASTER/SLAVE OPTION (TIMING REGISTER 0 TR0 = X X X X X 1 1 0 OR X X X X X 1 1 1)

In this mode, the ADV7320/ADV7321 accept or generate horizontal sync and odd/even field signals. When $\overline{\text{HSYNC}}$ is high, a transition of the field input indicates a new frame, that is, vertical retrace. The $\overline{\text{BLANK}}$ signal is optional. When the $\overline{\text{BLANK}}$ input is disabled, ADV7320/ADV7321 automatically blank all normally blank lines as per CCIR-624. $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, and $\overline{\text{VSYNC}}$ are output in master mode and input in slave mode on $\overline{\text{S_VSYNC}}$, $\overline{\text{S_BLANK}}$, and $\overline{\text{S_VSYNC}}$, respectively.

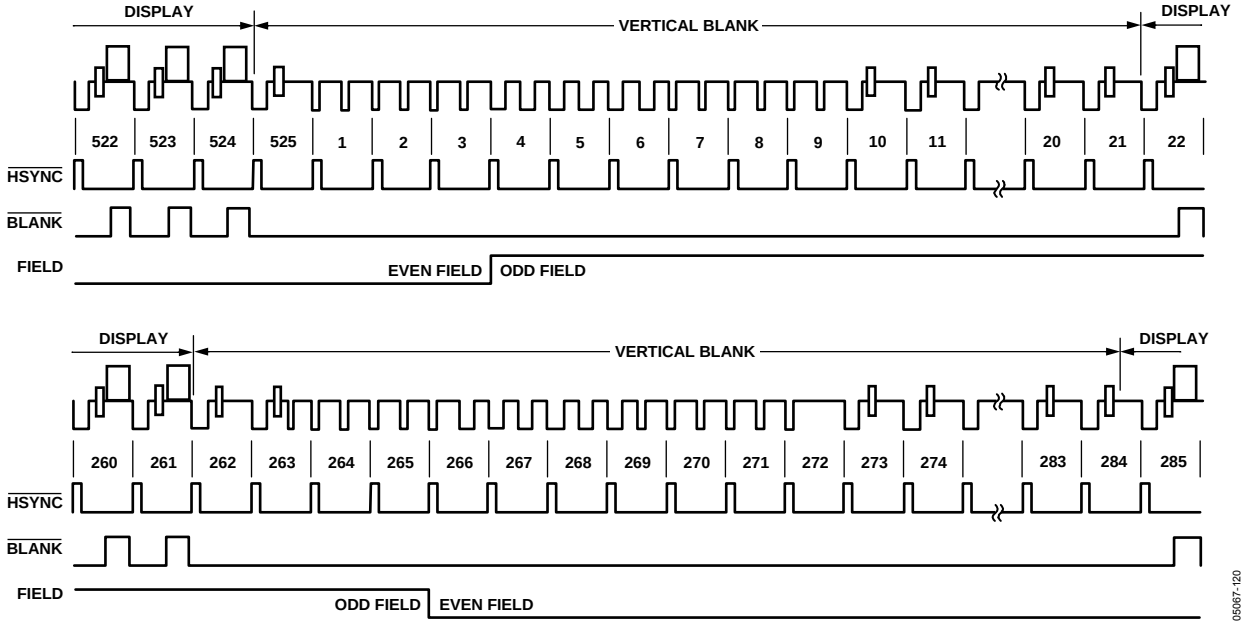


Figure 120. SD Timing Mode 3 (NTSC)

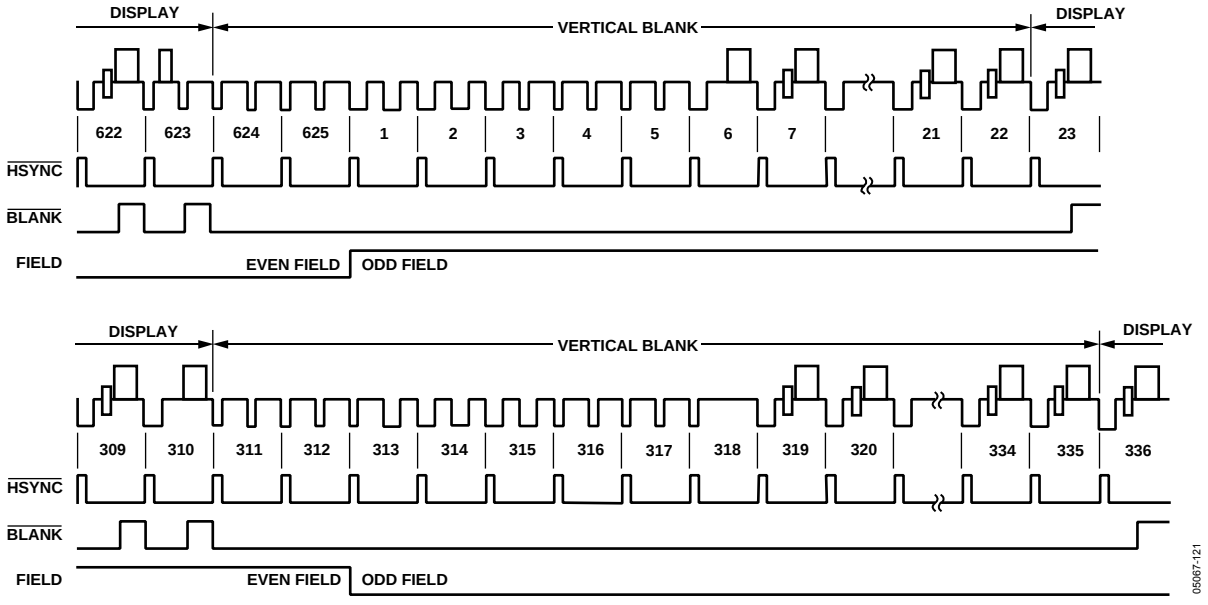


Figure 121. SD Timing Mode 3 (PAL)

APPENDIX 6—HD TIMING

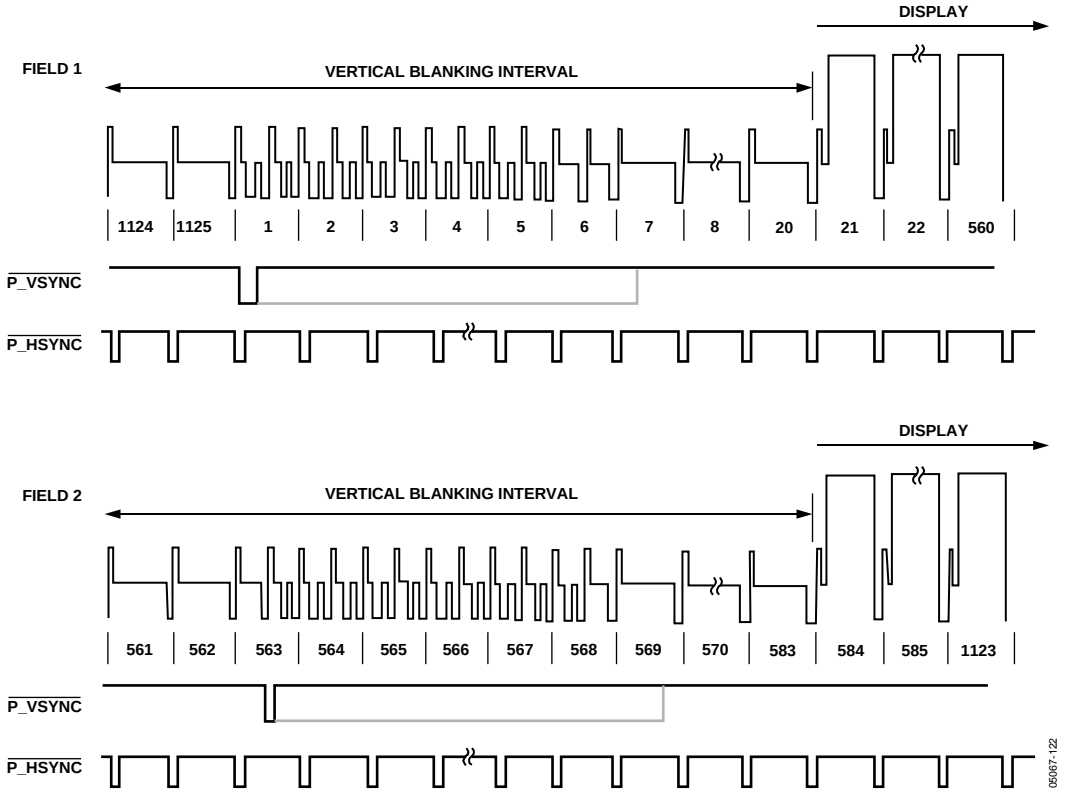


Figure 122. 1080i $\overline{HSYNC}$ and $\overline{VSYNC}$ Input Timing

APPENDIX 7—VIDEO OUTPUT LEVELS

HD YPrPb OUTPUT LEVELS

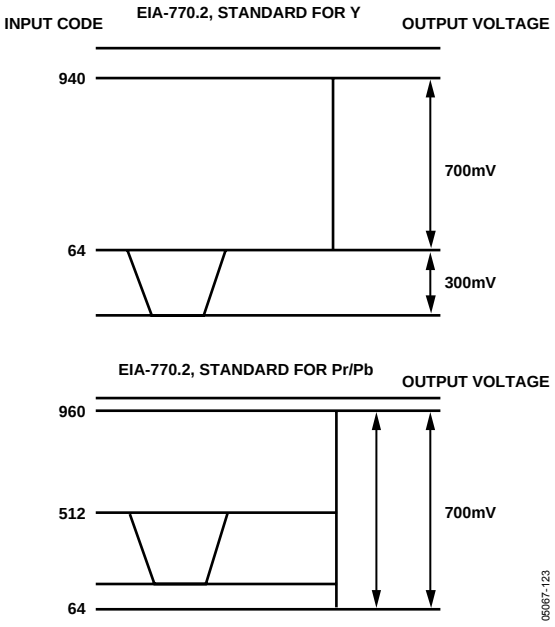


Figure 123. EIA 770.2 Standard Output Signals (525p/625p)

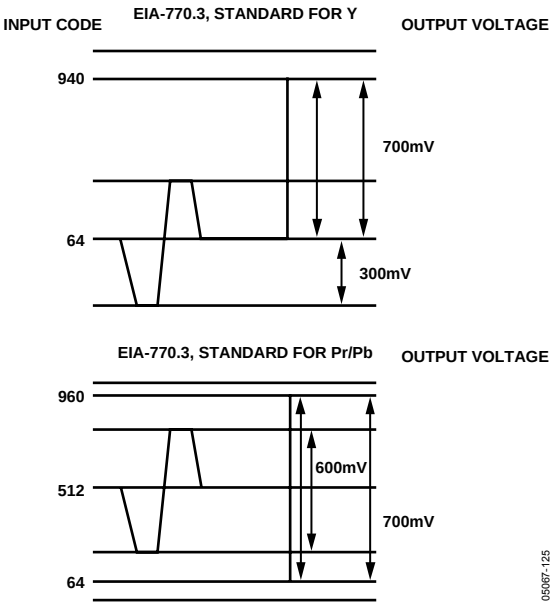


Figure 125. EIA 770.3 Standard Output Signals (1080i/720p)

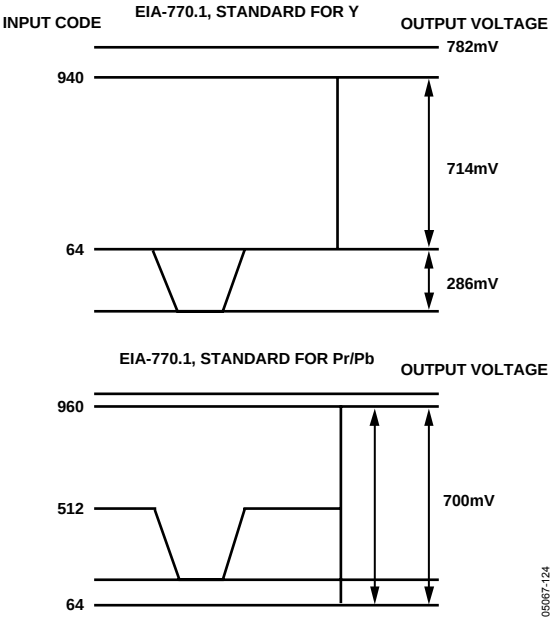


Figure 124. EIA 770.1 Standard Output Signals (525p/625p)

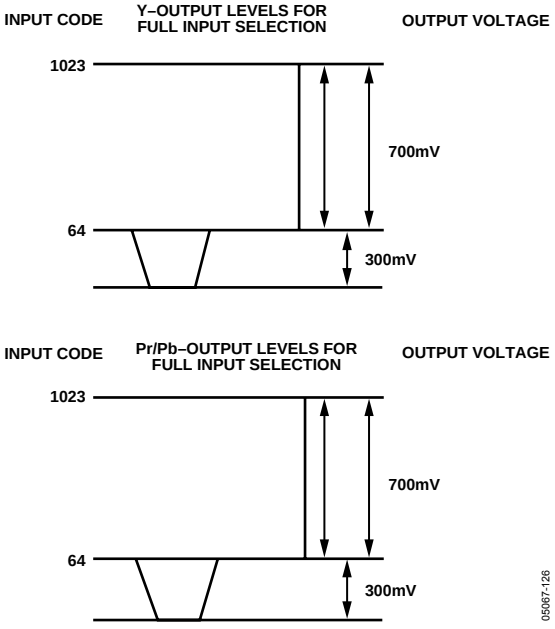


Figure 126. Output Levels for Full Input Selection

RGB OUTPUT LEVELS

Pattern: 100%/75% Color Bars

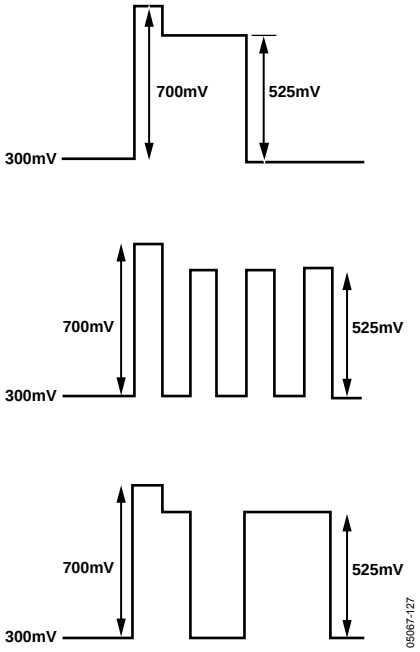


Figure 127. PS RGB Output Levels

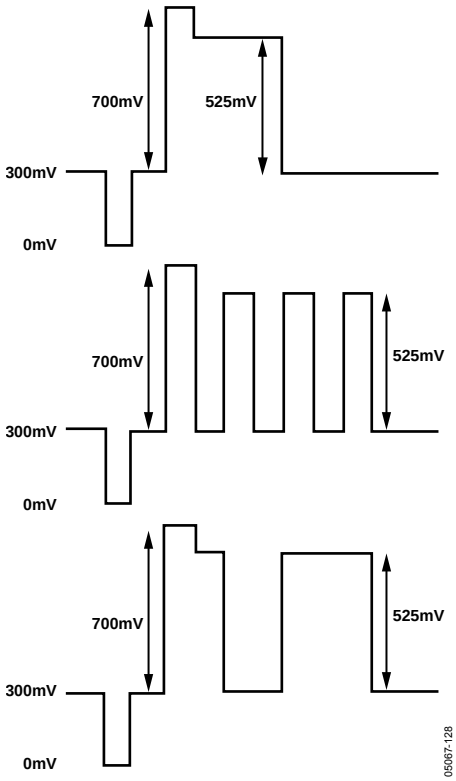


Figure 128. PS RGB Output Levels—RGB Sync Enabled

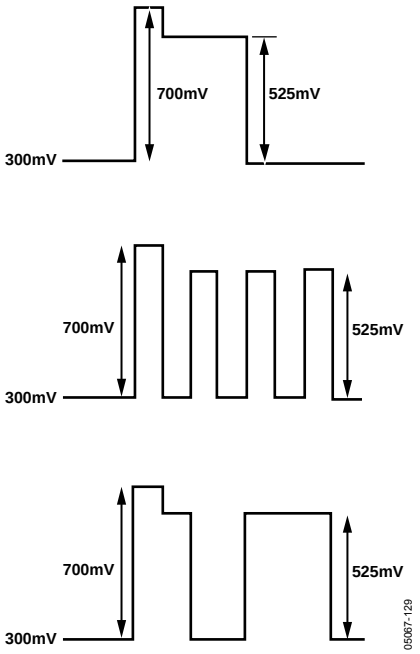


Figure 129. SD RGB Output Levels—RGB Sync Disabled

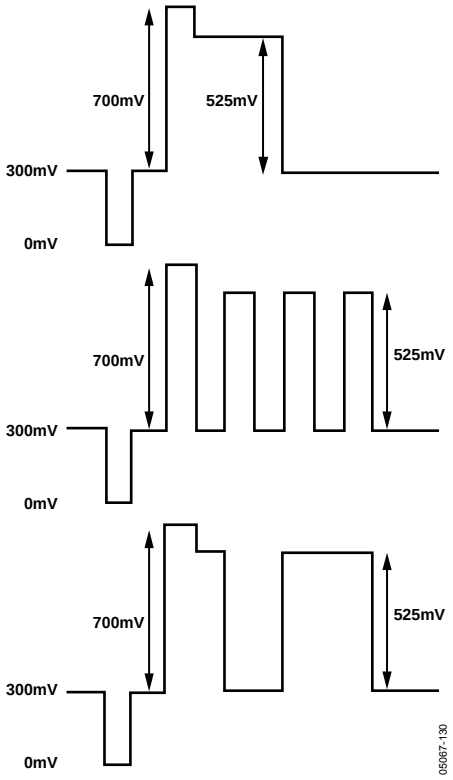


Figure 130. SD RGB Output Levels—RGB Sync Enabled

YPrPb LEVELS—SMPTE/EBU N10

Pattern: 100% Color Bars

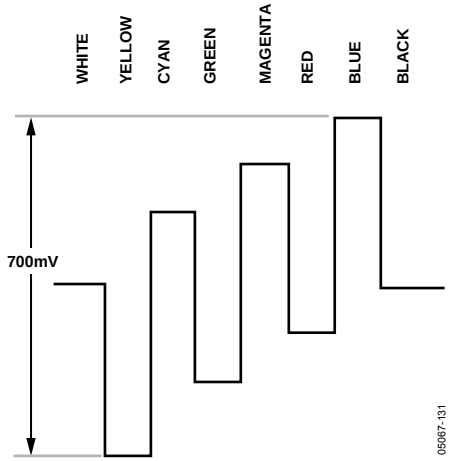


Figure 131. Pb Levels—NTSC

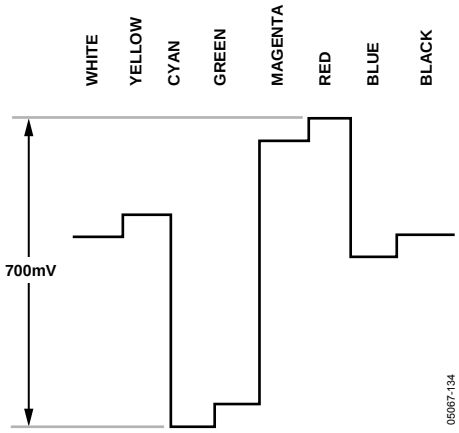


Figure 134. Pr Levels—PAL

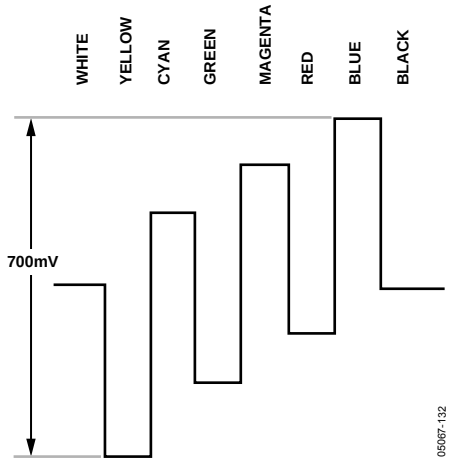


Figure 132. Pb Levels—PAL

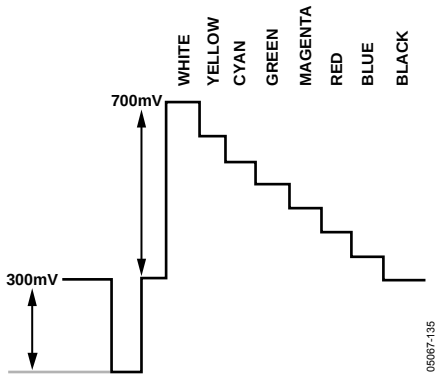


Figure 135. Y Levels—NTSC

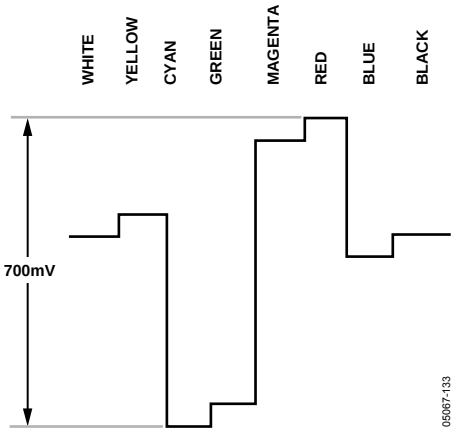


Figure 133. Pr Levels—NTSC

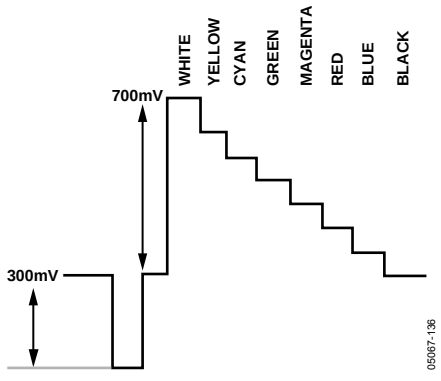


Figure 136. Y Levels—PAL

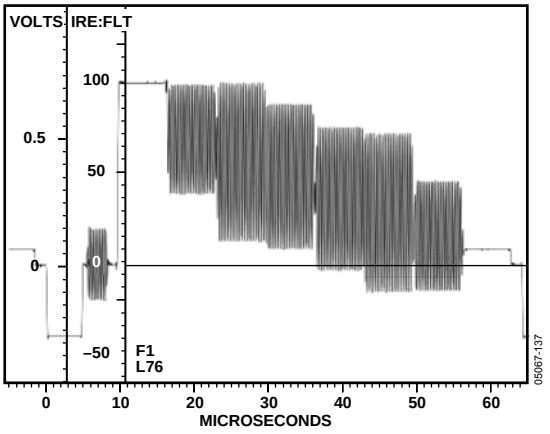


Figure 137. NTSC Color Bars 75%

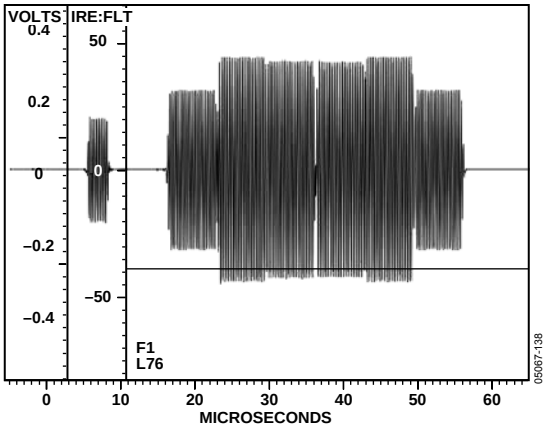


Figure 138. NTSC Chroma

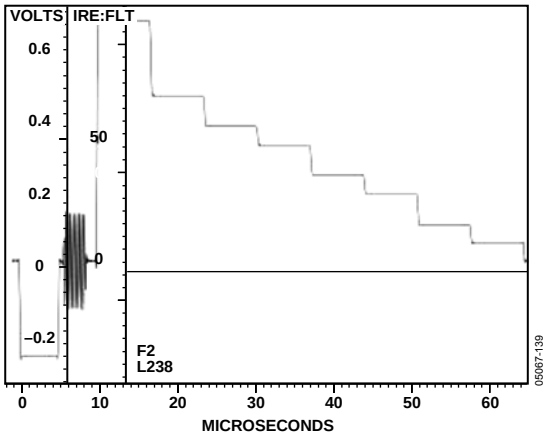


Figure 139. NTSC Luma

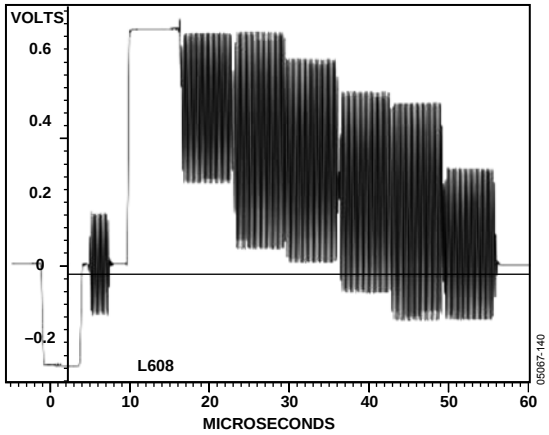


Figure 140. PAL Color Bars 75%

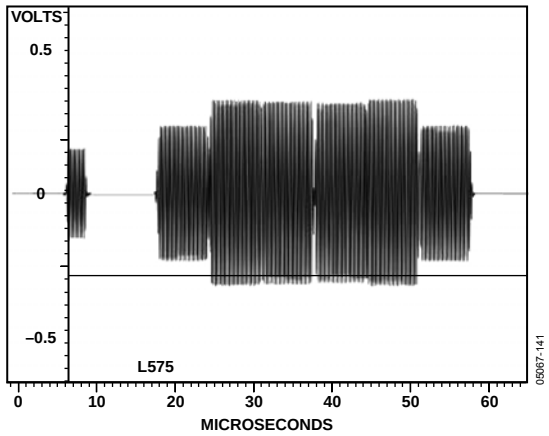


Figure 141. PAL Chroma

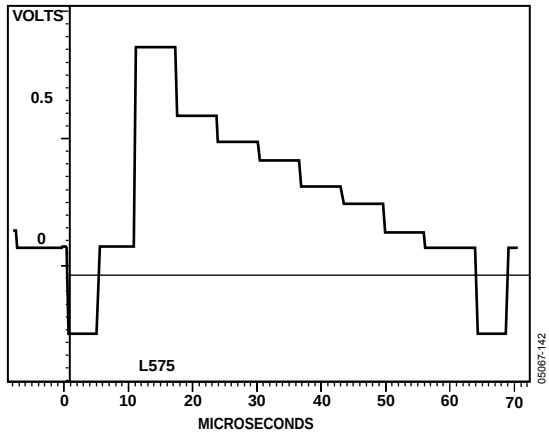


Figure 142. PAL Luma

APPENDIX 8—VIDEO STANDARDS

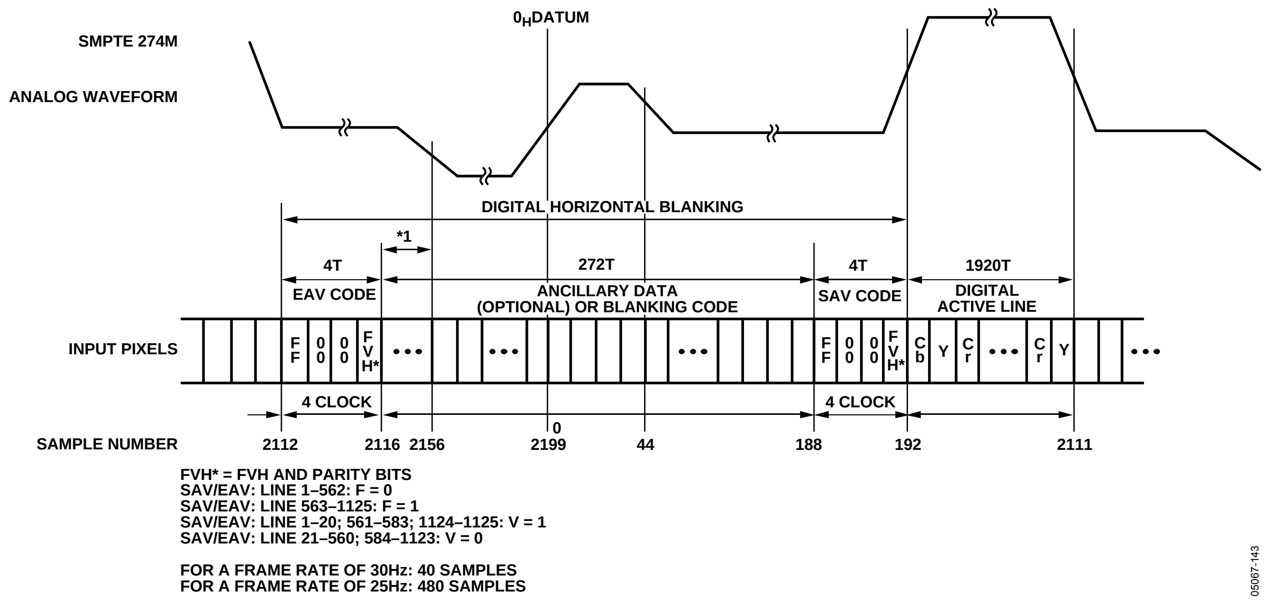


Figure 143. EAV/SAV Input Data Timing Diagram—SMPTE 274M

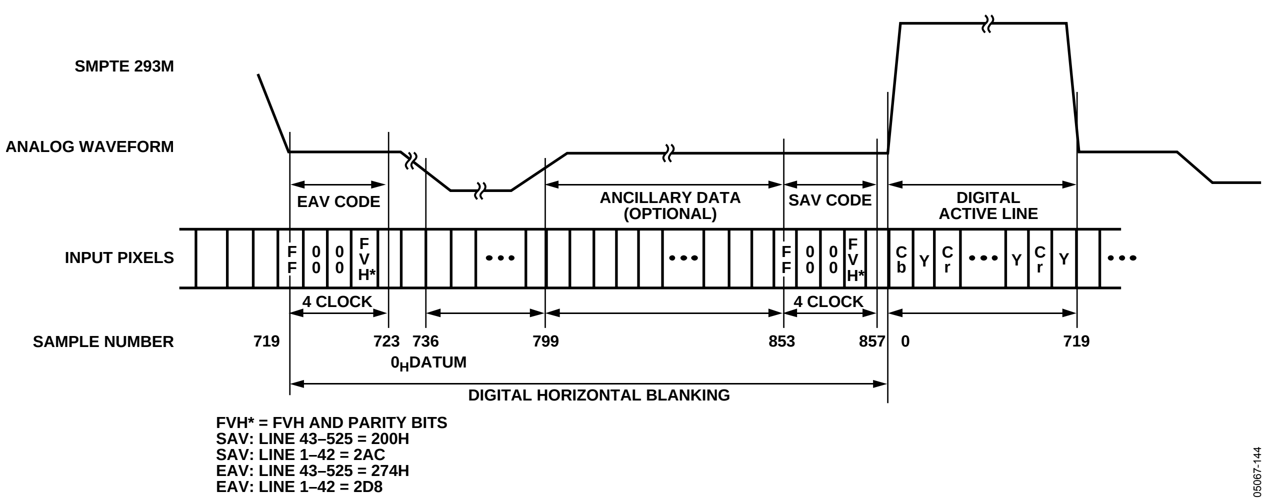


Figure 144. EAV/SAV Input Data Timing Diagram—SMPTE 293M

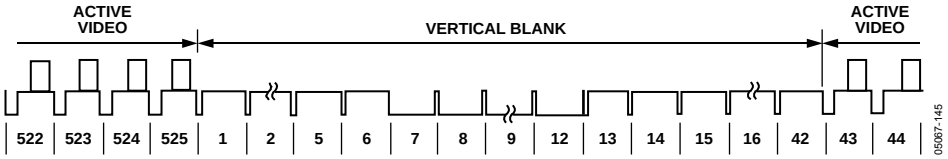


Figure 145. SMPTE 293M (525p)

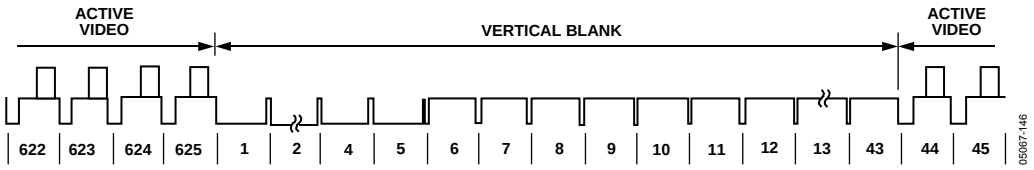


Figure 146. ITU-R BT.1358 (625p)

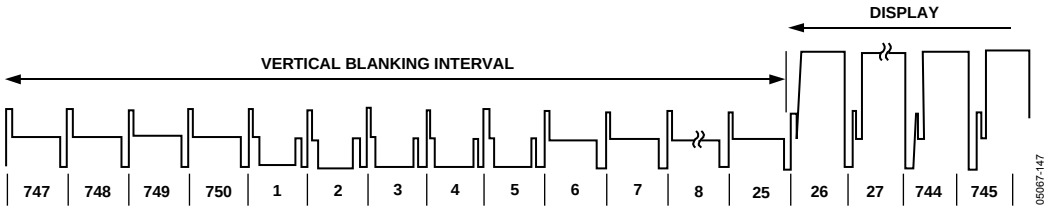


Figure 147. SMPTE 296M (720p)

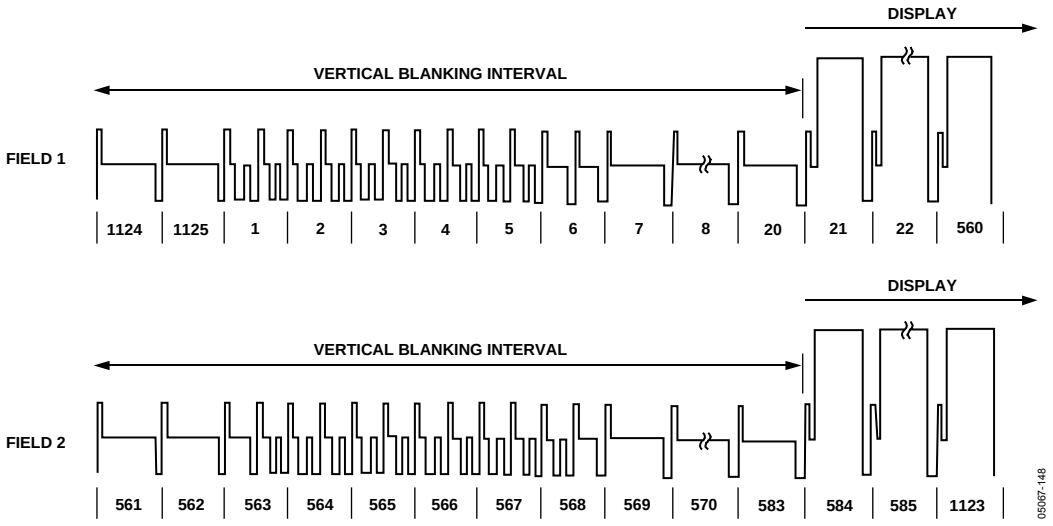


Figure 148. SMPTE 274M (1080i)

OUTLINE DIMENSIONS

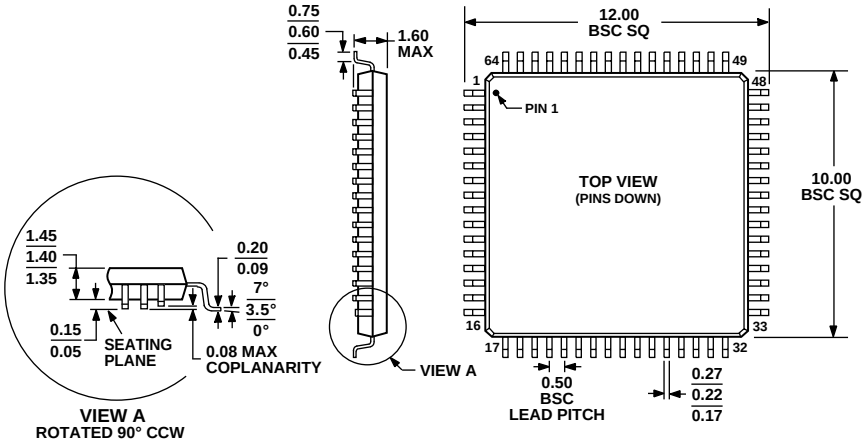


Figure 149. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADV7320KSTZ[1]	0°C to 70°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
ADV7321KSTZ[1]	0°C to 70°C	64-Lead Low Profile Quad Flat Package [LQFP]	ST-64-2
EVAL-ADV7320EB		Evaluation Board	
EVAL-ADV7321EB		Evaluation Board	

[1] Z = Pb-free part.

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