DS90CF384A/DS90CF364A +3.3V LVDS Receiver 24-Bit Flat Panel Display (FPD) Link - 65 MHz, +3.3V LVDS Receiver 18-Bit Flat Panel Display (FPD) Link - 65 MHz

Check for Samples: DS90CF364A, DS90CF384A

FEATURES

- **20 to 65 MHz Shift Clock Support**
- **50% Duty Cycle on Receiver Output Clock**
- **Best-in-Class Set & Hold Times on RxOUTPUTs**
- **Rx Power Consumption <142 mW (typ) @65MHz Grayscale**
- **Rx Power-down Mode <200µW (max)**
- **ESD Rating >7 kV (HBM), >700V (EIAJ)**
- **Supports VGA, SVGA, XGA and Dual Pixel SXGA.**
- **PLL Requires no External Components**
- **Compatible with TIA/EIA-644 LVDS Standard**
- **Low Profile 56-lead or 48-lead Packages**

DESCRIPTION

The DS90CF384A receiver converts the four LVDS data streams (Up to 1.8 Gbps throughput or 227 Megabytes/sec bandwidth) back into parallel 28 bits of CMOS/TTL data (24 bits of RGB and 4 bits of Hsync, Vsync, DE and CNTL). Also available is the DS90CF364A that converts the three LVDS data streams (Up to 1.3 Gbps throughput or 170 Megabytes/sec bandwidth) back into parallel 21 bits of CMOS/TTL data (18 bits of RGB and 3 bits of Hsync, Vsync and DE). Both Receivers' outputs are Falling edge strobe. A Rising edge or Falling edge strobe transmitter (DS90C383A/DS90C363A) will interoperate with a Falling edge strobe Receiver without any translation logic.

The DS90CF384A / DS90CF364A devices are enhanced over prior generation receivers and provided a wider data valid time on the receiver output.

This chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

BLOCK DIAGRAMS

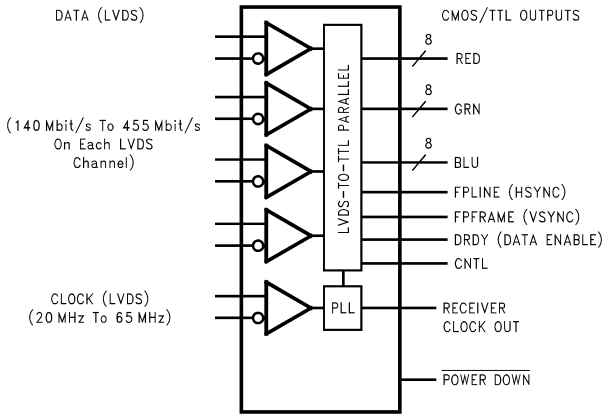


Figure 1. DS90CF384A DGG-56 (TSSOP)

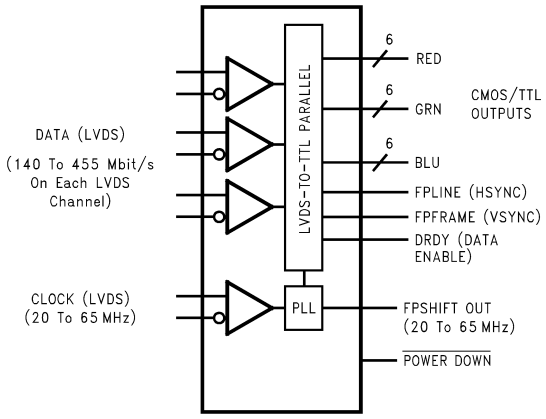


Figure 2. DS90CF364A DGG-48 (TSSOP)

Absolute Maximum Ratings(1)(2)

Supply Voltage (V_{CC})		−0.3V to +4V
CMOS/TTL Input Voltage		−0.3V to (V_{CC} + 0.3V)
CMOS/TTL Output Voltage		−0.3V to (V_{CC} + 0.3V)
LVDS Receiver Input Voltage		−0.3V to (V_{CC} + 0.3V)
Junction Temperature		+150°C
Storage Temperature		−65°C to +150°C
Lead Temperature (Soldering, 4 sec)		+260°C
Solder Reflow Temperature (20 sec for FBGA)		+220°C
Maximum Package Power Dissipation Capacity @ 25°C	DGG-56 (TSSOP) Package DS90CF384A	1.61 W
	DGG-48 (TSSOP) Package DS90CF364A	1.89 W
Package Derating	DS90CF384AMTD	12.4 mW/°C above +25°C
	DS90CF364AMTD	15 mW/°C above +25°C
ESD Rating	(HBM, 1.5 kΩ, 100 pF)	> 7 kV
	(EIAJ, 0Ω, 200 pF)	> 700V

(1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

Recommended OperatingConditions

	Min	Nom	Max	Units
Supply Voltage (V_{CC})	3.0	3.3	3.6	V
Operating Free Air Temperature (T_A)	−10	+25	+70	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage (V_{CC})			100	mV_{PP}

Electrical Characteristics(1)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS/TTL DC SPECIFICATIONS (For Power Down Pin)						
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA		−0.79	−1.5	V
I_{IN}	Input Current	V_{IN} = 0.4V, 2.5V or V_{CC}		+1.8	+10	µA
		V_{IN} = GND	−10	0		µA
CMOS/TTL DC SPECIFICATIONS						
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 mA	2.7	3.3		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.06	0.3	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0V		−60	−120	mA

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25C.

Electrical Characteristics[1] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
LVDS RECEIVER DC SPECIFICATIONS							
V_{TH}	Differential Input High Threshold	V_{CM} = +1.2V				+100	mV
V_{TL}	Differential Input Low Threshold			−100			mV
I_{IN}	Input Current	V_{IN} = +2.4V, V_{CC} = 3.6V				±10	µA
		V_{IN} = 0V, V_{CC} = 3.6V				±10	µA
RECEIVER SUPPLY CURRENT[2]							
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CF384A (Figure 3 Figure 6)	f = 32.5 MHz		49	65	mA
			f = 37.5 MHz		53	70	mA
			f = 65 MHz		81	105	mA
ICCRW	Receiver Supply Current Worst Case	C_L = 8 pF, Worst Case Pattern, DS90CF364A (Figure 3 Figure 6)	f = 32.5 MHz		49	55	mA
			f = 37.5 MHz		53	60	mA
			f = 65 MHz		78	90	mA
ICCRG	Receiver Supply Current, 16 Grayscale	C_L = 8 pF, 16 Grayscale Pattern, (Figure 4 Figure 5 Figure 6)	f = 32.5 MHz		28	45	mA
			f = 37.5 MHz		30	47	mA
			f = 65 MHz		43	60	mA
ICCRZ	Receiver Supply Current Power Down	$\overline{\text{Power Down}}$ = Low Receiver Outputs Stay Low during Power Down Mode			10	55	µA

(2) Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Receiver Switching Characteristics[1]

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
CLHT	CMOS/TTL Low-to-High Transition Time (Figure 6)			2	5	ns
CHLT	CMOS/TTL High-to-Low Transition Time (Figure 6)			1.8	5	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 13, Figure 14)	f = 25 MHz	1.20	1.96	2.82	ns
RSPos1	Receiver Input Strobe Position for Bit 1		6.91	7.67	8.53	ns
RSPos2	Receiver Input Strobe Position for Bit 2		12.62	13.38	14.24	ns
RSPos3	Receiver Input Strobe Position for Bit 3		18.33	19.09	19.95	ns
RSPos4	Receiver Input Strobe Position for Bit 4		24.04	24.80	25.66	ns
RSPos5	Receiver Input Strobe Position for Bit 5		29.75	30.51	31.37	ns
RSPos6	Receiver Input Strobe Position for Bit 6		35.46	36.22	37.08	ns
RSPos0	Receiver Input Strobe Position for Bit 0 (Figure 13, Figure 14)	f = 65 MHz	0.7	1.1	1.4	ns
RSPos1	Receiver Input Strobe Position for Bit 1		2.9	3.3	3.6	ns
RSPos2	Receiver Input Strobe Position for Bit 2		5.1	5.5	5.8	ns
RSPos3	Receiver Input Strobe Position for Bit 3		7.3	7.7	8.0	ns
RSPos4	Receiver Input Strobe Position for Bit 4		9.5	9.9	10.2	ns
RSPos5	Receiver Input Strobe Position for Bit 5		11.7	12.1	12.4	ns
RSPos6	Receiver Input Strobe Position for Bit 6		13.9	14.3	14.6	ns
RSKM	RxIN Skew Margin [2] (Figure 15)	f = 25 MHz	750			ps
		f = 65 MHz	500			ps

(1) Typical values are given for V_{CC} = 3.3V and T_A = +25C.
(2) Receiver Skew Margin is defined as the valid data sampling region at the receiver inputs. This margin takes into account the DS90C383B transmitter pulse positions (min and max) and the receiver input setup and hold time (internal data sampling window - RSPos). The RSKM will change when different transmitters are used. This margin allows for LVDS interconnect skew, inter-symbol interference (both dependent on type/length of cable), and clock jitter (less than 250 ps).

Receiver Switching Characteristics[1] (continued)

Over recommended operating supply and temperature ranges unless otherwise specified

Symbol	Parameter		Min	Typ	Max	Units
RCOP	RxCLK OUT Period (Figure 7)		15	T	50	ns
RCOH	RxCLK OUT High Time (Figure 7)	f = 65 MHz	5.0	7.6	9.0	ns
RCOL	RxCLK OUT Low Time (Figure 7)		5.0	6.3	9.0	ns
RSRC	RxOUT Setup to RxCLK OUT (Figure 7)		4.5	7.3		ns
RHRC	RxOUT Hold to RxCLK OUT (Figure 7)		4.0	6.3		ns
RCCD	RxCLK IN to RxCLK OUT Delay @ 25°C, V_{CC} = 3.3V (Figure 8)		3.5	5.0	7.5	ns
RPLLS	Receiver Phase Lock Loop Set (Figure 9)				10	ms
RPDD	Receiver Power Down Delay (Figure 12)				1	µs

AC Timing Diagrams

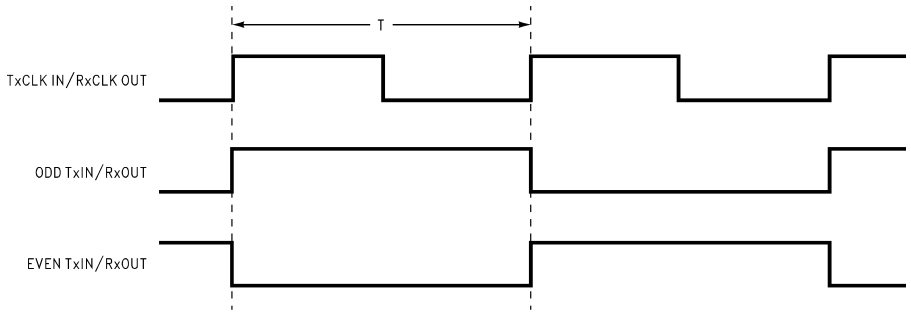
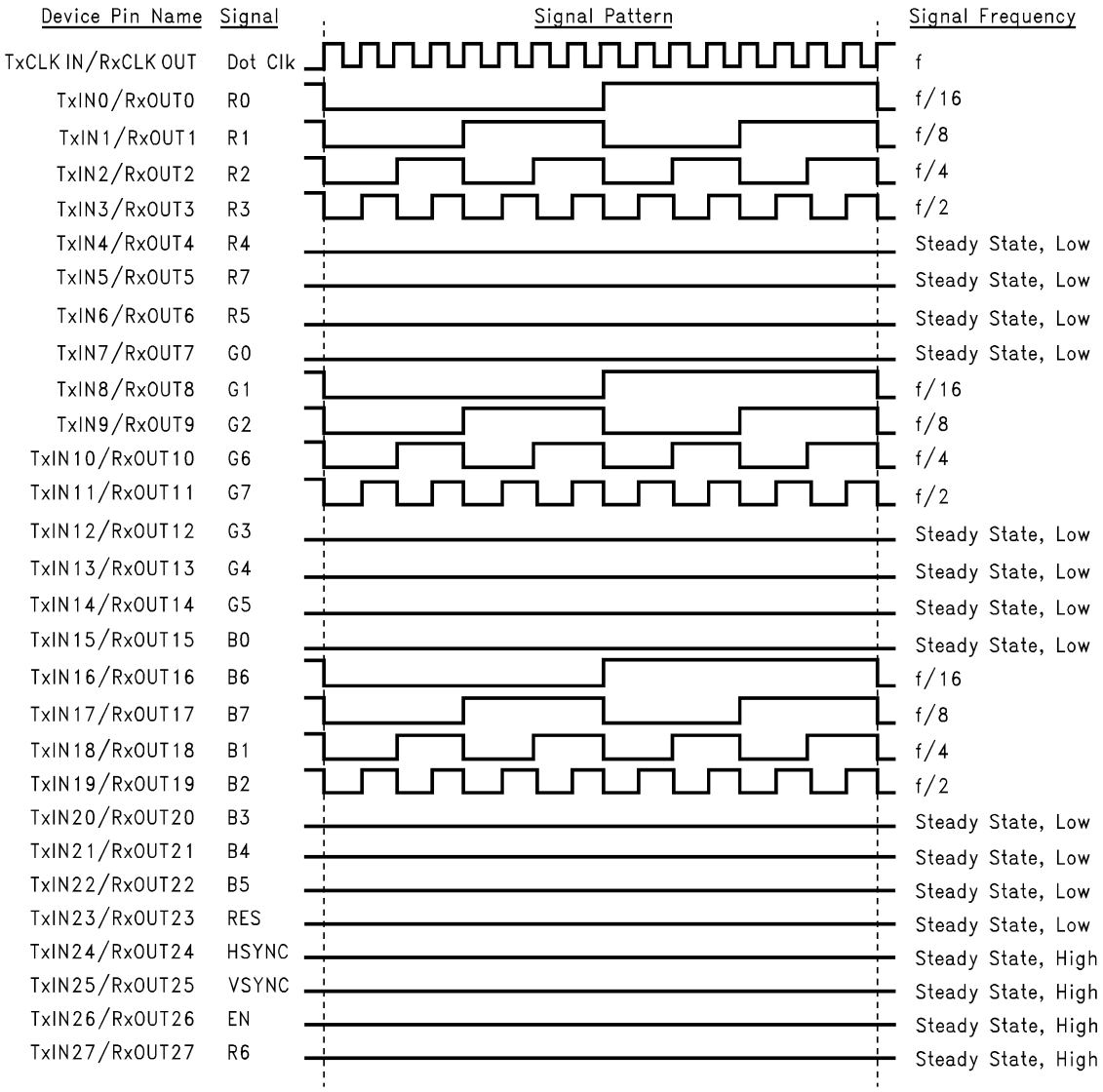


Figure 3. "Worst Case" Test Pattern



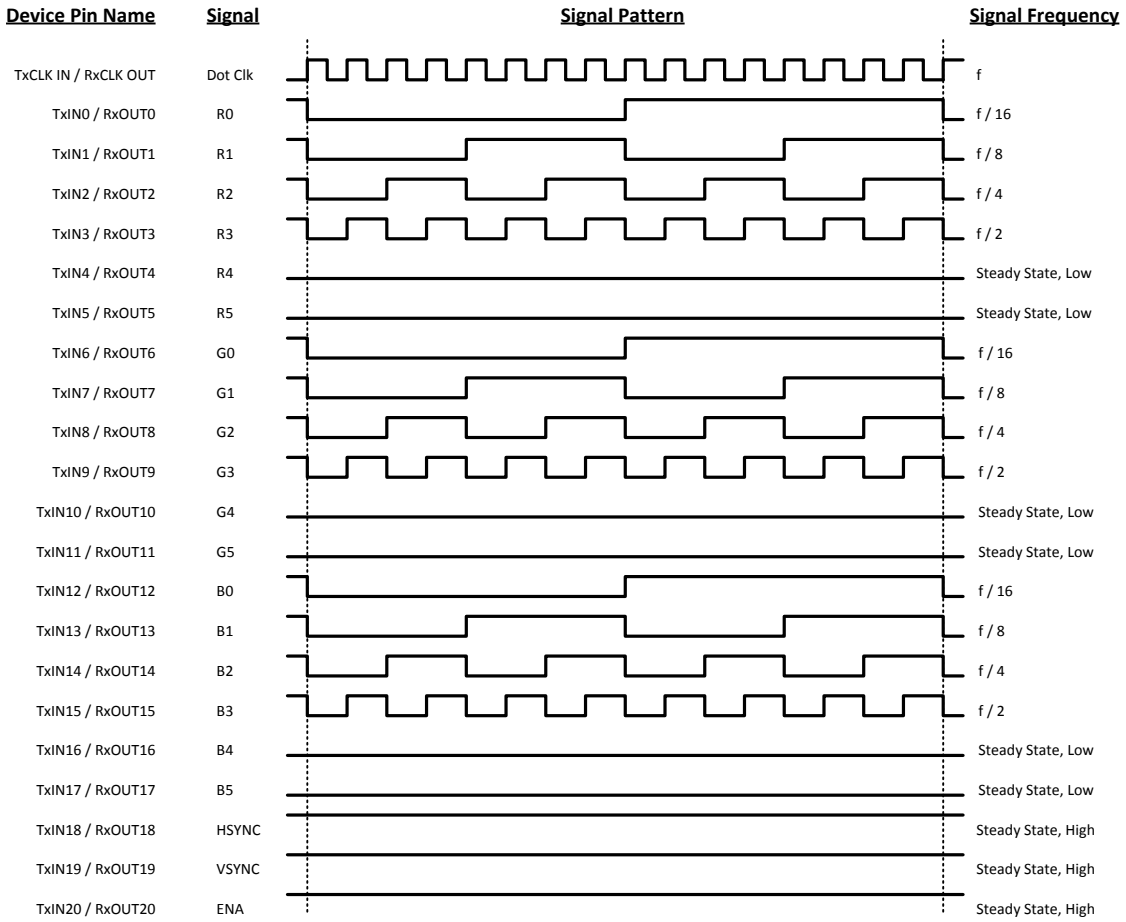
(1) The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

(2) The 16 grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

(3) Figure 3 and Figure 5 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

(4) Recommended pin to signal mapping. Customer may choose to define differently.

Figure 4. “16 Grayscale” Test Pattern (DS90CF384A)



(1) The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

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(3) Figure 3 and Figure 5 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

(4) Recommended pin to signal mapping. Customer may choose to define differently.

Figure 5. “16 Grayscale” Test Pattern (DS90CF364A)

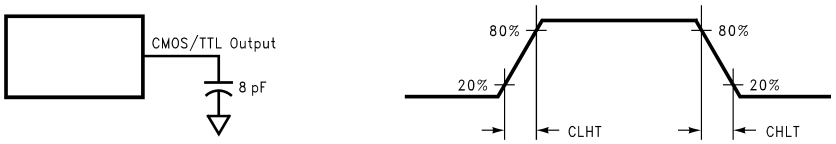


Figure 6. DS90CF384A/DS90CF364A (Receiver) CMOS/TTL Output Load and Transition Times

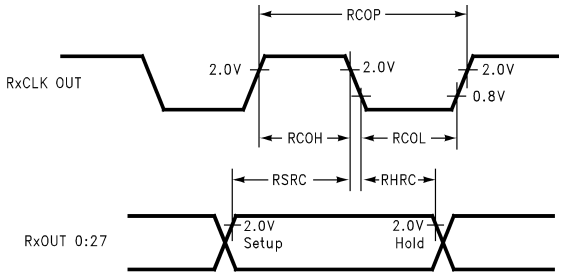


Figure 7. DS90CF384A/DS90CF364A (Receiver) Setup/Hold and High/Low Times

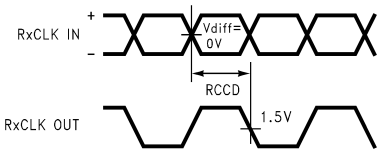


Figure 8. DS90CF384A/DS90CF364A (Receiver) Clock In to Clock Out Delay

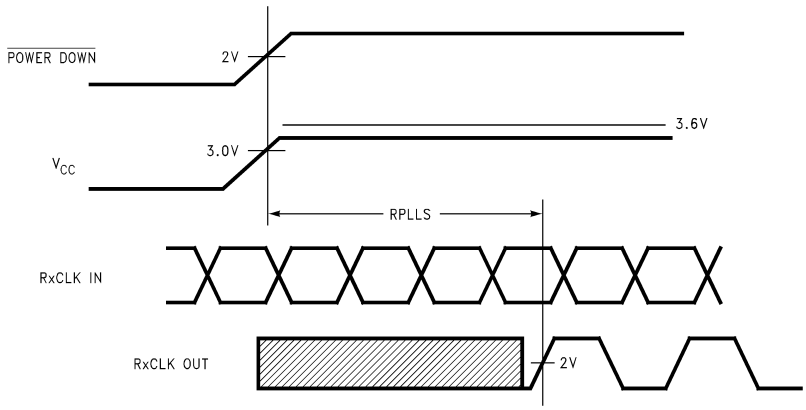


Figure 9. DS90CF384A/DS90CF364A (Receiver) Phase Lock Loop Set Time

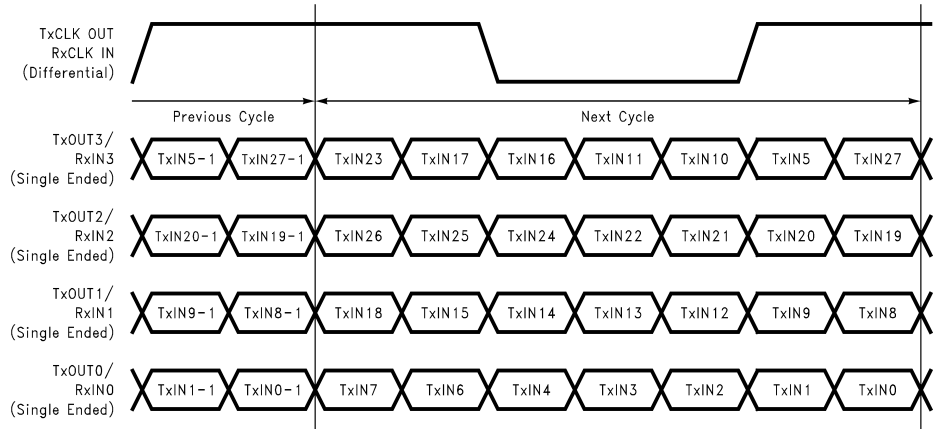


Figure 10. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90CF384A

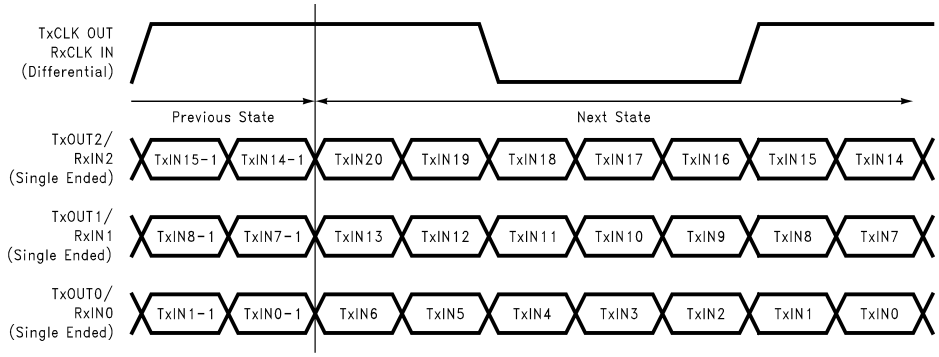


Figure 11. 21 Parallel TTL Data Inputs Mapped to LVDS Outputs - DS90CF364A

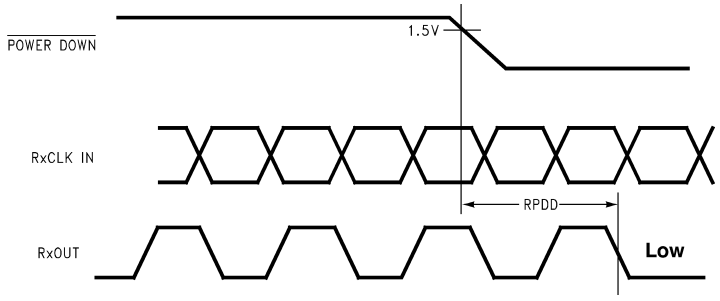


Figure 12. DS90CF384A/DS90CF364A (Receiver) Power Down Delay

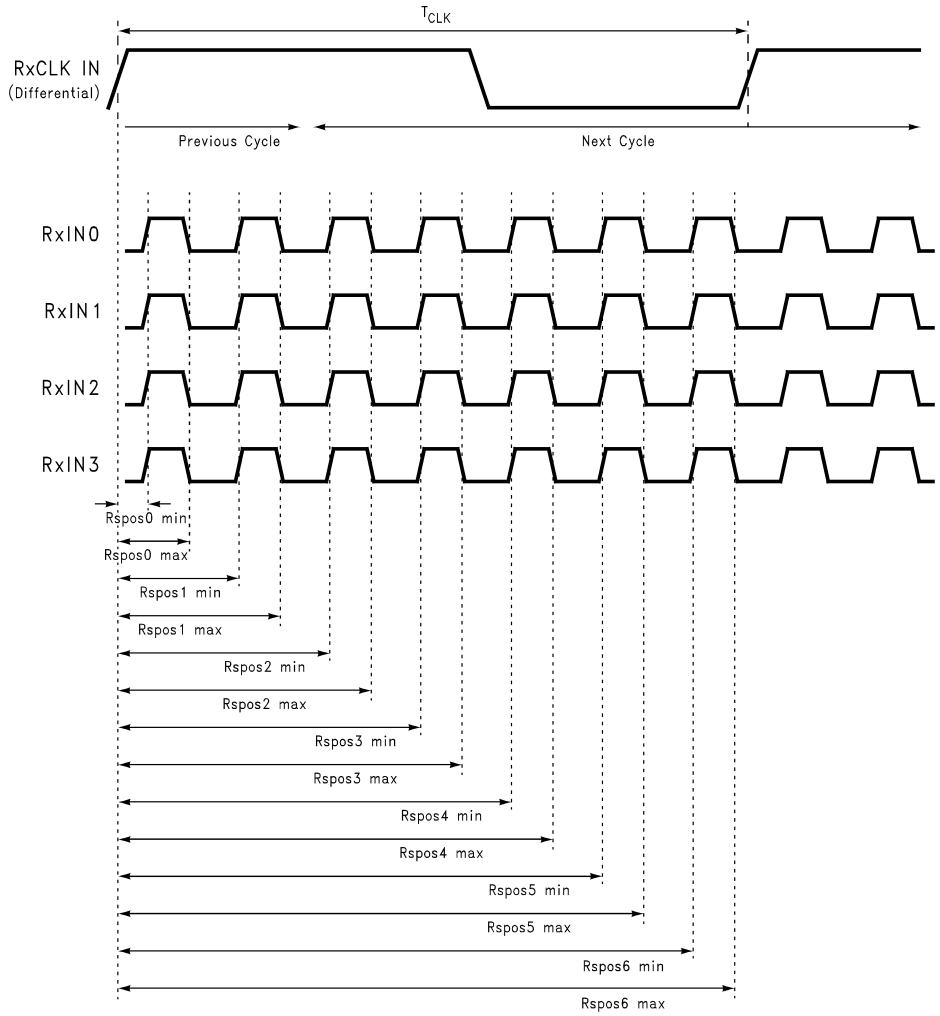


Figure 13. DS90CF384A (Receiver) LVDS Input Strobe Position

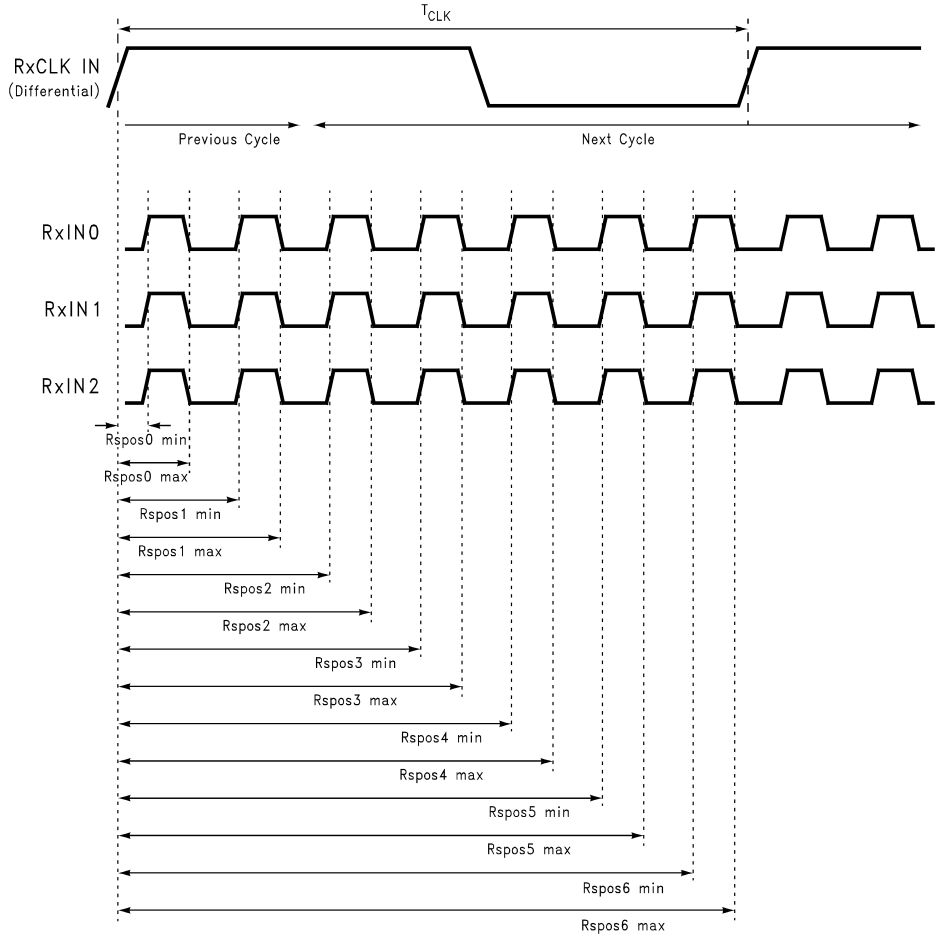
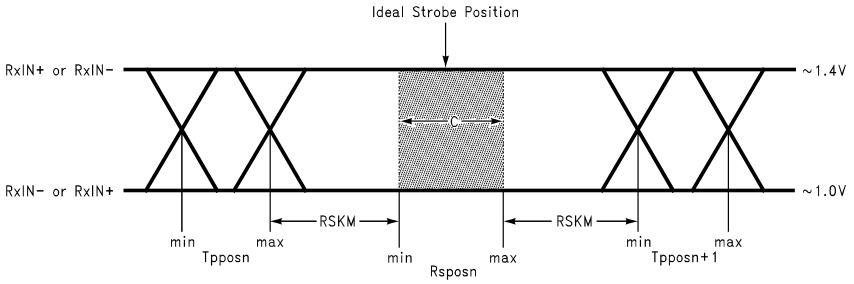


Figure 14. DS90CF364A (Receiver) LVDS Input Strobe Position



C—Setup and Hold Time (Internal data sampling window) defined by Rspos (receiver input strobe position) min and max

Tppos—Transmitter output pulse position (min and max)

RSKM = Cable Skew (type, length) + Source Clock Jitter (cycle to cycle)(1) + ISI (Inter-symbol interference)(2)

Cable Skew—typically 10 ps–40 ps per foot, media dependent

Cycle-to-cycle jitter is less than 250 ps at 65 MHz.

ISI is dependent on interconnect length; may be zero.

Figure 15. Receiver LVDS Input Skew Margin

DS90CF384A PIN DESCRIPTIONS — 56 Lead TSSOP Package — 24-Bit FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	4	Positive LVDS differential data inputs.
RxIN−	I	4	Negative LVDS differential data inputs.
RxOUT	O	28	TTL level data outputs. This includes: 8 Red, 8 Green, 8 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN−	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V_{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

DS90CF364A PIN DESCRIPTIONS — 48 Lead TSSOP Package — 18-Bit FPD Link Receiver

Pin Name	I/O	No.	Description
RxIN+	I	3	Positive LVDS differential data inputs.
RxIN−	I	3	Negative LVDS differential data inputs.
RxOUT	O	21	TTL level data outputs. This includes: 6 Red, 6 Green, 6 Blue, and 3 control lines—FPLINE, FPFRAME, DRDY (also referred to as HSYNC, VSYNC, Data Enable).
RxCLK IN+	I	1	Positive LVDS differential clock input.
RxCLK IN−	I	1	Negative LVDS differential clock input.
RxCLK OUT	O	1	TTL level clock output. The falling edge acts as data strobe.
$\overline{\text{PWR DOWN}}$	I	1	TTL level input. When asserted (low input) the receiver outputs are low.
V_{CC}	I	4	Power supply pins for TTL outputs.
GND	I	5	Ground pins for TTL outputs.
PLL V_{CC}	I	1	Power supply for PLL.
PLL GND	I	2	Ground pin for PLL.
LVDS V_{CC}	I	1	Power supply pin for LVDS inputs.
LVDS GND	I	3	Ground pins for LVDS inputs.

Pin Diagram for TSSOP Packages

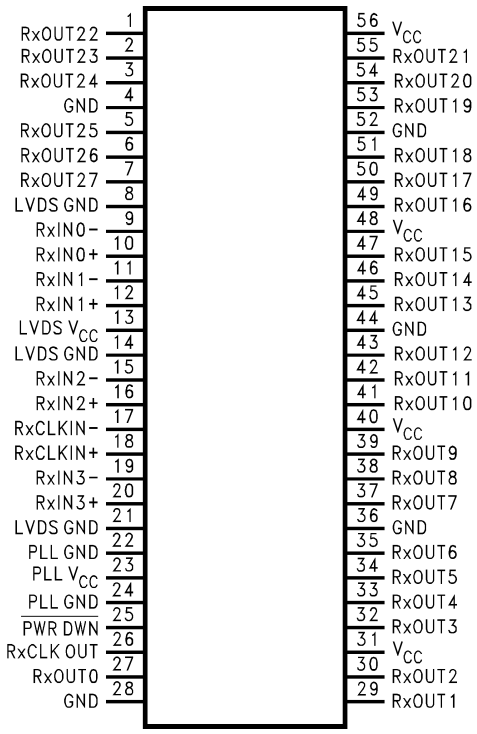


Figure 16. DS90CF384A DGG-56 Package

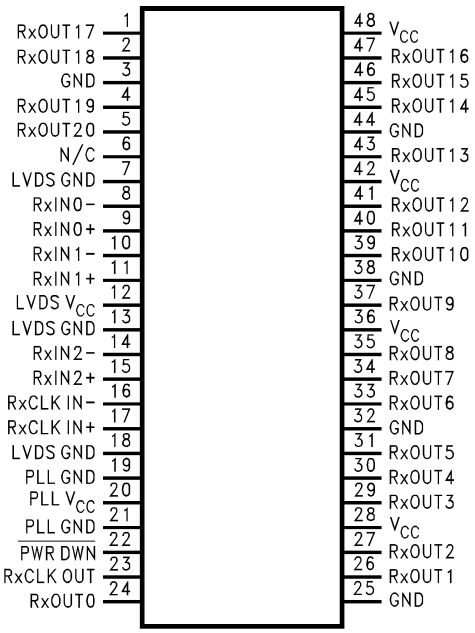


Figure 17. DS90CF364A DGG-48 Package

REVISION HISTORY

Changes from Revision H (April 2013) to Revision I	Page
• Changed layout of National Data Sheet to TI format	12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS90CF364AMTD	NRND	TSSOP	DGG	48	38	TBD	Call TI	Call TI	-10 to 70	DS90CF364AMTD >B	
DS90CF364AMTD/NOPB	ACTIVE	TSSOP	DGG	48	38	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CF364AMTD >B	Samples
DS90CF364AMTDX	NRND	TSSOP	DGG	48	1000	TBD	Call TI	Call TI	-10 to 70	DS90CF364AMTD >B	
DS90CF364AMTDX/NOPB	ACTIVE	TSSOP	DGG	48	1000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CF364AMTD >B	Samples
DS90CF384AMTD/NOPB	ACTIVE	TSSOP	DGG	56	34	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CF384AMTD >B	Samples
DS90CF384AMTDX/NOPB	ACTIVE	TSSOP	DGG	56	1000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-10 to 70	DS90CF384AMTD >B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

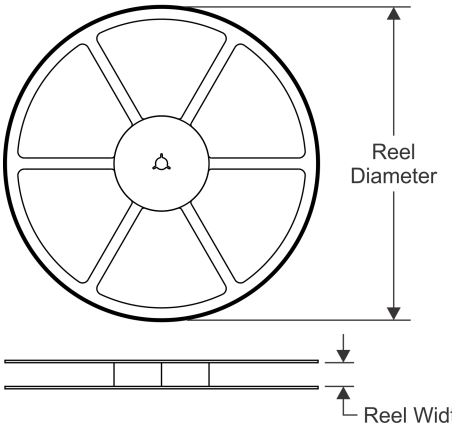
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

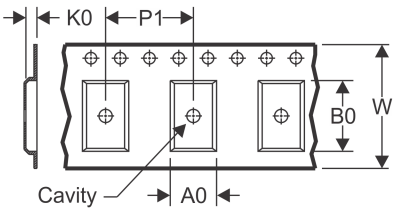
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

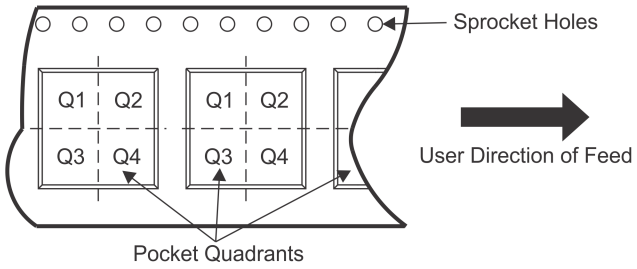


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

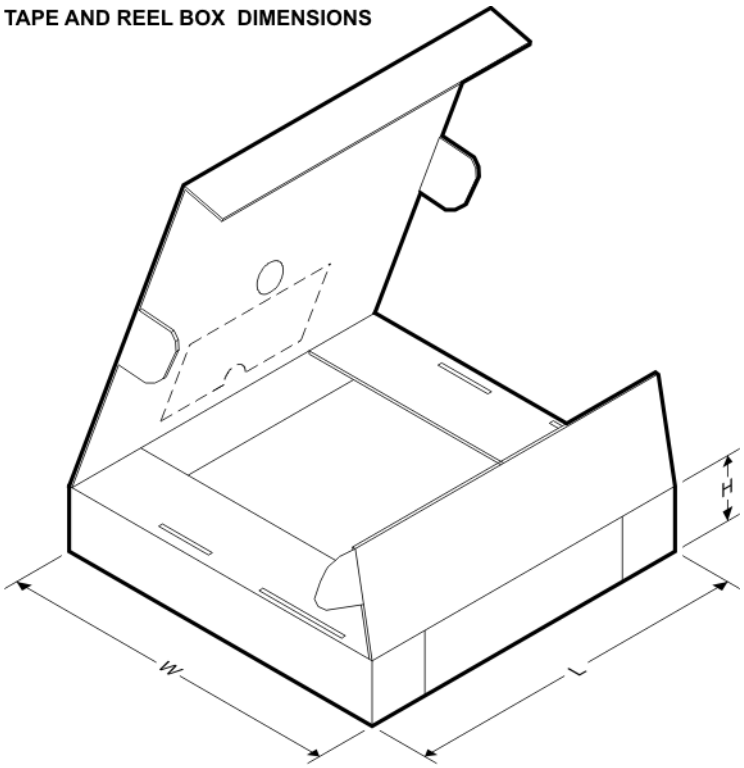
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90CF364AMTDX	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1
DS90CF364AMTDX/NOPB	TSSOP	DGG	48	1000	330.0	24.4	8.6	13.2	1.6	12.0	24.0	Q1
DS90CF384AMTDX/NOPB	TSSOP	DGG	56	1000	330.0	24.4	8.6	14.5	1.8	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

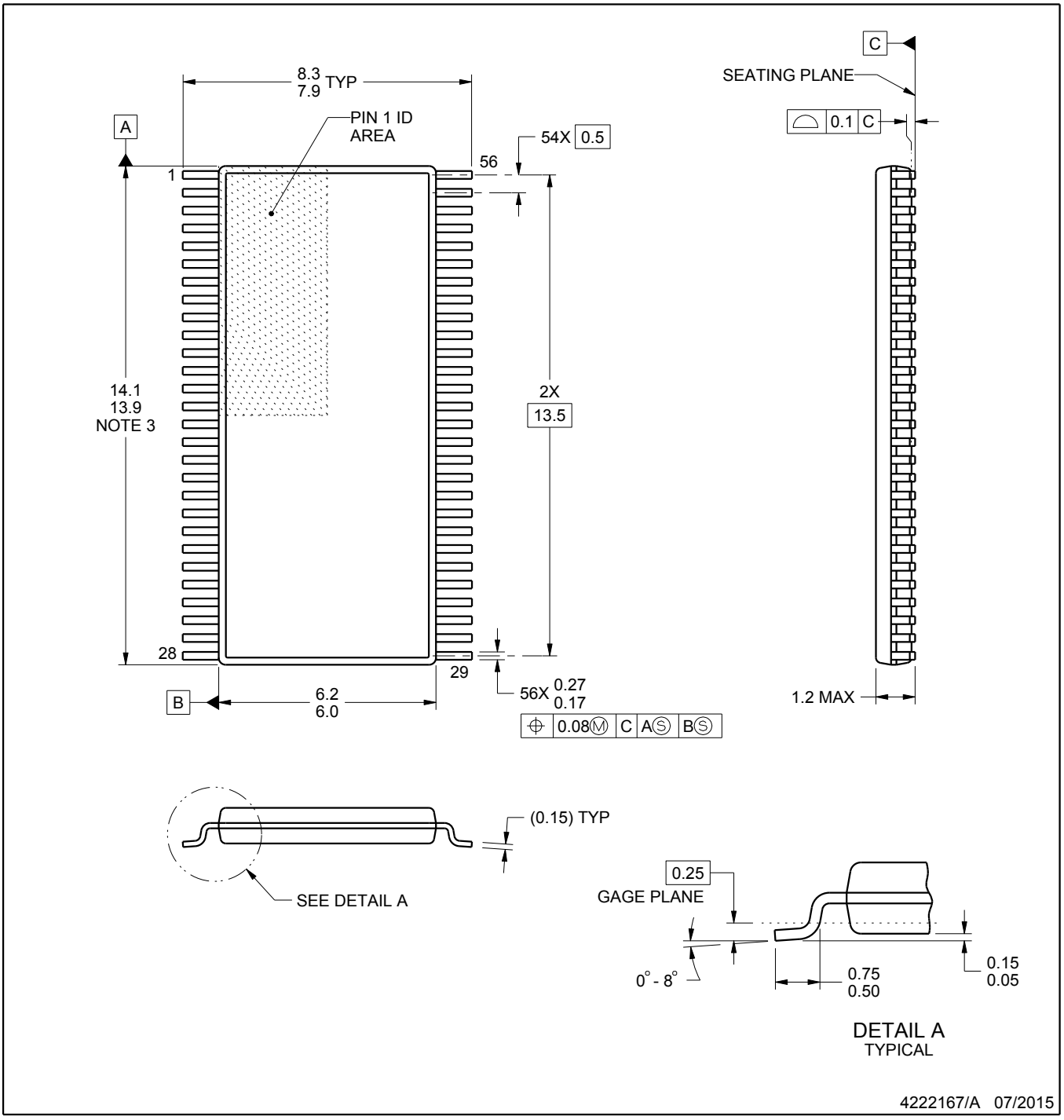
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90CF364AMTDX	TSSOP	DGG	48	1000	367.0	367.0	45.0
DS90CF364AMTDX/NOPB	TSSOP	DGG	48	1000	367.0	367.0	45.0
DS90CF384AMTDX/NOPB	TSSOP	DGG	56	1000	367.0	367.0	45.0

PACKAGE OUTLINE

DGG0056A

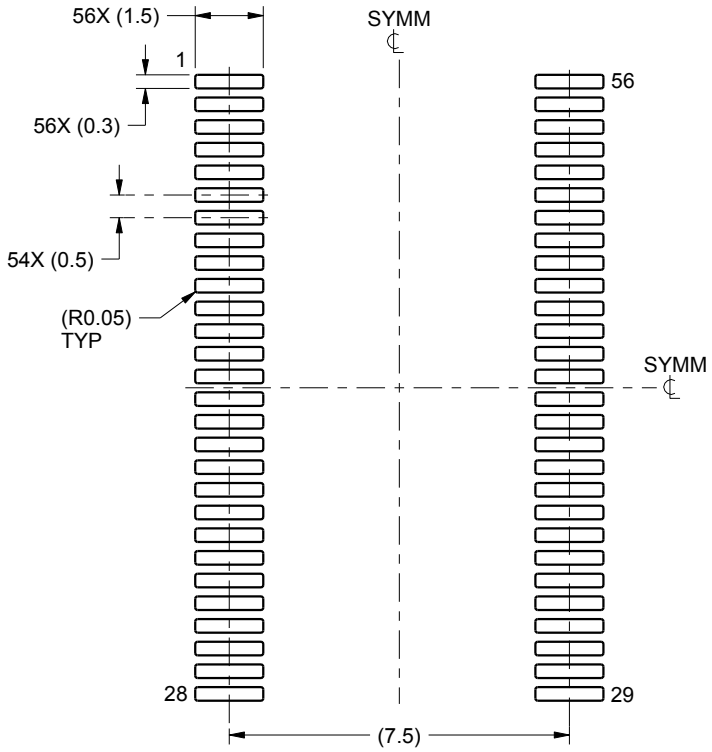
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

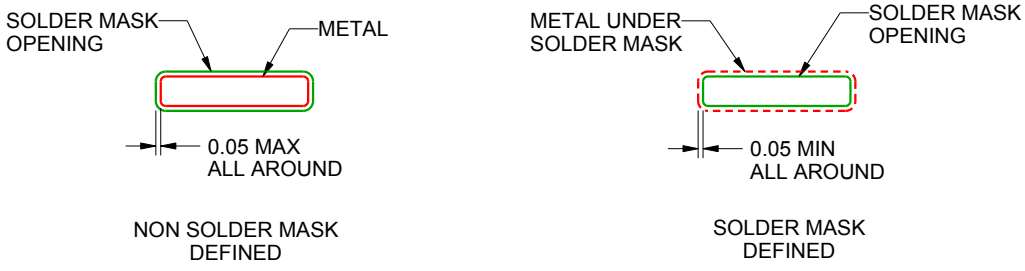


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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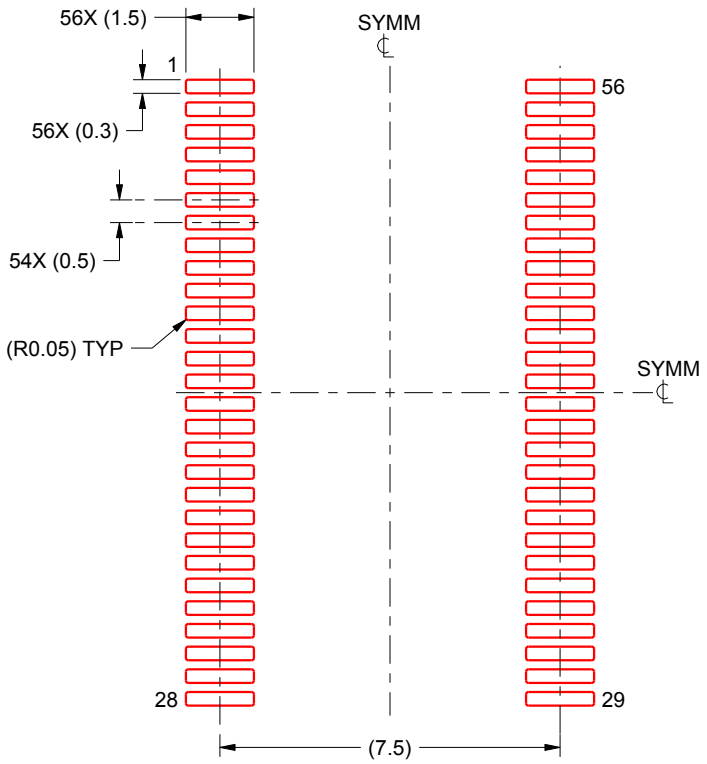
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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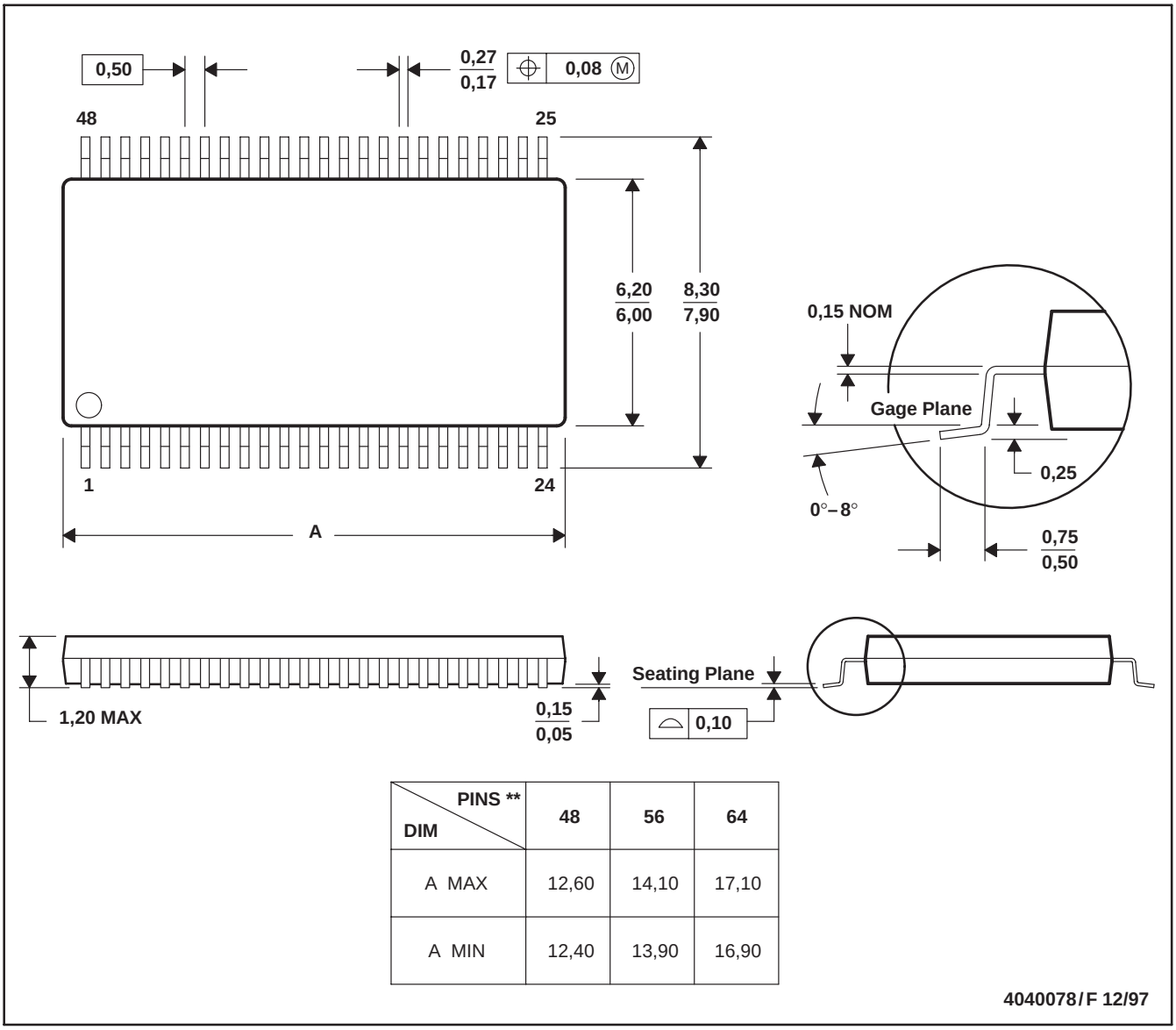
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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