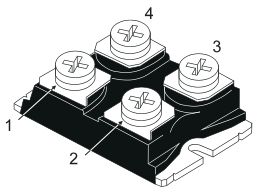
STE45NK80ZD

N-channel 800V - 0.11Ω - 45A ISOTOP SuperFREDmesh™ MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STE45NK80ZD	800V	<0.13Ω	45A	600W

- Extremely high dv/dt capability
- 100% avalanche tested
- Very low intrinsic capacitances
- Very good manufacturing repeatibility

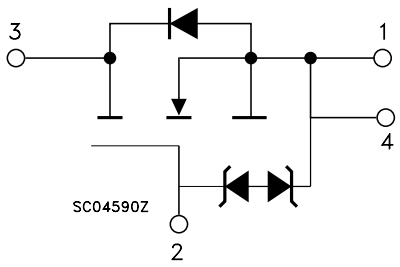


ISOTOP

Description

The SuperFREDMesh™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STE45NK80ZD	E45NK80ZD	ISOTOP	Tube

Obsolete Product(s) - Obsolete Product(s)

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Obsolete Product(s) - Obsolete Product(s)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	800	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kW)	800	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain Current (continuous) at T_C = 25°C (Steady State)	45	A A
I_D	Drain Current (continuous) at T_C = 100°C	28	A
I_{DM} (1)	Drain Current (pulsed)	180	A
P_{TOT}	Total Dissipation at T_C = 25°C (steady state)	600	W
P_{TOT}	Derating factor	5	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5kW)	7	KV
dv/dt (2)	Peak diode recovery voltage slope	8	V/ns
V_{ISO}	Insulation withstand voltage (AC-RMS) from all four terminals to external heatsink	2500	V
T_j Tstg	Operating junction temperature Storage temperature	- 65 to 150	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤45A, di/dt £ 500 A/µs, V_{DD} ≤$V_{(BR)DSS}$.

Table 2. Thermal data

Rthj-case	Thermal Resistance Junction-case Max	0.2	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	40	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	45	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 35 V)	1.2	J

Obsolete Product(s) - Obsolete Product(s)

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 1 mA, V_{GS} = 0	800			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			10 100	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 20V			±10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 150µA	2.5	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 22.5 A		0.11	0.13	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15V, I_D = 22.5 A		35		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		26000 1620 260		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{GS} = 0V, V_{DS} = 0V to 720V		700		pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 400 V, I_D = 20 A R_G = 4.7Ω, V_{GS} = 10 V (see *Figure 18*)		105 128 350 174		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400 V, I_D = 40 A, V_{GS} = 10V		558 121 307	781	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Coss eq. is defined as a constant equivalent capacitance giving the same charging time as Coss when V_{DS} increases from 0 to 80% V_{DSS}.

Obsolete Product(s) - Obsolete Product(s)

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				45 180	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 45 A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 40 A, di/dt = 100A/µs V_{DD} = 50 V, T_j = 25°C		375 4.65 24.8		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 40 A, di/dt = 100A/µs V_{DD} = 50 V, T_j = 150°C		568 9.66 34		ns µC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

Table 7. Gate-source zener diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs=± 1mA (open drain)	30			V

2.1 Protection features of gate-to-source zener diodes

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

Obsolete Product(s) - Obsolete Product(s)

2.2 Electrical characteristics (curves)

Figure 1. Safe operating area

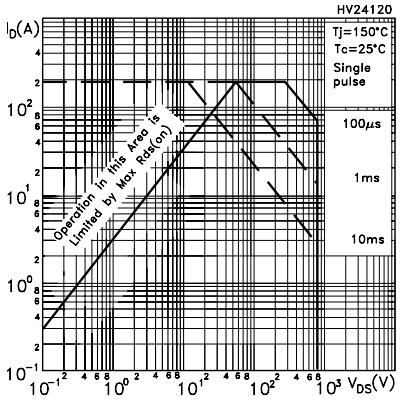


Figure 2. Thermal impedance

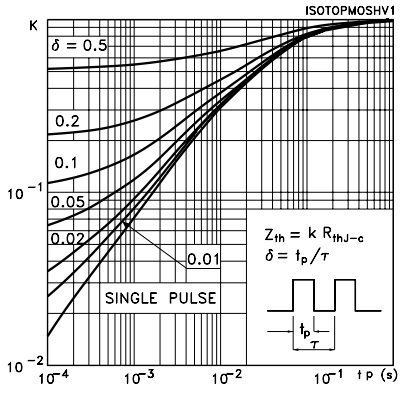


Figure 3. Output characterisics

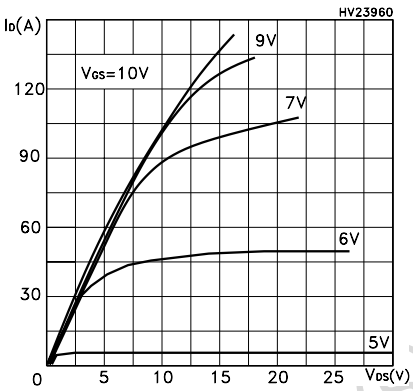


Figure 4. Transfer characteristics

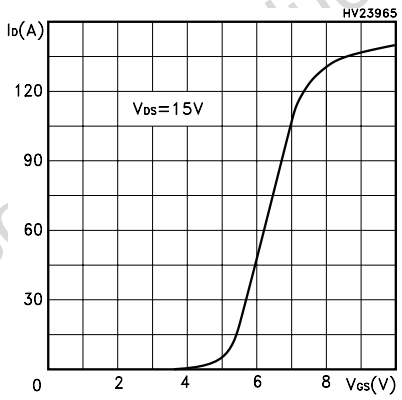


Figure 5. Transconductance

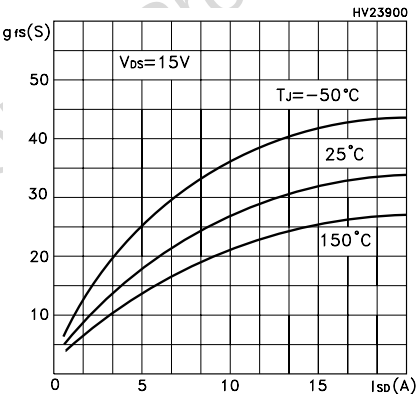
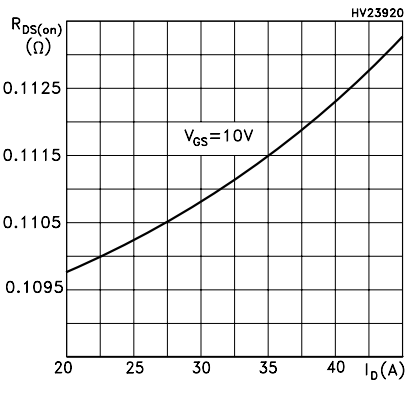


Figure 6. Static drain-source on resistance



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Figure 7. Gate charge vs gate-source voltage

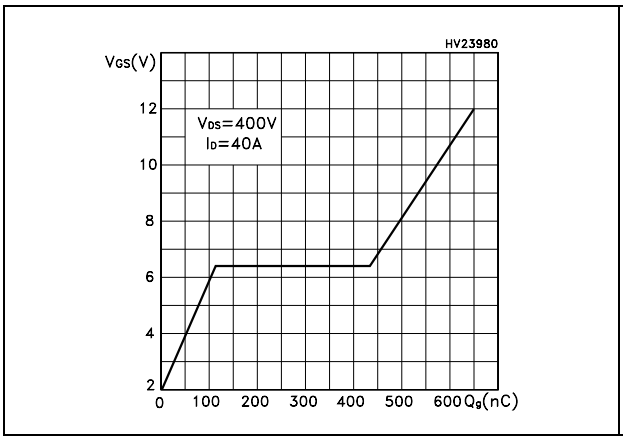


Figure 8. Capacitance variations

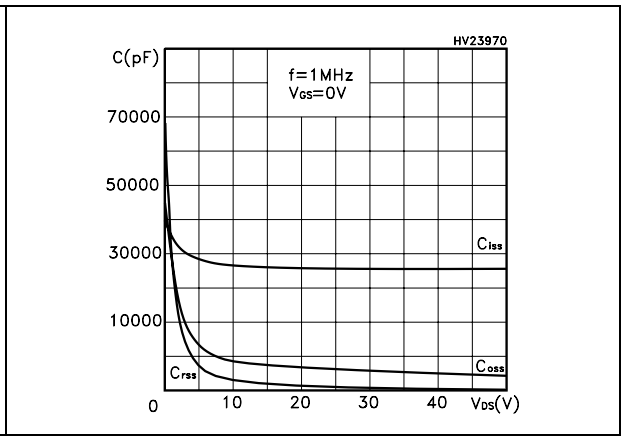


Figure 9. Normalized gate threshold voltage vs temperature

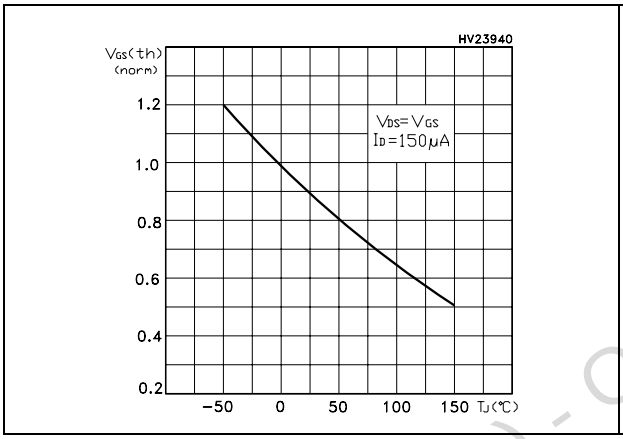


Figure 10. Normalized on resistance vs temperature

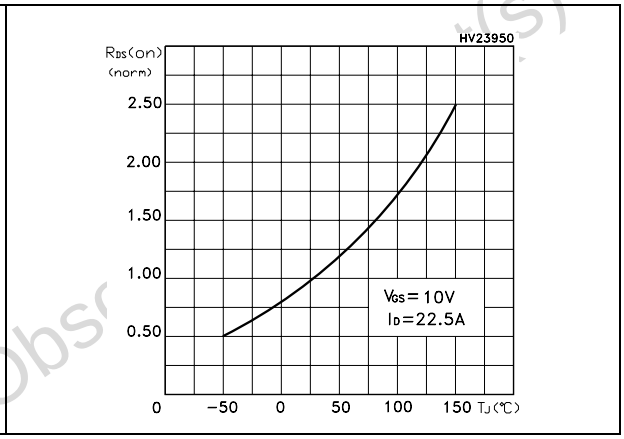


Figure 11. Source-drain diode forward characteristics

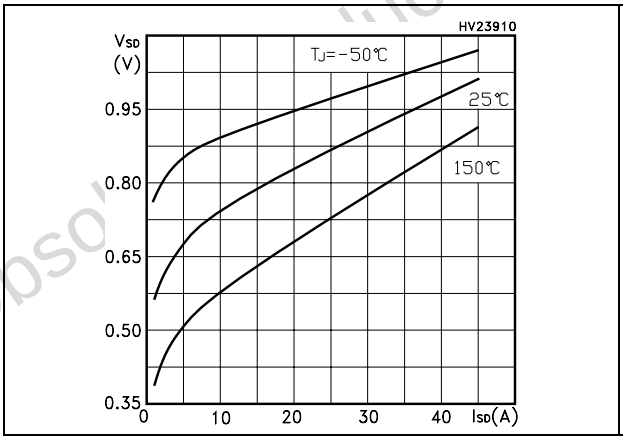


Figure 12. Normalized B_{VDSS} vs temperature

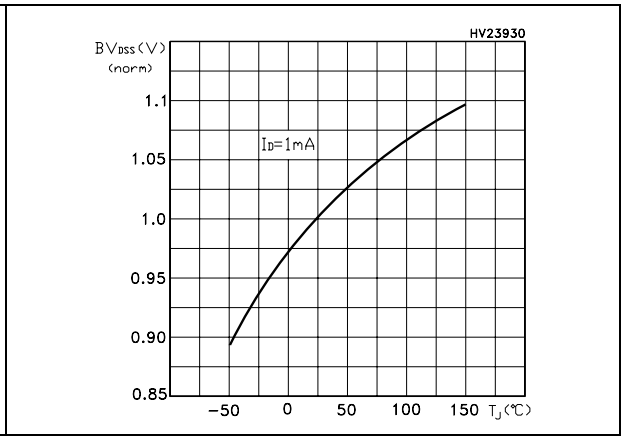
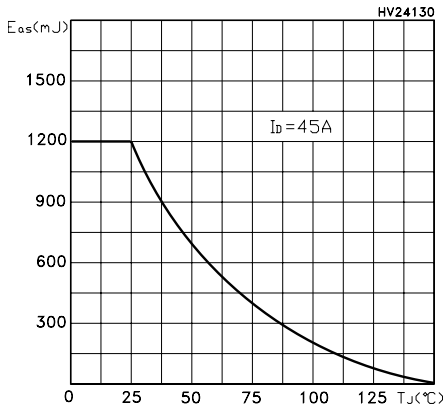


Figure 13. Avalanche energy vs starting Tj



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3 Test circuit

Figure 14. Unclamped Inductive load test circuit

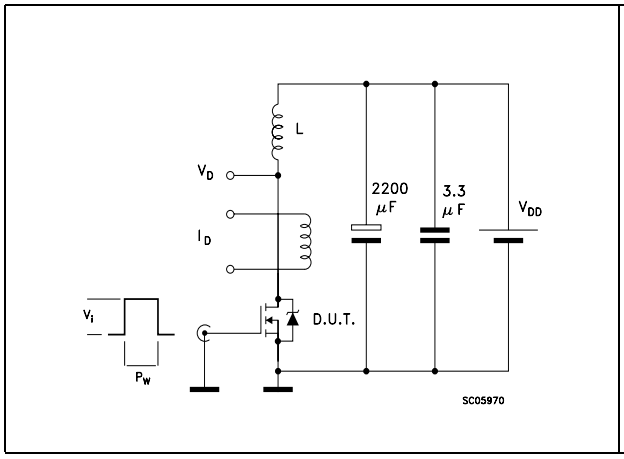


Figure 15. Unclamped inductive waveform

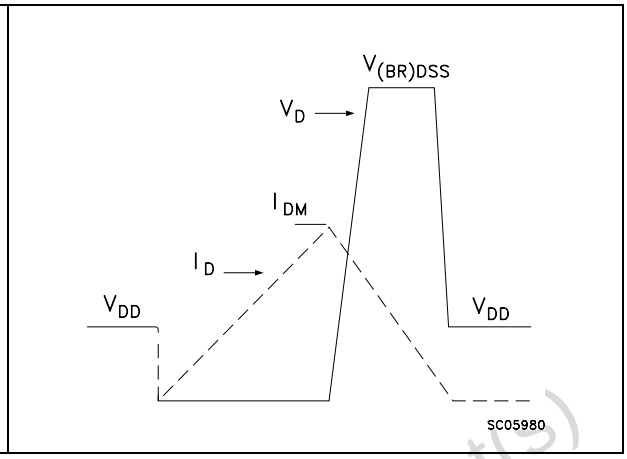


Figure 16. Switching times test circuit for resistive load

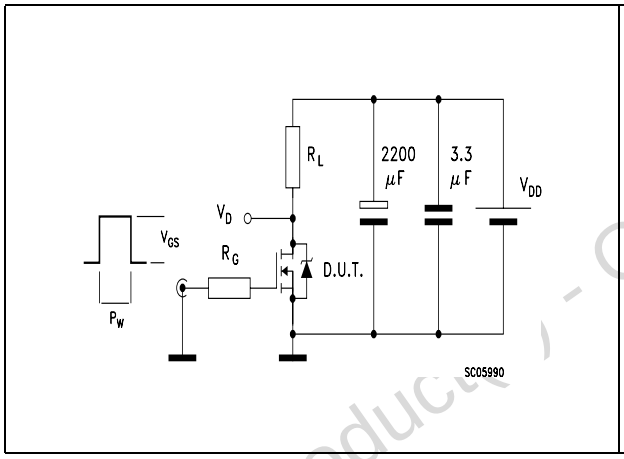


Figure 17. Gate charge test circuit

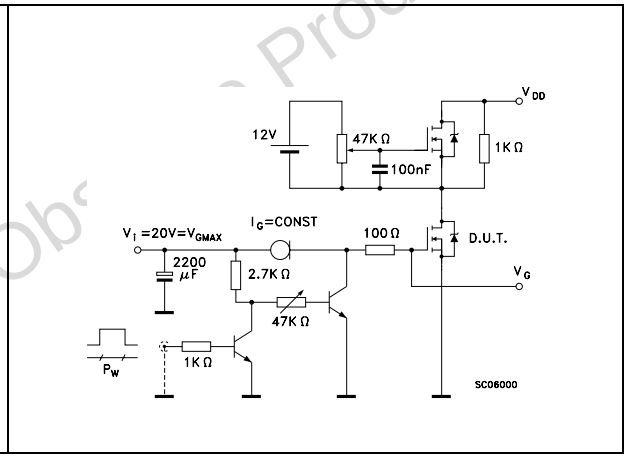
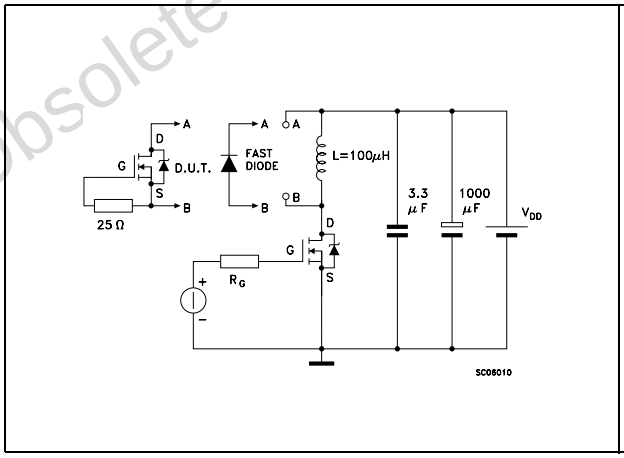


Figure 18. Test circuit for inductive load switching and diode recovery times



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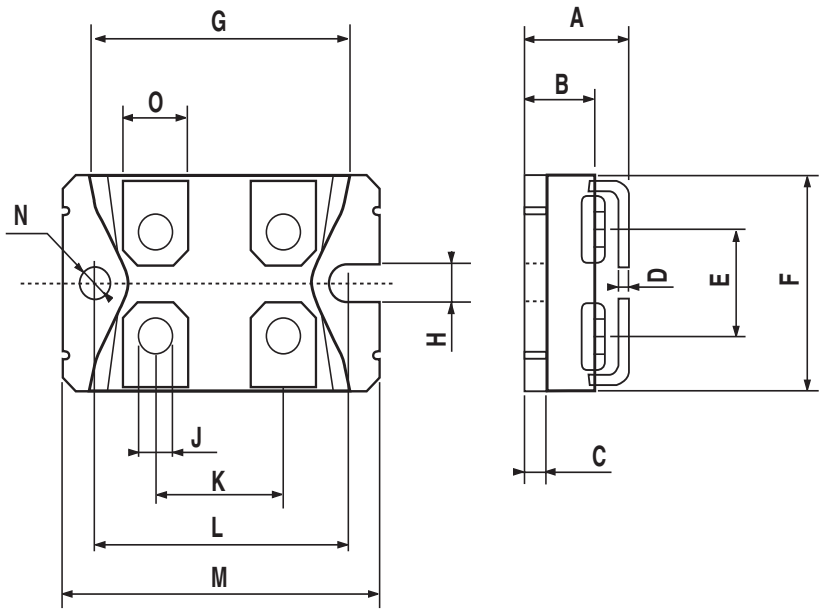
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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ISOTOP MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	11.8		12.2	0.466		0.480
B	8.9		9.1	0.350		0.358
C	1.95		2.05	0.076		0.080
D	0.75		0.85	0.029		0.033
E	12.6		12.8	0.496		0.503
F	25.15		25.5	0.990		1.003
G	31.5		31.7	1.240		1.248
H	4			0.157		
J	4.1		4.3	0.161		0.169
K	14.9		15.1	0.586		0.594
L	30.1		30.3	1.185		1.193
M	37.8		38.2	1.488		1.503
N	4			0.157		
O	7.8		8.2	0.307		0.322



Obsolete

5 Revision history

Table 8. Document revision history

Date	Revision	Changes
24-May-2005	1	First Release
10-Jun-2005	2	Inserted new row in *Table 6.: Switching times*
28-Sep-2005	3	Complete version
14-Oct-2005	4	Modified *Figure 3*, *Figure 6*
06-Mar-2006	5	New Stylesheet
29-Mar-2006	6	Modified value on *Table 4.*
27-Jun-2006	7	New template, no content change

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