ESD122 2-Channel ESD Protection Diode for USB Type-C and HDMI 2.0

1 Features

- IEC 61000-4-2 Level 4 ESD Protection
  - ±17-kV Contact Discharge
  - ±17-kV Air Gap Discharge
- Withstands over 10,000 ESD strikes per IEC 61000-4-2 Level 4 (Contact) without any performance degradation
- IEC 61000-4-4 EFT Protection
  - 80 A (5/50 ns)
- IEC 61000-4-5 Surge Protection
  - 2.5 A (8/20 µs)
- Low IO Capacitance
  - 0.1 pF (Typical) between IOs
  - 0.2 pF (Typical) IO to GND
- DC Breakdown Voltage: 5.1 V (Minimum)
- Ultra Low Leakage Current: 10 nA (Maximum)
- Low ESD Clamping Voltage: 8.4 V at 5-A TLP
- Supports High Speed Interfaces that exceed 10 Gbps
- Industrial Temperature Range: –40°C to +125°C
- Type C Friendly Two Channel Flow-Through Routing Package
- Pin-out to suit symmetric differential high-speed signal routing
- Two Different Package Options
  - 0402 Package, 0.6 mm × 1 mm, 0.34-mm Pitch
  - 0502 Package, 0.6 mm × 1.32 mm, 0.5-mm Pitch

2 Applications

- End Equipment
  - Mobile and Tablets
  - Laptops and Desktops
  - Set-Top Boxes
  - TV and Monitors
  - Servers
- Interfaces
  - USB Type-C
  - HDMI 2.0/1.4
  - USB 3.1 Gen 2/Gen1, USB 3.0, and USB 2.0
  - Thunderbolt-1 and Thunderbolt-2
  - Display Port 1.3
  - PCI Express 3.0
  - SATA

3 Description

The ESD122 is a bidirectional TVS ESD protection diode array for USB Type-C and HDMI 2.0 circuit protection. The ESD122 is rated to dissipate contact ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (17-kV Contact, 17-kV Air-gap).

This device features a low IO capacitance per channel and pin-out to suit symmetric differential high-speed signal routing making it ideal for protecting high-speed interfaces up to 10 Gbps such as USB 3.1 Gen2 and HDMI 2.0. The low dynamic resistance and low clamping voltage ensure system level protection against transient events.

Additionally, the ESD122 is an ideal ESD solution for the USB Type-C Tx/Rx lines. Since the USB Type-C connector has two layers, using 4-channel ESD devices require VIAs which degrade the signal integrity. Using four ESD122 (2-Ch) devices minimize the number of VIAs and simply the board layout.

The ESD122 is offered in two easy routing flow through packages.

Device Information(1)

PART NUMBER	PACKAGE		BODY SIZE (NOM)
ESD122	X2SON (3)	(DMX)	0.60 mm × 1.00 mm
		(DMY)	0.60 mm × 1.32 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

USB Type C Application Example

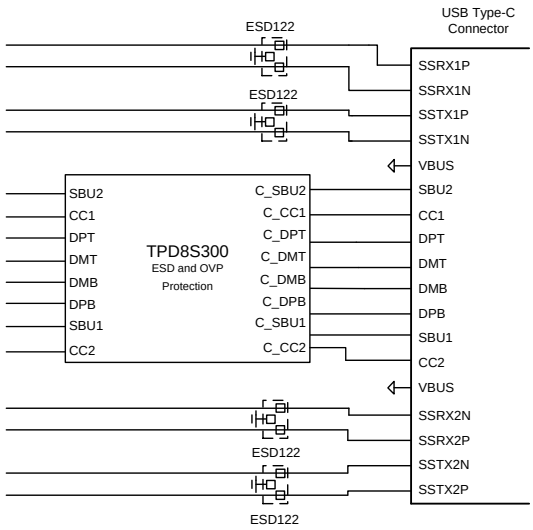


Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings—JEDEC Specification ... 4
6.3 ESD Ratings—IEC Specification ... 4
6.4 Recommended Operating Conditions ... 4
6.5 Thermal Information ... 4
6.6 Electrical Characteristics ... 5
6.7 Typical Characteristics ... 6
7 Detailed Description ... 8
7.1 Overview ... 8
7.2 Functional Block Diagram ... 8
7.3 Feature Description ... 8
7.4 Device Functional Modes ... 9
8 Application and Implementation ... 10
8.1 Application Information ... 10
8.2 Typical Applications ... 10
9 Power Supply Recommendations ... 14
10 Layout ... 14
10.1 Layout Guidelines ... 14
10.2 Layout Examples ... 14
11 Device and Documentation Support ... 16
11.1 Documentation Support ... 16
11.2 Receiving Notification of Documentation Updates 16
11.3 Community Resources ... 16
11.4 Trademarks ... 16
11.5 Electrostatic Discharge Caution ... 16
11.6 Glossary ... 16
12 Mechanical, Packaging, and Orderable Information ... 16

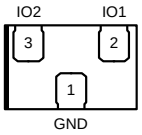
4 Revision History

Changes from Original (June 2017) to Revision A **Page**

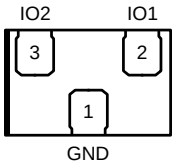
- Changed V_{BRF} From: MIN = 5.1, MAX = 7 To: MIN = 5 and MAX = 7.9 ... 5
- Changed V_{BRR} From: MIN = –7, MAX = –5.1 To: MIN = –7.9 and MAX = –5 ... 5

5 Pin Configuration and Functions

DMX Package
3-Pin X2SON
Top View



DMY Package
3-Pin X2SON
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	DMX NO.	DMY NO.		
GND	1	1	—	Ground
IO1	2	2	I	ESD protected channel
IO2	3	3	I	ESD protected channel

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-4 (5/50 ns) at 25°C		80	A
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20 µs) at 25°C		20	W
	IEC 61000-4-5 Current (t_p - 8/20 µs) at 25°C		2.5	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	DMD storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±17000	V
		IEC 61000-4-2 air-gap discharge	±17000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–3.6	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		ESD122		UNIT
		DMX (X2SON)	DMY (X2SON)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	617.8	717.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	286.2	300.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	455.1	526	°C/W
ψ_{JT}	Junction-to-top characterization parameter	99.3	113.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	453.4	523.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	–3.6		3.6	V
V_{BRF}	Breakdown voltage, any IO pin to GND(1)	I_{IO} = 1 mA, T_A = 25°C	5		7.9	V
V_{BRR}	Breakdown voltage, GND to any IO pin(1)	I_{IO} = 1 mA, T_A = 25°C	–7.9		–5	V
V_{HOLD}	Holding voltage(2)	I_{IO} = 1 mA		5.9		V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND, T_A = 25°C		6.4		V
		I_{PP} = 5 A, TLP, from IO to GND, T_A = 25°C		8.4		
		I_{PP} = 1 A, TLP, from GND to IO, T_A = 25°C		6.4		
		I_{PP} = 5 A, TLP, from GND to IO, T_A = 25°C		8.4		
I_{LEAK}	Leakage current, any IO to GND	V_{IO} = ±2.5 V			10	nA
R_{DYN}	Dynamic resistance	IO to GND, Measured between TLP I_{PP} of 10 A and 20 A, T_A = 25°C		0.5		Ω
		GND to IO, Measured between TLP I_{PP} of 10 A and 20 A, T_A = 25°C		0.5		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND, T_A = 25°C		0.2	0.27	pF
ΔC_L	Variation of line capacitance	Difference between the capacitance of the two IO pins measured with respect to ground, V_{IO} = 0 V, f = 1 MHz, T_A = 25°C, GND = 0 V			0.01	pF
C_{CROSS}	Channel to channel capacitance	Capacitance from one IO to another IO, V_{IO} = 0 V, f = 1 MHz, T_A = 25°C, GND = 0 V		0.1	0.14	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage obtained at 1 mA when sweeping the voltage up, before the device latches into the snapback state.
(2) V_{HOLD} is defined as the voltage when 1 mA is applied, after the device has successfully latched into the snapback state.

6.7 Typical Characteristics

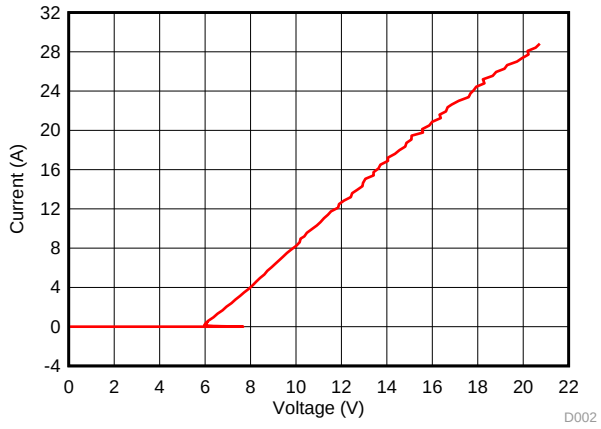


Figure 1. Positive TLP Curve, IO Pin to GND

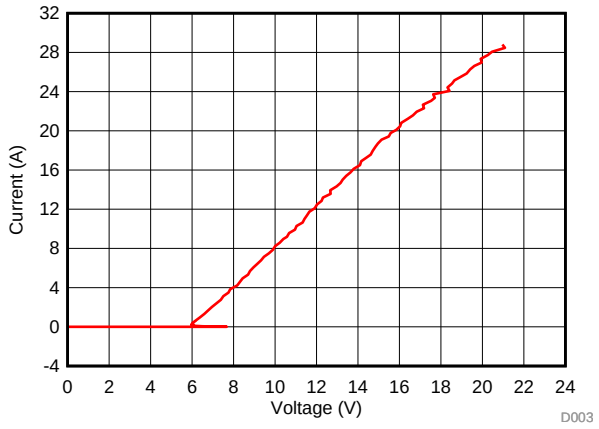


Figure 2. Negative TLP Curve, IO Pin to GND (Plotted as Positive TLP Curve GND to IO)

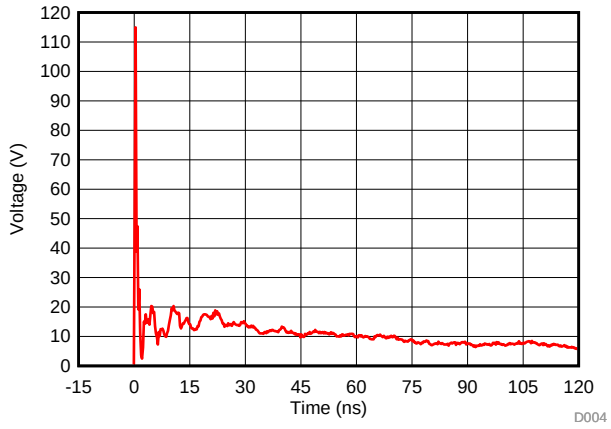


Figure 3. 8-kV IEC 61000-4-2 Waveform, IO Pin to GND

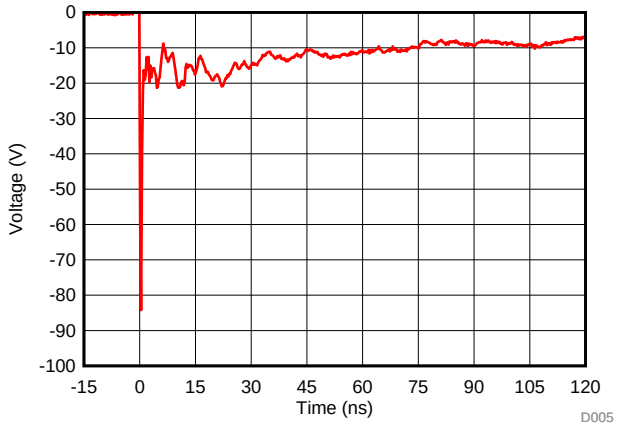


Figure 4. –8-kV IEC 61000-4-2 Waveform, IO Pin to GND

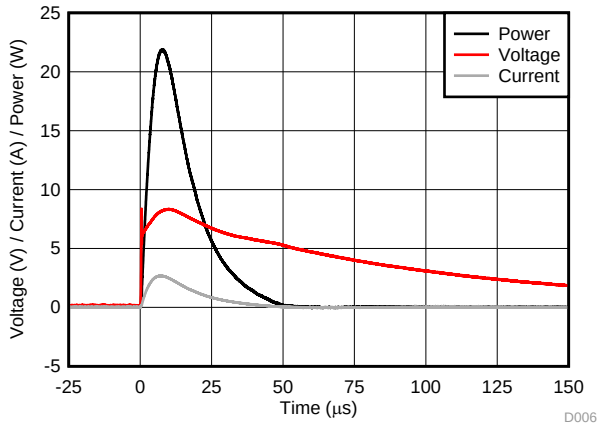


Figure 5. IEC 61000-4-5 Surge Curve (tp = 8/20µs), IO Pin to GND

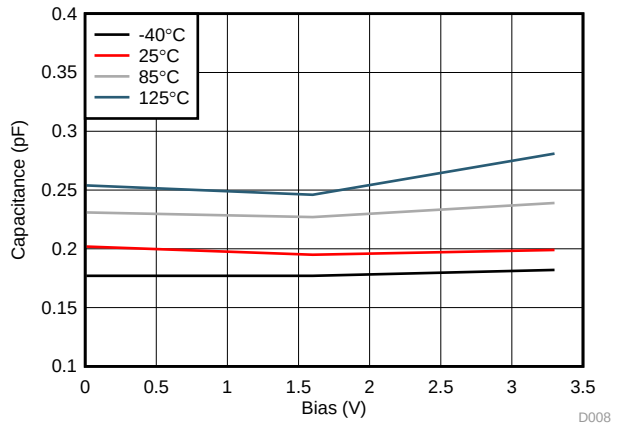


Figure 6. Capacitance vs Bias Voltage at Multiple Temperatures, IO Pin to GND

Typical Characteristics (continued)

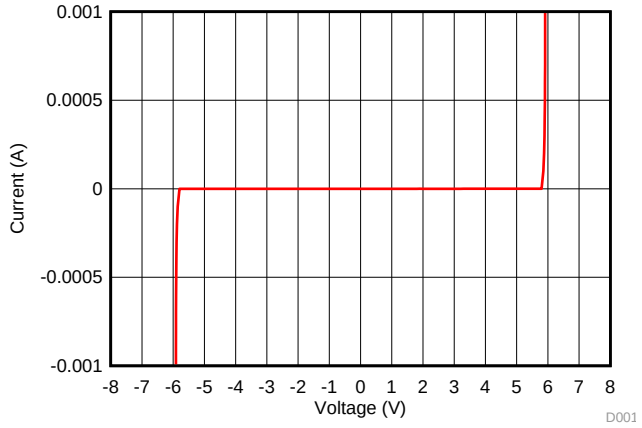


Figure 7. DC Voltage Sweep I-V Curve, IO Pin to GND

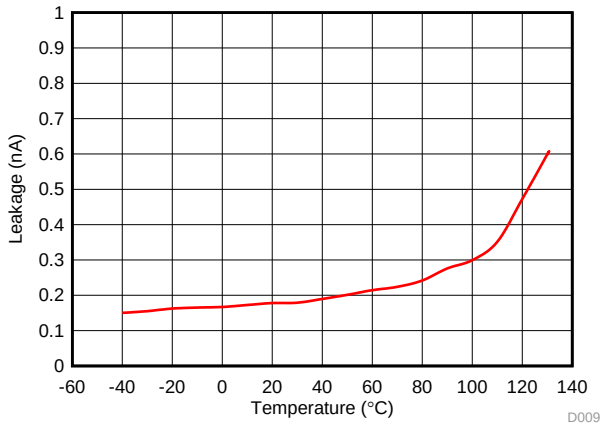


Figure 8. Leakage Current vs Temperature, IO Pin to GND, at 2.5 V Bias

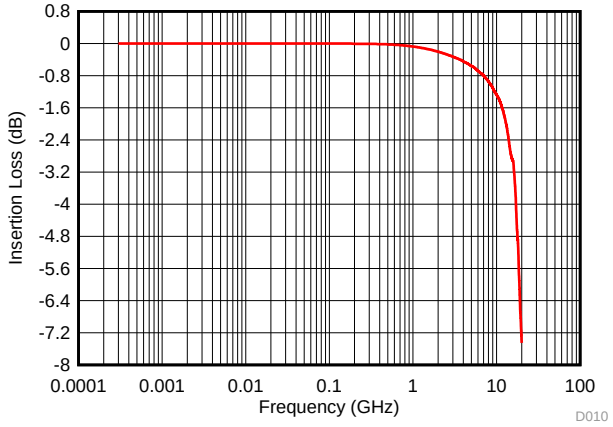


Figure 9. Insertion Loss

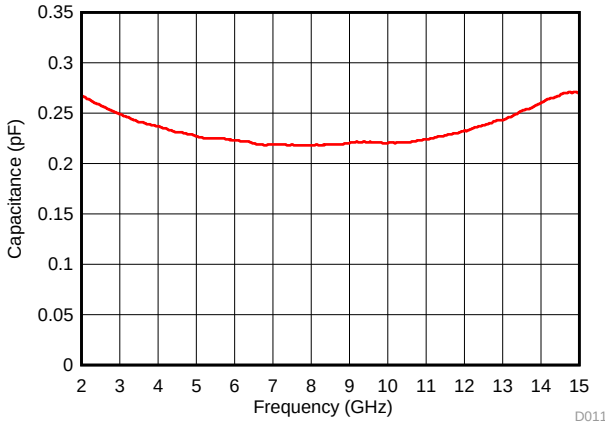


Figure 10. Capacitance vs Frequency

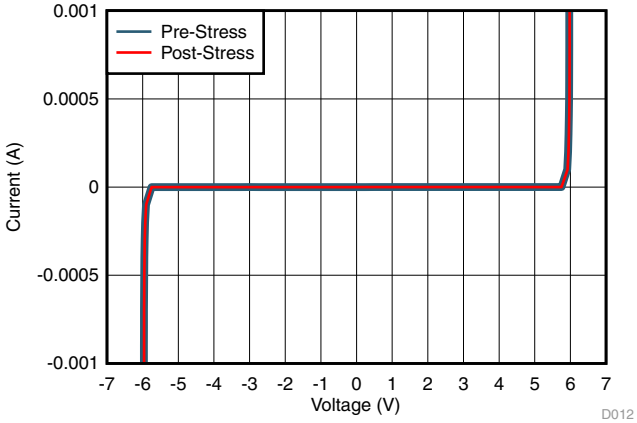


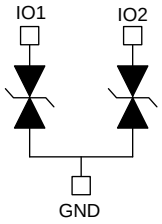
Figure 11. DC Voltage Sweep I-V Curve, IO Pin to GND, Pre and Post 10,000 Repetitive ESD Strikes per IEC 61000-4-2 Level 4 (Contact)

7 Detailed Description

7.1 Overview

The ESD122 is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins. Additionally, the ESD122 has two identical protection channels with a symmetrical pin-out that is suited for the differential high-speed signal lines.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±17-kV contact and air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50-ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2.5 A and 20 W (8/20-µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is very small and supports data rates up to 10 Gbps.

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of ±5.1 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

7.3.6 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of ±2.5 V.

7.3.7 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 8.4 V (I_{PP-TLP} = 5 A).

7.3.8 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 10 Gbps such as USB 3.1 Gen2 and Gen1, USB 3.0, USB 2.0, Thunderbolt-1, Thunderbolt-2, PCI express 3.0, Display Port 1.3, HDMI 2.0, and HDMI 1.4, because of the extremely low IO capacitance.

7.3.9 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

Feature Description (continued)

7.3.10 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. 2-channel setup provides easy, flexible routing and good matching between the channels.

7.4 Device Functional Modes

The ESD122 is a passive circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±17 kV (contact) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of ESD122 (usually within 10s of nano-seconds) the device reverts to passive.

Figure 12 shows typical TLP behavior of bi-directional ESD device.

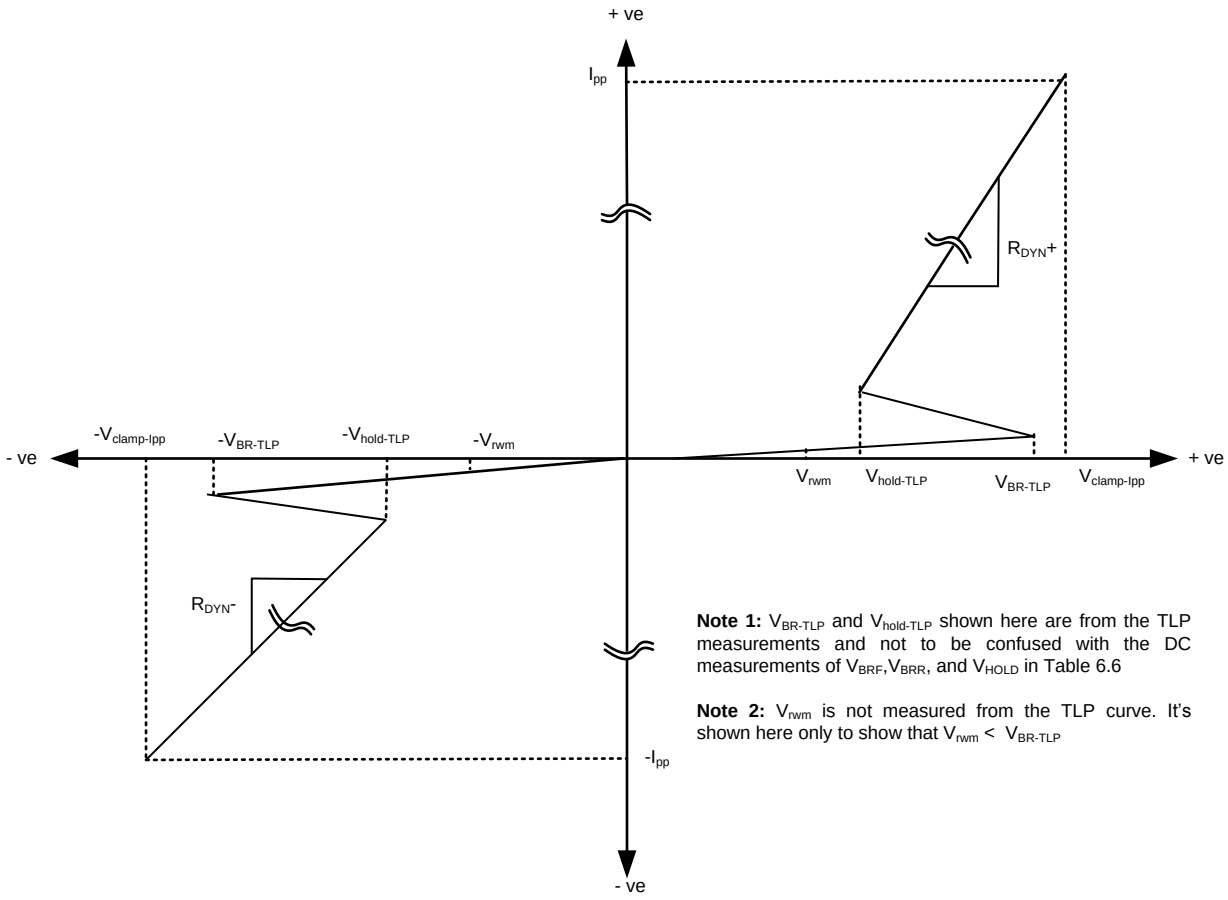


Figure 12. Generic TLP I-V Curve for a Bi-Directional ESD Device for the Illustration of V_{rwm}, V_{BR}, V_{hold} and V_{clamp}

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The ESD122 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Applications

8.2.1 USB 3.1 Gen 2 Application

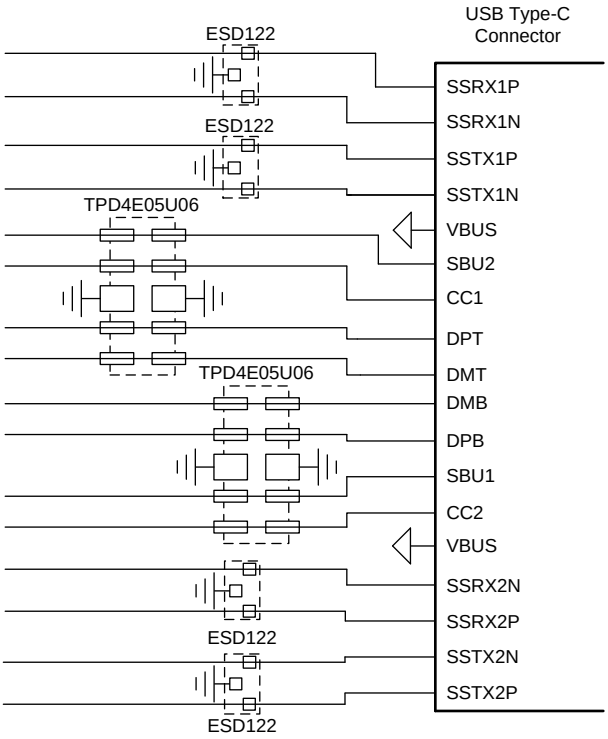


Figure 13. Typical Application

8.2.1.1 Design Requirements

For this design example, four ESD122 devices and two TPD4E05U06 devices are being used in a USB 3.1 Gen 2 Type-C application. This provides a complete ESD protection scheme.

Given the application, the parameters listed in Table 1 are known.

Typical Applications (continued)

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on Type C SuperSpeed+ lines	0 V to 3.6 V
Operating frequency on Type C USB 3.1 Gen 2 SuperSpeed+ lines	5 GHz
Signal range on CC, SBU, and DP/DM lines	0 V to 5 V
Operating frequency on CC, SBU, and DP/DM lines	up to 480 MHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Signal Range

The ESD122 supports signal ranges between –3.6 V and 3.6 V, which supports the SuperSpeed+ pairs on the USB Type-C application. The TPD4E05U06 supports signal ranges between 0 V and 5.5 V, which supports the CC, SBU, and DP/DM lines.

8.2.1.2.2 Operating Frequency

The ESD122 has a 0.27 pF (maximum) capacitance, which supports the USB 3.1 Gen 2 Type-C rate of 10 Gbps with sufficient capacitance margin. The TPD4E05U06 has a 0.5 pF (typical) capacitance, which easily supports the CC, SBU, and DP/DM data rates. The ESD122 has 2 identical protection channels for the differential HDMI high-speed signal lines. The symmetrical pin out of the device with a ground pin between the two differential signal pins makes it suitable for this application.

8.2.1.3 Application Curves

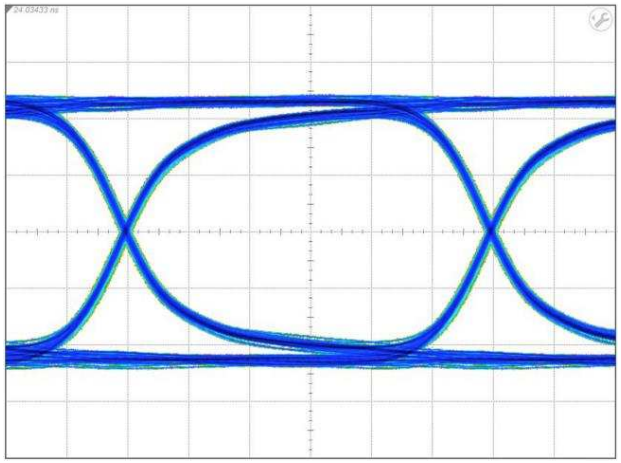


Figure 14. USB3.1 Gen2 10-Gbps Eye Diagram Without ESD122

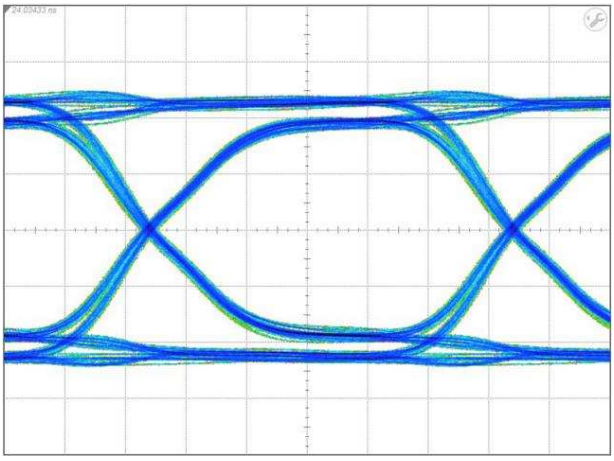


Figure 15. : USB3.1 Gen2 10-Gbps Eye Diagram With ESD122

8.2.2 HDMI 2.0 Application

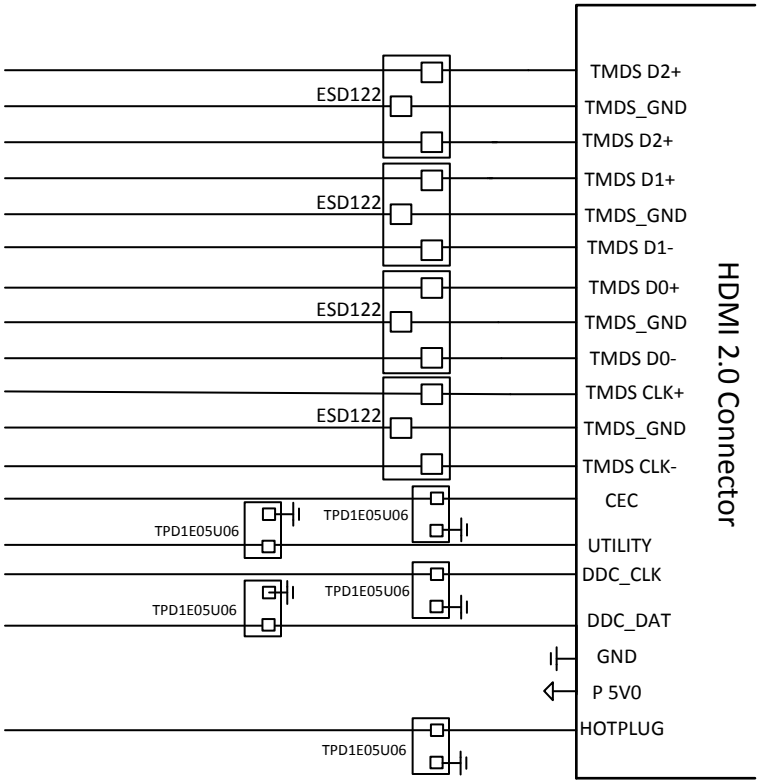


Figure 16. HDMI 2.0 Schematic

8.2.2.1 Design Requirements

For this design example, the four ESD122 devices for the HDMI 2.0 high-speed lines, and four TPD1E05U06 devices on the control lines HDMI 2.0 control lines. This provides a complete port protection scheme.

Given the HDMI 2.0 application, the parameters listed in Table 2 are known.

Table 2. Design Parameters

DESIGN PARAMETER	VALUE
Signal voltage range on the high-speed pins	0 V to 3.3 V
Signal voltage range on the control pins	0 V to 5 V
Max operating frequency of high-speed lines	3 GHz

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Signal Range

The ESD122 supports signal ranges between –3.6 V and 3.6 V, which supports the high-speed lines on the HDMI 2.0 application. The TPD1E05U06 supports signal ranges between 0 V and 5.5 V, which supports the HDMI control lines.

8.2.2.2.2 Operating Frequency

The ESD122 has a 0.27 pF (maximum) capacitance, which supports the HDMI 2.0 rate of 6 Gbps with sufficient capacitance margin. The TPD1E05U06 has a 0.42 pF (typical) capacitance, which easily supports the control lines. The ESD122 has 2 identical protection channels for the differential HDMI high-speed signal lines. The symmetrical pin out of the device with a ground pin between the two differential signal pins makes it suitable for this application.

8.2.2.3 Application Curves

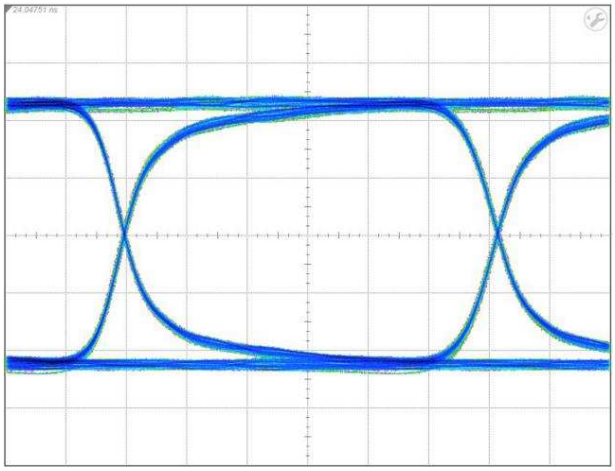


Figure 17. HDMI 2.0 6-Gbps Eye Diagram Without ESD122

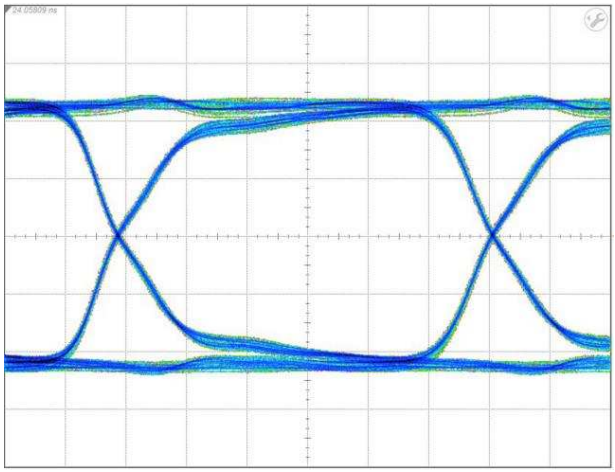


Figure 18. HDMI 2.0 6-Gbps Eye Diagram With ESD122

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible. Use as few vias as possible for 10-Gbps application.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Examples

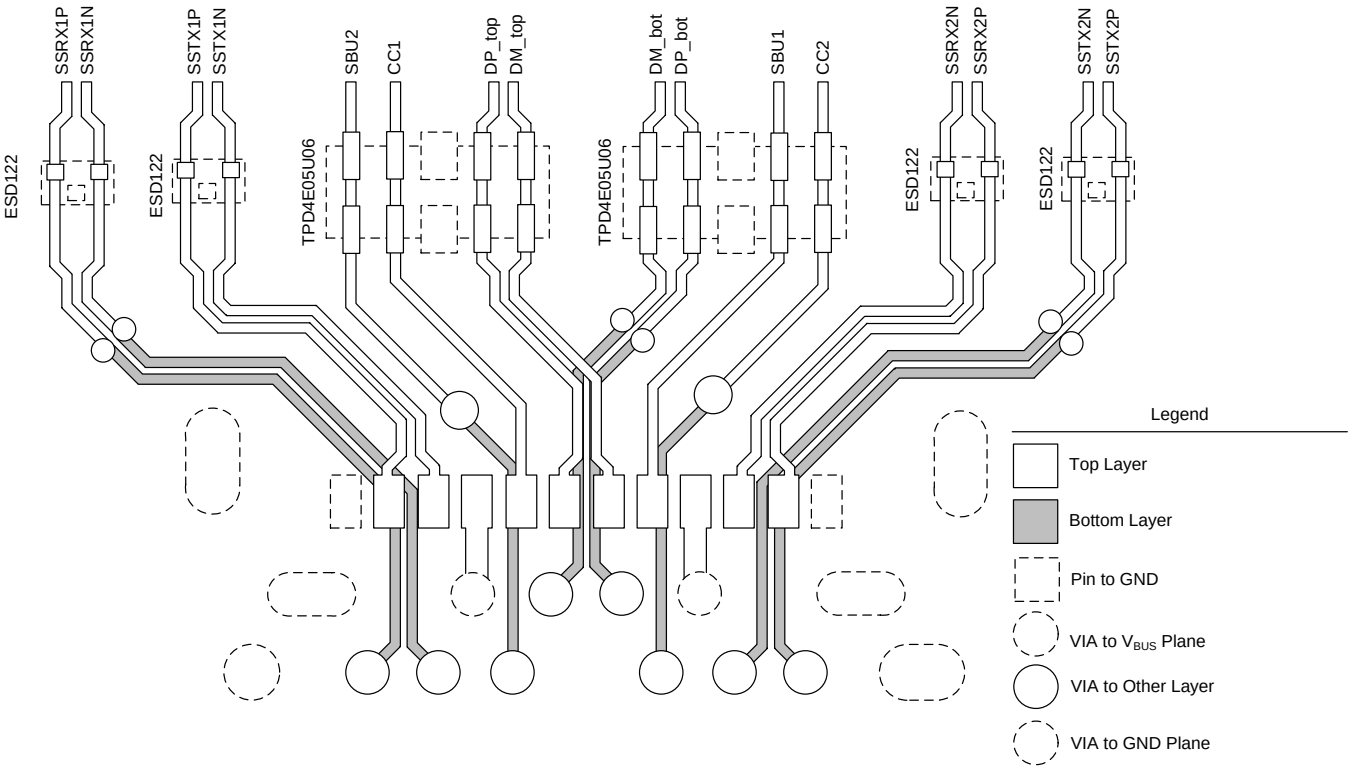


Figure 19. USB 3.1 Gen 2 SuperSpeed Lines Protected by ESD122

Layout Examples (continued)

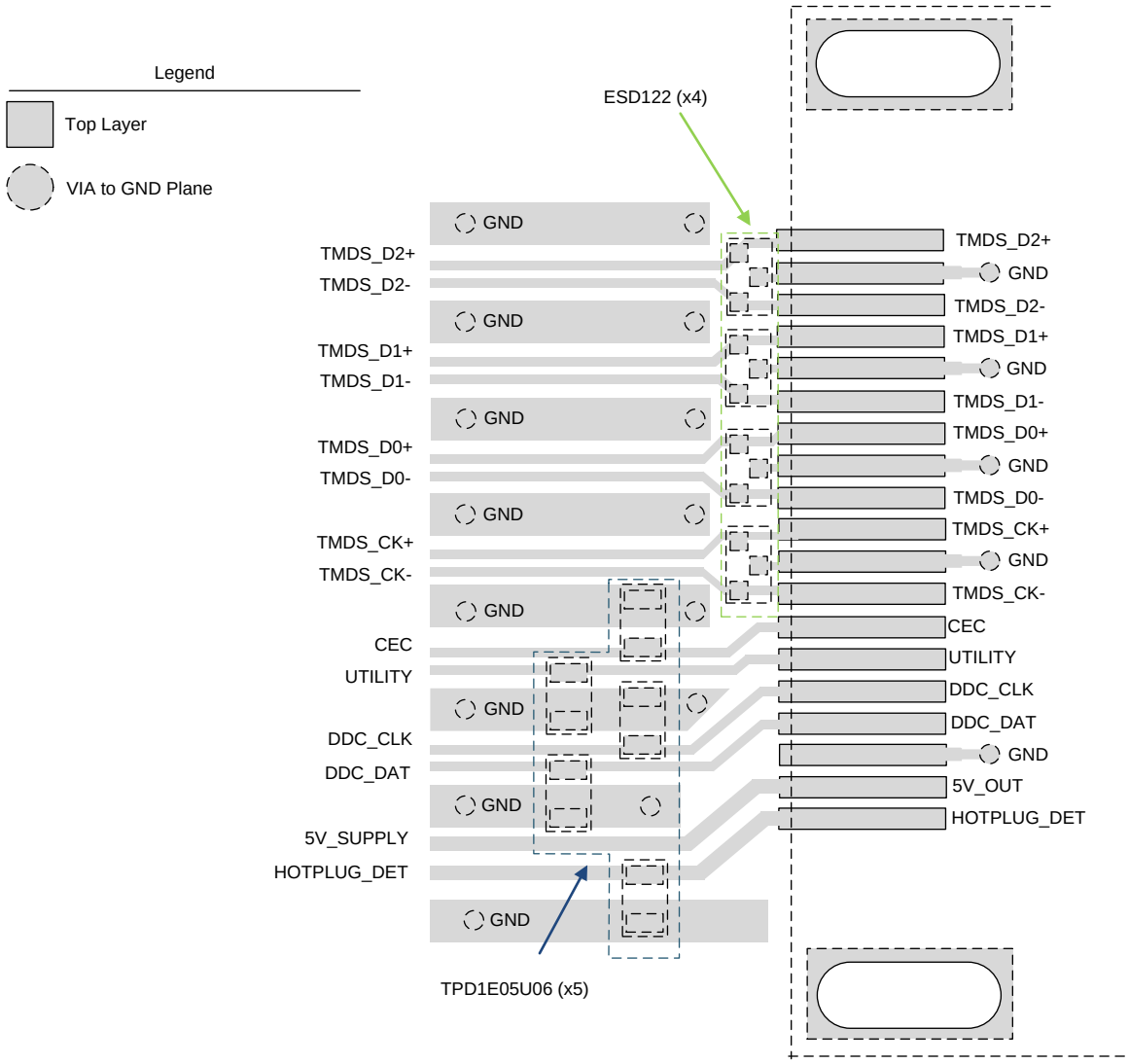


Figure 20. HDMI2_Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

ESD122 Evaluation Module

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
SATA is a trademark of others.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD122DMXR	ACTIVE	X2SON	DMX	3	10000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6U	Samples
ESD122DMYR	ACTIVE	X2SON	DMY	3	10000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	6V	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

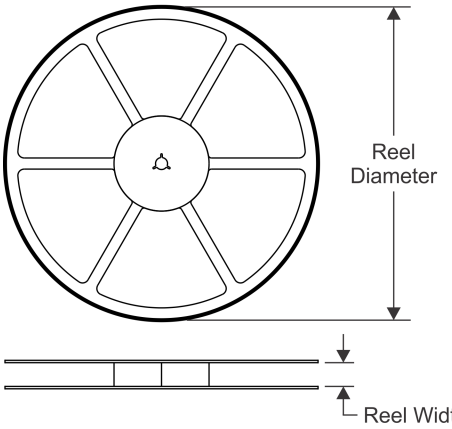
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

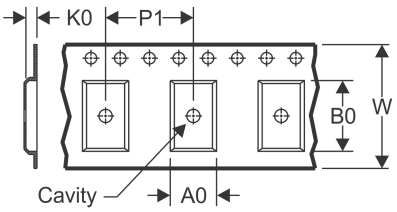
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

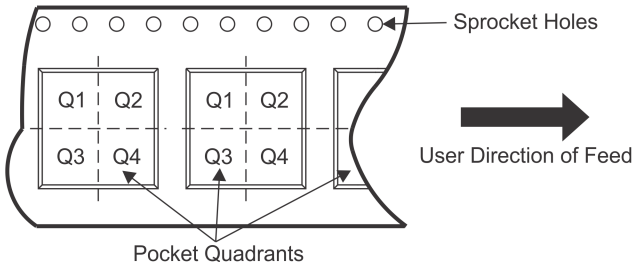


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

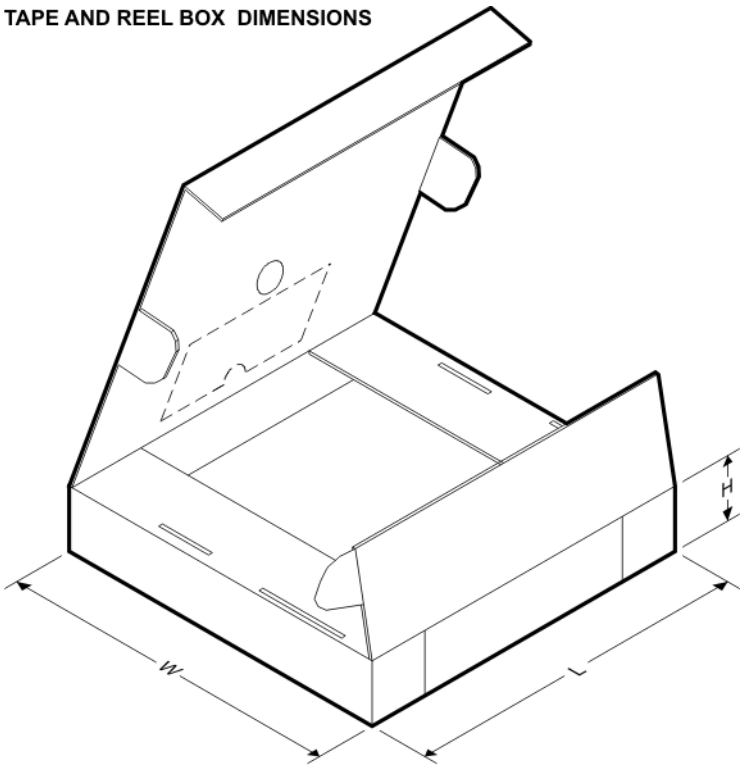
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD122DMXR	X2SON	DMX	3	10000	180.0	9.5	0.72	1.12	0.43	2.0	8.0	Q1
ESD122DMYR	X2SON	DMY	3	10000	180.0	9.5	0.72	1.42	0.43	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

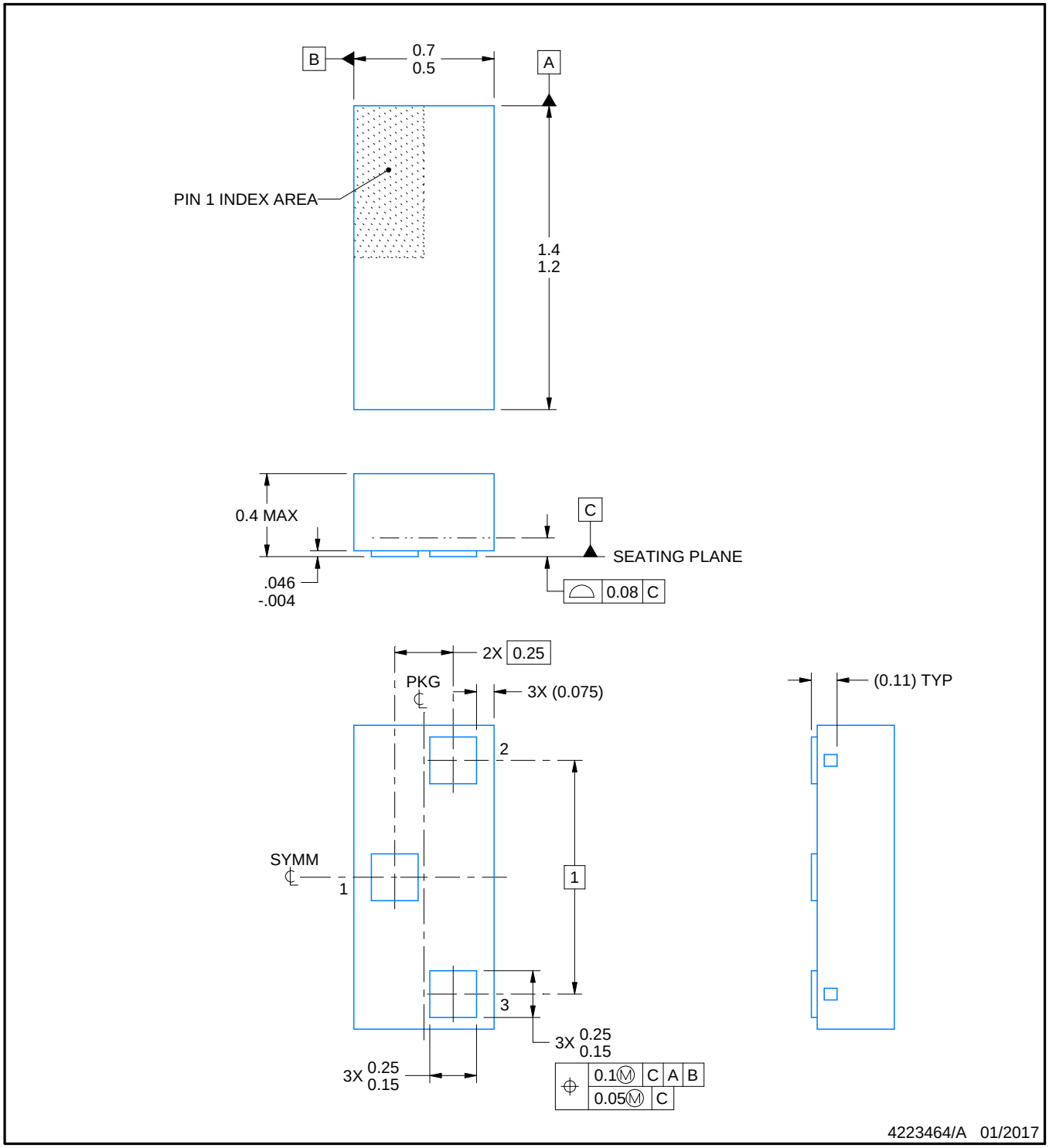
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD122DMXR	X2SON	DMX	3	10000	189.0	185.0	36.0
ESD122DMYR	X2SON	DMY	3	10000	189.0	185.0	36.0

PACKAGE OUTLINE

DMY0003A

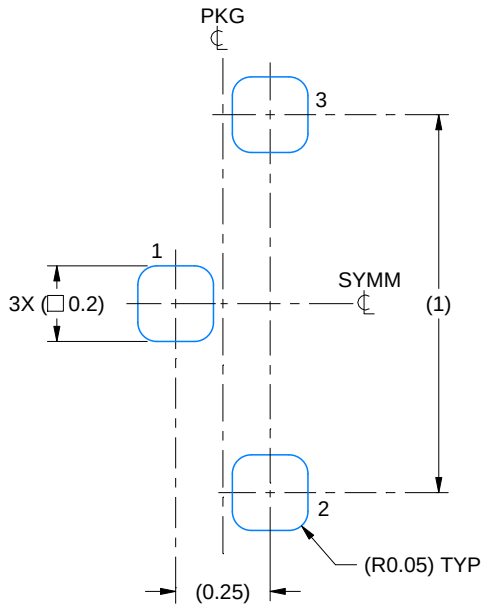
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

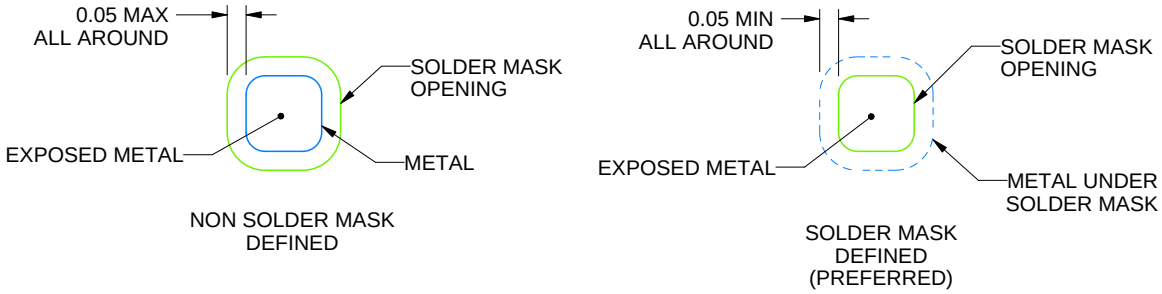


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X

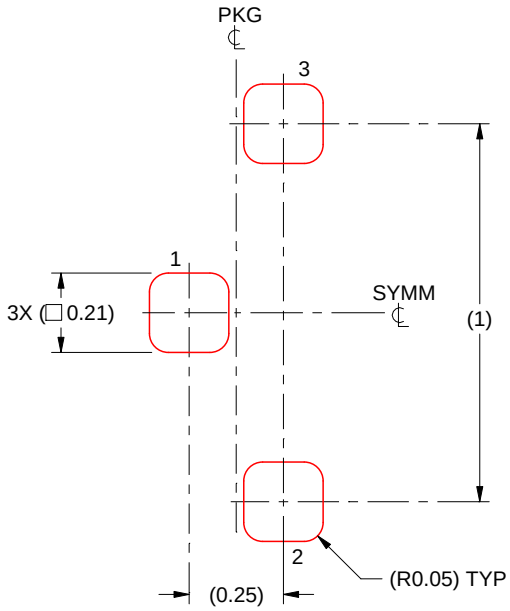


SOLDER MASK DETAILS

4223464/A 01/2017

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271)



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE: 50X

4223464/A 01/2017

NOTES: (continued)

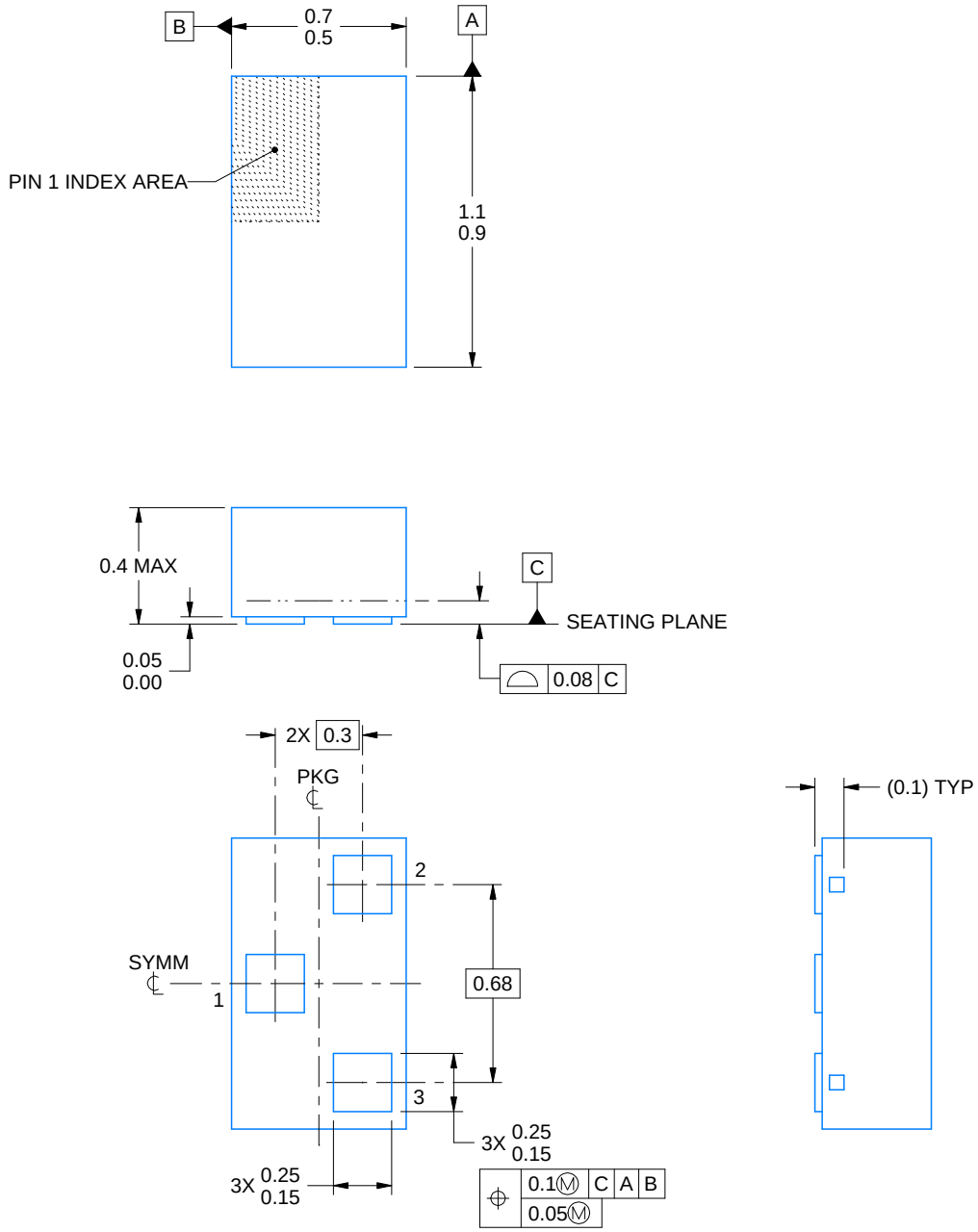
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DMX0003A

X2SON - 0.4 mm max height

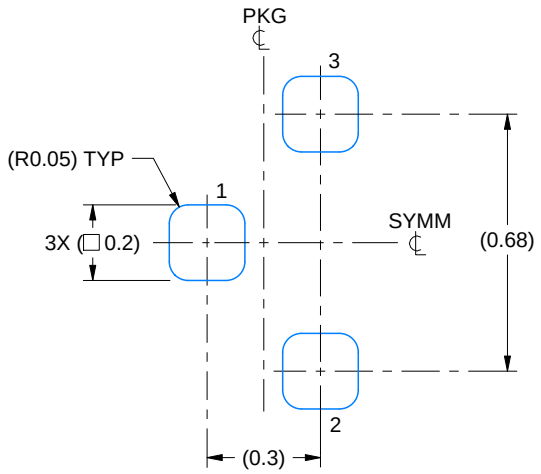
PLASTIC QUAD FLATPACK - NO LEAD



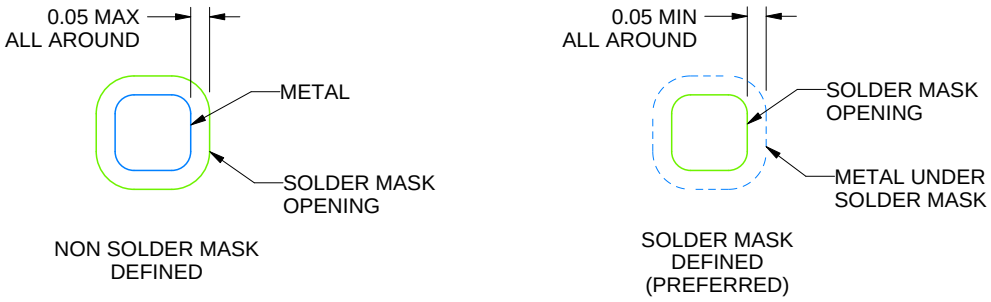
4223380/A 10/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:50X

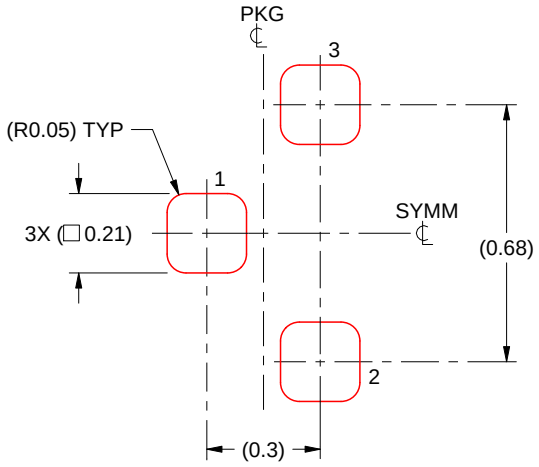


SOLDER MASK DETAILS

4223380/A 10/2016

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:50X

4223380/A 10/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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