PIC24FJ1024GA610/GB610 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ1024GA610/GB610 family devices conform functionally to the current Device Data Sheet (DS30010074**G**),except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ1024GA610/GB610 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A6**).

Data Sheet clarifications and corrections start on page 10, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ1024GA610/GB610 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)				
		A2	A3	A4	A5	A6
PIC24FJ128GA606	6000h	0x02	0x03	0x04	0x05	0x06
PIC24FJ256GA606	6008h					
PIC24FJ512GA606	6010h					
PIC24FJ1024GA606	6018h					
PIC24FJ128GA610	6001h					
PIC24FJ256GA610	6009h					
PIC24FJ512GA610	6011h					
PIC24FJ1024GA610	6019h					
PIC24FJ128GB606	6004h					
PIC24FJ256GB606	600Ch					

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJ1024GA610/GB610 Family Flash Programming Specification"* (DS30010057) for detailed information on Device and Revision IDs for your specific device.

TABLE 1: SILICON DEVREV VALUES (CONTINUED)

Part Number	Device ID[1]	Revision ID for Silicon Revision[2]				
		A2	A3	A4	A5	A6
PIC24FJ512GB606	6014h	0x02	0x03	0x04	0x05	0x06
PIC24FJ1024GB606	601Ch					
PIC24FJ128GB610	6005h					
PIC24FJ256GB610	600Dh					
PIC24FJ512GB610	6015h					
PIC24FJ1024GB610	601Dh					

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.

2: Refer to the *“PIC24FJ1024GA610/GB610 Family Flash Programming Specification”* (DS30010057) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions[1]				
				A2	A3	A4	A5	A6
Power	Low-Voltage Retention Regulator	1.	If a wake-up trigger occurs within 2 µS of entering Retention Sleep, the part may not properly wake from Retention Sleep.	X				
Power	CPU	2.	Part fails to start from power-on when the temperature is below -10ºC and VDD is ≤ 2.7V.	X				
Power	Low-Voltage Retention Regulator	3.	Repeated Wake Retention Sleep cycling can cause the internal LDO to exceed its maximum voltage output specification.	X				
ADC	Charge Injection	4.	At the beginning of conversion, a small current can be injected into the ADC input pin. This will cause a voltage spike dependent on the source resistance.	X	X	X	X	X
I^2C	Slave Addressing	5.	When AHEN (I2CxCONH[1]) = 1, a slave interrupt is asserted for invalid address or software NACK (after 9th clock).	X	X	X	X	X
MCCP/SCCP	Output Compare	6.	Single Edge Output Compare Event Status bit (SCEVT) is not setting for MOD[3:0] = 0010.	X	X	X	X	X
Reset	Trap Conflict	7.	The TRAPR bit is not getting set when a hard trap conflict occurs.	X	X	X	X	X
I^2C	Slave Mode	8.	In 10-Bit Addressing Slave mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence.	X	X	X	X	X
Primary XT Oscillator (POSC)	Primary Oscillator Start-up Timer (OST)	9.	OST may indicate oscillator is ready for use too early.	X	X	X	X	X
Power	Sleep Mode	10.	Sleep current may exceed the value specified in the data sheet.	X	X			
Power	Retention Sleep Mode	11.	When the device wakes up from Retention Sleep mode (RETEN bit (RCON[12]) = 1, $\overline{\text{LPCFG}}$ bit (FPOR[2]) = 0), a device Reset may occur. The BOR, POR and EXTR bits in RCON register are set erroneously for this Reset.	X	X			
I/O	Schmitt Trigger	12.	Schmitt trigger may have glitches for slow signal rise/fall times.	X	X	X		
SPI	Slave Mode	13.	The SRMT bit may be set when the FIFO or Shift register is not empty.	X	X	X	X	X
ADC	Electrical Characteristics	14.	At cold temperatures, ADC characteristics may be beyond the data sheet specification.	X	X	X	X	
Power	BOR	15.	The main BOR may not function.	X	X	X		
I/O	I/O	16.	I/O is not tri-stated if TRISx bit is changed from '0' to '1'.	X	X	X	X	X
ADC	Current	17.	ADC draws additional current when enabled.	X	X	X	X	
Oscillator	96 MHz PLL Mode	18.	PLL in 96 MHz mode may not operate under certain conditions.	X	X	X	X	
Oscillator	Fail-Safe Clock Monitor	19.	When FSCM is enabled and selected clock fails, an oscillator trap may not occur.	X	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**).

1. Module: Power

If a wake-up trigger occurs within 2 µS of entering Retention Sleep, the part may not properly wake from Retention Sleep.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X							

2. Module: Power

Part fails to start from power-on when the temperature is below -10ºC and V_{DD} is ≤ 2.7V.

Work around

Ensure the V_{DD} and AV_{DD} are 2.75V or higher, or that the device will not be exposed to temperatures below -10ºC.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X							

3. Module: Power

Repeated Wake Retention Sleep cycling can cause the internal LDO to exceed its maximum voltage output specification if the VREGS bit (RCON[8]) = 1.

Work around

The code must execute for 1 ms minimum before returning to Retention Sleep mode or VREGS can be set to '0' in the application.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X							

4. Module: ADC

At the beginning of conversion, a small current can be injected into the ADC input pin. This will cause a voltage spike dependent on the source resistance.

Work around

Any of the following solutions can be used:

- Use external buffer on transducer output if the source resistance is greater than 2 kΩ.
- Increase the T_{AD} time to be 1 µS or greater.
- Increase the sample time to be longer than 1 µS.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

5. Module: I^2C

When AHEN (I2CxCONH[1]) = 1, a slave interrupt is asserted for an invalid address or software NACK (after 9th clock).

Work around

User application should ignore the extra interrupt until a Stop condition is seen on the data bus.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

6. Module: MCCP/SCCP

The Single Edge Compare Event Status bit, SCEVT (CCPxSTATL[3]), may not set for Single Edge mode (drive output low on match (MOD[3:0] = 0010)). In this case, the comparator output is still driven low on the first CCPxRA match, but will not be reset by writing '0' to the SCEVT bit.

All MCCPs/SCCPs are affected.

Work around

This mode may be used to trigger a single event before the module must be reinitialized by clearing and setting CCPON (CCP1CON1L[15]).

The Capture/Compare Interrupt Flag (CCPxIF) still occurs on a match with CCPxRA, and can be used to update the user that a compare event has been triggered and the module needs to be reset.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

7. Module: Reset

If a lower priority address error trap occurs while a higher priority oscillator failure trap is being processed, the TRAPR bit (RCON[15]) is not set. A Trap Conflict Reset does not occur as expected and the device may stop executing code.

Work around

None. However, a Reset (such as $\overline{\text{MCLR}}$, POR or WDT) will recover the device.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

8. Module: I^2C

In I^2C Slave 10-Bit Addressing mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit, ACKTIM (I2CxSTAT[13]), is not asserted during an Acknowledgment sequence.

This issue is not seen during the reception of the lower address byte (A7 to A0) and data bytes. The hardware asserts the ACKTIM bit on the falling edge of the eighth clock and deasserts on the rising edge of the ninth clock. In this case, ACKTIM is not asserted on the upper address byte reception.

When AHEN (I2CxCONL[1]) = 1, the clock is stretched after the 8th falling edge and the ACKTIM bit is asserted until the clock is released. If AHEN = 0, the clock is not stretched and ACKTIM is asserted during the Acknowledgment sequence, which is of a very short duration.

Therefore, the user application can see this issue of the ACKTIM bit not getting asserted when AHEN = 1.

Work around

Instead of polling for ACKTIM to be asserted, poll for the RBF flag (I2CxSTAT[1]).

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

9. Module: Primary XT Oscillator (POSC)

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects the XT mode only.

Work around

1. Use HS Primary Oscillator mode.
2. Make sure that the XT Primary Oscillator clock is ready before using it by following these steps:
   a) Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
   b) Provide a delay to stabilize the POSC.
   c) Switch to the POSC source.

Example 1 shows a work around for the device power-on and Example 2 explains the work around when the device wakes from Sleep.

EXAMPLE 1: USING POSC AT POWER-ON

```
#pragma config FNOSC = FRC            // Oscillator Selection bits (Fast RC oscillator (FRC))
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
int     main()
{
    // configure REFO to request POSC
    REFOCONLbits.ROSEL = 2;           // POSC
    REFOCONLbits.ROOUT = 0;           // disable output
    REFOCONLbits.ROEN = 1;            // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout and components
    {   // delay for 9 ms
        unsigned int delayms = 9;
        while(delayms--) asm volatile("repeat #(8000000/1000/2) \n nop");
    }

    // switch to POSC = 2
    __builtin_write_OSCCONH(2);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch
```

EXAMPLE 2: USING POSC WHEN WAKING FROM SLEEP

```
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
    // switch to FRC = 0 before entering sleep
    __builtin_write_OSCCONH(0);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch

    // enter sleep mode
    Sleep();

    // configure REFO to request POSC
    REFOCONLbits.ROSEL = 2;           // POSC
    REFOCONLbits.ROOUT = 0;           // disable output
    REFOCONLbits.ROEN = 1;            // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout and components
    {   // delay for 9 ms
        unsigned int delay ms = 9;
        while(delayms--) asm volatile("repeat #(8000000/1000/2) \n nop");
    }

    // switch to POSC = 2
    __builtin_write_OSCCONH(2);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch
```

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

10. Module: Power

The Sleep current may exceed a value specified in the data sheet. The issue affects regular (non-Retention) Sleep modes.

Work around

Set the RETEN bit (RCON[12]) = 1 and disable the Retention Sleep mode by setting the LPCFG Configuration bit (FPOR[2]) = 1.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X						

11. Module: Power

When the device wakes up from Retention Sleep mode (RETEN bit (RCON[12]) = 1, LPCFG bit (FPOR[2]) = 0), occasionally a device Reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.

Work around

To provide a consistent behavior when the device wakes up from the Retention Sleep mode, the software RESET instruction should be inserted following the SLEEP instruction. In this case, a Reset will always be generated when the device wakes up from Retention Sleep. Example 3 shows the software RESET instruction implementation:

EXAMPLE 3: SOFTWARE RESET AFTER SLEEP INSTRUCTION

```
// ENTER SLEEP MODE.
asm volatile ("pwrsav #0");
// SOFTWARE RESET RIGHT AFTER SLEEP.
asm volatile ("reset");
```

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X						

12. Module: I/O

If the input signal rise or fall time is greater than 200 nS, the I/O Schmitt trigger output may have glitches.

Work around

The rise/fall times must be less than 200 nS.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X					

13. Module: SPI

In SPI Slave mode, the SRMT bit may be set when the TX FIFO or Shift register is not empty.

Work around

The following work arounds can be implemented in the application to detect when the FIFO and Shift register are empty:

1. Check the SPITBF bit before checking the SRMT bit. If the SPITBF flag is cleared and the SRMT flag is set, then all data were transmitted. Example 4 demonstrates the SPITBF and SRMT bits polling.
2. Read the SRMT bit twice, back-to-back. If the SRMT bit is set two reads in a row, then the FIFO and Shift Register are empty. Example 5 demonstrates the SRMT bit polling using double read.

EXAMPLE 4: EMPTY STATUS DETECTION USING SPITBF AND SRMT BITS POLLING

```
// Both flags must indicate empty status.
   while(SPI1STATLbits.SPITBF);
   while(!SPI1STATLbits.SRMT);
```

EXAMPLE 5: EMPTY STATUS DETECTION USING SRMT BIT POLLING WITH BACK-TO-BACK READS

```
// If SRMT bit is set two reads in a row then
it set correctly.
   asm volatile("loop:\n"
                "btsc SPI1STATL, #7\n"
                "btss SPI1STATL, #7\n"
                "bra  loop");
```

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

14. Module: ADC

When the ADC input voltage is above (AVDD – 0.2)V, and the device operates in the temperature range of 0°C to -40°C, the INL and Gain error can get bigger as the ADC input voltage increases, up to -11 LSB Gain and -13 LSB INL.

Work around

Choose the ADC positive reference (VREF+) below (AVDD – 0.2)V. This ensures the ADC input voltage will operate to ADC full scale without affecting the ADC specification.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X				

15. Module: Power

The main BOR may not occur when the operating voltage drops below the BOR trip voltage.

Work around

Ensure the device operating voltage does not violate the specified values. Use an external supervisor circuit to reset the device if the operating voltage can be outside the specified values.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X					

16. Module: I/O

5V tolerant I/Os may not be set to a high-impedance state if the corresponding TRISx bit is changed from '0' to '1'. The I/O state change from output to high-impedance may be delayed up to 100 mS, depending on external connections. On Silicon Revision A5 and later, only the following I/Os are affected by this issue: RA2, RA3, RA14, RA15, RD9, RD10, RE6, RE7, RF4, RF5, RG2 and RG3.

Work around

Set I/O to low level (LATx bit = 0) before switching to input (TRISx bit = 1).

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

17. Module: ADC

On some devices, the current draw may increase when the ADC is enabled. This current draw is not affected by the device Power Save modes or ADC configuration. This additional current does not affect the ADC or device performance.

Work around

Disable the ADC when it is not converting or not used in the application.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X				

18. Module: Oscillator

The PLL in 96 MHz mode may not function when the device starts up and the capacitor on the VCAP pin is discharged. This condition is applicable in both Two-Speed Oscillator Start-up and clock switching at run time.

Work around

1. The 8x/6x/4x PLL modes are functional and available for use.
2. If 96 MHz PLL mode is required for application (ex: USB), connect a 1 µF capacitor between VDD and VCAP to precharge the VCAP capacitor.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X				

19. Module: Oscillator

If a clock failure event occurs when Fail-Safe Clock Monitor (FSCM) is enabled, the oscillator trap may not occur. Instead of the oscillator trap, a clock failure condition can result in instruction misexecution, with other traps or Resets generated.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6			
X	X	X	X	X			

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (30010074**G**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (11/2015)

Initial release of this document; issued for Silicon Revision A2.

Rev B Document (11/2015)

Added data sheet clarification 1 (Device Names and Peripherals).

Rev C Document (3/2016)

Added silicon revision A3.

Removed data sheet clarification 1 (Device Names and Peripherals).

Rev D Document (7/2016)

Added silicon issue 9 (Primary XT and HS Oscillator (POSC)) and silicon issue 10 (Power).

Added data sheet clarifications 1 and 2 (DC Characteristics).

Rev E Document (12/2016)

Added silicon issue 11 (Power).

Removed data sheet clarifications 1 and 2 (DC Characteristics).

Rev F Document (4/2017)

Added Silicon Revision A4.

Added silicon issue 12 (I/O) and silicon issue 13 (SPI).

Added data sheet clarification 1 (Electrical Characteristics).

Rev G Document (7/2017)

Added silicon issues 14 (ADC) and 15 (Power).

Removed data sheet clarification 1 (Electrical Characteristics) because the issue was corrected in the latest data sheet revision.

Rev H Document (3/2018)

Added Silicon Revision A5.

Added silicon issue 16 (I/O).

Rev J Document (1/2019)

Added Silicon issue 17 (ADC).

Added data sheet clarification 1 (Electrical Characteristics).

Rev K Document (7/2019)

Added silicon revision A6.

Added silicon issue 18 (Oscillator).

Rev L Document (2/2020)

Added silicon issue 19 (Oscillator).

Updated silicon issue 9 (Primary XT Oscillator (POSC).

Removed data sheet clarification 1 (Electrical Characteristics) because the issue was corrected in the latest data sheet revision.

NOTES:

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