# TPS4333xEVM

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# 1 Introduction

The Texas Instruments TPS4333xEVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS4333x family of Switch Mode Power Supplies – Multiple-output voltage regulator.

The EVM contains one DC / DC converter (see Table 1).

**Table 1. Device and Package Configurations**

| Converter | IC | Package |
|---|---|---|
| U1 | TPS43330QDAPQ1 | DAP-38 |
| | TPS43332QDAPQ1 | |
| | TPS43335QDAPQ1 | |
| | TPS43336QDAPQ1 | |

# 2 Setup

This section describes the jumpers and connectors on the EVM as well and how to properly connect, set up and use the TPS4333xEVM.

## 2.1 Input/Output Connector Description

**J1 – Input** is the protected power input terminal for the converter with a voltage range from 2V-40V (Boost enabled) or 4V-40V (Boost disabled). The terminal block provides a power ($V_{bat}$) and ground (GND) connection to allow the user to attach the EVM to a cable. harness. The power path provides a series Schottky diode for reverse battery protection.

**J2 – VOUTA** is the output terminal for the TPS4333x buck controller A. The terminal block provides a power (VOUTA) and ground (GND) connection.

**J3 – VOUTB** is the output terminal for the TPS4333x buck controller B. The terminal block provides a power (VOUTB) and ground (GND) connection.

**JP1 – DIV** is the jumper used to select the output voltage for the boost pre-regulator stage. The boost output is 7V when DIV is low, 10V when DIV floating and 11V when DIV is pulled high.

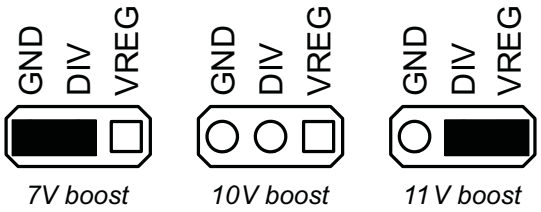



**Figure 1. DIV Jumper Settings**

**JP2 – ENA** is the jumper used to enable buck controller A. The controller will be enabled when the ENA is high and disabled when low.

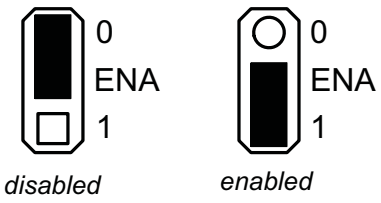



**Figure 2. ENA Jumper Settings**



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**JP3 – ENB** is the jumper used to enable buck controller B. The controller will be enabled when the ENB is high and disabled when low.

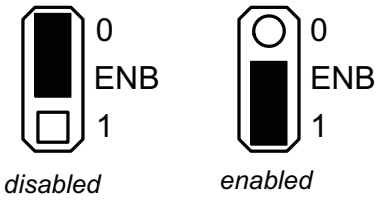



**Figure 3. ENB Jumper Settings**

**JP3 – ENC** is the jumper used to enable the boost pre-regulator. The converter will be enabled when the ENC is high and disabled when low.

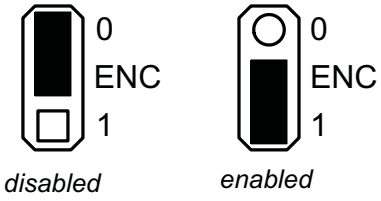



**Figure 4. ENC Jumper Settings**

**JP4 – SYNC** is the external clock input for switching frequency synchronization of the buck converters and to enable Low Power Mode (LPM). The external clock source can be attached to the center pin of JP4. A high logic level on this pin ensures forced continuous mode operation of the buck controllers and inhibits transition to low power mode. An open or low allows discontinuous mode operation, and entry into low power mode at light loads. On the TPS43332 and TPS43336, a high level enables frequency-hopping spread spectrum while an open or a low level disables the spectrum.

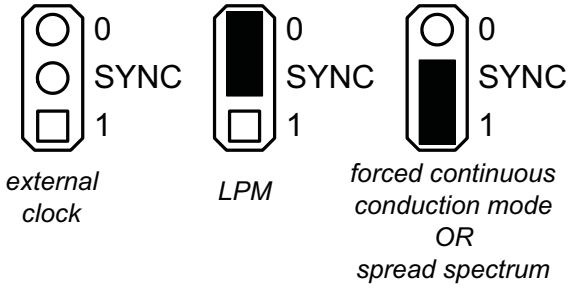



**Figure 5. SYNC Jumper Setting**

**JP5 – RT** is the jumper used to choose the switching frequency of the Buck controllers. The operating frequency can be set to 240 KHz, 400 KHz or 600 KHz.

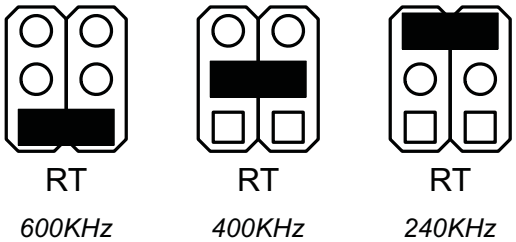



**Figure 6. RT Jumper Setting**


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**JP6 – EXTSUP** is the jumper used to choose one of the Buck output voltages (VOUTA or VOUTB) to provide the internal voltage VREG. If no jumper is plugged, VREG is generated from the input voltage.




*VOUTA selected* *VOUTB selected*

**Figure 7. EXTSUP Jumper Setting**

**Test Points**

| | |
|---|---|
| • DLYAB | Power Good Delay for Buck Controller A and B |
| • DS | Drain-Source Current Sense for Boost FET |
| • GND (x4) | Ground |
| • PGA | Power Good for Buck Controller A |
| • PGB | Power Good for Buck Controller B |
| • PHA | Buck Controller A phase pin |
| • PHB | Buck Controller B phase pin |
| • SSA | Soft Start for Buck Controller A |
| • SSB | Soft Start for Buck Controller B |
| • VBAT | Power Input before the boost regulator stage |
| • VIN | Power Input after the boost regulator stage |
| • VOUTA | Buck Controller A output |
| • VOUTB | Buck Controller B output |

## 2.2 Setup

The input voltage range for the converter is 2 V to 40 V. A load should be applied to the output terminal for proper operation.



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### 2.3 Operation

For proper operation of the TPS43330, DIV, ENA, ENB, ENC, EXTSUP, JP5 (OSC) and SYNC jumpers should be properly configured. The recommended setting, using the switch and shorting blocks.

| | |
|---|---|
| DIV | VREG |
| ENA | enabled |
| ENB | enabled |
| ENC | enabled |
| EXTSUP | A |
| RT | 400KHz |
| SYNC | LPM |

In this configuration, the regulators will turn on when power is applied. DIV selects the output voltage for the Boost pre-regulator stage. ENA, ENB and ENC turn the regulators on or off, disabled or enabled. EXTSUP selects the power supply source for the gate drive. RT sets the switching frequency for the regulators to approximately 240KHz, 400KHz or 600KHz. SYNC enabled LPM or forced continuous conduction mode and is the external clock input for switching frequency synchronization of the buck converters. SYNC will disable spread spectrum operation on the TPS43332 and TPS43336 when set low or left open. The device can be setup to run in low power mode, to reduce the quiescent operating current, by connecting the Sync test point to ground. Low power mode will allow the device to switch into a PFM mode of operation if the load current demand is low. It will automatically switch back to PWM mode as the load current increases.

| Regulator | Output Voltage | Maximum Output Current |
|---|---|---|
| Buck Controller A: | 5 V | 2A |
| Buck Controller B: | 3.3 V | 4A |

If jitter is observed on the phase signal of the regulator, then noise may be entering the feedback interface and a capacitive filter may be required. The EVM provides a footprint across the low-side feedback resistors to add these capacitors, if needed. A capacitor has been added across the low-side resistor on the EVM. Typically 47pF to 100pF is sufficient to filter any noise issues.

## 3 Board Layout

Figure 8, through Figure 11 show the board layout for the TPS43330EVM PWB.

The TPS43330 controller offers high efficiency, but does dissipate power. The PowerPAD™ package offers an exposed thermal pad to enhance thermal performance. This must be soldered to the copper landing on the PCB for optimal performance. The PCB provides 2 oz copper planes on the top and bottom to dissipate heat


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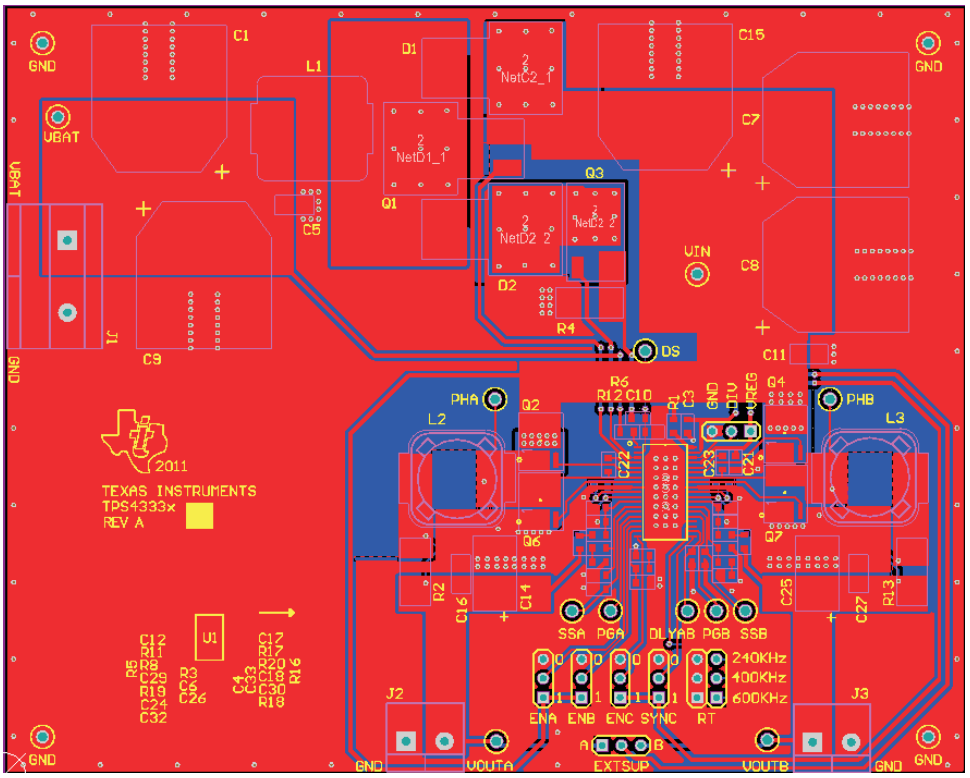



**Figure 8. Top Assembly Layer**

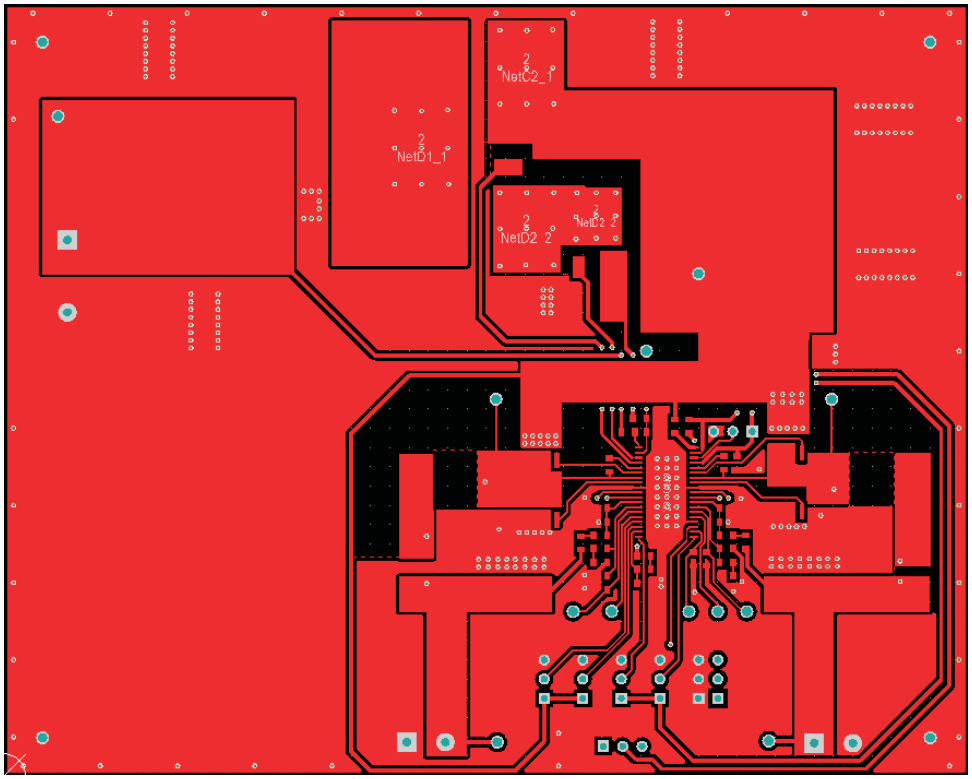



**Figure 9. Top Layer Routing**



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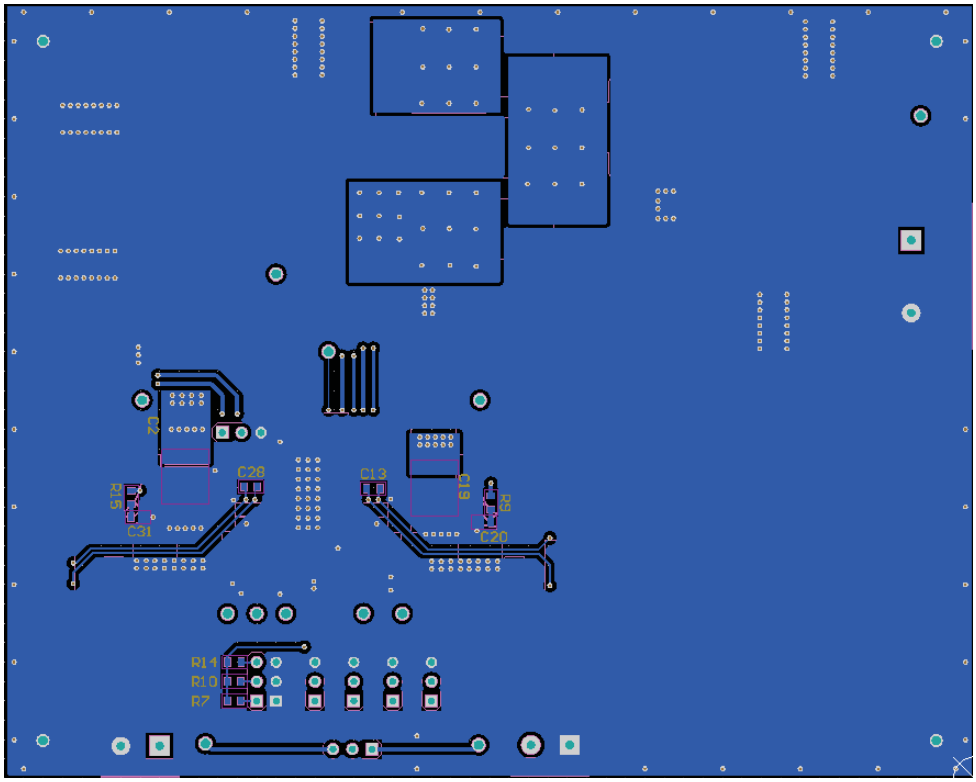



**Figure 10. Bottom Assembly Layer**

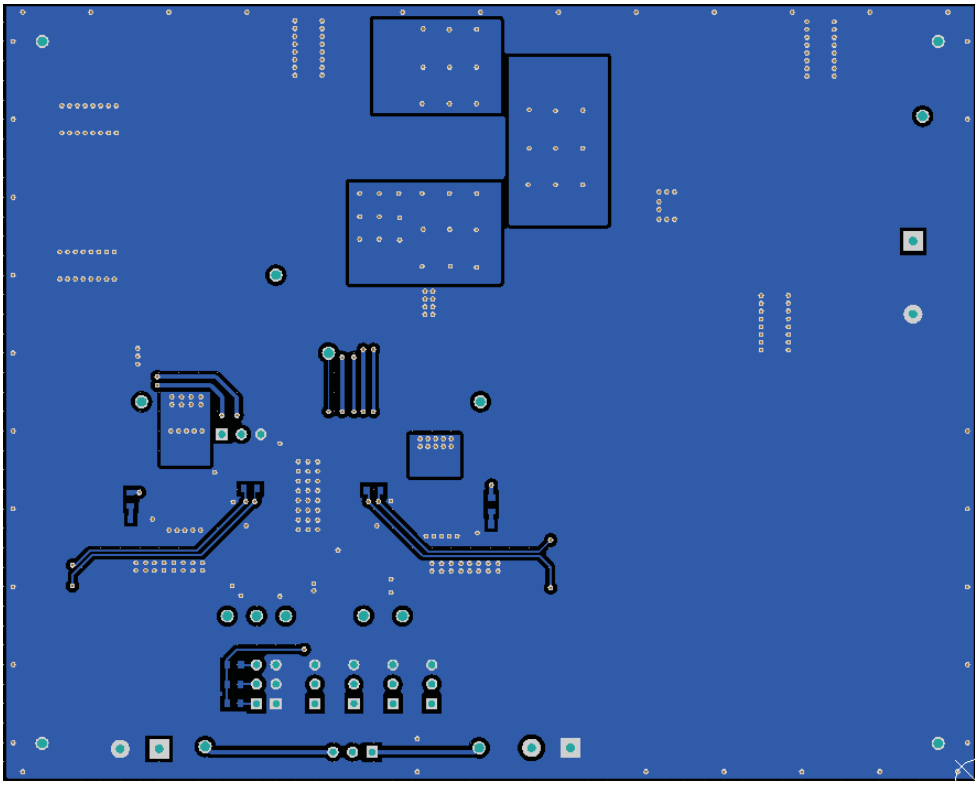


**Figure 11. Bottom Layer Routing**


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# 4 Schematic and Bill of Materials

## 4.1 Schematic

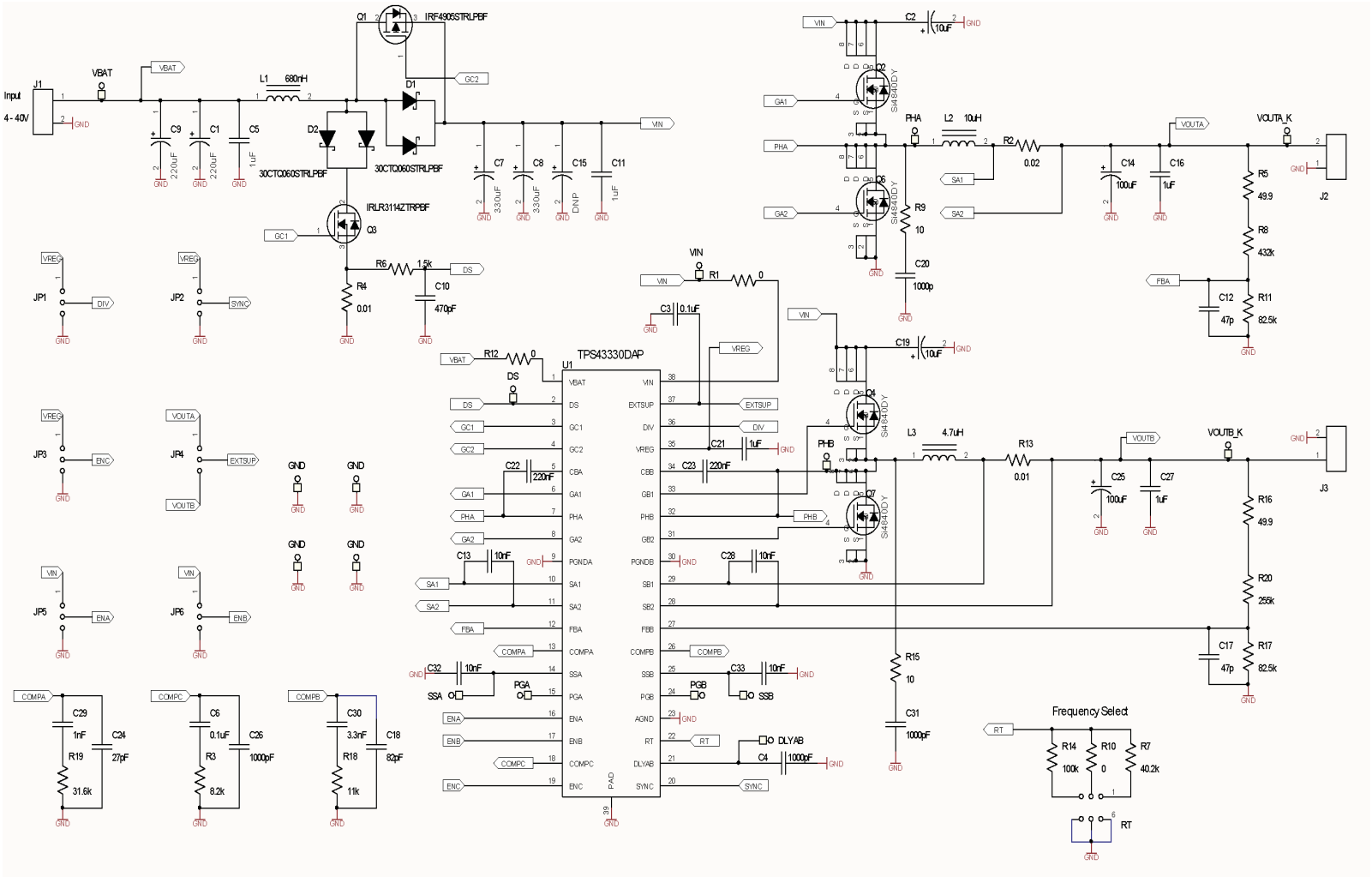



**Figure 12. TPS4333xEVM Schematic**



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## 4.2 Bill of Materials

**Table 2. TPS4333xEVM Bill of Materials**

| COUNT | REF DES | DESCRIPTION | SIZE | MFR | PART NUMBER |
|---|---|---|---|---|---|
| 2 | C1, C9 | Capacitor, electrolytic, 220uF, 50V, 20% | G | Panasonic | EEE-FK1H221P |
| 2 | C2, C19 | Capacitor, ceramic, 10uF, 50V, 10% | 2220 | TDK | C5750X7R1H106M |
| 2 | C3, C6 | Capacitor, ceramic, 0.1uF, 50V, 10% | 603 | Std | Std |
| 5 | C4, C20, C26, C29, C31 | Capacitor, ceramic, 1000pF, 50V, 10% | 603 | Std | Std |
| 2 | C5, C11 | Capacitor, ceramic, 1uF, 100V, 10% | 1206 | Std | Std |
| 2 | C7, C8 | Capacitor, electrolytic, 330uF, 50V, 20% | H13 | Panasonic | EEV-FK1H331Q |
| 1 | C10 | Capacitor, ceramic, 470pF, 50V, 10% | 603 | Std | Std |
| 2 | C12, C17 | Capacitor, ceramic, 47pF, 50V, 10% | 603 | Std | Std |
| 4 | C13, C28, C32, C33 | Capacitor, ceramic, 0.01uF, 50V, 10% | 603 | Std | Std |
| 2 | C14, C25 | Capacitor, tantalum, 100uF, 16V, 10% | 7343 | AVX | TPSD107K016R0060 |
| 1 | C15 | Do not populate | | | |
| 3 | C16, C21, C27 | Capacitor, ceramic, 1uF, 16V, 10% | 603 | Std | Std |
| 1 | C18 | Capacitor, ceramic, 82pF, 50V, 10% | 603 | Std | Std |
| 2 | C22, C23 | Capacitor, ceramic, 220nF, 50V, 10% | 603 | Std | Std |
| 1 | C24 | Capacitor, ceramic, 27pF, 50V, 10% | 603 | Std | Std |
| 1 | C30 | Capacitor, ceramic, 3.3nF, 50V, 10% | 603 | Std | Std |
| 2 | D1, D2 | Diode, Schottky, 15A, 60V | D2PAK | Vishay | 30CTQ060STRLPBF |
| 1 | J1 | Terminal block, 2-pin, 25A | 9.52MM | OST | OSTT7022150 |
| 2 | J2, J3 | Terminal block, 2-pin, 15A | 2 x 5.1mm | OST | OSTTA024163 |
| 6 | JP1, JP2, JP3, JP4, JP5, JP6 | Header, 3-pin, 100-mil spacing | 0.100 x 3 | Sullins | PEC03SAAN |
| 1 | RT | Header, 6-pin, 100-mil spacing | 0.100 x 3 | Sullins | PEC06DAAN |
| 7 | JP1, JP2, JP3, JP4, JP5, JP6, RT | Connector jumper, shorting, 100-mil spacing | 0.1 | Sullins | SPC02SYAN |
| 1 | L1 | Inductor, SMT, 0.68uH, 28A | 13.2mm x 12.9mm | Vishay | IHLP5050CEERR68M01 |
| 1 | L2 | Inductor, SMT, 10-uH, 6.04A | 12.3mm x 12.3mm | Coilcraft | MSS1278T-103ML |
| 1 | L3 | Inductor, SMT, 4.7-uH, 4.3A | 12.3mm x 12.3mm | Coilcraft | MSS1278T-472ML |
| 1 | Q1 | MOSFET P-CH 55V 42A | D2PAK | IR | IRF4905STRLPBF |
| 4 | Q2, Q4, Q6, Q7 | MOSFET, n-channel | SOIC | Vishay | SI4840DY |
| 1 | Q3 | MOSFET, n-channel | DPAK | IR | IRLR3114ZTRPBF |
| 3 | R1, R10, R12 | Resistor, chip, 0-ohms, 1/16W, 5% | 603 | Std | Std |


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**Table 2. TPS4333xEVM Bill of Materials (continued)**

| COUNT | REF DES | DESCRIPTION | SIZE | MFR | PART NUMBER |
|---|---|---|---|---|---|
| 1 | R2 | Resistor, chip, 0.02-ohm, 2W | 2512 | Stackpole | CSRN2512FK20L0 |
| 1 | R3 | Resistor, chip, 8.2-kohms, 1/16W, 1% | 603 | Std | Std |
| 2 | R4, R13 | Resistor, chip, 0.01-ohm, 2W | 2512 | Stackpole | CSRN2512FK10L0 |
| 2 | R5, R16 | Resistor, chip, 49.9-ohms, 1/16W, 1% | 603 | Std | Std |
| 1 | R6 | Resistor, chip, 1.5-kohms, 1/16W, 1% | 603 | Std | Std |
| 1 | R7 | Resistor, chip, 40.2-kohms, 1/16W, 1% | 603 | Std | Std |
| 1 | R8 | Resistor, chip, 432-kohms, 1/16W, 1% | 603 | Std | Std |
| 2 | R9, R15 | Resistor, chip, 10-ohms, 1/16W, 1% | 603 | Std | Std |
| 2 | R11, R17 | Resistor, chip, 82.5-kohms, 1/16W, 1% | 603 | Std | Std |
| 1 | R14 | Resistor, chip, 100-kohms, 1/16W, 1% | 603 | Std | Std |
| 1 | R18 | Resistor, chip, 11-kohms, 1/16W, 1% | 603 | Std | Std |
| 1 | R19 | Resistor, chip, 31.6-kohms, 1/16W, 1% | 603 | Std | Std |
| 1 | R20 | Resistor, chip, 255-kohms, 1/16W, 1% | 603 | Std | Std |
| 16 | DLYAB, DS, GND (x4), PGA, PGB, PHA, PHB, SSA, SSB, VBAT, VIN, VOUTA_K, VOUTB_K | Test point, 52-mil | 0.052 | Std | Std |
| 1 | U1 | IC,<br>TPS43330DAPRQ1 or<br>TPS43332DAPRQ1 or<br>TPS43335DAPRQ1 or<br>TPS43336DAPRQ1 | | TI | TPS43330-Q1or<br>TPS43332-Q1 or<br>TPS43335-Q1 or<br>TPS43336-Q1 |
| | - | PCB, 5-inch x 4-inch x 0.062 | | Any | TPS4333X, REV A |


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It is important to operate this EVM within the input voltage range of 2 V to 40 V (Boost enabled) or 4V to 40 V (Boost disabled) and the output voltage range of 9 V to 11 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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