TEXAS INSTRUMENTS

Application Report
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PGA411-Q1 PCB Design Guidelines

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ABSTRACT

The PGA411-Q1 device is a resolver-to-digital converter, with an integrated exciter-amplifier, boost-converter power supply, that is capable of both exciting and reading the sine and cosine output from a resolver sensor.

This document presents several guidelines for designing a PGA411-Q1 based PCB and includes recommendations for device placement and proper layout.

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1 Overview

The PGA411-Q1 device is a resolver-sensor interface device with an integrated exciter amplifier and boost-converter power supply. The PGA411-Q1 device is capable of running with either 10-bit or 12-bit resolution. The internal, boost-converter power supply for the exciter can operate in the range of 10 V to 17 V (typical) which enables the exciter output to be adjustable between 4Vrms or 7Vrms mode.

The integrated exciter amplifier provides up to 145 mA of excitation current with an exciter frequency from 10 kHz to 20 kHz. The integration of the exciter amplifier and boost supply with protection in the PGA411-Q1 device enables space reductions on the printed circuit board (PCB) because of the elimination of most external components.

This application report is a complementary document and is not intended to replace the device data sheet. As a result, system designers should still reference all relevant device data sheets and application materials during system-level design to facilitate development of the highest-quality end product.

The guidelines presented in this document are based on Texas Instruments' reference platforms and general design recommendations. Follow these rules to avoid unnecessary mistakes that can result in multiple PCB spins and delay time-to-market of the end product.

For questions or issues that arise during the layout process, go to TI's E2E™ online community, e2e.ti.com.

Figure 1 shows the block diagram of the PGA411-Q1 device.

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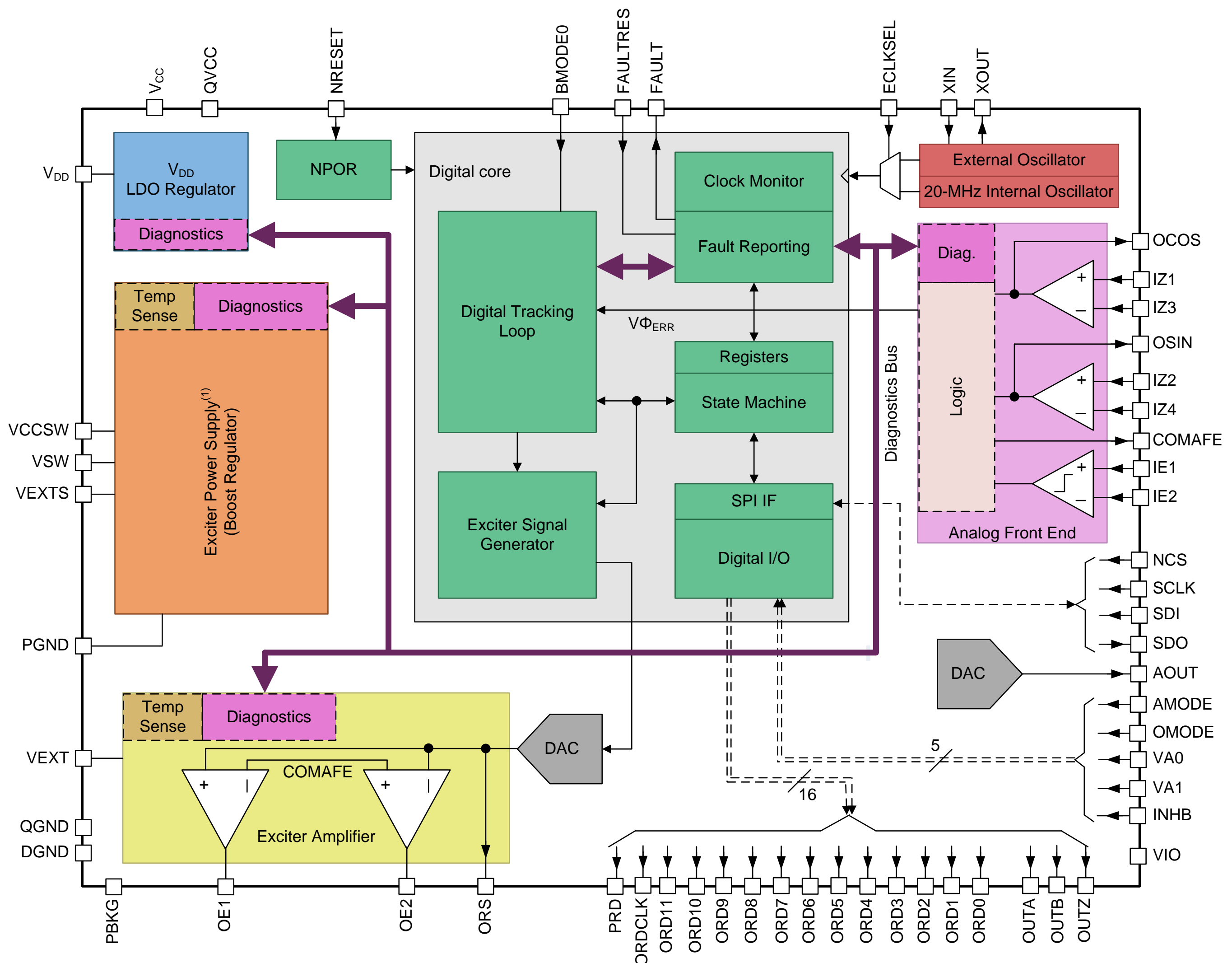

Figure 1. Block Diagram of PGA411-Q1

2 Layout Stack Up

The PCB used for the following reference design has four layers and is fabricated with FR-4 material. The four layers are defined as follows:

Top layer — This layer is generally used for the analog and digital signals.

Mid layer 1 — This layer is assigned to both the analog and digital ground planes.

Mid layer 2 — This layer is assigned to the power-supply nets.

Bottom layer — This layer is assigned to the digital signals and analog ground plane.

The ground planes and power nets are predominately on the inner layers and partly on the bottom layer. These layers help with shielding and making signal traces available for probing, allow for making modifications on the top and bottom layers, and provide the advantage of distributed capacitance between the power and ground trace.

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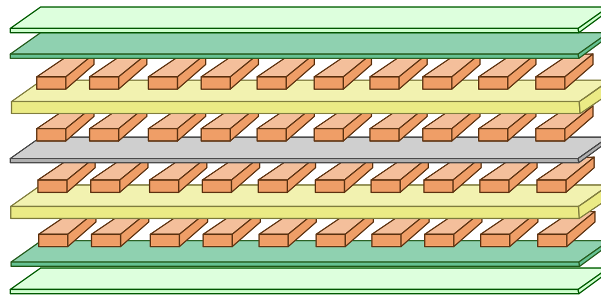

Figure 2. Board Stack Up

Table 1. Board Stack Up

Layer Name	Type	Material	Thickness
Top overlay	Service print	—	—
Top solder	Solder mask	Surface material	0.03 mm
Top layer	Signal layer	Copper	0.018 mm (0.035 mm after galvanic plating)
Dielectric 1	Dielectric	Prepreg	0.3 mm
Signal layer 1	Signal layer	Copper	0.035 mm
Dielectric 3	Dielectric	Prepreg	0.71 mm
Signal layer 2	Signal layer	Copper	0.035 mm
Dielectric 2	Dielectric	Prepreg	0.3 mm
Bottom layer	Signal layer	Copper	0.018 mm (0.035 mm after galvanic plating)
Bottom solder	Solder mask	Surface material	0.03 mm
Bottom overlay	Service print	—	—

The exposed power pad on the backside of the PGA411-Q1 package must be soldered to the PCB ground. Ensure that a sufficient amount of thermal vias [1] are placed directly under the IC, connecting to the ground plane on the other layers. The PCB file used for this guide will be available on the TIDA-00796 tool folder . For more information, go to the PGA411-Q1 product folder (www.ti.com/product/PGA411-Q1).

(1) For more information, see the *PowerPAD™ Thermally Enhanced Package* application report (SLMA002).

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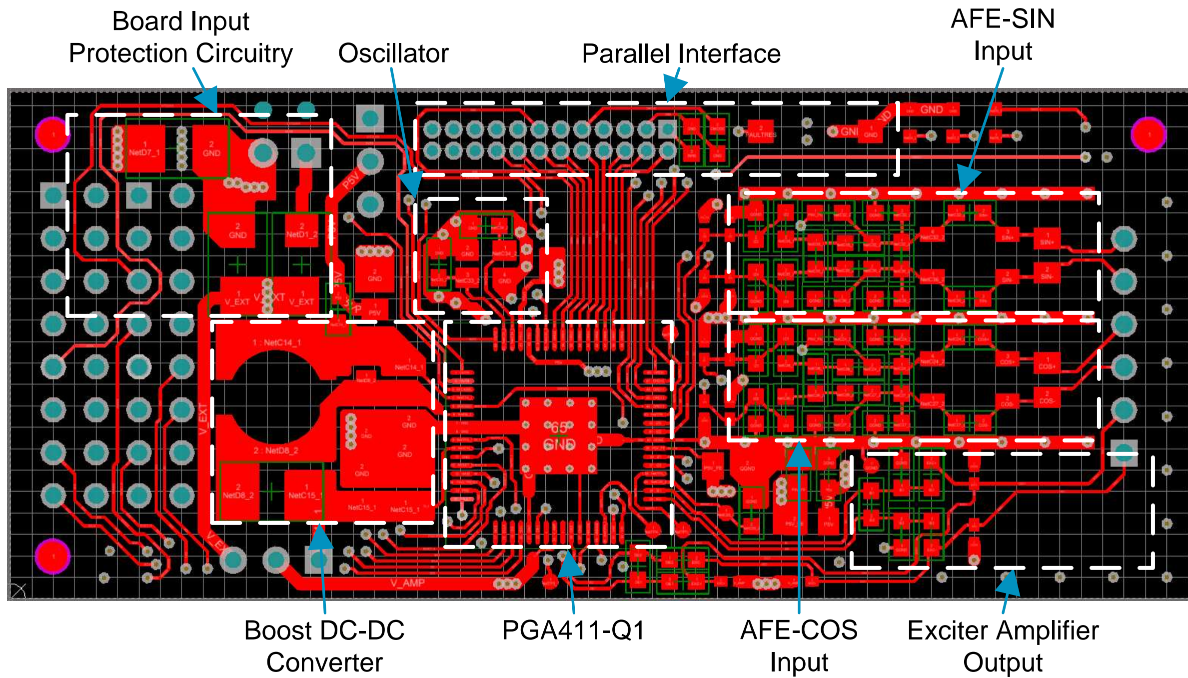

Figure 3. Top Layer

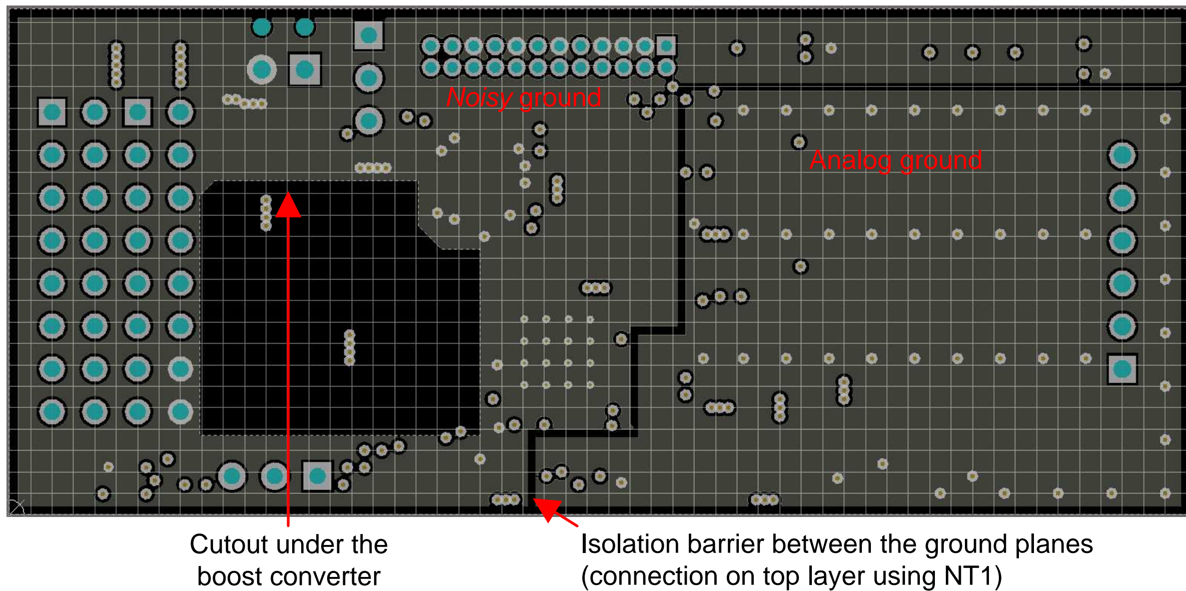

Figure 4. Mid Layer 1

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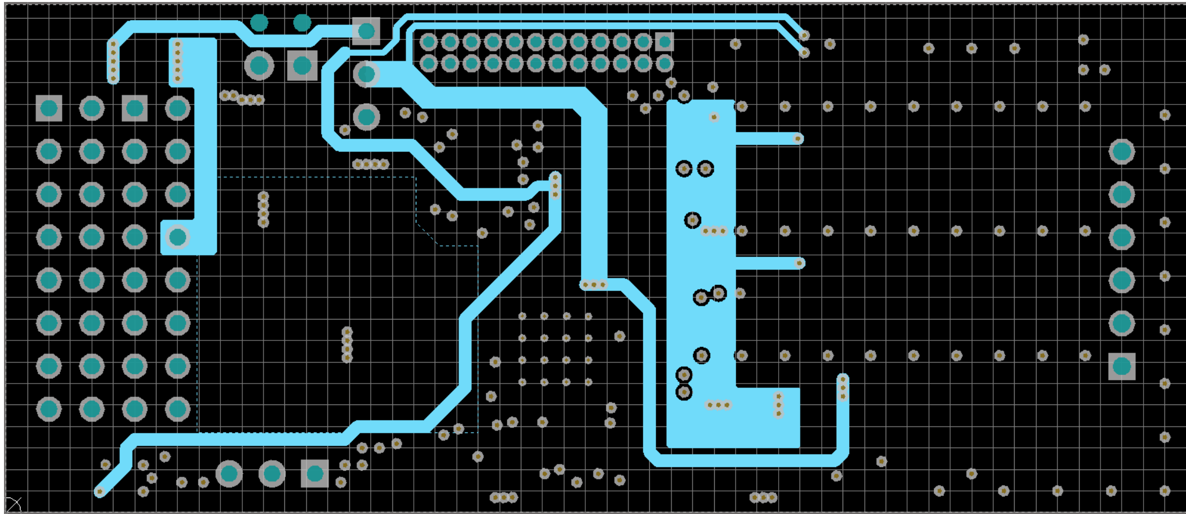

Figure 5. Mid Layer 2

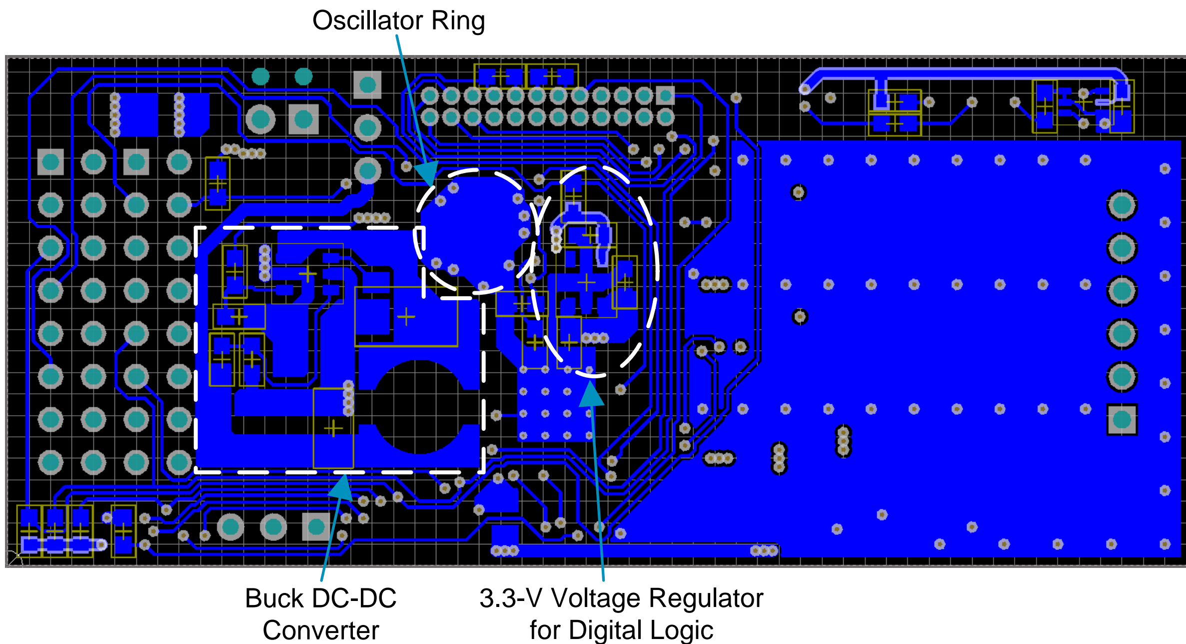

Figure 6. Bottom Layer

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3 Reference Planes

3.1 Power (QVCC, V_{CC}, and V_{DD}) and Ground (PGND, DGND, and QGND) Planes

The decoupling capacitors should be placed next to the IC pins. The trace connection should be as short as possible. Refer to Figure 7 for the correct placement of the decoupling capacitors between a low-noise ground and the 5-V supply.

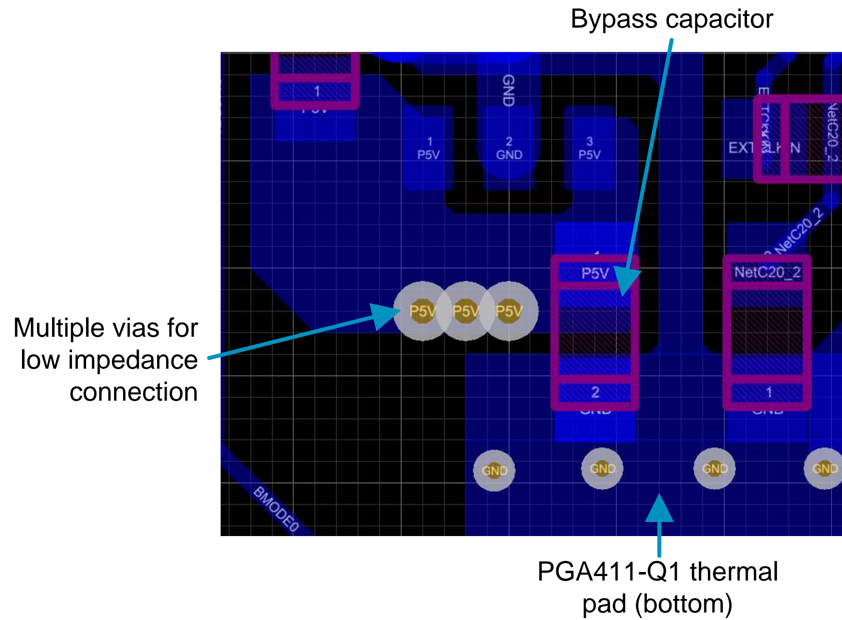

Figure 7. Bypass Capacitor Example

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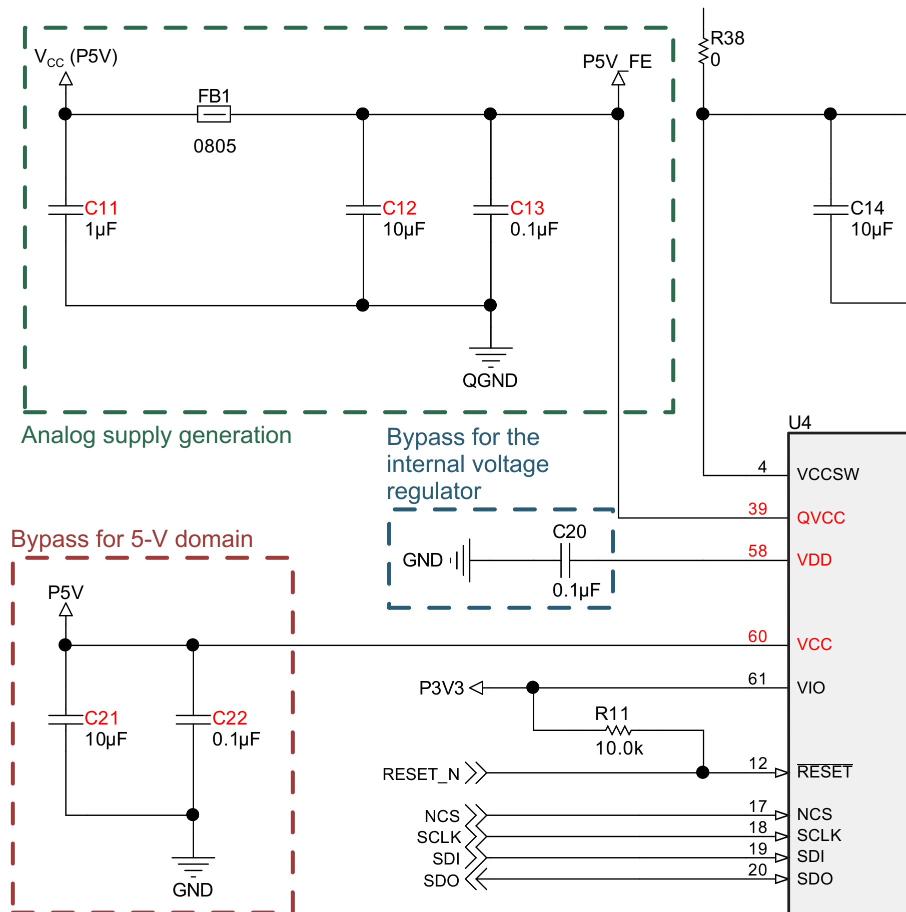

Figure 8. Power Supply Generation for the PGA411-Q1

NOTE: The AFE is referenced to the quiet ground pin (QGND) and powered by the quiet voltage supply pin (P5V_FE). The supply for the QVCC pin must go high at the same time as V_{CC} for normal operation of the device. TI recommends tying QVCC to V_{CC} with additional local capacitance to filter further noise from being introduced.

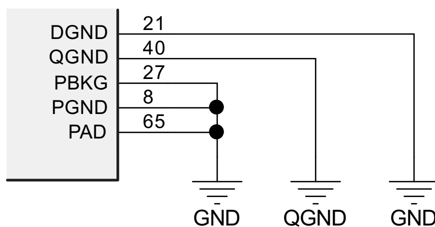

Figure 9. PGA411-Q1 Ground Connections

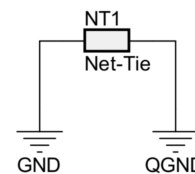

Figure 10. Star Ground Connection Using Net Tie (NT1)

Separate the grounding for the analog and digital portions of circuitry for the best noise suppression.

Use of a star-ground topology technique is recommended for connecting the grounds (see Figure 10). An ideal location for the ground reference point is the thermal pad. Figure 11 shows the implementation for the TIDA-00796 reference design.

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Route the analog ground separately from the power ground. Connect the analog ground and connect the power ground separately. Connect the analog ground and power ground together using the PowerPAD™ as the single ground connection point or using a 0-Ω resistor to tie the analog ground to the power ground (the PowerPAD should tie to the analog ground in this case, if possible). In this case, Net Tie (NT1) connects the *noisy* power ground, PGND and the digital ground, GND, (refer to Figure 9) to the *quiet* ground plane, QGND (refer to Figure 10). These two ground planes only connect at one point as shown in Figure 11.

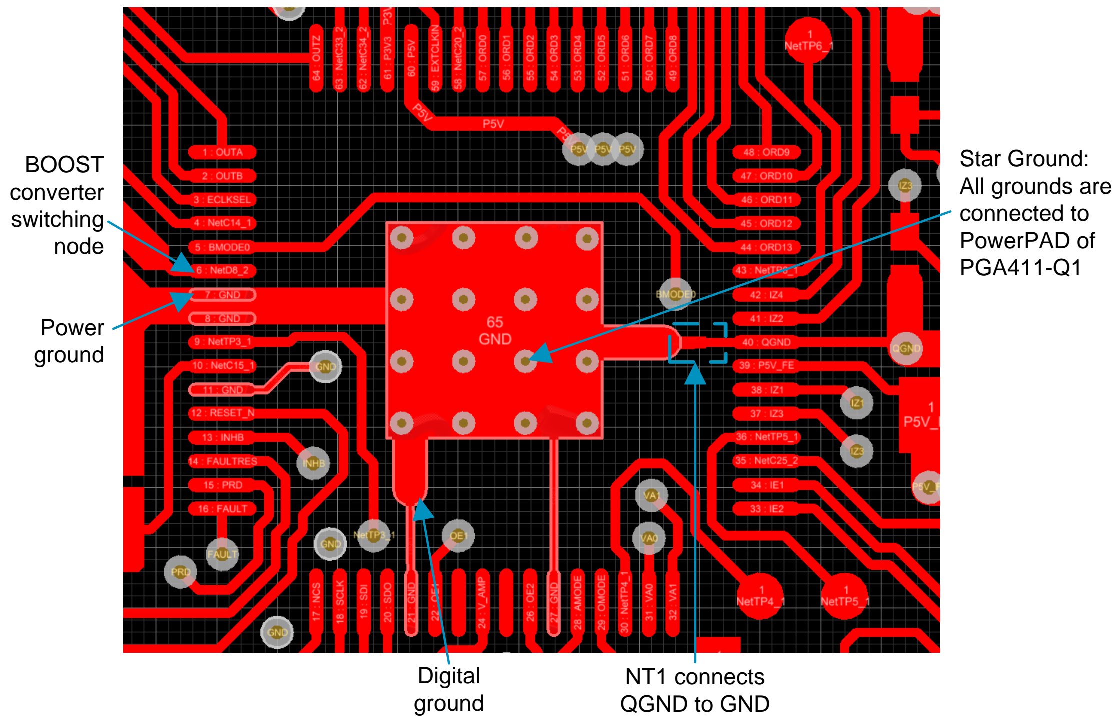

Figure 11. Star Ground Technique for PGA411-Q1

Figure 12 shows a filter for the analog supply pin (QVCC). All filter components are referenced to QGND.

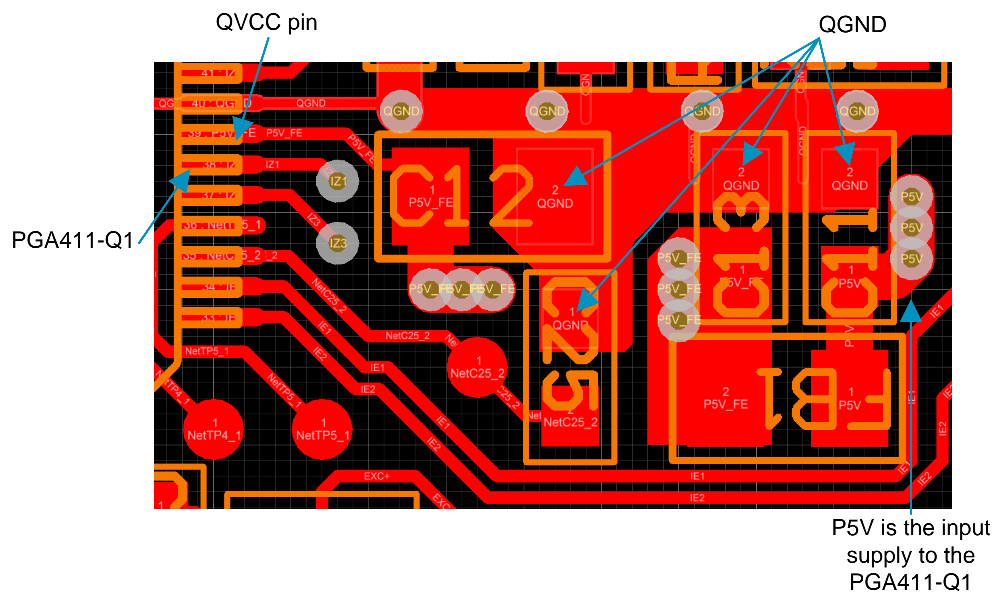

Figure 12. Analog Filter layout

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QVCC (P5V_FE) is generated as shown in Figure 13 from V_{CC} (P5V). A ferrite bead (FB1) with three capacitors forms a filter (refer to Figure 13).

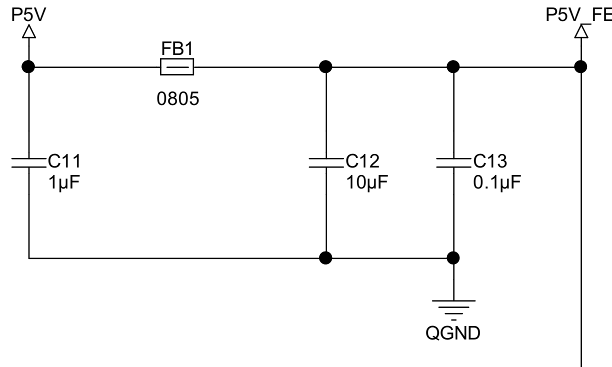

Figure 13. Analog Supply

Refer to Figure 8 for the component schematic that highlights C11, C12, C13, and FB1.

4 Boost-Converter Power Supply (for the Exciter)

Figure 14 shows a boost-converter circuit for the exciter amplifier.

- Identify traces with fast current transients which is very important to mitigate EMI.
- Keep these traces as short as possible which is very important to mitigate EMI.
- Place the input capacitor as close as possible to supply and ground connections of the switching MOSFET and use the shortest possible copper trace connection.
- Place these components on the same PCB layer instead of on different layers.
- Keep all nets for a DC-DC converter in one signal layer. Figure 15 shows an example of such a solution. Because the highest transient occurs at the off time, t_{off}, the C15 capacitor helps reduce high-frequency content while the C16 capacitor serves as the energy storage.
- Use the D11 diode for optional protection for the internal switch (usually not needed).
- Add shielding if necessary.

The boost-converter power supply implements spread spectrum (f_{SW} is 410 kHz ±10%). For more information refer to the PGA411-Q1 data sheet, SLASE76.

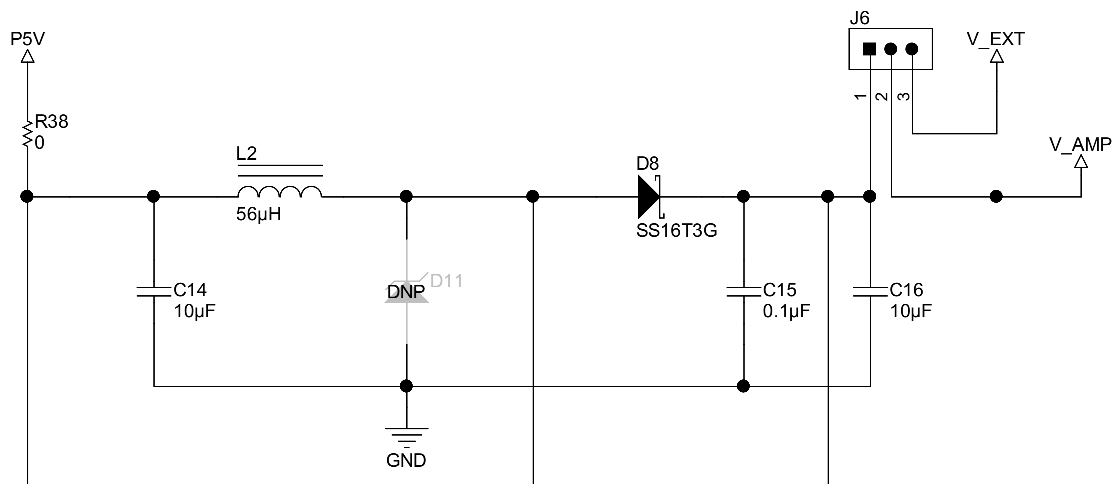

Figure 14. Boost Converter for the Exciter Amplifier

Figure 15 provides a layout example for the boost-converter power supply.

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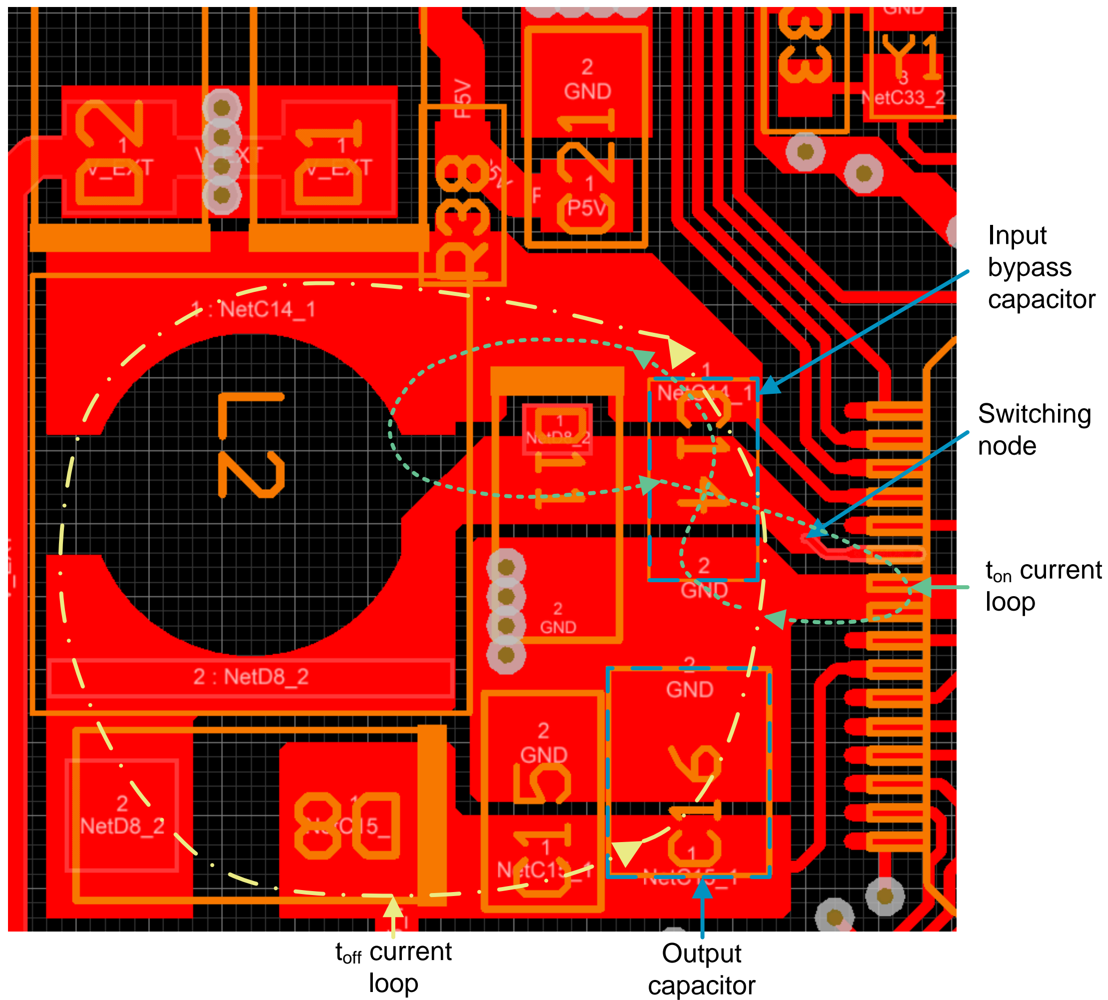

Figure 15. Layout Example for the Boost DC-DC Converter

In this board, a cutout was created underneath the boost converter to isolate any noise from the boost circuit to that could be coupled to other planes. A keep-out was kept in all the layers below the boost circuit (as shown in Figure 4). This keep-out helps isolate the noise coupling to the other grounds and circuits.

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5 Analog Front End

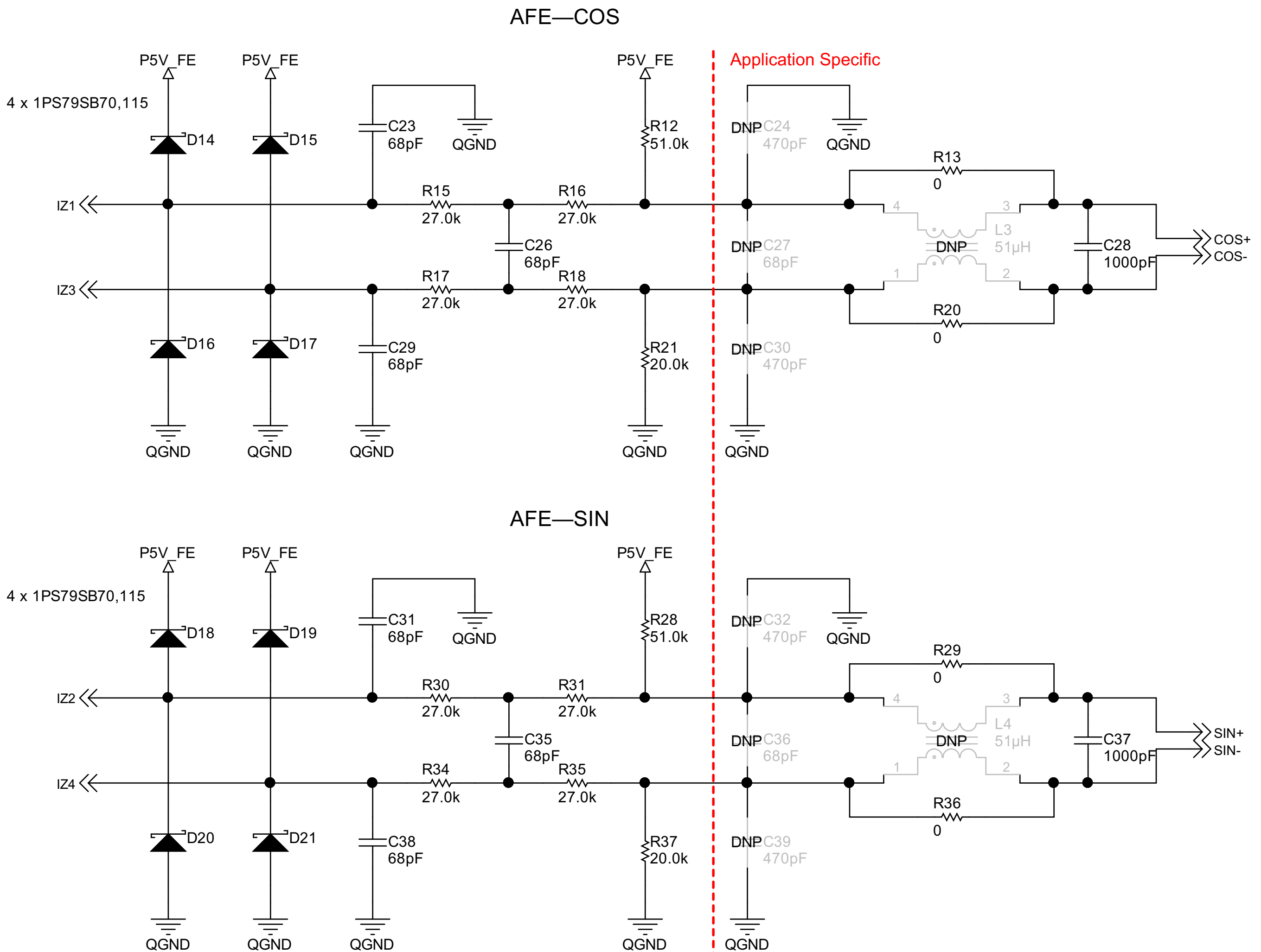

Figure 16. AFE Circuit Diagram

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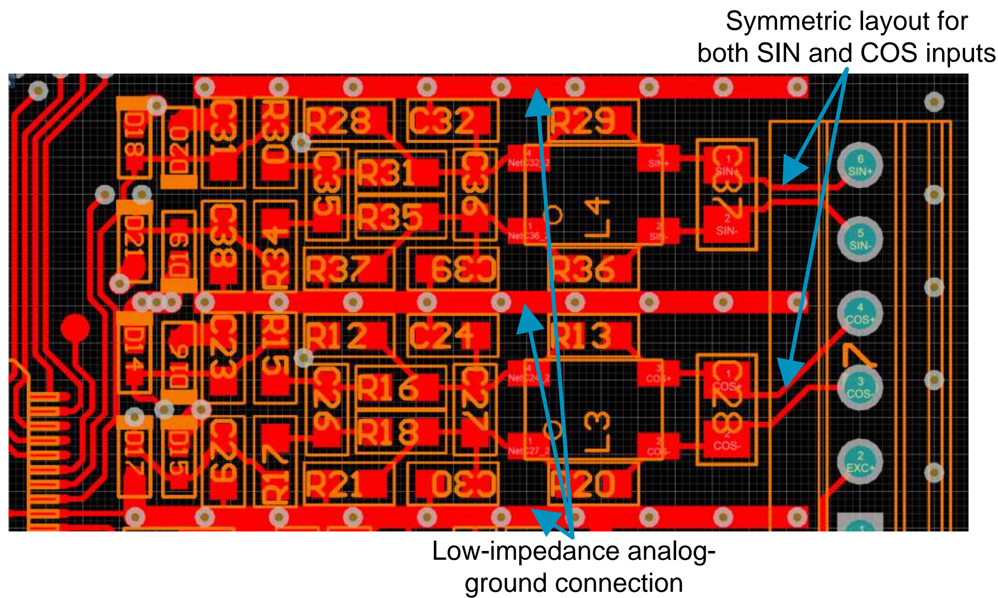

Figure 17. TIDA-00796 AFE PCB Layout

NOTE: Make sure the input AFE layers of the input filter are symmetrical.

The AFE is referenced to the QGND and QVCC (P5V_FE).

The AFE has gain setting resistors, RC filters, and ESD protection for the differential SIN signals of the resolver (a similar circuit is also available for the COS signals). The filtering circuit for the AFE must be referenced to QVCC and QGND.

The ground can also be run between the input sine and cosine (IZx) pins for better noise coupling. Shielding the inputs of the analog front end with the COMAFE pin on both sides is a good practice. Use large and small decoupling capacitors in parallel to optimize for ESR at higher frequencies. Using a smaller footprint with a smaller capacitor is best. Further layout improvement is possible by moving the AFE filter components symmetrical to IZ1 and IZ3 pins, and the IZ2 and IZ4 pins of the PGA411-Q1 device.

Notes:

- Run the differential traces for IZ2 and IZ4 together.
- Run the common mode (COMAFE) or QGND traces between the SIN and COSINE traces.
- Run the differential traces for IZ1 and IZ3 together.

In case any other power controller or high-frequency switching block (that can lead to EMI) exists on the board, care must be taken to route the inductor, diode, and other switching components away from the AFE of the PGA411-Q1 device. System performance may be impacted if these recommendations are not followed properly.

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6 Digital Connections

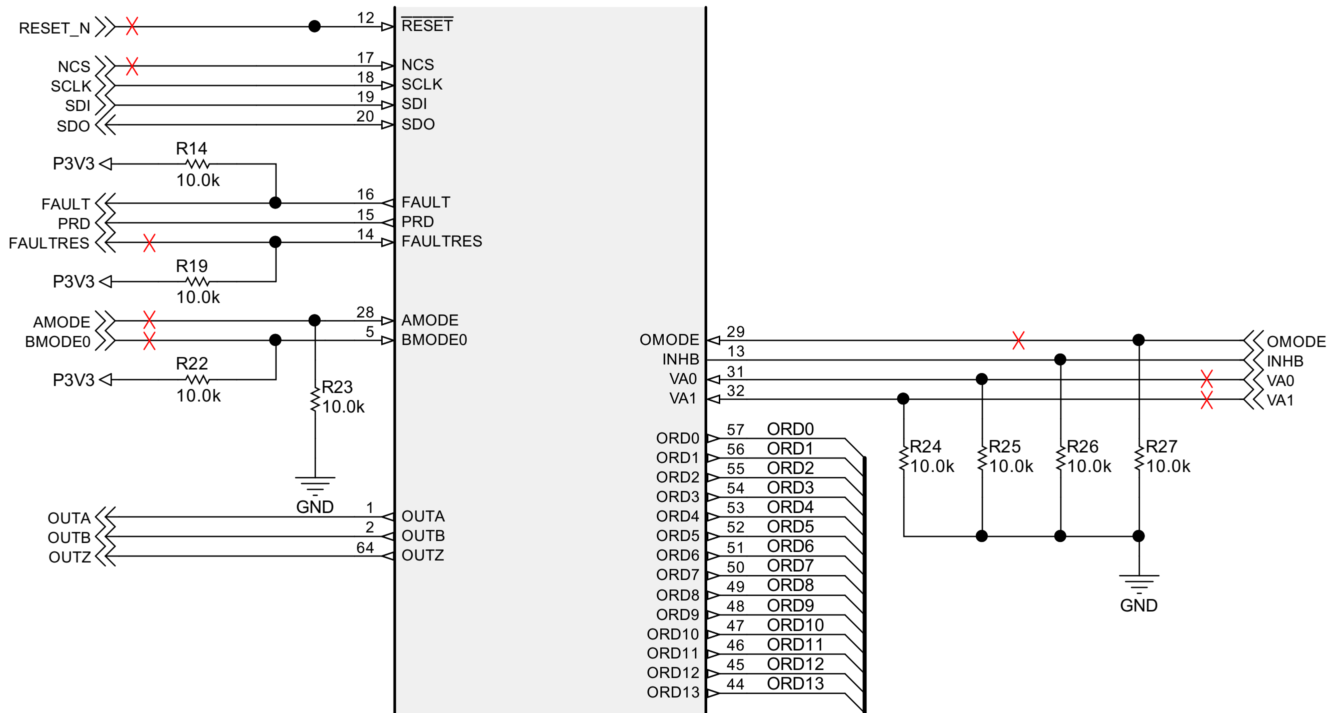

Figure 18. Digital Connections

The digital connections must be routed away from the analog filter inputs. TI does not recommend routing the SPI pins underneath the AFE filter. Refer to Figure 3 for how these traces avoid the AFE and the power supply.

7 Excitation Amplifier Output

The IE1 and IE2 traces are symmetrical and have a similar phase delay at the PGA411-Q1 input. Refer to Figure 19. The ESD diodes can also be placed directly at the input pins depending upon compliance requirements.

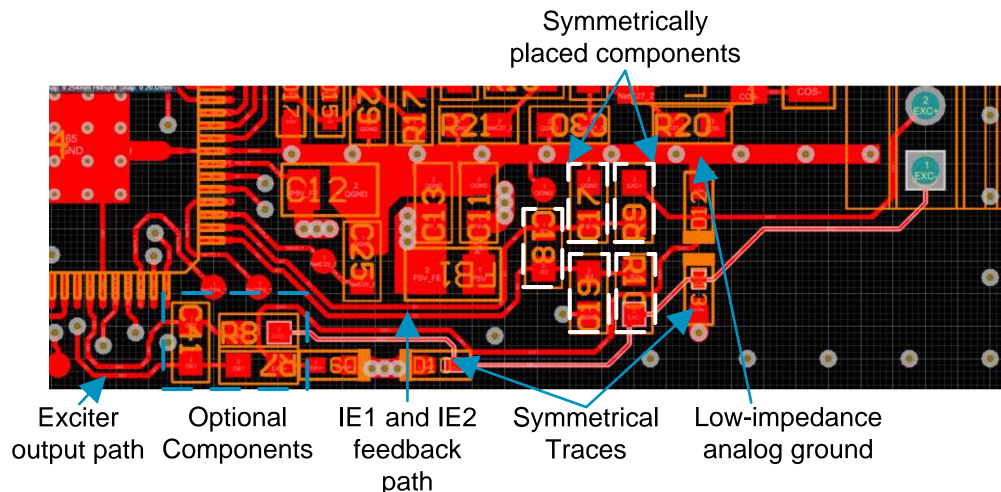

Figure 19. Excitation Amplifier

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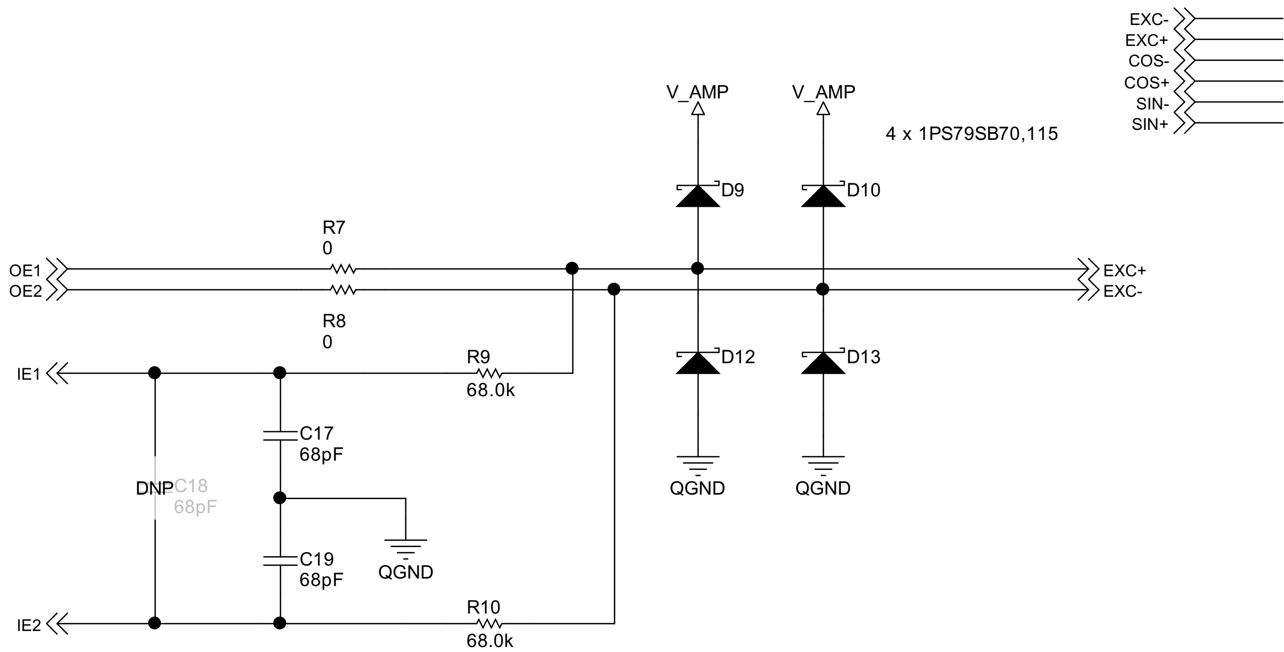

Figure 20. Resolver Excitation Output + Feedback

VEXT/VEXTS: The thickness of the VEXT trace must support the output current. Increase the thickness to match that of the VSW trace. The VEXT pin is the external-amplifier supply and the VEXTS pin is for monitoring and boosting feedback.

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8 Oscillator

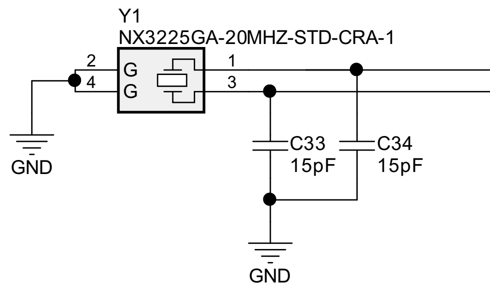

Figure 21. Oscillator Schematic

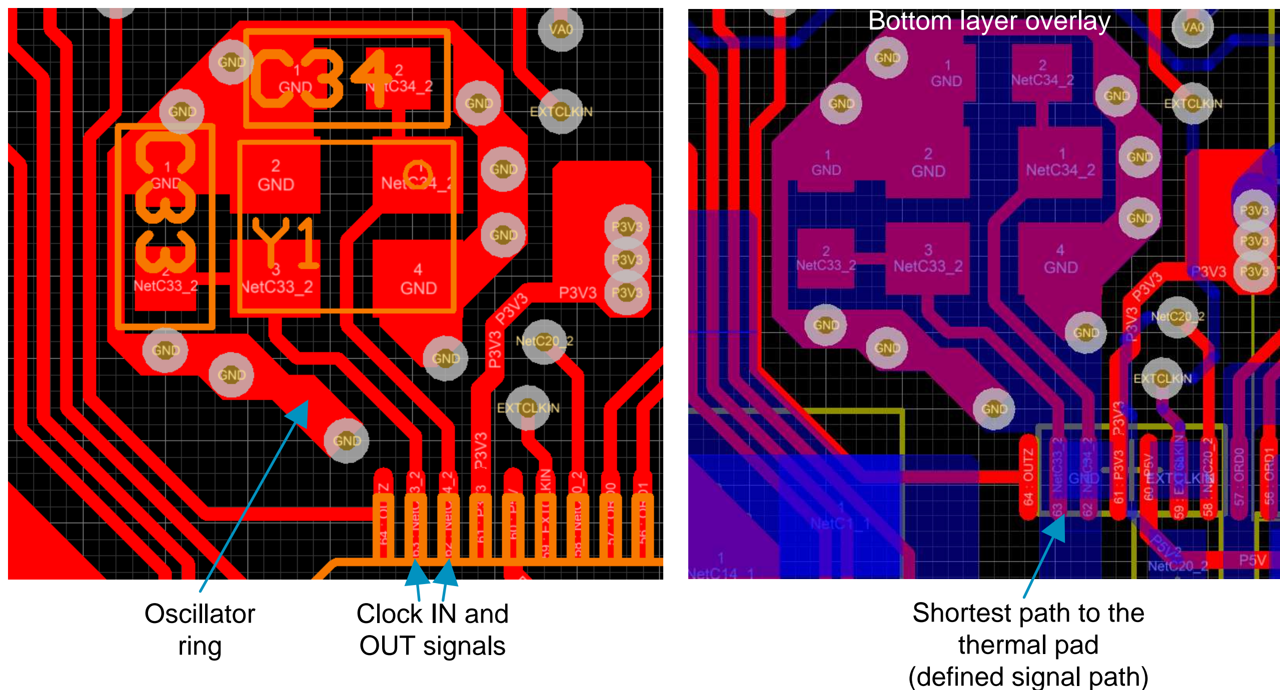

Figure 22. Crystal Oscillator Layout Using Oscillator Ring Technique

Another technique to reduce the risk of EMC issues is using the oscillator ring technique. High-frequency content copies the transmission line rather than the low resistance path. The oscillator ring defines the path while keeping the path short. This technique reduces radiated emissions.

Place the crystal as close as possible to the pins. The capacitors can be in parallel to the crystal.

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