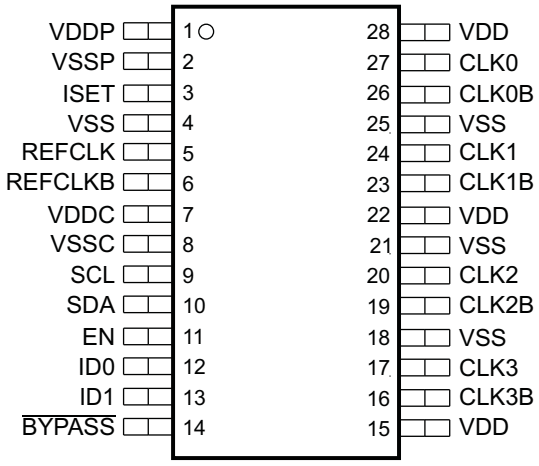
Rambus™ XDR™ CLOCK GENERATOR

FEATURES

- **High-Speed Clock Support: 300-MHz–667-MHz Clock Source for XDR Memory Subsystems and Redwood Logic Interface**
- **Quad (Open-Drain) Differential Output Drivers**
- **Spread-Spectrum Compatible Clock Input Can Be Distributed to Minimize EMI**
- **Differential or Single-Ended Reference Clock Input of 100 MHz or 133 MHz**
- **Serial Interface Features: Programmable Frequency Multiplier, Select Any One to Four Outputs and Mode of Operation**
- **Supports Frequency Multiplication Factors of: ×3, ×4, ×5, ×6, ×8, ×9/2, ×15/2, ×15/4**
- **All PLL Loop Filter Components Are Integrated**
- **Low \|Cycle-to-Cycle\| of 1–6 Cycle Jitter:**
  - **40 ps: 300–635 MHz**
  - **30 ps: 636–667 MHz**
- **PLLs Are Powered Down if No Valid REF Clock (<10 MHz) Is Detected or VDD Is Below 1.6 V**
- **Operates From Single 2.5-V Supply (±0.125 V)**
- **Packaged in TSSOP-28**
- **Commercial Temperature Range 0°C to 70°C**

PW PACKAGE
(TOP VIEW)



P0043-01

APPLICATIONS

- **XDR Memory Subsystem and Redwood Logic Interface**

DESCRIPTION

The CDCD5704 clock generator provides the necessary clock signals to support an XDR memory subsystem and Redwood logic interface using a reference clock input with or without spread-spectrum modulation. Contained in a 28-pin TSSOP package that includes four differential clock outputs, the CDCD5704 provides an off-the-shelf solution for a broad range of high-performance interface applications.

The block diagram shows the major components of the CDCD5704, which include a phase-locked loop, a bypass multiplexer, and four differential output buffers (CLK0 to CLK3). All four outputs can be disabled by a logical low at the input of the EN pin. An output is enabled when EN is high and a value of 1 is in its serial interface register (RegA–RegD).

The PLL receives a reference clock input signal, REFCLK, and outputs a clock signal at a frequency equal to the input frequency times the multiplication factor. The PLL output clock signal is fed to the differential output buffers to drive the enabled clocks. Disabled outputs are set to high impedance.

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The bypass mode routes the input clock REFCLK to the differential output buffers, bypassing the PLL.

To ensure that the CDCD5704 clock generator always performs correctly, the device switches off the PLL and the outputs are in the high-impedance state, once the clock input is below 10 MHz. If the supply voltage VDD is less than V_{PUC}, all logic gates are reset, the PLL is powered down, and the outputs are in the high-impedance state. Therefore, the device only starts its operation if these minimum requirements are met.

Because the CDCD5704 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. With use of an external reference clock, this signal must be fixed-frequency and fixed-phase prior to the start of stabilization time.

The device operates from a single 2.5-V supply voltage. The CDCD5704 device is characterized for operation from 0°C to 70°C.

FUNCTIONAL BLOCK DIAGRAM

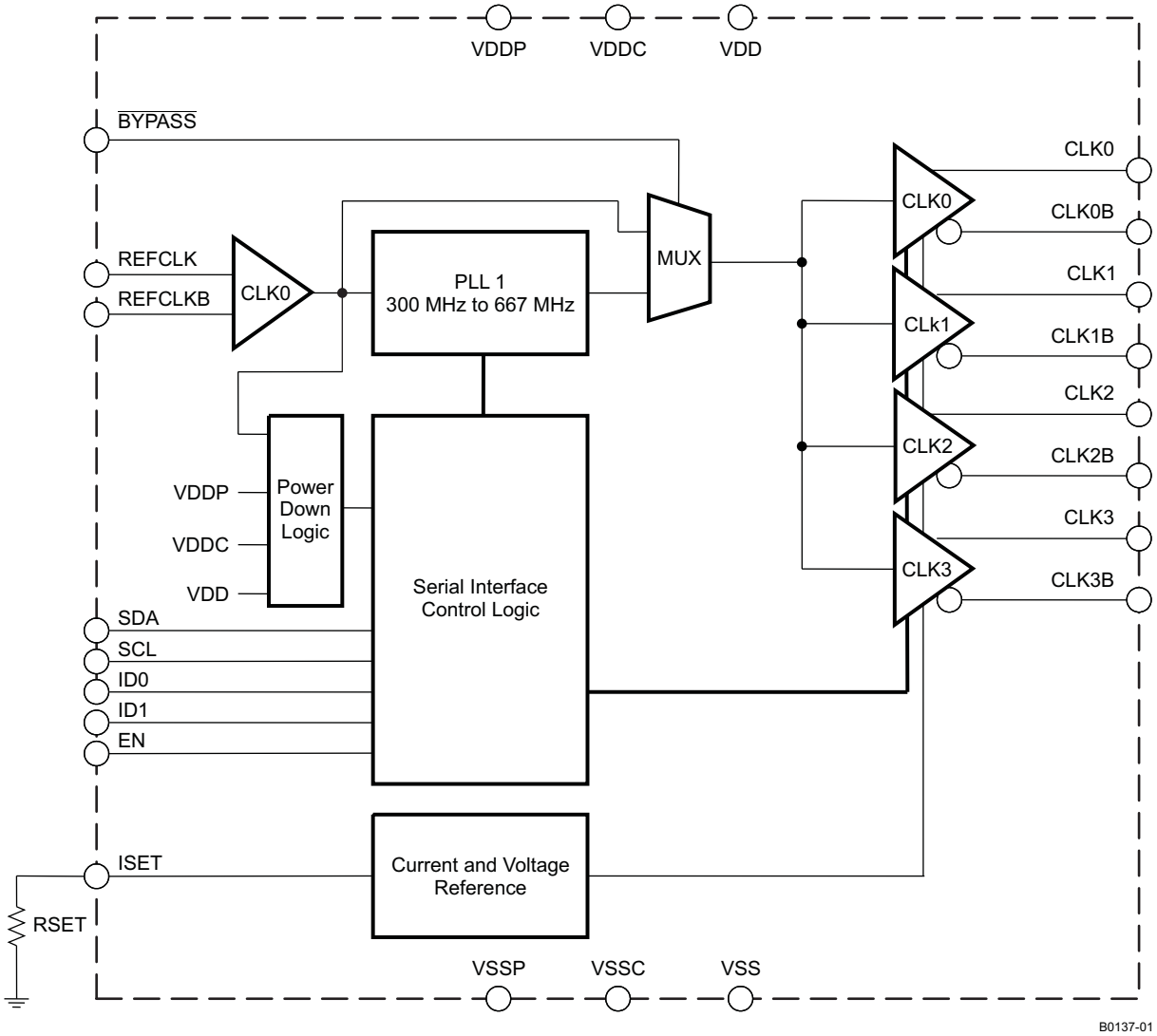


Table 1. TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
$\overline{\text{BYPASS}}$	14	Input	If 0, the PLL is bypassed and the PLL is switched off.
CLK0	27	Output	Output for Clock0
CLK0B	26	Output	Complementary output for Clock0
CLK1	24	Output	Output for Clock1
CLK1B	23	Output	Complementary output for Clock1
CLK2	20	Output	Output for Clock2
CLK2B	19	Output	Complementary output for Clock2
CLK3	17	Output	Output for Clock3
CLK3B	16	Output	Complementary output for Clock3
EN	11	Input	Output enable; if 0, all outputs are disabled.
ID0	12	Input	Device ID, bit 0
ID1	13	Input	Device ID, bit 1
ISET	3	Output	Set clock driver current with external resistor
REFCLK	5	Input	Reference clock input
REFCLKB	6	Input	Complementary reference clock input
SCL	9	Input	Serial interface clock, 3.3-V compatible
SDA	10	Input	Serial interface data, 3.3-V compatible
VDD	15, 22, 28	Power	2.5-V power supply for outputs
VDDC	7	Power	2.5-V power supply for core
VDDP	1	Power	2.5-V power supply for PLL
VSS	4, 18, 21, 25	Ground	Ground
VSSC	8	Ground	Ground for core
VSSP	2	Ground	Ground for PLL

SERIAL INTERFACE

The following section describes the serial interface programming. In general, the serial interface slave supports byte-write/-read and word-write/-read protocol as defined in the SMBus or I^2C specification.

Serial Interface Operation Requirement

The internal timing of the serial interface logic block in the CDCD5704 requires a timing reference derived from the input clock (REFCLK). A reference clock must be present at the REFCLK pin for the serial interface to be operational.

Serial Interface Device Address

A6	A5	A4	A3	A2	A1	A0	W/R
1	1	0	1	1	ID1	ID0	0/1

The device-ID is determined by the external pins ID0 and ID1. They are part of the device 8-bit address. Therefore, four different devices (00, 01, 10, and 11) can be addressed via the same serial interface. The least significant bit of the address designates a write or read operation.

R/W Bit:

0 = write to CDCD5704 device

1 = read from CDCD5704 device

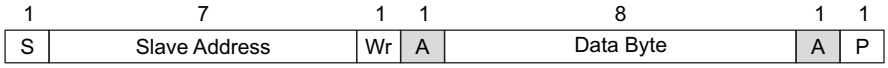
Command Code Definition

Bit	Description
C7	1 = byte-write/-read or word-write/-read operation
(C6:C0)	Byte offset for byte-write/-read or word-write/-read operation

Command Code for Byte-Write/-Read Operation	Hex Code	C7	C6	C5	C4	C3	C2	C1	C0
Byte 0	80h	1	0	0	0	0	0	0	0
Byte 1	81h	1	0	0	0	0	0	0	1
Byte 2	82h	1	0	0	0	0	0	1	0

Command Code for Word-Write/-Read Operation	Hex Code	C7	C6	C5	C4	C3	C2	C1	C0
Word 0: Byte 0 and byte 1	80h	1	0	0	0	0	0	0	0
Word 1: Byte 1 and byte 2	81h	1	0	0	0	0	0	0	1

Serial Interface Generic Programming Sequence



S Start Condition

Sr Repeated Start Condition

Rd Read (Bit Value = 1)

Wr Write (Bit Value = 0)

A Acknowledge (ACK = 0 and NACK = 1)

P Stop Condition

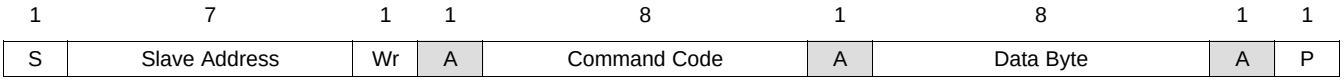
PE Packet Error

Master-to-Slave Transmission

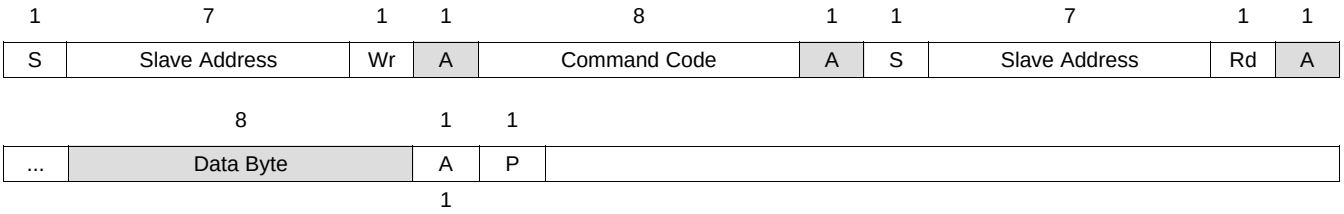
Slave-to-Master Transmission

M0053-01

Byte-Write Programming Sequence



Byte-Read Programming Sequence



Word-Write Programming Sequence

1	7	1	1	8	1	8	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A

8	1	1	
Data Byte High	A	P	...

Word-Read Programming Sequence

1	7	1	1	8	1	1	7	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A

8	1	8	1	1	
Data Byte	A	Data Byte	A	P	...

1

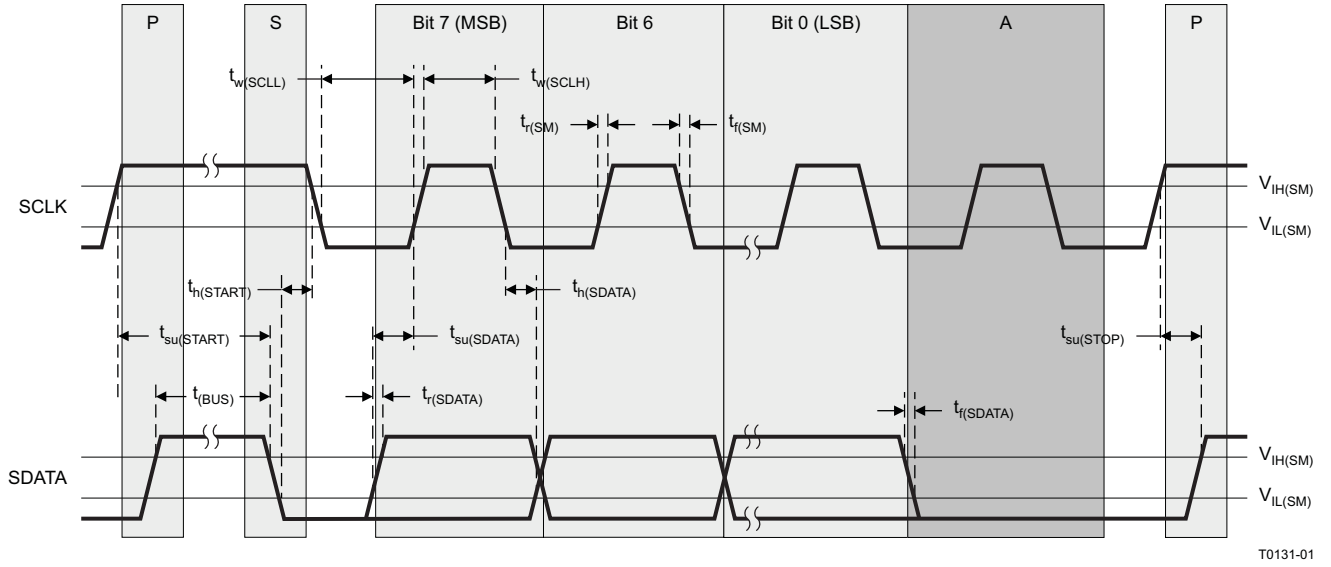


Figure 1. Timing Diagram, Serial Control Interface

Serial Interface Configuration Command Bitmap

Byte 0

Bit	Bit Name	Description/Function	Type	Power-Up Condition
7	RES	Reserved	R/W	0
6	MULT2	Multiplication factor, bit 2	R/W	0
5	MULT1	Multiplication factor, bit 1	R/W	0
4	MULT0	Multiplication factor, bit 0	R/W	1
3	RegA	Enable CLK0	R/W	1
2	RegB	Enable CLK1	R/W	1
1	RegC	Enable CLK2	R/W	1
0	RegD	Enable CLK3	R/W	1

Byte 1

Bit	Bit Name	Description/Function	Type	Power-Up Condition
7	RES	Reserved	R/W	0
6	RES	Reserved	R/W	0
5	RES	Reserved	R/W	0
4	RES	Reserved	R/W	0
3	RES	Reserved for vendor option	R/W	0
2	RES	Reserved for vendor option	R/W	0
1	RES	Reserved for vendor option	R/W	0
0	RegTest	Vendor test register. If high, then Vendor Test	R/W	0

Byte 2

Bit	Bit Name	Description/Function	Type	Power-Up Condition
7	REV0	Device revision, bit 4	R	0
6	REV0	Device revision, bit 3	R	0
5	REV0	Device revision, bit 2	R	0
4	REV0	Device revision, bit 1	R	0
3	REV0	Device revision, bit 0	R	0
2	VID2	Vendor ID bit 2	R	0
1	VID1	Vendor ID bit 1	R	1
0	VID0	Vendor ID bit 0	R	1

FUNCTIONAL DESCRIPTION OF THE LOGIC

PLL Multiplication Factor Selection

Mult2	Mult1	Mult0	Multiplication Factor	Output Frequency (MHz)	
				REFCLK = 100 MHz	REFCLK = 133 MHz
0	0	0	3	300	400
0(1)	0(1)	1(1)	4(1)	400	533
0	1	0	5	500	667
0	1	1	6	600	800(2)
1	0	0	8	800(2)	–(2)
1	0	1	9/2	450	600
1	1	0	15/2	750(2)	–(2)
1	1	1	15/4	375	500

(1) Default settings after power up
(2) Output at this frequency does not conform to all the ac device characteristics in the *Device Characteristics* table, or ouput frequency is not supported.

Modes of Operation

EN	$\overline{\text{BYPASS}}$	Reg-Test	RegA	RegB	RegC	RegD	CLK0	CLK1	CLK2	CLK3
L	X	X	X	X	X	X	HI-Z	HI-Z	HI-Z	HI-Z
H	X	1	X	X	X	X	RESERVED FOR VENDOR TEST			
H	L	0	X	X	X	X	REFCLK	REFCLK	REFCLK	REFCLK
H	H	0	0	0	0	0	HI-Z	HI-Z	HI-Z	HI-Z
H	H	0	1	0	0	0	PLL CLK	HI-Z	HI-Z	HI-Z
H	H	0	0	1	0	0	HI-Z	PLL CLK	HI-Z	HI-Z
H	H	0	1	1	0	0	PLL CLK	PLL CLK	HI-Z	HI-Z
H	H	0	0	0	1	0	HI-Z	HI-Z	PLL CLK	HI-Z
H	H	0	1	0	1	0	PLL CLK	HI-Z	PLL CLK	HI-Z
H	H	0	0	1	1	0	HI-Z	PLL CLK	PLL CLK	HI-Z
H	H	0	1	1	1	0	PLL CLK	PLL CLK	PLL CLK	HI-Z
H	H	0	0	0	0	1	HI-Z	HI-Z	HI-Z	PLL CLK
H	H	0	1	0	0	1	PLL CLK	HI-Z	HI-Z	PLL CLK
H	H	0	0	1	0	1	HI-Z	PLL CLK	HI-Z	PLL CLK
H	H	0	1	1	0	1	PLL CLK	PLL CLK	HI-Z	PLL CLK
H	H	0	0	0	1	1	HI-Z	HI-Z	PLL CLK	PLL CLK
H	H	0	1	0	1	1	PLL CLK	HI-Z	PLL CLK	PLL CLK
H	H	0	0	1	1	1	HI-Z	PLL CLK	PLL CLK	PLL CLK
H	H	0(1)	1(1)	1(1)	1(1)	1(1)	PLL CLK	PLL CLK	PLL CLK	PLL CLK

(1) Default settings after power up

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE	UNIT
V_{DD}	Supply voltage range		–0.3 to 2.8	V
V_I	Input voltage range (2)	For SCL and SDA	–0.3 to 3.6	V
		For all other inputs	–0.3 to V_{DD} + 0.25	
V_O	Output voltage range (2)		–0.5 to V_{DD} + 0.5	V
I_{IK}	Input clamp current, (V_I < 0, V_I > V_{DD})		±20	mA
I_O	Continuous output current		±50	mA
$R_{\theta JA}$	Thermal resistance, junction-to-ambient (3)	No airflow	94.4	K/W
		Airflow 150 ft/min	82.8	
		Airflow 250 ft/min	79.1	
		Airflow 500 ft/min	74	
$R_{\theta JC}$	Thermal resistance, junction-to-case (3)	No airflow	31.8	K/W
$R_{\theta JB}$	Thermal resistance, junction-to-board (3)	No airflow	68.9	K/W
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature range		–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51 and JEDEC2S1P (high-k board).

RECOMMENDED DC OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{DDP}	Supply voltage for PLL	2.375	2.5	2.625	V
V_{DDC}	Supply voltage for core	2.375	2.5	2.625	V
V_{DD}	Supply voltage for clock buffers	2.375	2.5	2.625	V
T_A	Operating free-air temperature	0		70	°C
$V_{IL,CLK}$	Low-level input voltage, REFCLK/REFCLKB	–0.15		0.15	V
$V_{IX,CLK}$	Crossing-point voltage, input voltage threshold, REFCLK/REFCLKB	0.2		0.55	V
$V_{IH,CLKD}$	High-level input voltage, REFCLK/REFCLKB	0.6		0.95	V
$\Delta V_{IX,CLK}$	Difference in crossing-point voltage			0.15	V
$V_{IL\ SE}$	Low-level, single-ended input voltage, REFCLK	–0.15		$V_{th\ SE}$ – 0.3	V
$V_{th\ SE}$	Single-ended input-voltage threshold, REFCLK (1)	0.35		0.5 V_{DD}	V
$V_{IH\ SE}$	High-level, single-ended input voltage, REFCLK	$V_{th\ SE}$ + 0.3		2.625	V
$V_{IL\ L}$	Low-level input voltage, ID0, ID1, EN, $\overline{\text{BYPASS}}$	–0.15		0.8	V
$V_{IH\ L}$	High-level input voltage, ID0, ID1, EN, $\overline{\text{BYPASS}}$	1.4		2.625	V
$V_{IL\ SM}$	Low-level input voltage, SCL, SDA (2)	–0.15		0.8	V
$V_{IH\ SM}$	High-level input voltage, SCL, SDA (2)	1.4		3.465	V

(1) When using a single-ended clock input, V_{th} is supplied to the REFCLKB pin. Duty cycle of single-ended REFCLK input is measured at V_{th}.
(2) This range of SCL and SDA input high voltage allows the CDCD5704 to co-exist with 3.3 V, 2.5 V, and 1.8 V devices on the same serial-interface bus system.

RECOMMENDED AC OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$t_{CYCLE,IN}$	REFCLK/REFCLKB input cycle time	7		11	ns
$t_{CYC,TEST}$	REFCLK/REFCLKB input cycle time for $\overline{BYPASS}$	4		40	ns
$t_{J,IN}$	Input |cycle-to-cycle| jitter(1)			185	ps
DC_{IN}	Input duty cycle over 10,000 cycles(2)	40%		60%	
t_r/t_f	Rise and fall time for REFCLK signal from 20% to 80% of input voltage V_{IN}	175		700	ps
t_{cr}/t_{cf}	Difference between rise time and fall time of REFCLK signal from 20% to 80%			150	ps
$f_{m,IN}$	SSC frequency modulation repeat frequency(3)	30		33	kHz
$P_{m\ tria}$	Modulation index (= frequency deviation/center frequency) for triangle modulation(3)			0.6%	
$P_{m\ n\ tria}$	Modulation index (= frequency deviation/center frequency) for non-triangle modulation(4)			0.5%	
t_{SR}	Input slew rate REFCLK/REFCLKB	1		4	V/ns
SERIAL INTERFACE TIMING					
f_{SCLK}	SCLK frequency(5)	0		100	kHz
$t_{h(START)}$	START hold time(5)	4			µs
$t_{w(SCLL)}$	SCLK low-pulse duration(5)	4.7			µs
$t_{w(SCLH)}$	SCLK high-pulse duration(5)	4			µs
$t_{su(START)}$	START setup time(5)	4.7			µs
$t_{h(SDATA)}$	SDATA hold time(5)	300			ps
$t_{su(SDATA)}$	SDATA setup time(5)	250			ps
$t_{r(SDATA)}/t_{r(SM)}$	SDATA/SCLK input rise time(5)			1000	ns
$t_{f(SDATA)}/t_{f(SM)}$	SDATA/SCLK input fall time(5)			300	ns
$t_{su(STOP)}$	STOP setup time(5)	4			µs
$t_{(BUS)}$	Bus free time	4.7			µs

(1) RefCLK jitter is measured at ($V_{IH(nom)}$ – $V_{IL(nom)}$)/2 and is the absolute value of the worst-case deviation.
(2) Measured at crossing points for differential clock input or at input threshold voltage V_{TH} for single-ended clock input.
(3) If input modulation is used; input modulation is allowed but not required.
(4) The amount of allowed spreading for any non-triangular modulation is determined by the induced downstream tracking skew, which cannot exceed the skew generated by the specified 0.6% triangular modulation. Typically, the amount of allowed non-triangular modulation is about 0.5%.
(5) See Figure 1 for the timing behavior of the serial interface.

DEVICE CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OVERALL PARAMETER						
I_{DD}	Supply current (= I_{VDD} + I_{VDDP} + I_{VDDC})	At 300 MHz and 2.625 V		70	85	mA
		At 667 MHz and 2.625 V		90	115	
V_{PUC}	Supply voltage threshold for power-up control circuit	Over complete supply voltage range	1.1	1.8	2.2	V
DC DEVICE CHARACTERISTICS						
V_{OX}	Differential output crossing-point voltage(1)	Output load; see Figure 3.	0.9	1	1.1	V
V_{COS}	Output voltage swing (p-p, single-ended)(2)		0.3	0.325	0.35	V
$V_{OL,ABS}$	Absolute output low voltage(3)		0.85			V
V_{ISET}	Reference voltage for swing control current IREF(4)	V_{DD} = 2.375 V to 2.625 V, T = 0°C to 70°C	0.98	1	1.02	V

(1) V_{OX} is measured on external divider as shown in Figure 3.
(2) V_{COS} = (clock output high voltage – clock output low voltage), at the measurement points shown in Figure 3, excluding overshoot and undershoot.
(3) $V_{OL,ABS}$ is measured at the clock output of the package, instead of the measurement points of Figure 3.
(4) I_{REF} is equal to V_{ISET}/R_{RC}. Tolerance of R_{RC} must be ±1% or smaller.

DEVICE CHARACTERISTICS (continued)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OL}/I_{REF}	Ratio of output low current to reference current		6.8	7	7.2	
$I_{OL,ABS}$	Minimum current at $V_{OL,ABS}$ (5)	$V_{OL,ABS}$ = 0.85 V	45			mA
$V_{OL,SDA}$	SDA output low voltage	V_{DD} = 2.375 V to 2.625 V, I_{OH} = 4 mA			0.4	V
$I_{OL,SDA}$	SDA output low current	V_{DD} = 2.375 V to 2.625 V, V_O = 0.8 V	6			mA
I_{OZ}	Output 3-state current	CLK0 to CLK4			±50	µA
I_{IR}	REFCLK input current	V_I = 0 V or V_{DD}			±5	µA
I_{IL}	Logic input current	V_I = 0 V or V_{DD}			±10	µA
AC DEVICE CHARACTERISTICS						
C_{IR}	Input capacitance, REFCLK, REFCLKB (6)			2	7	pF
C_{IL}	Input capacitance logic pins (7)			2	10	pF
t_{CYCLE}	Clock cycle time (8)	300 MHz to 667 MHz, possible SSC is not taken into account	1.5		3.33	ns
$t_{jit(per)}$	|Cycle-to-cycle jitter| of 1–6 clock cycles	10,000 cycles, 300 MHz to 635 MHz (9)			40	ps
		10,000 cycles, 636 MHz to 667 MHz (9)			30	
L_1	SSB phase noise at 1 MHz	300-MHz–667-MHz output (10)		–115	–97	dBc/Hz
L_{20}	SSB phase noise at 20 MHz	300-MHz–667-MHz output (10)		–150	–128	dBc/Hz
$\Delta t_{skew(o)}$	Drift in $t_{skew(o)}$ (11)	V_{DD} = 2.375 V to 2.625 V, T = 0 to 70°C			15	ps
odc	Output duty cycle		45%	50%	55%	
$t_{ODC,ERR}$	|Cycle-to-cycle| duty-cycle error	300 MHz to 635 MHz			40	ps
		636 MHz to 667 MHz			30	
$t_{ERR,SSC}$	PLL output phase error when tracking SSC		–100		100	ps
t_r/t_f	Output rise and fall time	V_{OUT} = 20%–80%	100		300	ps
t_{cr}/t_{cf}	Difference between output rise and fall times	V_{OUT} = 20%–80%, f_{out} = 300 MHz to 667 MHz			100	ps
Z_{OUT}	Output dynamic impedance (12)	V_{OL} = 0.9 V	750			Ω
t_L	Power-up lock time	Time from VDD, VDDP, VDDC being applied and settled until clock outputs are settled			3	ms
$t_{L(\omega)}$	PLL lock time after (1) frequency change via serial interface (programming of SCL and SDA pins completed) or (2) EN and/or $\overline{\text{BYPASS}}$ changed state	Time from signals for selecting a mode of operation (1) or (2) applied and settled until clock outputs are settled			3	ms

(5) Minimum $I_{OL,ABS}$ is measured at the clock output pins of the package, as shown in Figure 3.
(6) Capacitance measured at frequency = 1 MHz, dc bias = 0.9 V, and V_{AC} < 100 mV
(7) Capacitance measured at frequency = 1 MHz, dc bias = 0.9 V, and V_{AC} < 100 mV
(8) Maximum and minimum output clock cycle times are based on nominal output frequency of 300 MHz and 667 MHz, respectively. For spread-spectrum-modulated differential or single-ended REFCLK, the output clock tracks the modulation of the input.
(9) Output short-term jitter specification is the absolute value of the worst-case deviation and is defined in the *Jitter* section.
(10) Device must not exceed the upper limit of L(f) for 1-MHz to 100-MHz offset as shown in the *Phase Noise* section.
(11) t_{skew} is the timing difference between any two of the four differential clocks and is measured at common-mode voltage. Δt_{skew} is the change in t_{skew} when the operating temperature and supply voltage change.
(12) Z_{OUT} is defined at the output pins directly. The value is determined as the ac small-signal impedance at low frequencies (< 100 kHz) and when output is driving a high state.

PHASE NOISE

For the offset frequency range from 1 MHz to 100 MHz, phase noise of the CDCD5704 does not exceed the single-sideband phase noise (spectral purity) described by the following equation given by Rambus.

$$L(f) = 10 \log [1 + (50 \times 10^6 / f)^{2.4}] - 138 \text{ dBc/Hz}$$

Selected numerical values are in given in the following table.

f = offset frequency	1 (L_1)	5	10	15	20 (L_{20})	40	80	100	MHz
L(f) = SSB phase noise	–97	–114	–121	–125	–128	–134	–137	–138	dBc/Hz

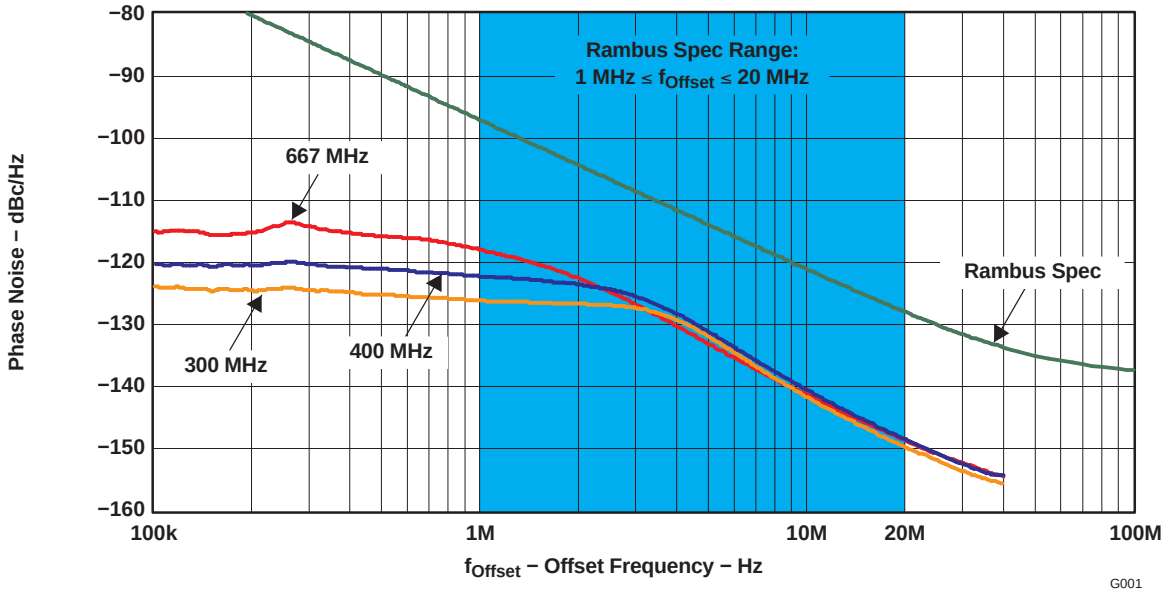
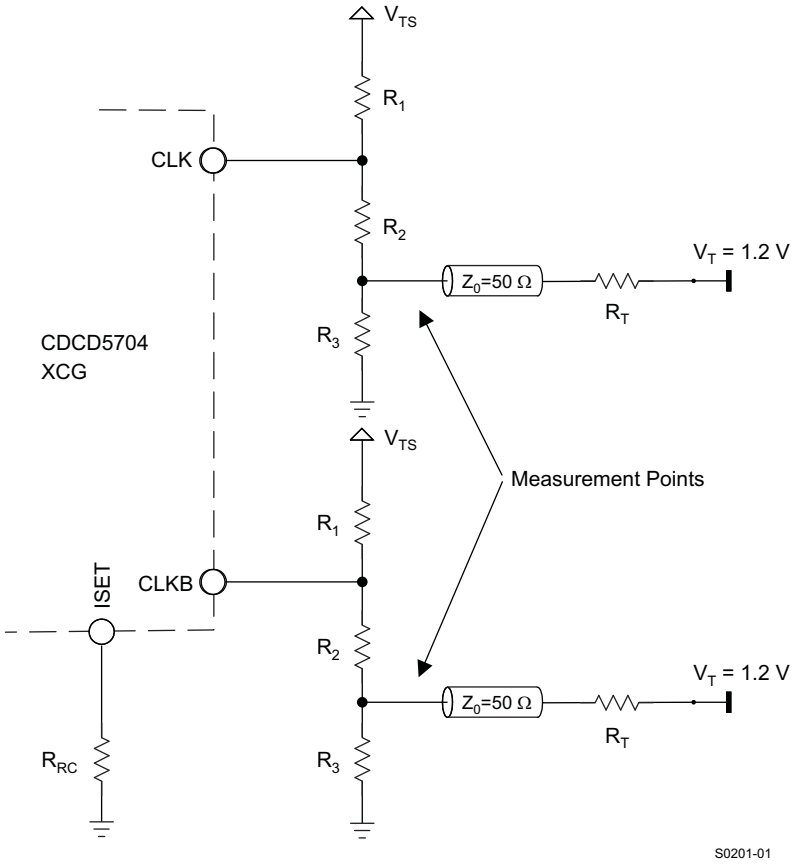


Figure 2. Phase Noise Plot



NOTE: In the power-up sequence, the rise time for the external voltage applied to the clock output pins (V_{TS}) must be equal to or longer than the rise time for the supply voltage of the device (V_{DD}, V_{DDP}, V_{DDC}).

PARAMETER		VALUE for 50-Ω LINE	VALUE for $I_{OL,ABS}$	TOLERANCE	UNIT
R_1	Termination resistor	39.2	34	±1%	Ω
R_2	Termination resistor	66.5	31.8	±1%	Ω
R_3	Termination resistor	93.1	48.7	±1%	Ω
R_T	Termination resistor	49.9	28	±1%	Ω
R_{RC}	Swing control resistor	200	147	±1%	Ω
V_{TS}	Source termination voltage	2.5	2.5	±5%	V
V_T	Termination voltage	1.2	1.2	±5%	V

Figure 3. Output Test Load

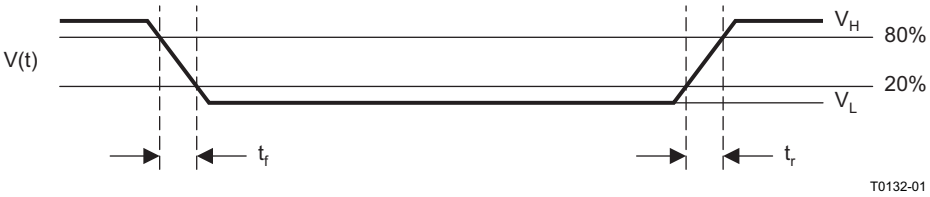


Figure 4. Input and Output Waveforms

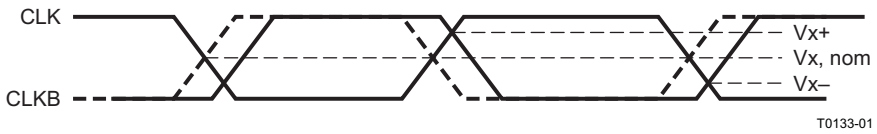


Figure 5. Crossing-Point Voltage

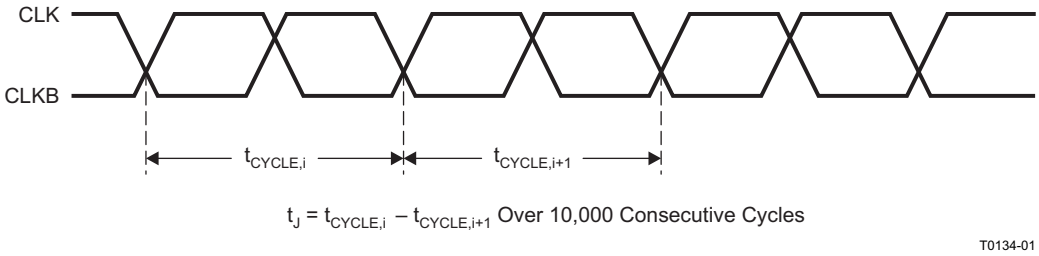


Figure 6. One-Period Cycle-to-Cycle Jitter

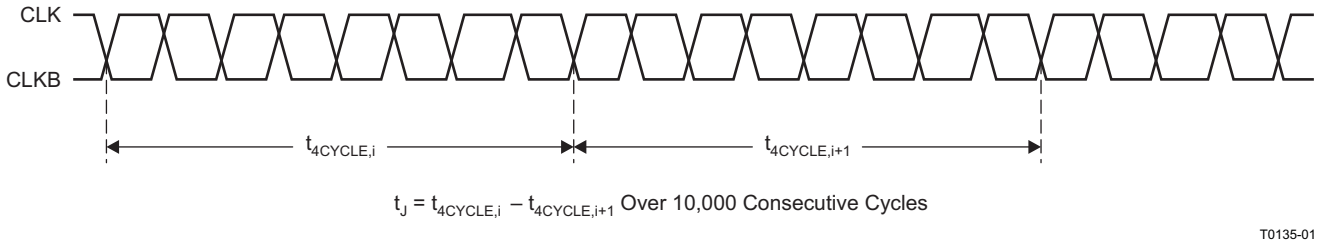


Figure 7. Four-Period Cycle-to-Cycle Jitter

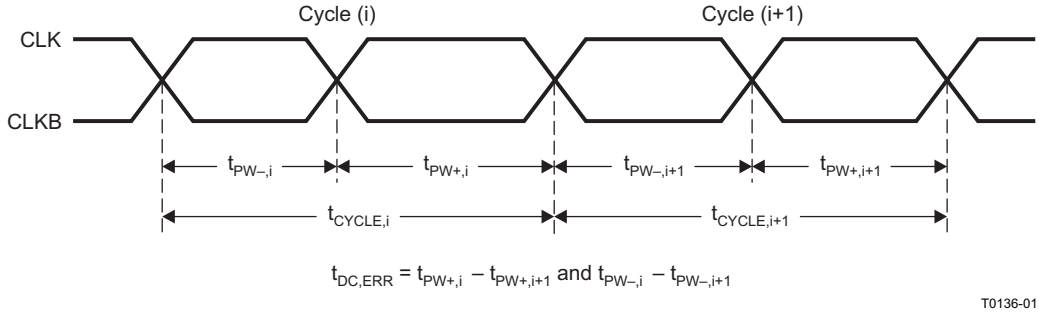
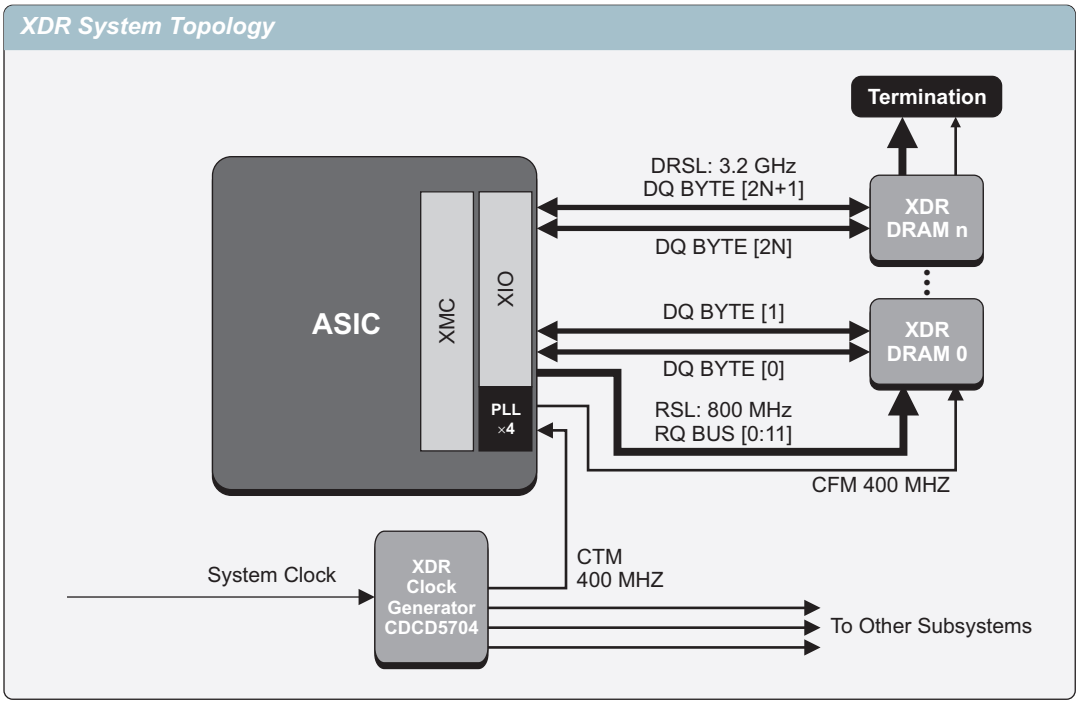


Figure 8. Cycle-to-Cycle Duty-Cycle Error

APPLICATION INFORMATION

XDR Memory Subsystem (Source: Rambus)



M0054-01

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCD5704PW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDCD5704.	Samples
CDCD5704PWG4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDCD5704.	Samples
CDCD5704PWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDCD5704.	Samples
CDCD5704PWRG4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	CDCD5704.	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

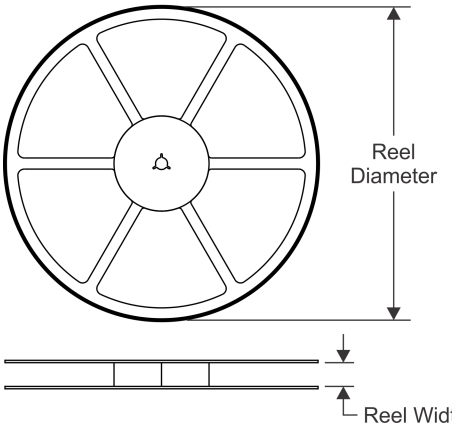
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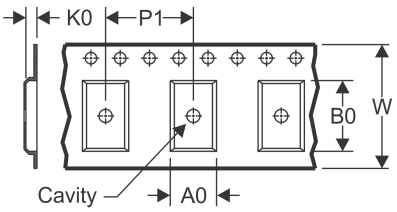
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

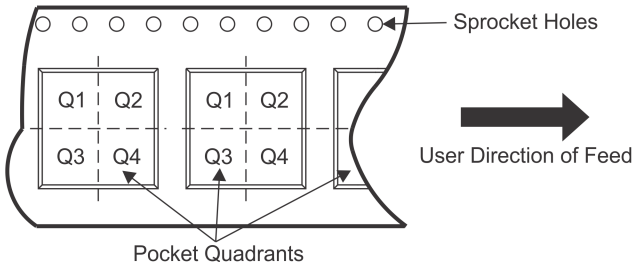


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

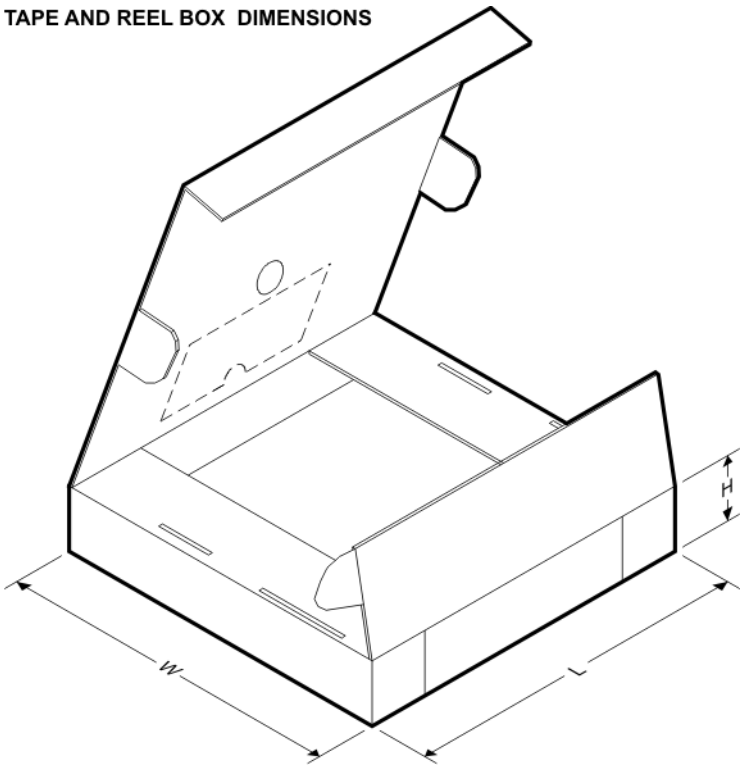
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCD5704PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

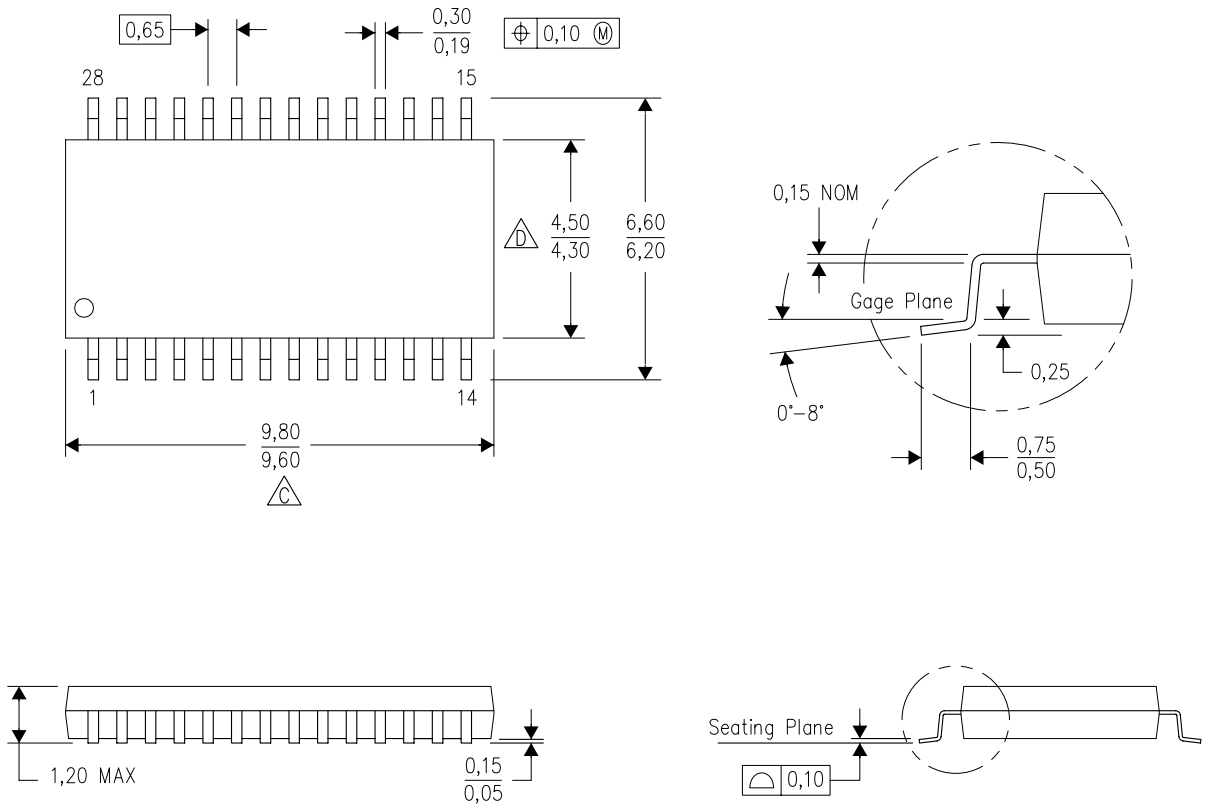
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCD5704PWR	TSSOP	PW	28	2000	367.0	367.0	38.0

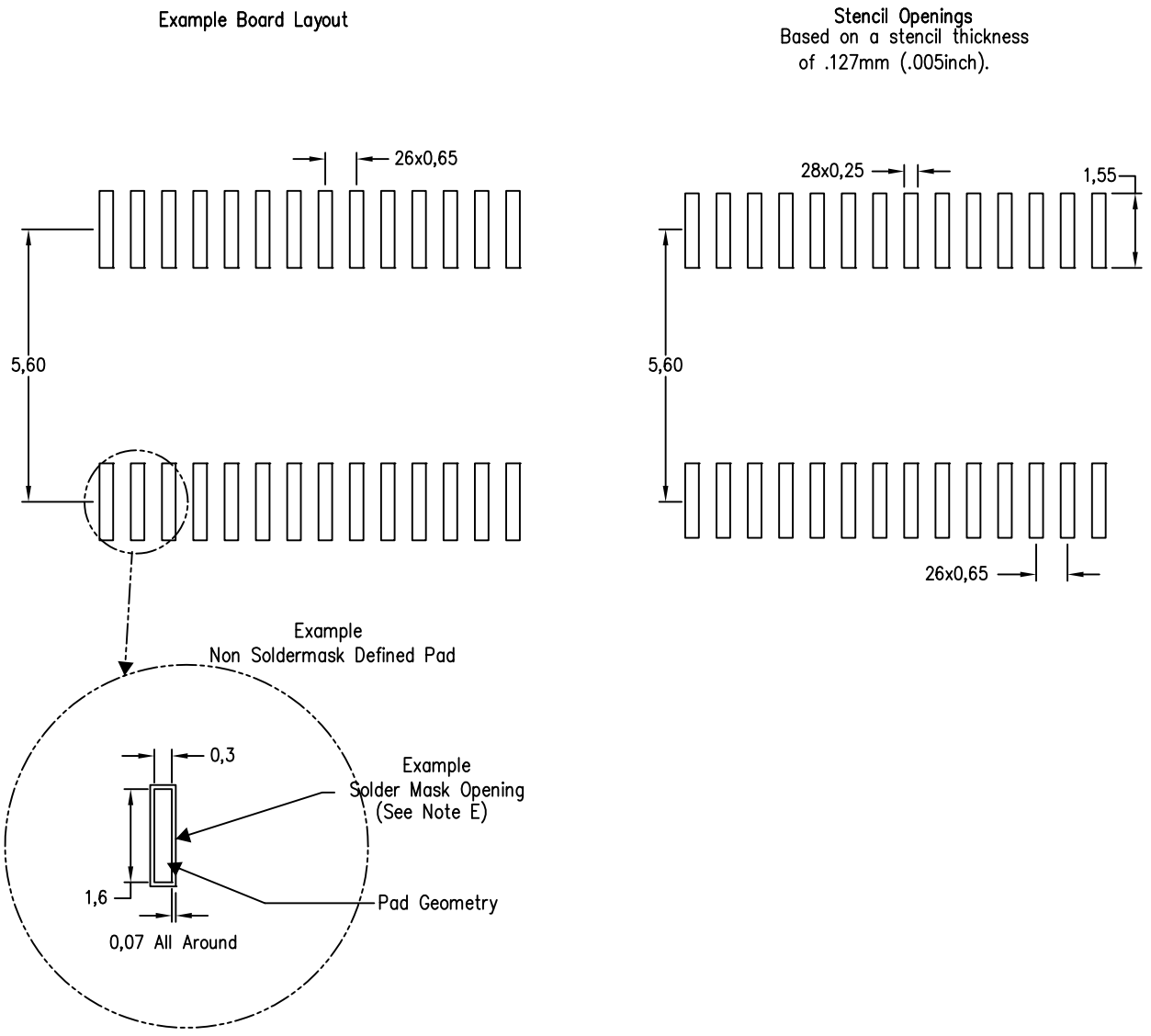
PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



4040064–7/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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