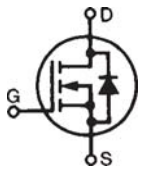
IXYS

HiPerFET™ Power MOSFETs Q2-Class

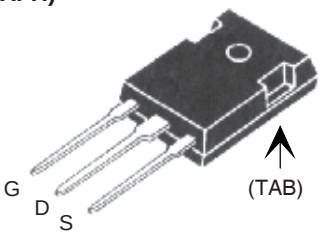
IXFH40N50Q2

V_{DSS} = 500V
I_{D25} = 40A
$R_{DS(on)}$ ≤ 160mΩ
t_{rr} ≤ 250ns



N-Channel Enhancement Mode
Avalanche Rated, High dv/dt, Low Q_g
Low intrinsic R_g, low t_{rr}

TO-247 (IXFH)



G = Gate D = Drain
S = Source TAB = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	500	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	500	V
V_{GSS}	Continuous	±30	V
V_{GSM}	Transient	±40	V
I_{D25}	T_C = 25°C	40	A
I_{DM}	T_C = 25°C, pulse width limited by T_{JM}	160	A
I_A	T_C = 25°C	40	A
E_{AS}	T_C = 25°C	2.5	J
dV/dt	$I_S \le I_{DM}$, $V_{DD} \le V_{DSS}$, $T_J \le 150°C$	20	V/ns
P_D	T_C = 25°C	560	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6mm (0.063 in) from case for 10s	300	°C
M_d	Mounting torque	1.13/10	Nm/lb.in.
Weight		6	g

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
V_{DSS}	V_{GS} = 0V, I_D = 250μA	500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4mA	3.0		5.5	V
I_{GSS}	V_{GS} = ±30V, V_{DS} = 0V			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0V			25	μA
	T_J = 125°C			1	mA
$R_{DS(on)}$	V_{GS} = 10V, $I_D = 0.5 \bullet I_{D25}$, Note 1			160	mΩ

Features

- Double metal process for low gate resistance
- International standard package
- Epoxy meet UL 94 V-0, flammability classification
- Avalanche energy and current rated
- Fast intrinsic Rectifier

Applications

- DC-DC converters
- Switched-mode and resonant-mode power supplies, >500kHz switching
- DC choppers
- Pulse generation
- Laser drivers

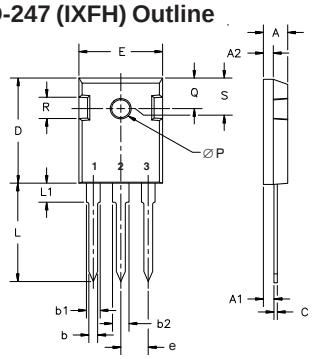
Advantages

- Easy to mount
- Space savings
- High power density

© 2008 IXYS CORPORATION, All rights reserved

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 10V, I_D = 0.5 • I_{D25}, Note 1	15	28		S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		4850		pF
C_{oss}			680		pF
C_{rss}			170		pF
$t_{d(on)}$	Resistive Switching Times		17		ns
t_r	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		13		ns
$t_{d(off)}$	R_G = 2Ω (External)		42		ns
t_f			8		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 0.5 • V_{DSS}, I_D = 0.5 • I_{D25}		110		nC
Q_{gs}			25		nC
Q_{gd}			50		nC
R_{thJC}				0.22	°C/W
R_{thCK}			0.21		°C/W

TO-247 (IXFH) Outline



Terminals: 1 - Gate 2 - Drain

Dim.	Millimeter Min.	Max.	Inches Min.	Max.
A	4.7	5.3	.185	.209
A_1	2.2	2.54	.087	.102
A_2	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b_1	1.65	2.13	.065	.084
b_2	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
ØP	3.55	3.65	.140	.144
Q	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			40	A
I_{SM}	Repetitive, pulse width limited by T_{JM}			160	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Note 1			1.5	V
t_{rr}	I_F = 25A, -di/dt = 100 A/µs, V_R = 100 V			250	ns
Q_{RM}			1		µC
I_{RM}			9		A

Notes: 1. Pulse test, t ≤ 300µs; duty cycle, d ≤ 2%.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405 B2 6,710,463 6,727,585 6,759,692 6,771,478 B2 7,005,734 B2 7,063,975 B2 7,071,537 7,157,338B2

Fig. 1. Output Characteristics @ 25ºC

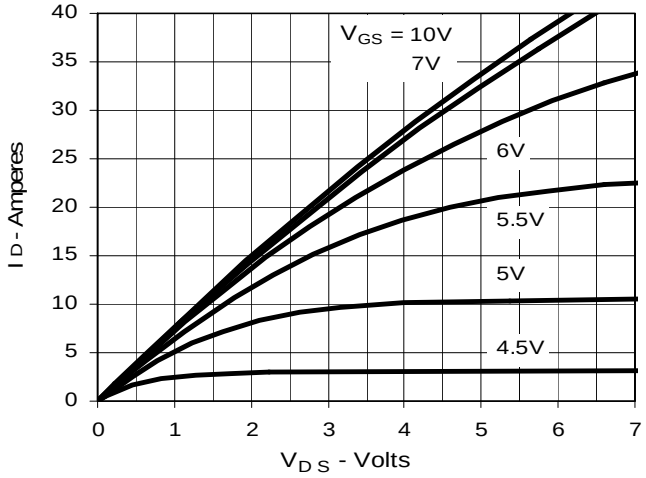


Fig. 2. Extended Output Characteristics @ 25ºC

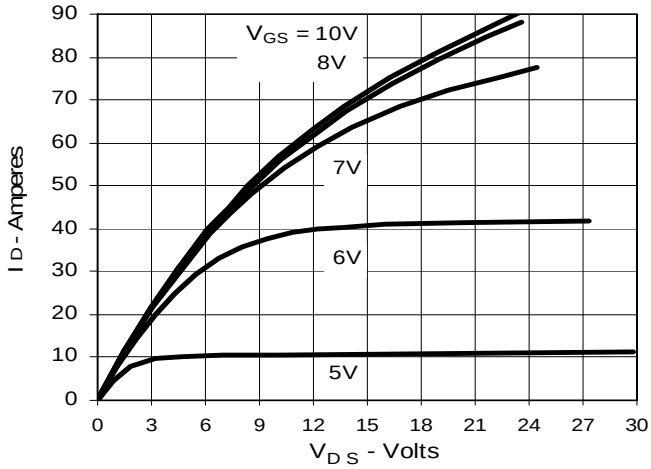


Fig. 3. Output Characteristics @ 125ºC

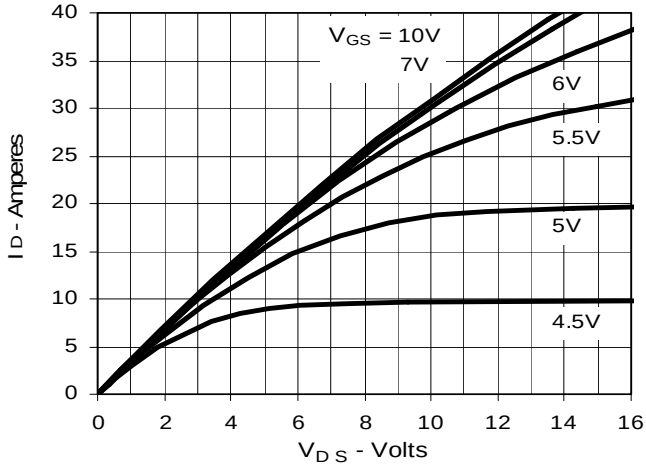


Fig. 4. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. Junction Temperature

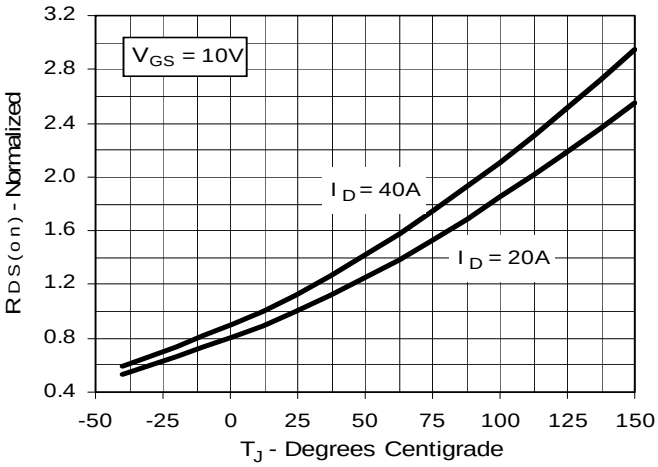


Fig. 5. $R_{DS(on)}$ Normalized to 0.5 I_{D25} Value vs. I_D

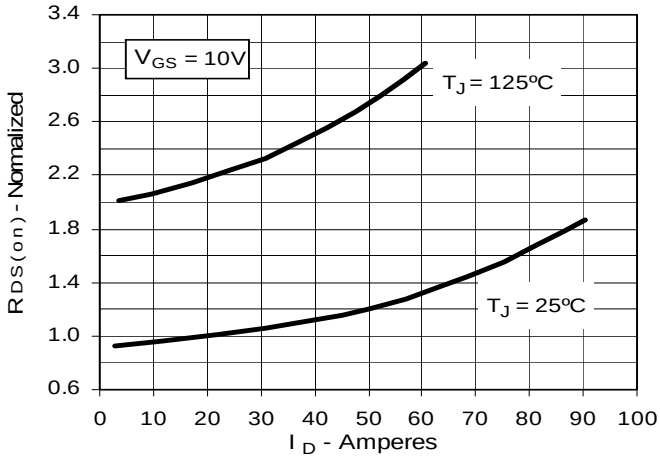
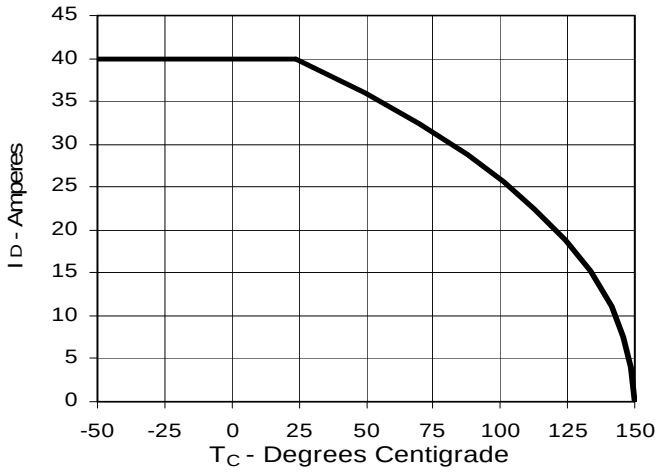


Fig. 6. Drain Current vs. Case Temperature



© 2008 IXYS CORPORATION, All rights reserved

Fig. 7. Input Admittance

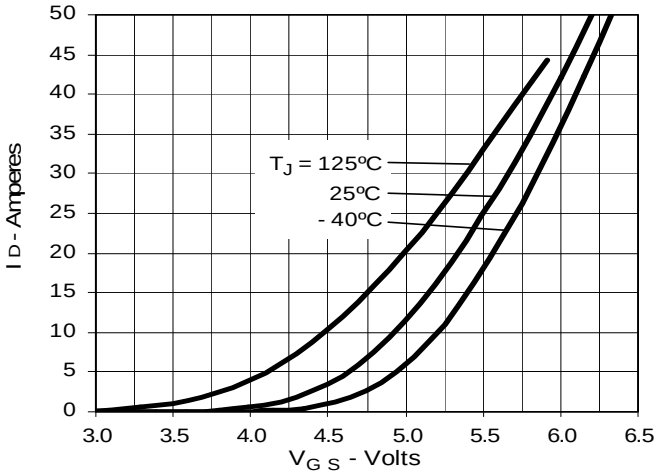


Fig. 8. Transconductance

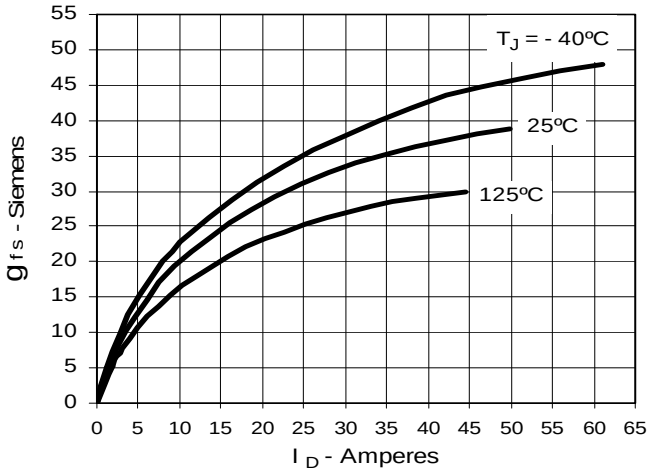


Fig. 9. Source Current vs. Source-To-Drain Voltage

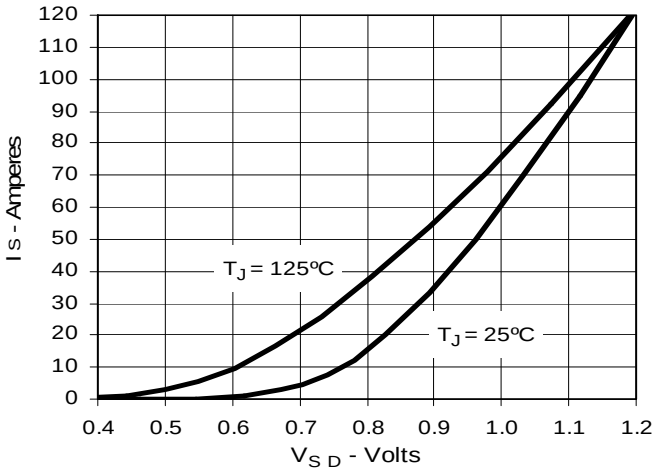


Fig. 10. Gate Charge

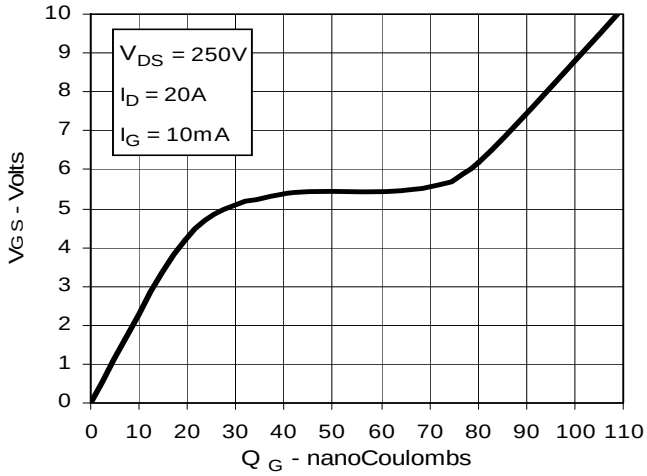


Fig. 11. Capacitance

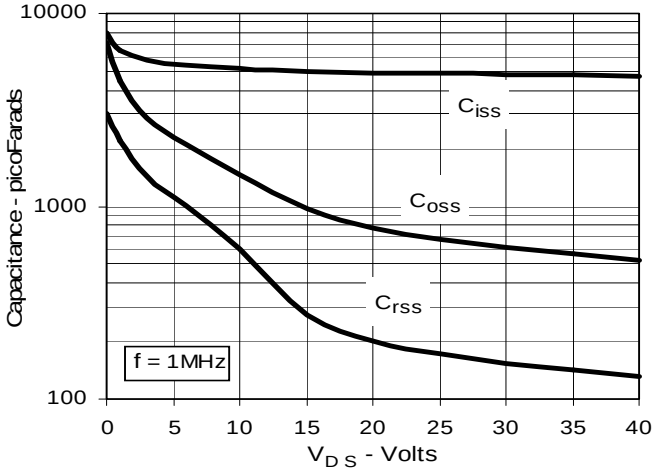
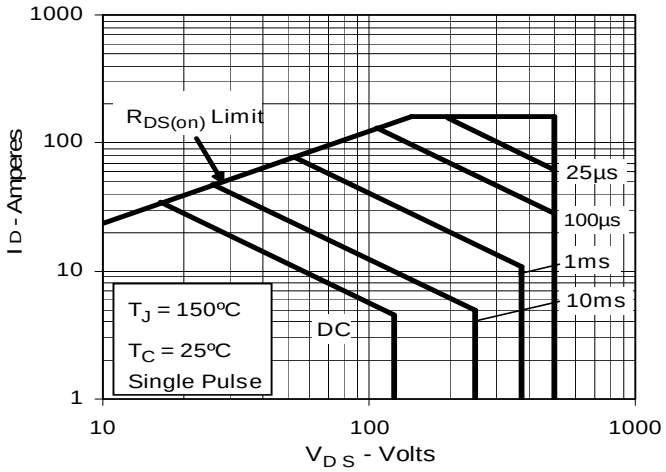
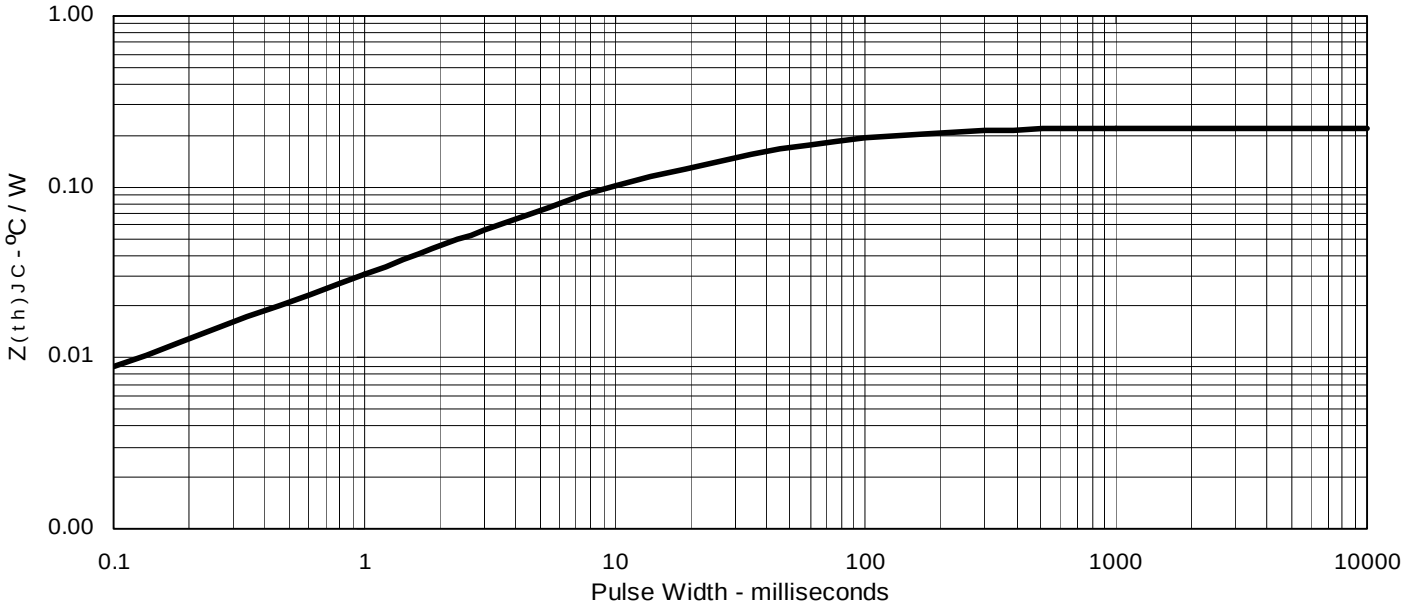


Fig. 12. Forward-Bias Safe Operating Area



IXYS reserves the right to change limits, test conditions, and dimensions.

Fig. 13. Maximum Transient Thermal Impedance



© 2008 IXYS CORPORATION, All rights reserved