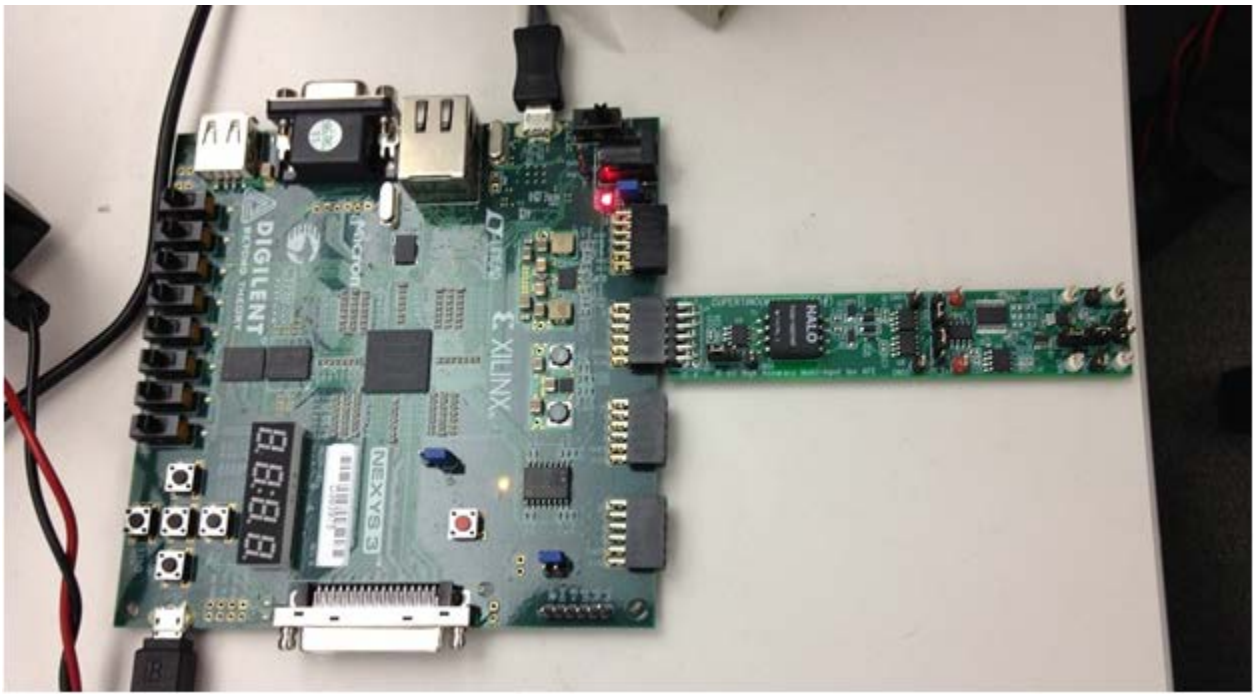
Santa Fe (MAXREFDES5#) Nexys 3 Quick Start Guide

Rev 1; 2/14



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1. Required Equipment

- PC with Windows® OS with Xilinx® ISE®/SDK version 13.4 or later and two USB ports
- License for Xilinx EDK/SDK version 13.4 or later
- Santa Fe (MAXREFDES5#) board
- Nexys™3 development kit
- Industrial sensor or signal source

2. Overview

Below is a high-level overview of the steps required to quickly get the Santa Fe design running by downloading and running the FPGA project. Detailed instructions for each step are provided in the following pages. **The Santa Fe (MAXREFDES5#) subsystem reference design will be referred to as Santa Fe throughout this document.**

1) Connect the Santa Fe board to the JB1 port of a Nexys 3 development kit as shown in Figure 1. Ensure the connector is aligned as shown in Figure 2.
2) Download the latest **RD5V01_00.ZIP** file located at the Santa Fe page.
3) Extract the **RD5V01_00.ZIP** file to a directory on your PC.
4) Open the Xilinx SDK.
5) Download the bitstream (.BIT) file to the board. This bitstream contains the FPGA hardware design and software bootloader.
6) Open a terminal program to communicate with FPGA board.
7) Use Xilinx SDK to download and run the executable file (.ELF) on the MicroBlaze™.

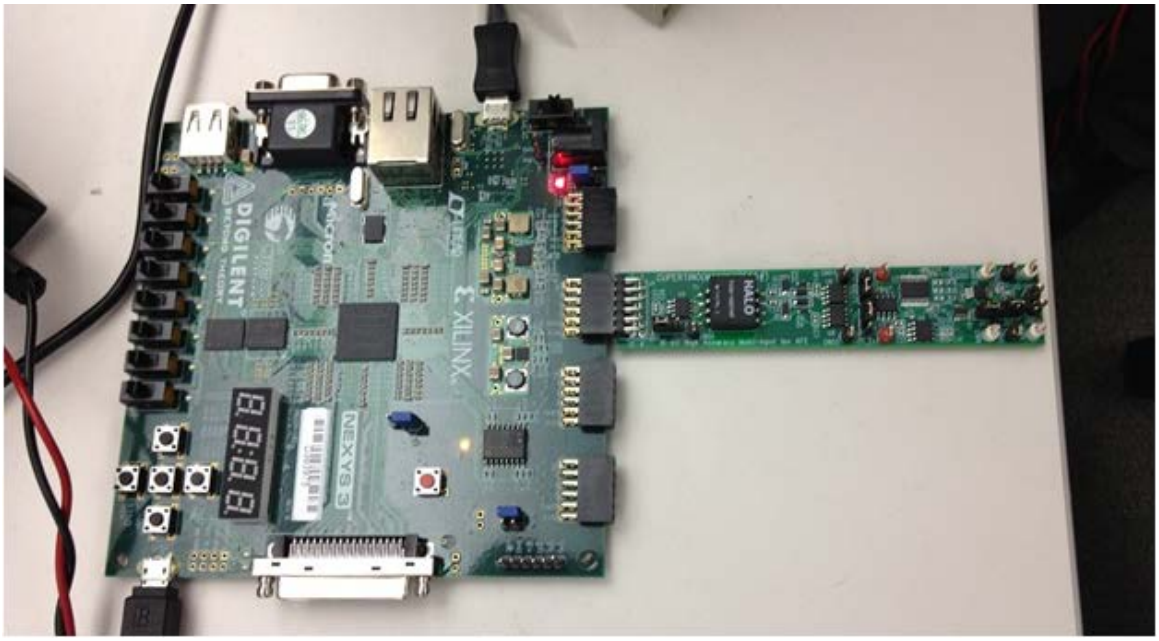


Figure 1. Santa Fe Board Connected to Nexys 3 Development Kit

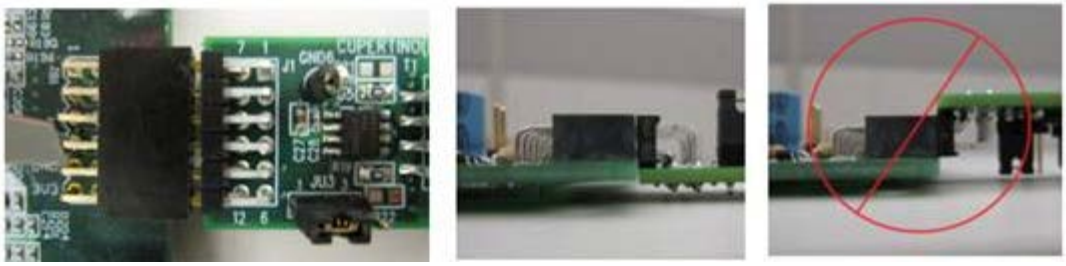


Figure 2. Pmod™ Connector Alignment

3. Included Files

The top level of the hardware design is a Xilinx ISE Project Navigator Project (.XISE) for Xilinx ISE version 13.4. The Verilog-based HDL design instantiates the MicroBlaze core, the support hardware required to run the MicroBlaze, and the peripherals that interface to the Pmod ports. This is supplied as a Xilinx software development kit (SDK) project that includes a demonstration software application to evaluate the Santa Fe subsystem reference design. The lower level c-code driver routines are portable to the user's own software project.

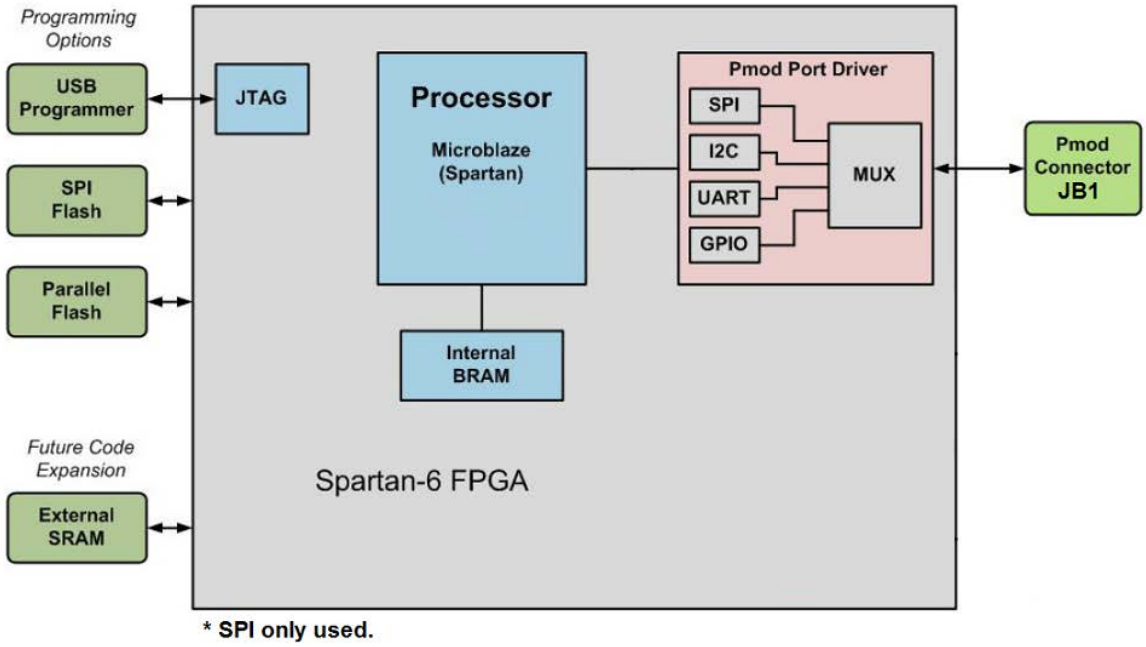


Figure 3. Block Diagram of FPGA Hardware Design

4. Procedure

1. Connect the Santa Fe board to the JB1 port of a Nexys 3 development kit as shown in Figure 1. Power up the Nexys 3 development kit. The Santa Fe board is completely powered from the Nexys 3 development kit and no external power is required.

2. Download the latest **RD5V01_00.ZIP** file at **www.maximintegrated.com/AN5561**. All files available for download are available at the bottom of the page.

3. Extract the **RD5V01_00.ZIP** file to a directory on your PC. The location is arbitrary but the path prior to where you extract the .ZIP file must not exceed 82 characters due to the Windows 250-character total path limitation. For example, this 90-character preceding path would be an example of a path that would be too long:

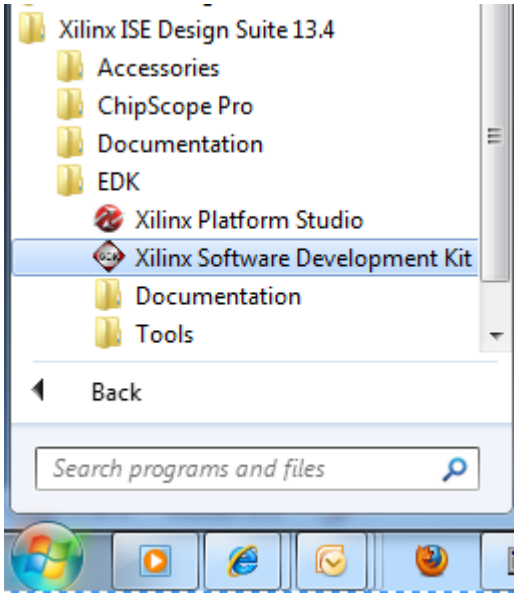
   C:\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\0123456789\RD5V01_00.ZIP
   (This path is too long.)

   In addition, the Xilinx tools require the path to not contain any spaces.

   C:\Do Not Use Spaces In The Path\RD5V01_00.ZIP
   (This path has spaces.)

   For the purposes of this document, it will be **C:\designs\maxim\RD5V01_00**. See **Appendix A: Project Structure and Key Filenames** in this document for the project structure and key filenames.

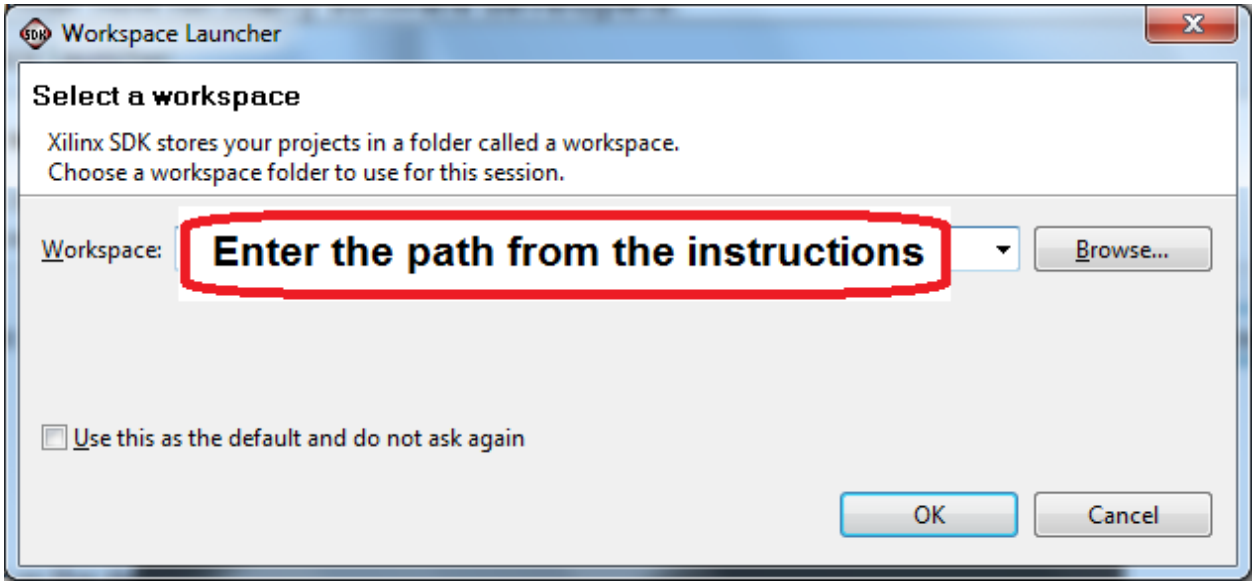
4. Open the **Xilinx Software Development Kit (SDK)** from the Windows **Start** menu.



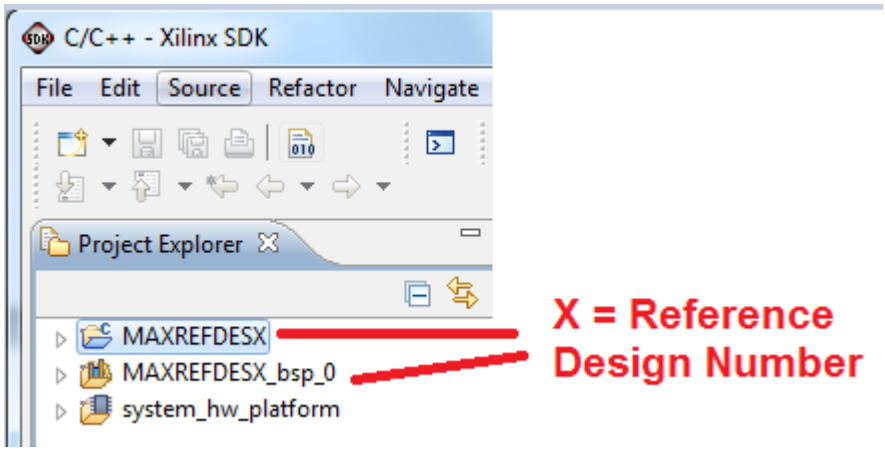
5. SDK will prompt for a workspace directory, which is the location where the software project is located. For this example, it is:

   C:\designs\maxim\RD5V01_00\RD5_NEXYS3_V01_00\Design_Files\sdkWorkspace

   Click **OK** and SDK will open. The Xilinx SDK is based on an Eclipse™-based IDE, so it will be a familiar flow for many software developers.



6. Review the SDK IDE. The **Project Explorer** in the upper left tab should have three components as shown in the image below. If all three subfolders are present, you can skip the next step.

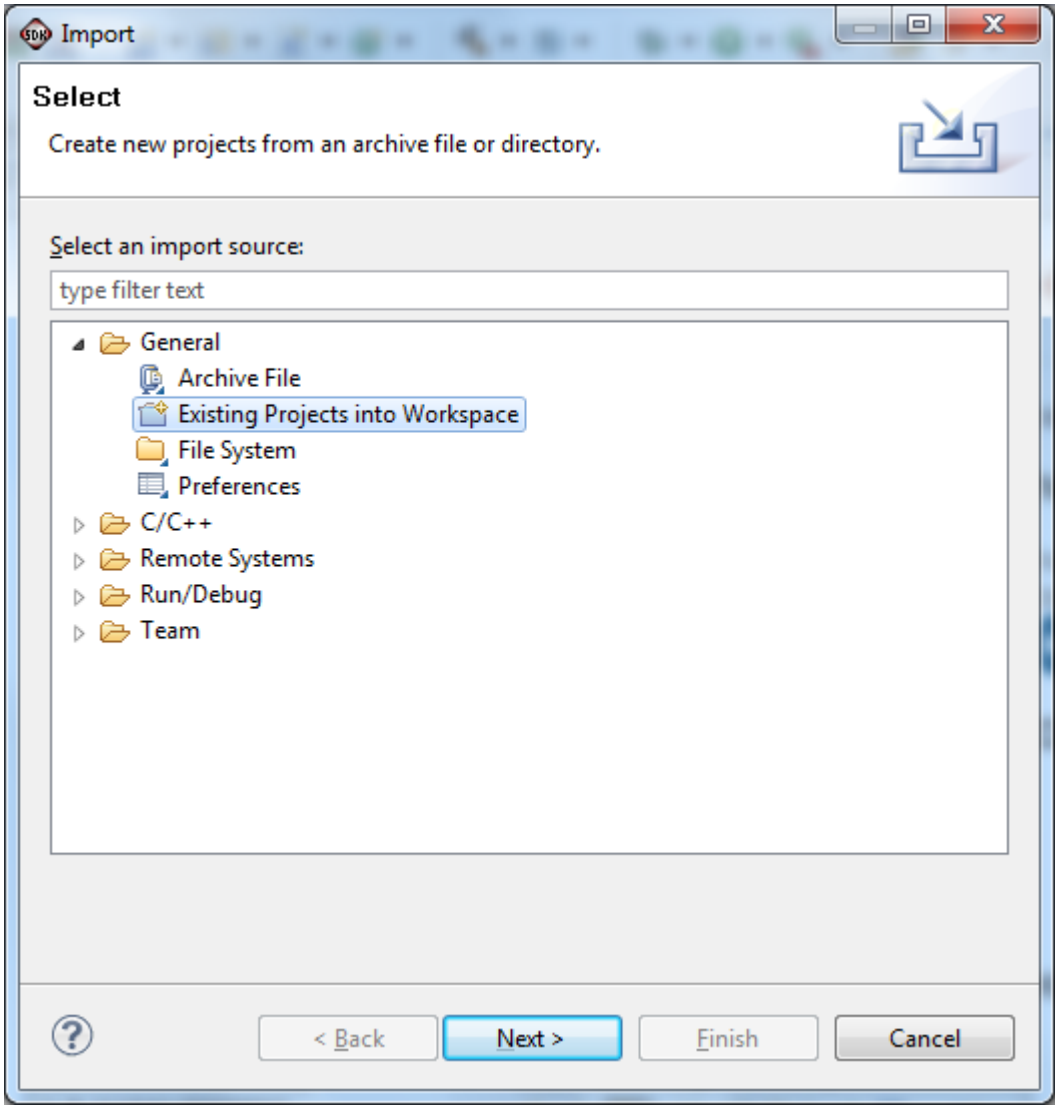


7. If the **Project Explorer** does not contain these three subfolders, launch the **File | Import** menu, expand the **General** folder, and select **Existing Projects into Workspace**. Click **Next**. Set the root directory to:

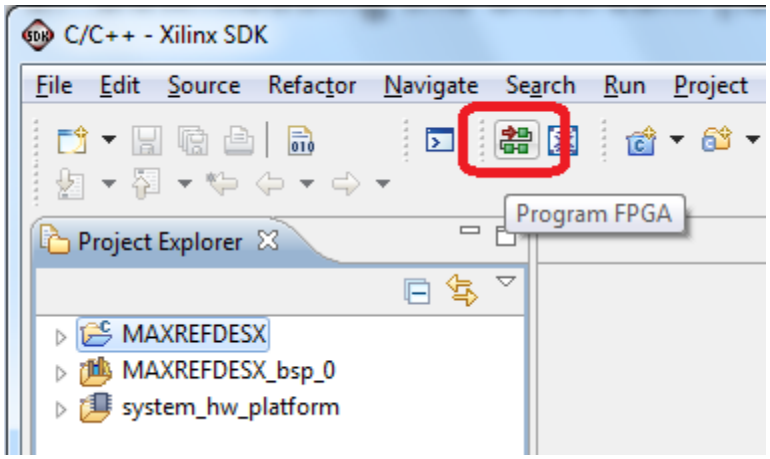
   C:\designs\maxim\RD5V01_00\RD5_NEXYS3_V01_00\Design_Files\sdkWorkspace

   and the missing projects should appear in SDK **Project Explorer** with their checkboxes checked.

   Click **Finish** to import the projects.



8. To download the bitstream (.BIT) file to the board, click on the **Program FPGA** icon (which looks like a green chain of devices).

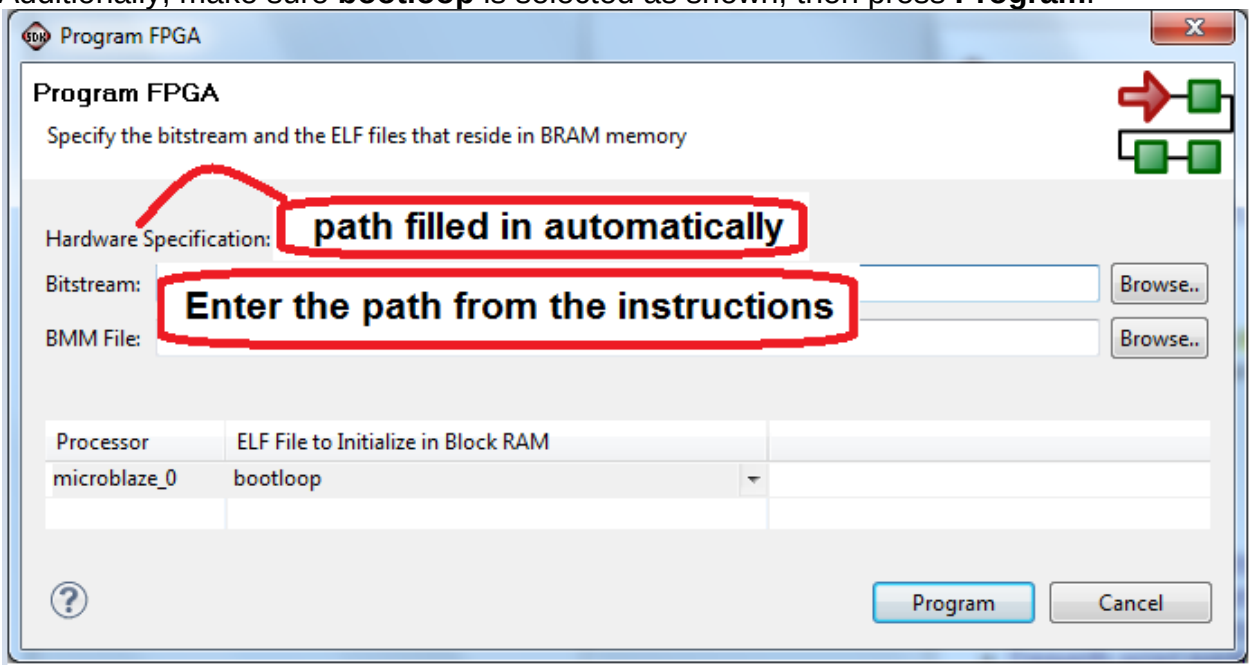


The **Program FPGA** dialog box appears. From here, an FPGA bitstream (.BIT) file is selected as well as an FPGA BMM (.BMM) file. Be sure to select the .BIT file and the .BMM by using the paths below.

Bitstream:
C:\designs\maxim\RD5V01_00\RD5_NEXYS3_V01_00\Design_Files\sdkWorkspace\system_hw_platform\system.bit

BMM File:
C:\designs\maxim\RD5V01_00\RD5_NEXYS3_V01_00\Design_Files\sdkWorkspace\system_hw_platform\system_bd.bmm

Additionally, make sure **bootloop** is selected as shown, then press **Program**.



It takes approximately 10 seconds to download the FPGA, then a message box indicating **FPGA configuration complete** appears.

9. Set up the terminal program to run on the PC using the following steps. Before loading the executable firmware file on the FPGA, the terminal program on the PC should be running. The example firmware running on the FPGA communicates with the PC via a USB port set up to emulate a serial port (UART). To establish this communication link, the PC must be configured with the appropriate Windows drivers. A suitable terminal program such as Tera Term or HyperTerminal should be invoked.

   The Nexys 3 utilizes the FTDI FT232 USB-UART bridge IC, so you need to install FTDI's virtual COM port (VCP) driver for the FT232 device family. Make sure to choose the driver that supports a **Virtual Com Port**, also known as VCP. These can be obtained from the FTDI website (www.ftdichip.com).

   Once installed, Windows assigns a previously unused COM port. Use the Windows **Control Panel | System | Device Manager** to determine the COM port number. (It will be named **USB Serial Port**). Make a note of which COM port this is. That information is needed in the next step.

   Next, a terminal emulation program needs to be installed and launched. For Windows XP® and earlier systems, the HyperTerminal program is the usual choice. However, since HyperTerminal was eliminated from Windows 7, it may be necessary to locate an alternative. Several are available; one good choice is called Tera Term (http://ttssh2.sourceforge.jp/). Whatever terminal program you

choose, the communication should be set up by opening the COM port number previously described above and the port configured as:

bits per second: **460,800**;

data bits: **8**;

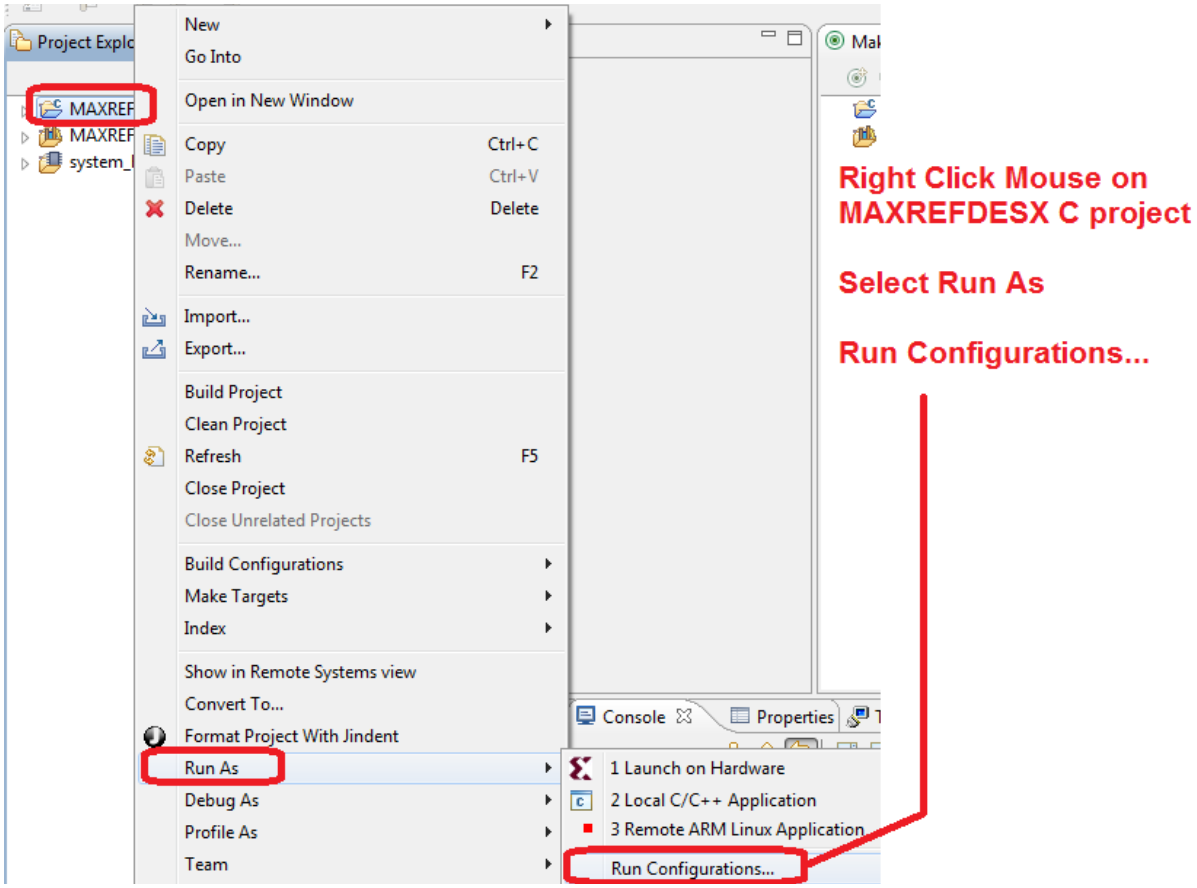
parity: **none**;

stop bits: **1**;

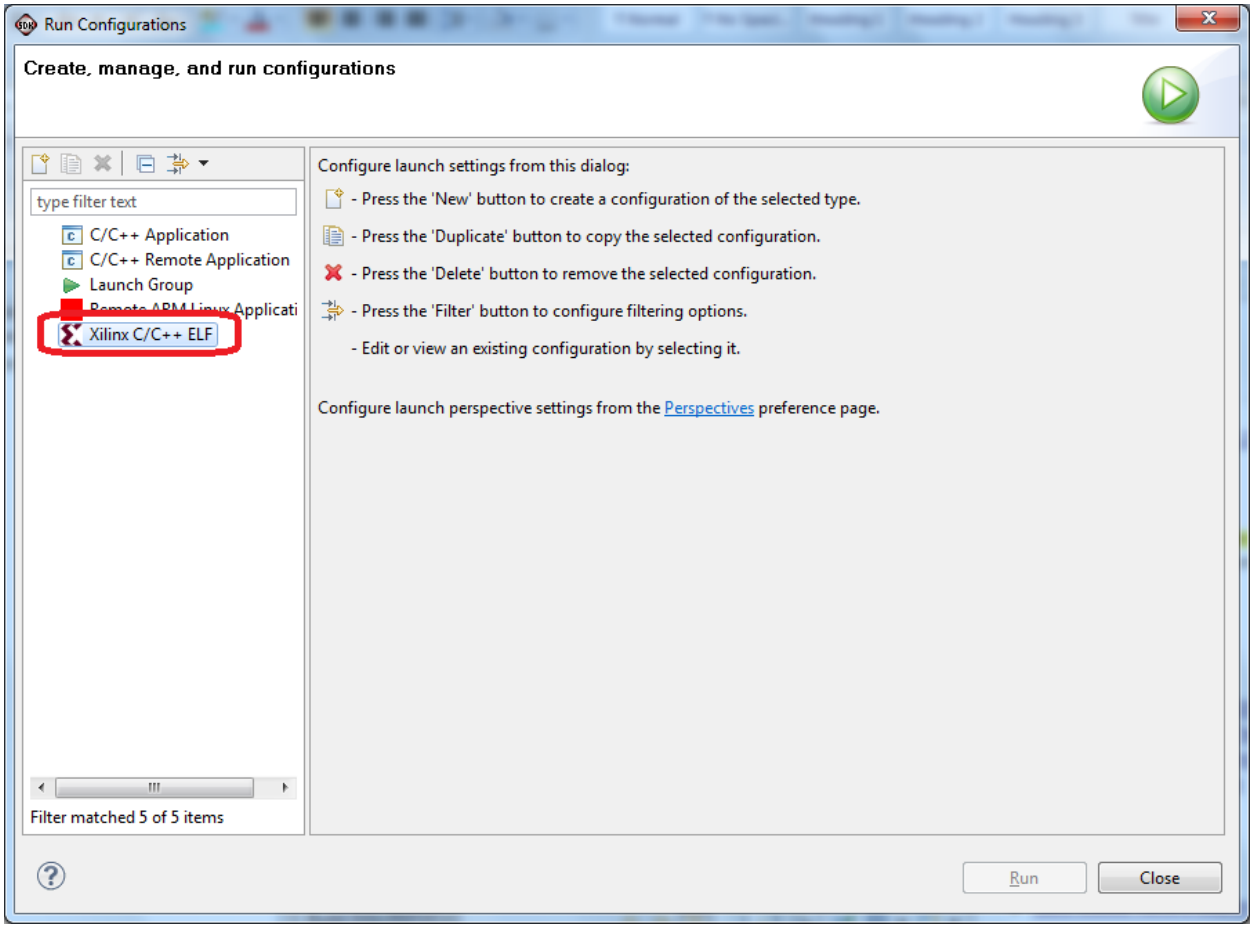
flow control: **none**.

10. Use the Xilinx SDK to download and run the executable ELF (.ELF) file on the MicroBlaze using the following steps.

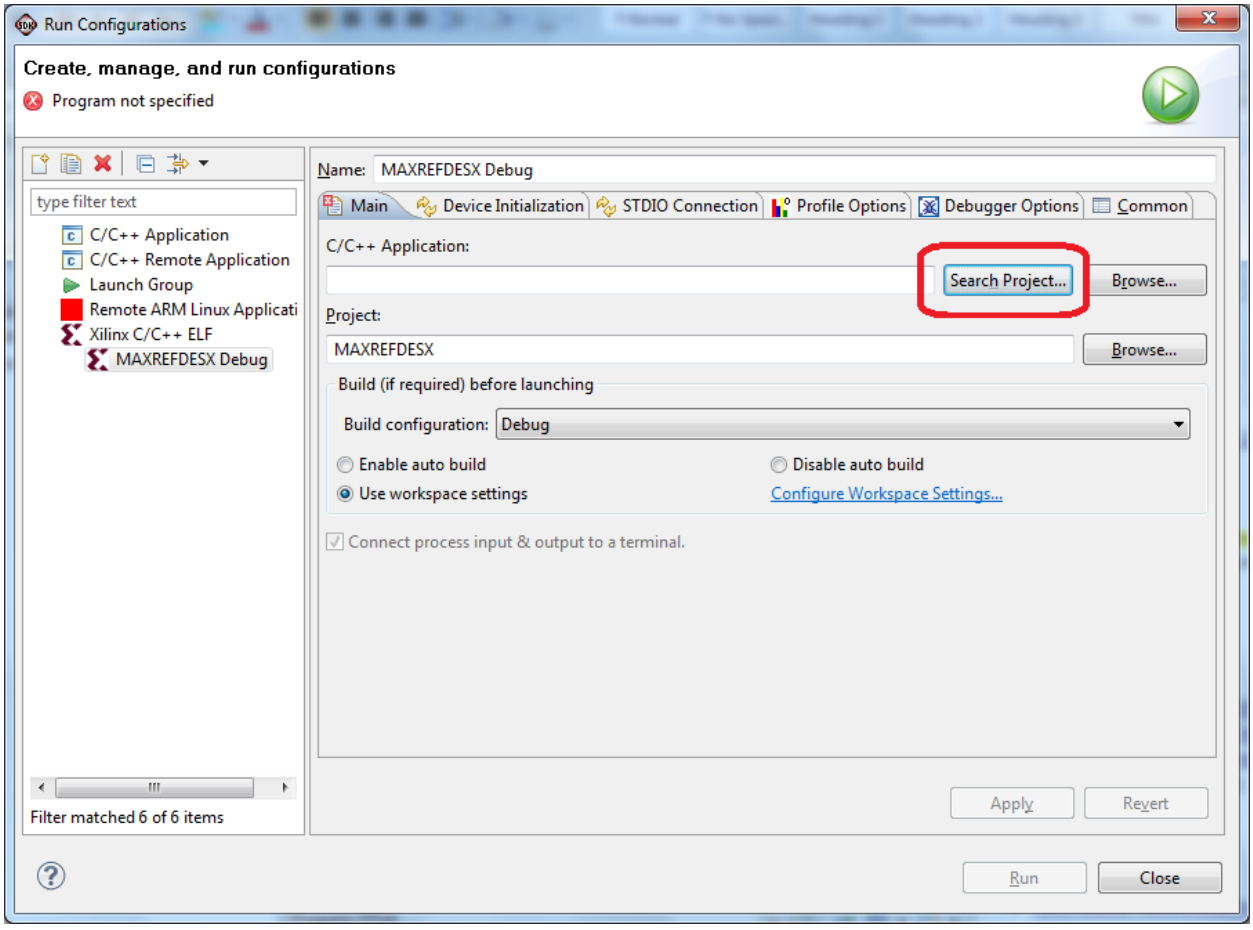
    Right-click the mouse while the **MAXREFDES5 C** project is selected, choose the **Run As** menu, and then **Run Configurations…** menu as shown below.



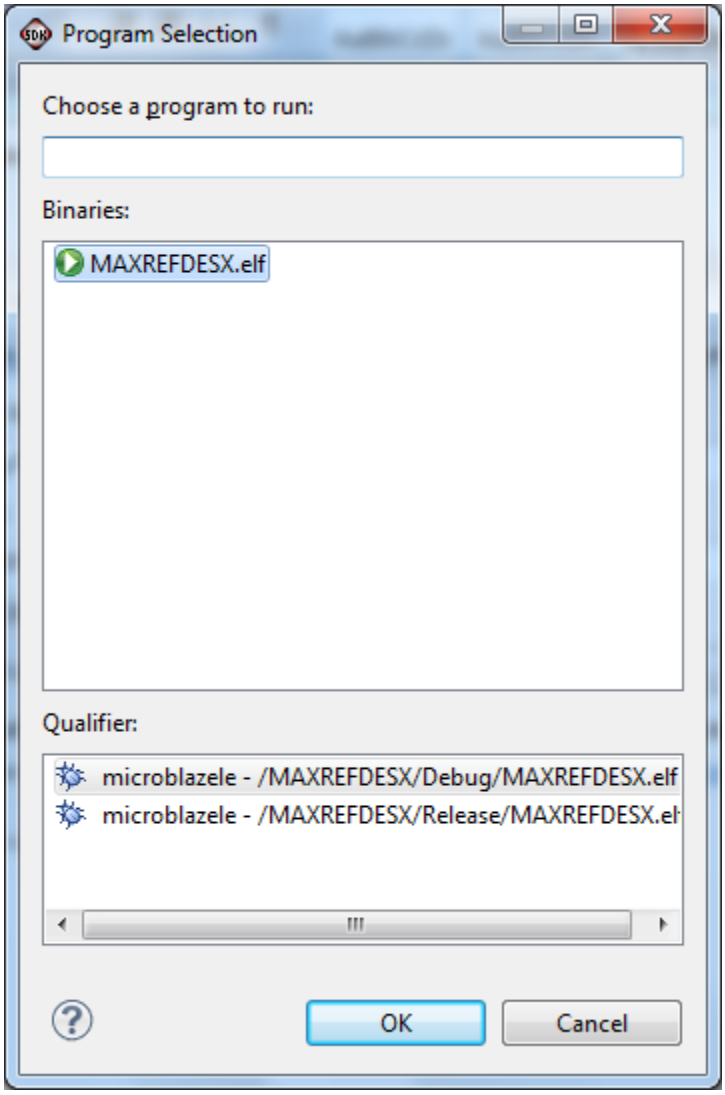
Next, double-click the mouse on the **Xilinx C/C++ ELF** menu.



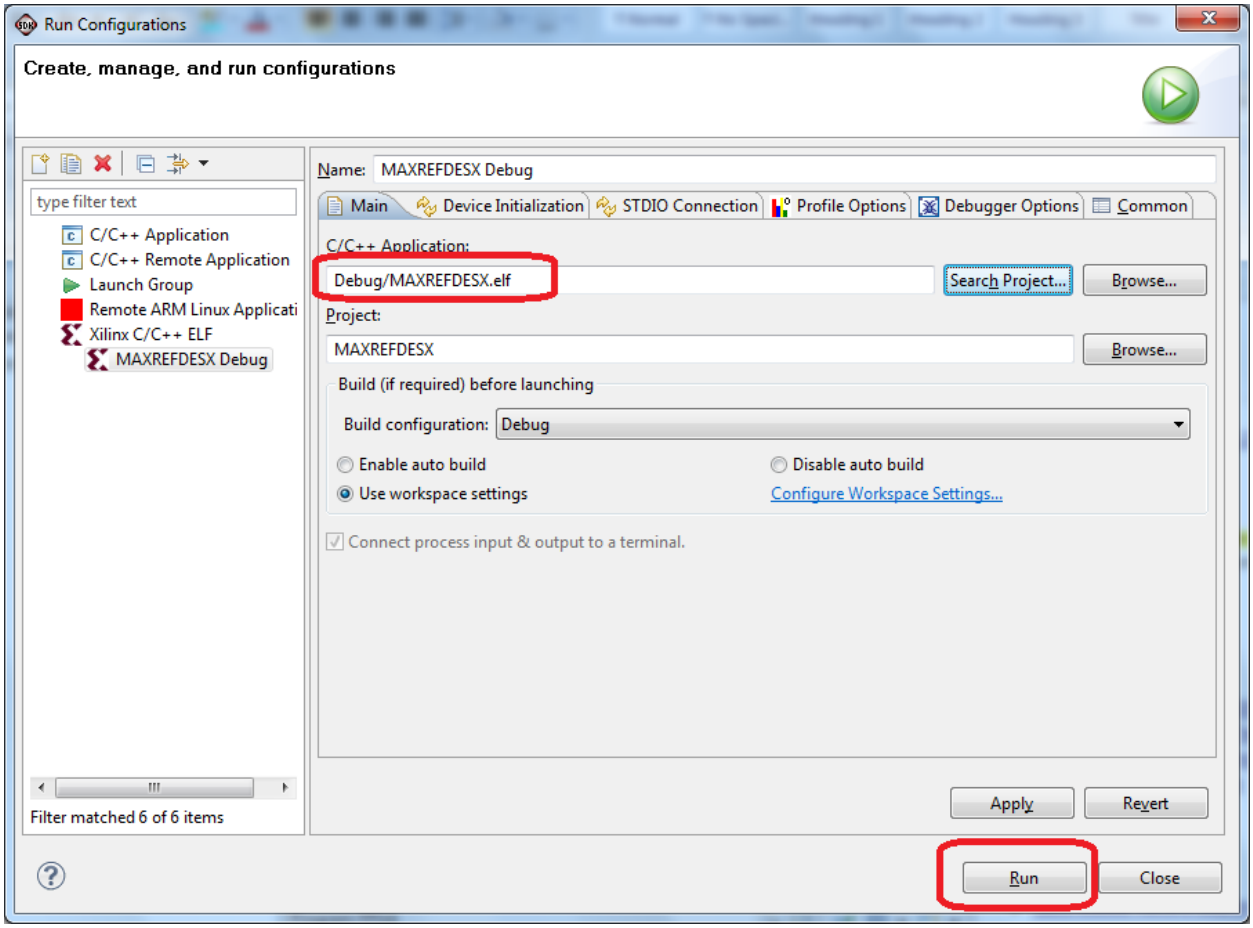
Next, press the **Search Project** button.



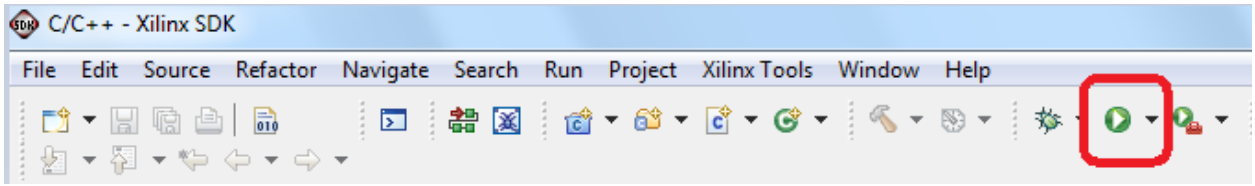
Double-click on the **MAXREFDES5.elf** binary.



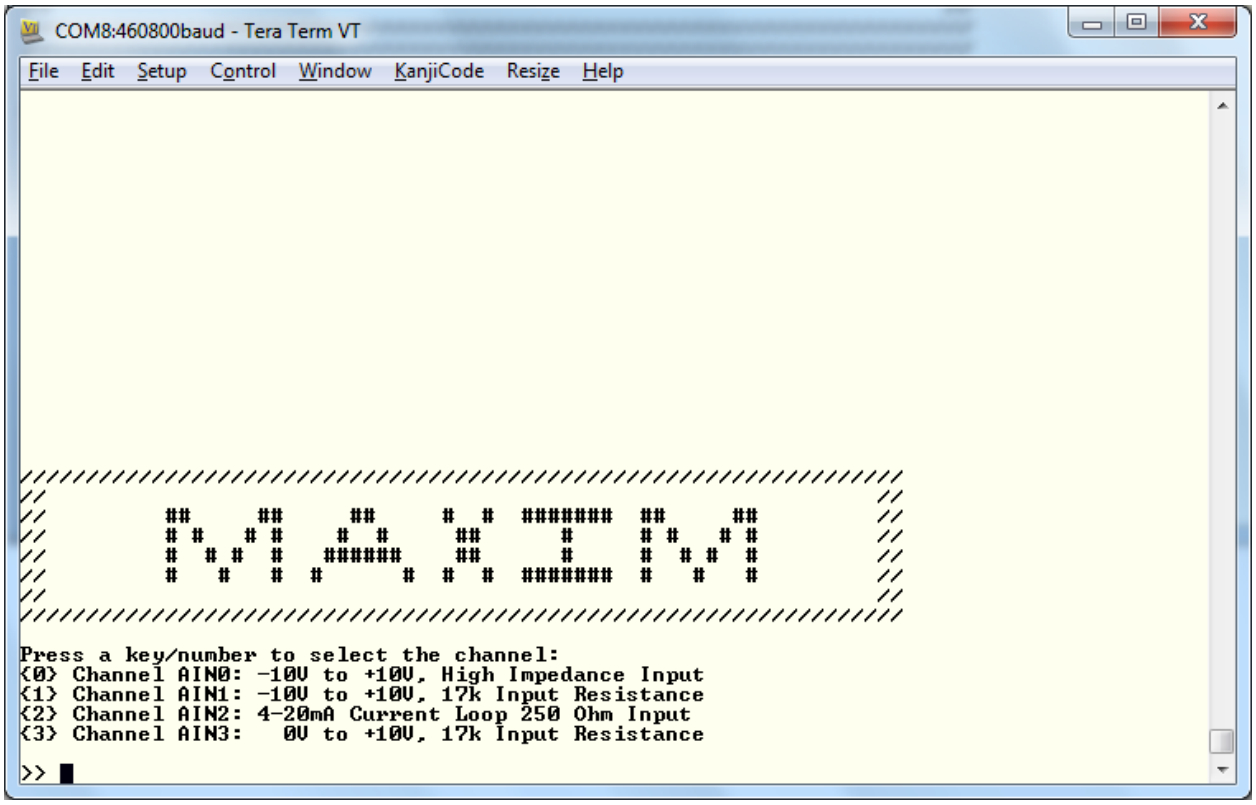
Verify the application is selected and press the **Run** button.



Once the Debug/MAXREFDES5 configuration is set up once, you just need to press the **Run** button if you ever want to run the program again.

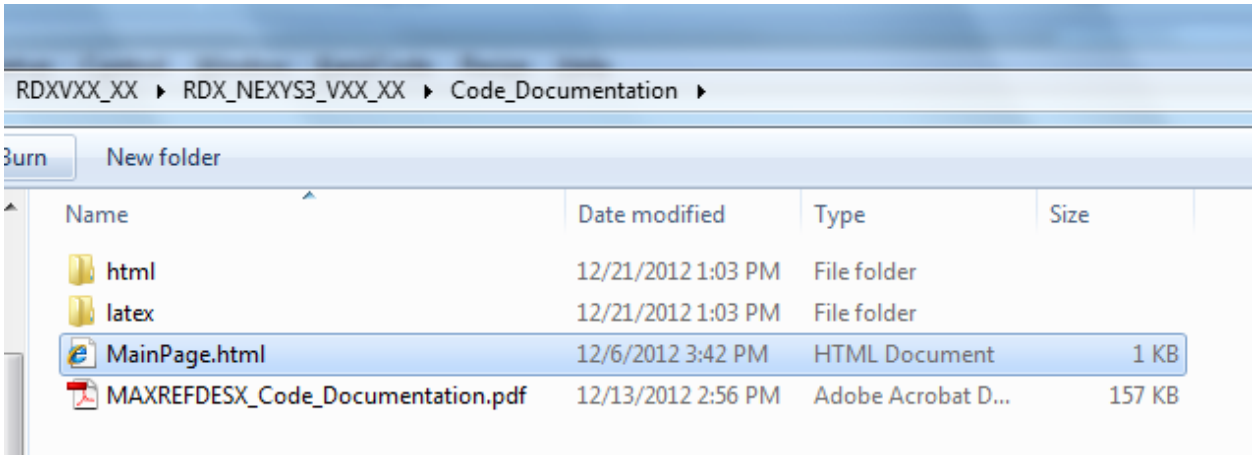


At this point, the application is running on the MicroBlaze and the terminal program should show the menu below. Make the desired selections by pressing the appropriate keys on the keyboard. For example, to select channel AIN0, press **0**.



5. Code Documentation

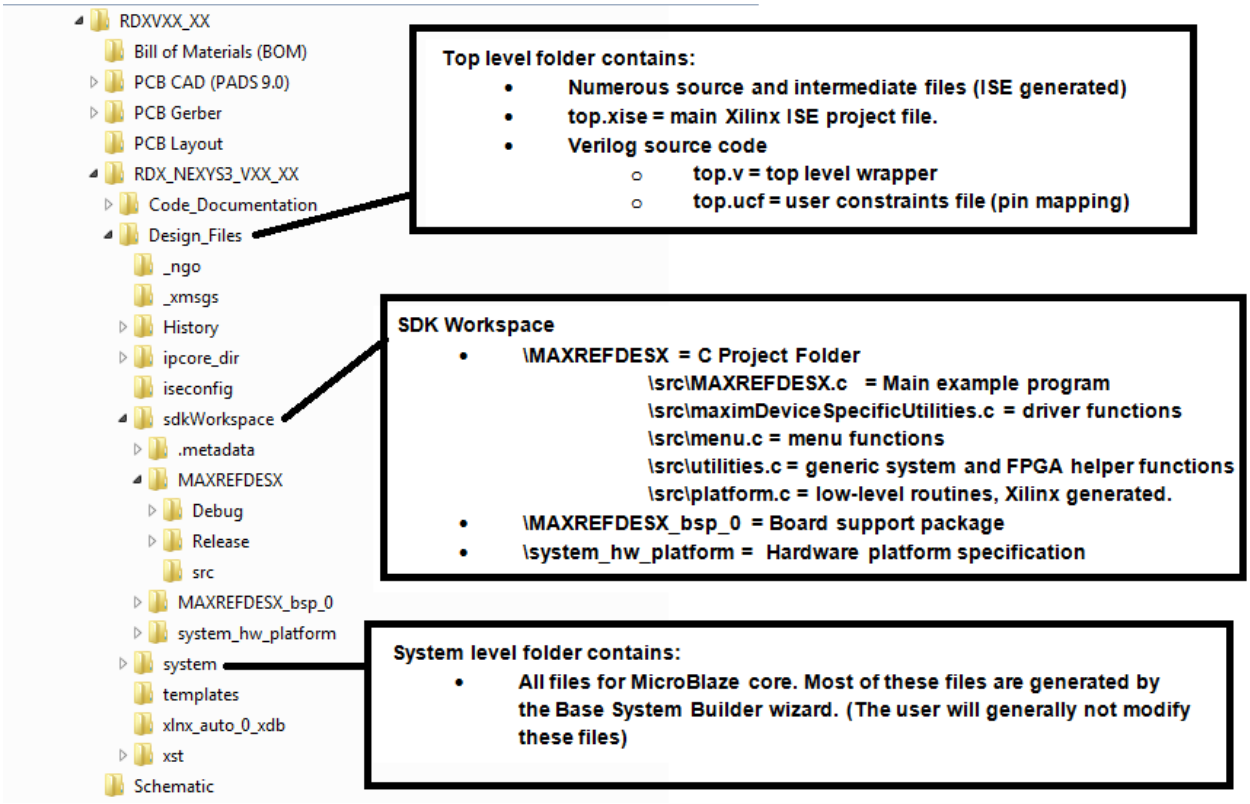
Code documentation can be found at:
C:\...\RD5V01_00\RD5_NEXYS3_V01_00\Code_Documentation



To view the code documentation in HTML format with a browser, open the **MainPage.html** file.

To view the code documentation in .PDF format with a PDF reader, open the **MAXREFDES5_Code_Documentation.pdf** file.

6. Appendix A: Project Structure and Key Filenames



7. Trademarks

Eclipse is a trademark of Eclipse Foundation, Inc.
MicroBlaze is a trademark of Xilinx, Inc.
Nexys is a trademark of Digilent, Inc.
Pmod is a trademark of Digilent, Inc.
Spartan is a registered trademark of Xilinx, Inc.
Windows is a registered trademark and registered service mark and Windows XP is a registered trademark of Microsoft Corporation.
Xilinx is a registered trademark and registered service mark of Xilinx, Inc.

8. Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/13	Initial release	—
1	2/14	Replaced the board name “Cupertino” with “Santa Fe”	All