11 mW Power, 2.3 V to 5.5 V, Complete DDS

AD9838

FEATURES

2.3 V to 5.5 V power supply
MCLK speed: 16 MHz (B grade), 5 MHz (A grade)
Output frequency up to 8 MHz
Sinusoidal and triangular outputs
On-board comparator
3-wire SPI interface
Extended temperature range: –40°C to +125°C
Power-down option
11 mW power consumption at 2.3 V
20-lead LFCSP

APPLICATIONS

Frequency stimulus/waveform generation
Frequency phase tuning and modulation
Low power RF/communications systems
Liquid and gas flow measurement
Sensory applications: proximity, motion, and defect detection
Test and medical equipment

GENERAL DESCRIPTION

The AD9838 is a low power DDS device capable of producing high performance sine and triangular outputs. It also has an on-board comparator that allows a square wave to be produced for clock generation. Consuming only 11 mW of power at 2.3 V, the AD9838 is an ideal candidate for power-sensitive applications.

Capability for phase modulation and frequency modulation is provided. The frequency registers are 28 bits wide: with a 16 MHz clock rate, resolution of 0.06 Hz can be achieved; with a 5 MHz clock rate, the AD9838 can be tuned to 0.02 Hz resolution. Frequency and phase modulation are configured by loading registers through the serial interface and by toggling the registers using software or the FSELECT and PSELECT pins, respectively.

The AD9838 is written to via a 3-wire serial interface. This serial interface operates at clock rates up to 40 MHz and is compatible with DSP and microcontroller standards.

The device operates with a power supply from 2.3 V to 5.5 V. The analog and digital sections are independent and can be run from different power supplies; for example, AVDD can equal 5 V with DVDD equal to 3 V.

The AD9838 has a power-down pin (SLEEP) that allows external control of the power-down mode. Sections of the device that are not being used can be powered down to minimize current consumption. For example, the DAC can be powered down when a clock output is being generated.

The AD9838 is available in a 20-lead LFCSP_WQ package.

FUNCTIONAL BLOCK DIAGRAM

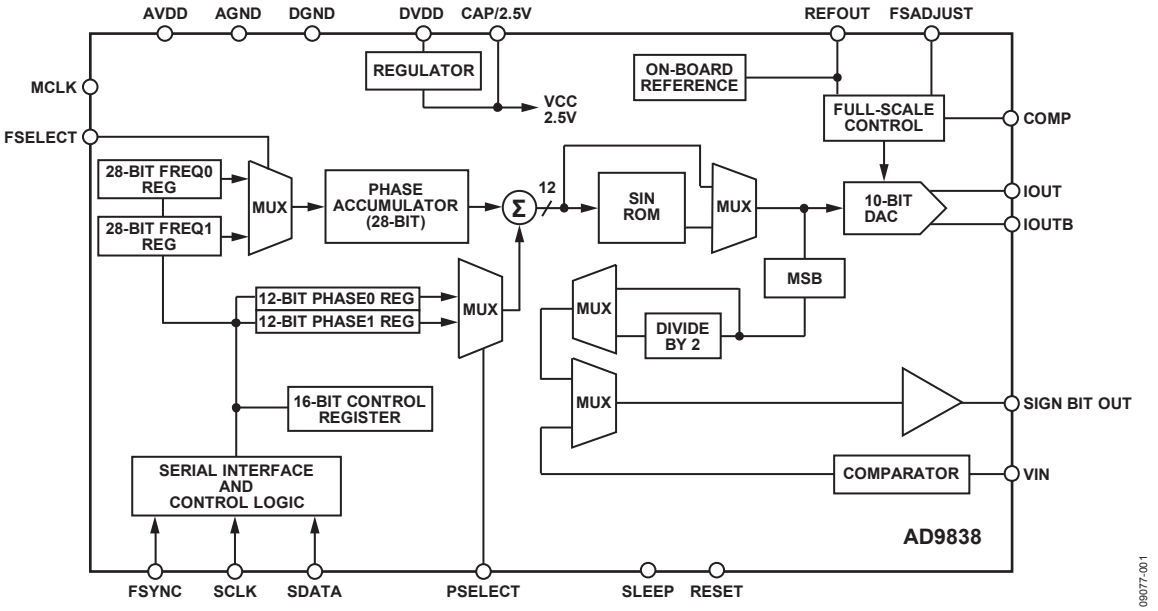

Figure 1.

Rev. A

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REVISION HISTORY

4/11—Rev. 0 to Rev. A

Change to Title ... 1
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4/11—Revision 0: Initial Version

SPECIFICATIONS

AVDD = DVDD = 2.3 V to 5.5 V, AGND = DGND = 0 V, $T_A = T_{MIN}$ to T_{MAX}, R_{SET} = 6.8 kΩ, R_{LOAD} = 200 Ω for IOUT and IOUTB, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
SIGNAL DAC SPECIFICATIONS					
Resolution		10		Bits	
Update Rate					
A Grade			5	MSPS	
B Grade			16	MSPS	
I_{OUT} Full Scale[2]		3.0		mA	
V_{OUT} Maximum		0.6		V	
V_{OUT} Minimum		30		mV	
Output Compliance[3]			0.8	V	
DC Accuracy					
Integral Nonlinearity (INL)		±1		LSB	
Differential Nonlinearity (DNL)		±0.5		LSB	
DDS SPECIFICATIONS					
Dynamic Specifications					
Signal-to-Noise Ratio (SNR)					
A Grade		−63		dB	f_{MCLK} = 5 MHz, $f_{OUT} = f_{MCLK}/4096$
B Grade		−64		dB	f_{MCLK} = 16 MHz, $f_{OUT} = f_{MCLK}/4096$
Total Harmonic Distortion (THD)					
A Grade		−64		dBc	f_{MCLK} = 5 MHz, $f_{OUT} = f_{MCLK}/4096$
B Grade		−64		dBc	f_{MCLK} = 16 MHz, $f_{OUT} = f_{MCLK}/4096$
Spurious-Free Dynamic Range (SFDR)					
Wideband (0 to Nyquist)					
A Grade		−68		dBc	f_{MCLK} = 5 MHz, $f_{OUT} = f_{MCLK}/50$
B Grade		−66		dBc	f_{MCLK} = 16 MHz, $f_{OUT} = f_{MCLK}/50$
Narrow-Band (±200 kHz)					
A Grade		−97		dBc	f_{MCLK} = 5 MHz, $f_{OUT} = f_{MCLK}/50$
B Grade		−92		dBc	f_{MCLK} = 16 MHz, $f_{OUT} = f_{MCLK}/50$
Clock Feedthrough					
A Grade		−68		dBc	f_{MCLK} = 5 MHz, f_{OUT} = reset
B Grade		−65		dBc	f_{MCLK} = 16 MHz, f_{OUT} = reset
Wake-Up Time		1		ms	
COMPARATOR					
Input Voltage Range			1	V p-p	AC-coupled internally
Input Capacitance		10		pF	
Input High-Pass Cutoff Frequency		3		MHz	
Input DC Resistance		5		MΩ	
Input Leakage Current			10	µA	
OUTPUT BUFFER					
Output Rise/Fall Time		12		ns	Using a 15 pF load
Output Jitter		120		ps rms	3 MHz sine wave 0.6 V p-p
VOLTAGE REFERENCE					
Internal Reference	1.11	1.18	1.24	V	
REFOUT Output Impedance[4]		1		kΩ	
Reference TC		100		ppm/°C	
FSADJUST Voltage		1.14		V	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
Input High Voltage, V_{INH}	1.7			V	2.3 V to 2.7 V power supply
	2.0			V	2.7 V to 3.6 V power supply
	2.8			V	4.5 V to 5.5 V power supply
Input Low Voltage, V_{INL}			0.6	V	2.3 V to 2.7 V power supply
			0.7	V	2.7 V to 3.6 V power supply
			0.8	V	4.5 V to 5.5 V power supply
Input Current, I_{INH}/I_{INL}			10	μA	
Input Capacitance, C_{IN}		3		pF	
POWER SUPPLIES					
AVDD	2.3		5.5	V	f_{MCLK} = 16 MHz, $f_{OUT} = f_{MCLK}/4096$
DVDD	2.3		5.5	V	
I_{AA}[5]		3.7	5	mA	
I_{DD}[5]					I_{DD} code dependent; see Figure 7
A Grade		0.9	2	mA	
B Grade		1.2	2.4	mA	
$I_{AA} + I_{DD}$[5]					See Figure 6
A Grade		4.6	7	mA	
B Grade		4.9	7.4	mA	
Low Power Sleep Mode					DAC powered down; see Table 17
A Grade		0.4		mA	
B Grade		0.4		mA	

[1] Operating temperature range is −40°C to +125°C; typical specifications are at 25°C.
[2] For compliance with the specified load of 200 Ω, I_{OUT} full scale should not exceed 4 mA.
[3] Guaranteed by design.
[4] Applies when REFOUT is sourcing current. The impedance is higher when REFOUT is sinking current.
[5] Measured with the digital inputs static and equal to 0 V or DVDD.

TIMING CHARACTERISTICS

DVDD = 2.3 V to 5.5 V, AGND = DGND = 0 V, unless otherwise noted.

Table 2.

Parameter[1]	Limit at T_{MIN} to T_{MAX}	Unit	Description
t_1	200/62.5	ns min	MCLK period (5 MHz/16 MHz)
t_2	80/26	ns min	MCLK high duration (5 MHz/16 MHz)
t_3	80/26	ns min	MCLK low duration (5 MHz/16 MHz)
t_4	25	ns min	SCLK period
t_5	10	ns min	SCLK high duration
t_6	10	ns min	SCLK low duration
t_7	5	ns min	FSYNC to SCLK falling edge setup time
t_8	10	ns min	SCLK falling edge to FSYNC rising edge time
	$t_4 - 5$	ns max	
t_9	5	ns min	Data setup time
t_{10}	3	ns min	Data hold time
t_{11}	8	ns min	FSELECT, PSELECT setup time before MCLK rising edge
t_{11A}	8	ns min	FSELECT, PSELECT setup time after MCLK rising edge
t_{12}	5	ns min	SCLK high to FSYNC falling edge setup time

[1] Guaranteed by design; not production tested.

Timing Diagrams

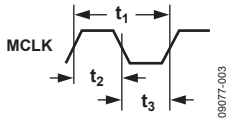


Figure 2. Master Clock

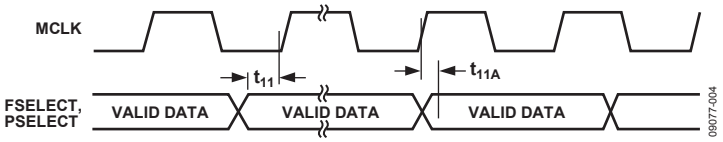


Figure 3. Control Timing

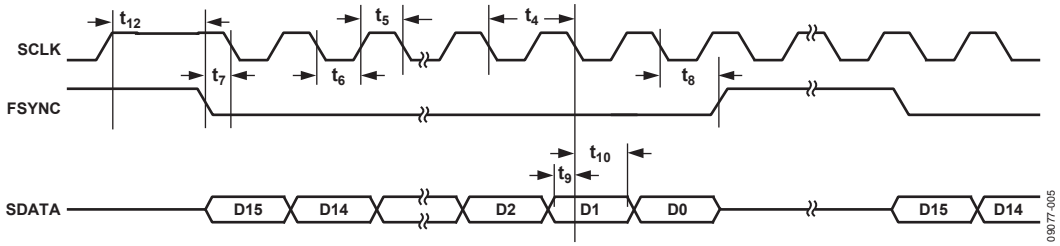


Figure 4. Serial Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AVDD to AGND	−0.3 V to +6 V
DVDD to DGND	−0.3 V to +6 V
AVDD to DVDD	−0.3 V to +0.3 V
AGND to DGND	−0.3 V to +0.3 V
CAP/2.5V	2.75 V
Digital I/O Voltage to DGND	−0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND	−0.3 V to AVDD + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C
Reflow Soldering (Pb Free)	
Peak Temperature	260°C (+0/−5)
Time at Peak Temperature	10 sec to 40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead LFCSP_WQ (CP-20-10)	49.5	5.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

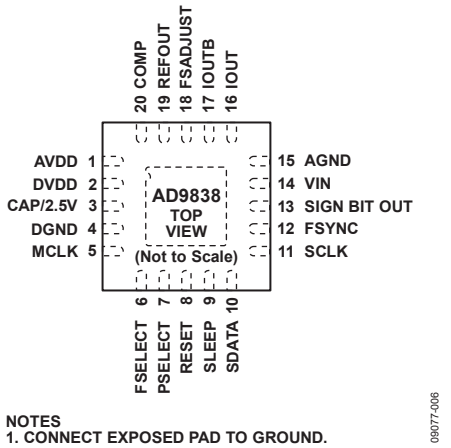


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	AVDD	Positive Power Supply for the Analog Section. AVDD can have a value from 2.3 V to 5.5 V. A 0.1 µF decoupling capacitor should be connected between AVDD and AGND.
2	DVDD	Positive Power Supply for the Digital Section. DVDD can have a value from 2.3 V to 5.5 V. A 0.1 µF decoupling capacitor should be connected between DVDD and DGND.
3	CAP/2.5V	The digital circuitry operates from a 2.5 V power supply. This 2.5 V is generated from DVDD using an on-board regulator when DVDD exceeds 2.7 V. The regulator requires a decoupling capacitor of 100 nF typical, which is connected from CAP/2.5V to DGND. If DVDD is less than or equal to 2.7 V, CAP/2.5V should be shorted to DVDD.
4	DGND	Digital Ground.
5	MCLK	Digital Clock Input. DDS output frequencies are expressed as a binary fraction of the frequency of MCLK. The output frequency accuracy and phase noise are determined by this clock.
6	FSELECT	Frequency Select Input. FSELECT controls which frequency register, FREQ0 or FREQ1, is used in the phase accumulator. The frequency register to be used can be selected using the FSELECT pin or the FSEL bit. When the FSEL bit is used to select the frequency register, the FSELECT pin should be tied to CMOS high or low.
7	PSELECT	Phase Select Input. PSELECT controls which phase register, PHASE0 or PHASE1, is added to the phase accumulator output. The phase register to be used can be selected using the PSELECT pin or the PSEL bit. When the PSEL bit is used to select the phase register, the PSELECT pin should be tied to CMOS high or low.
8	RESET	Active High Digital Input. This pin resets the appropriate internal registers to 0 (this corresponds to an analog output of midscale). RESET does not affect any of the addressable registers.
9	SLEEP	Active High Digital Input. When this pin is high, the DAC is powered down. This pin has the same function as the SLEEP12 control bit.
10	SDATA	Serial Data Input. The 16-bit serial data-word is applied to this input.
11	SCLK	Serial Clock Input. Data is clocked into the AD9838 on each falling edge of SCLK.
12	FSYNC	Active Low Control Input. FSYNC is the frame synchronization signal for the input data. When FSYNC is taken low, the internal logic is informed that a new word is being loaded into the device.
13	SIGN BIT OUT	Logic Output. The comparator output is available on this pin or, alternatively, the MSB from the NCO can be output on this pin. Setting the OPBITEN bit in the control register to 1 enables this output pin. The SIGN/PIB bit determines whether the comparator output or the MSB from the NCO is output on this pin.
14	VIN	Input to Comparator. The comparator can be used to generate a square wave from the sinusoidal DAC output. The DAC output should be filtered appropriately before it is applied to the comparator to reduce jitter. When the OPBITEN and SIGN/PIB bits in the control register are set to 1, the comparator input is connected to VIN.
15	AGND	Analog Ground.
16, 17	IOUT, IOUTB	Current Output. This is a high impedance current source. A load resistor of nominally 200 Ω should be connected between IOUT and AGND. IOUTB should be tied to AGND through an external load resistor of 200 Ω, but it can be tied directly to AGND. A 20 pF capacitor to AGND is also recommended to prevent clock feedthrough.

Pin No.	Mnemonic	Description
18	FSADJUST	Full-Scale Adjust Control. A resistor (R_{SET}) is connected between this pin and AGND to determine the magnitude of the full-scale DAC current. The relationship between R_{SET} and the full-scale current is as follows: $IOUT_{FULL\ SCALE} = 18 \times FSADJUST/R_{SET}$ $FSADJUST$ = 1.14 V nominal, R_{SET} = 6.8 kΩ typical
19	REFOUT	Voltage Reference Output. The AD9838 has an internal 1.20 V reference that is available at this pin.
20	COMP	DAC Bias Pin. This pin is used for decoupling the DAC bias voltage.
	EP	Exposed Pad. Connect the exposed pad to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

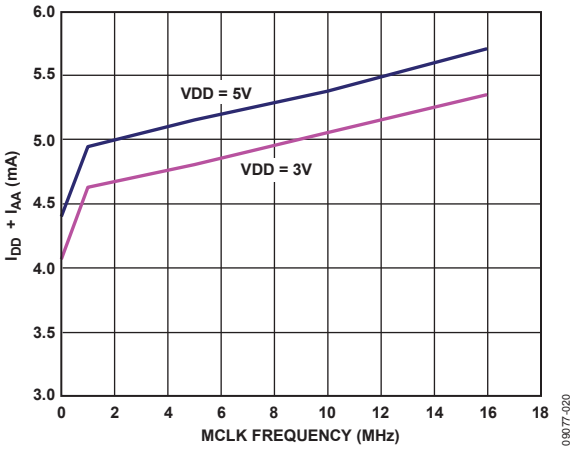


Figure 6. Typical Current Consumption (I_{DD} + I_{AA}) vs. MCLK Frequency for f_{OUT} = MCLK/10

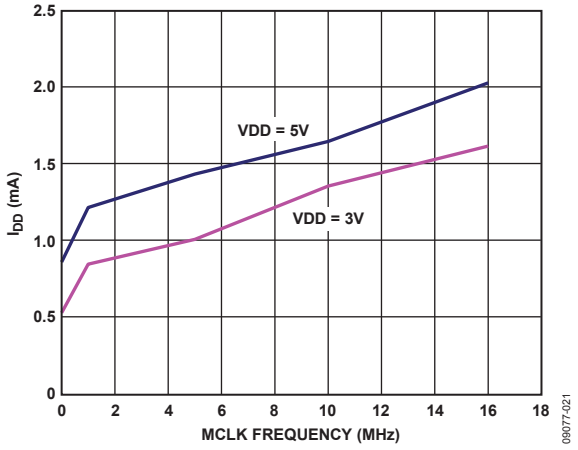


Figure 7. Typical Current Consumption (I_{DD}) vs. MCLK Frequency for f_{OUT} = MCLK/10

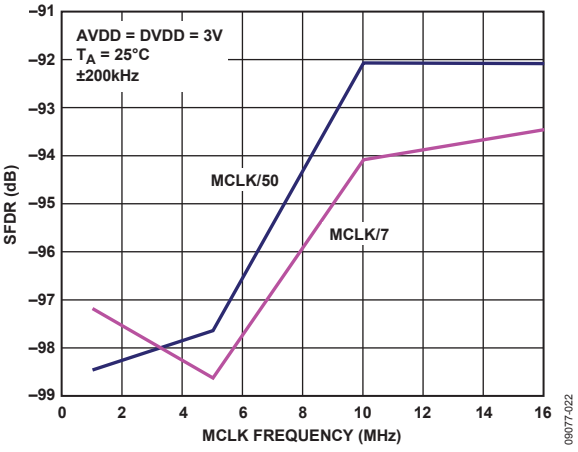


Figure 8. Narrow-Band SFDR vs. MCLK Frequency

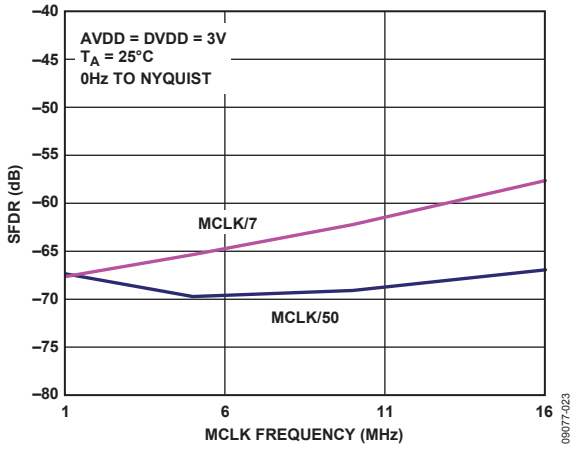


Figure 9. Wideband SFDR vs. MCLK Frequency

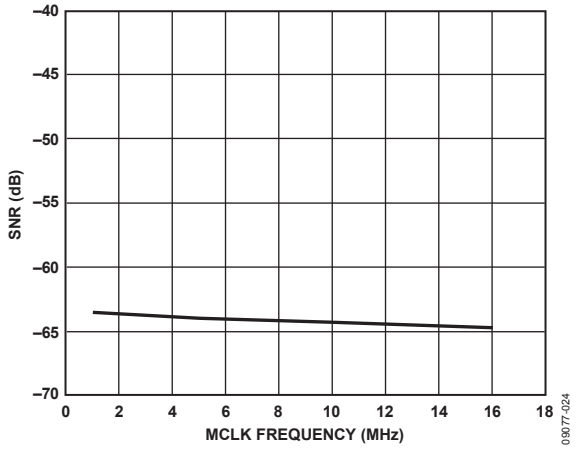


Figure 10. SNR vs. MCLK Frequency

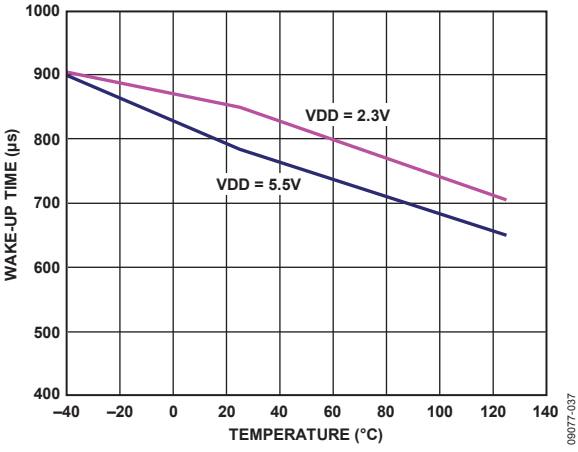


Figure 11. Wake-Up Time vs. Temperature

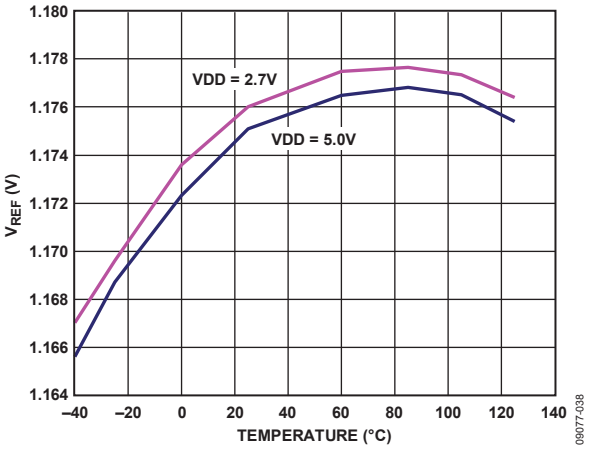


Figure 12. V_{REF} vs. Temperature

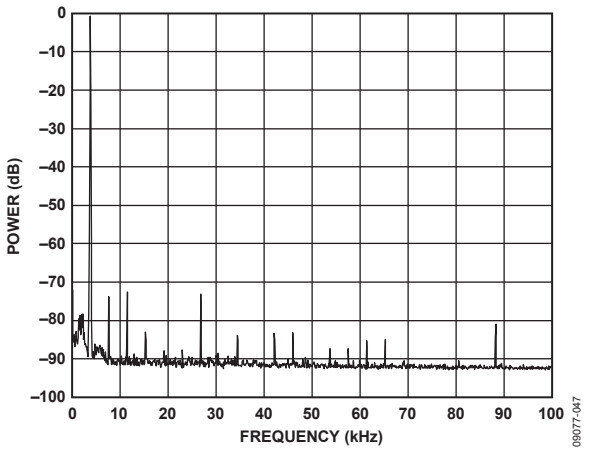


Figure 15. Power vs. Frequency, f_{MCLK} = 16 MHz, f_{OUT} = 3.8 kHz, Frequency Word = 0x000FBA9

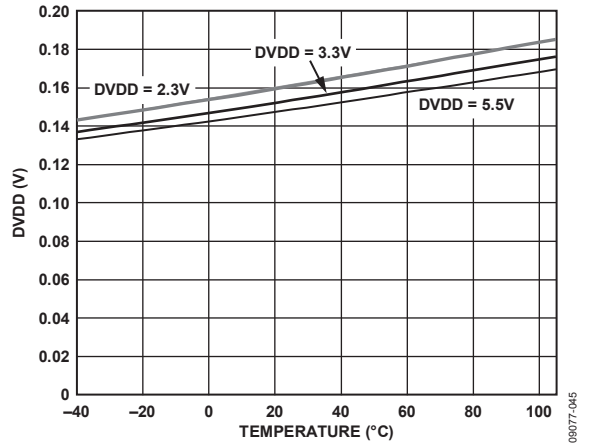


Figure 13. SIGN BIT OUT Pin, Low Level, I_{SINK} = 1 mA

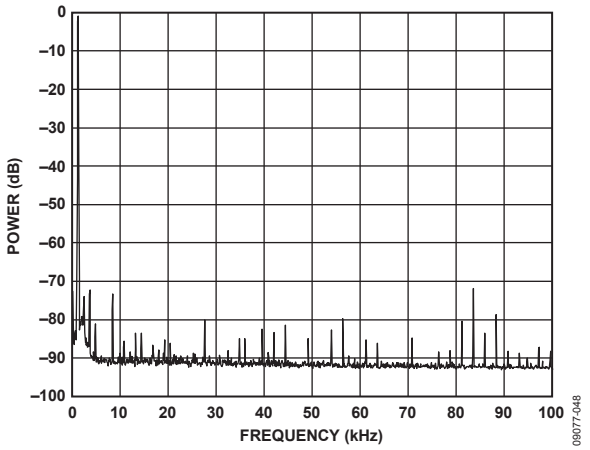


Figure 16. Power vs. Frequency, f_{MCLK} = 5 MHz, f_{OUT} = 1.2 kHz, Frequency Word = 0x000FBA9

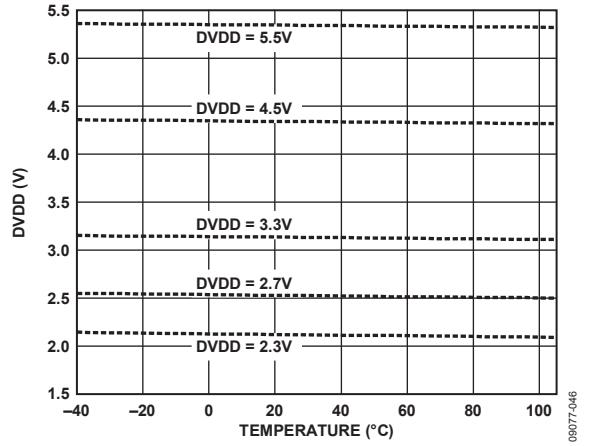


Figure 14. SIGN BIT OUT Pin, High Level, I_{SINK} = 1 mA

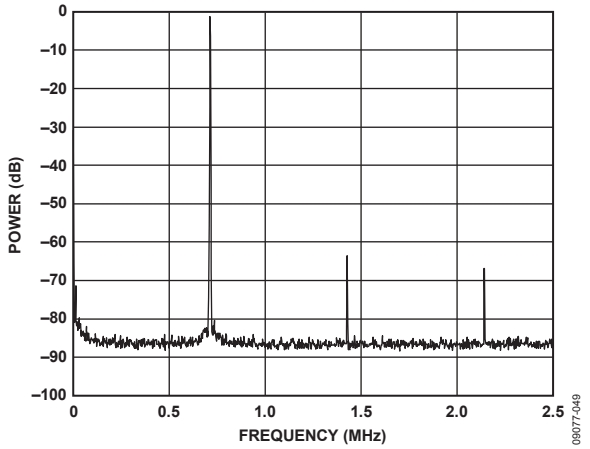


Figure 17. Power vs. Frequency, f_{MCLK} = 5 MHz, f_{OUT} = 0.714 MHz = f_{MCLK}/7, Frequency Word = 0x2492492

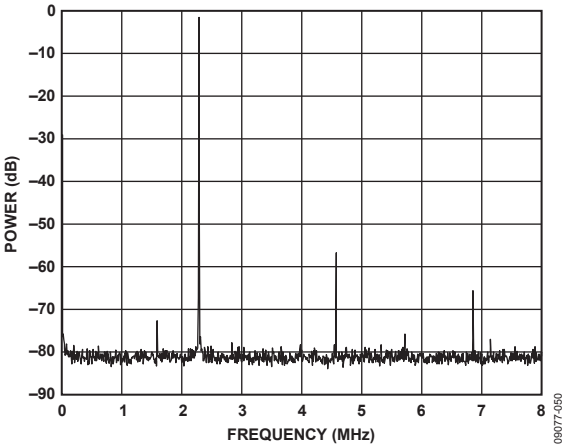


Figure 18. Power vs. Frequency, f_{MCLK} = 16 MHz, f_{OUT} = 2.28 MHz, Frequency Word = 0x2492492

TEST CIRCUIT

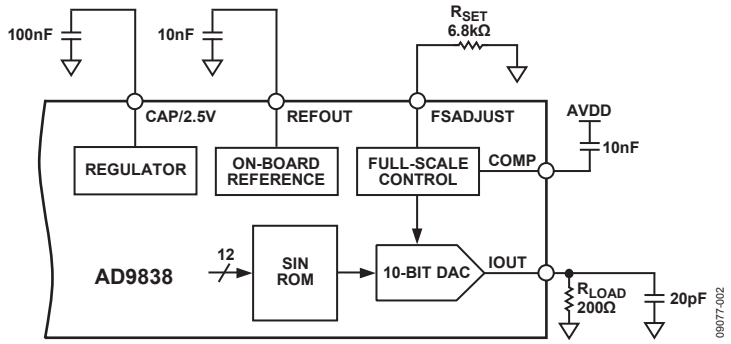


Figure 19. Test Circuit Used to Test Specifications

TERMINOLOGY

Integral Nonlinearity (INL)
INL is the maximum deviation of any code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale, a point 0.5 LSB below the first code transition (000 … 00 to 000 … 01), and full scale, a point 0.5 LSB above the last code transition (111 … 10 to 111 … 11). The error is expressed in LSBs.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and ideal 1 LSB change between two adjacent codes in the DAC. A specified DNL of ±1 LSB maximum ensures monotonicity.

Output Compliance
Output compliance refers to the maximum voltage that can be generated at the output of the DAC to meet the specifications. When voltages greater than that specified for the output compliance are generated, the AD9838 may not meet the specifications listed in the data sheet.

Spurious-Free Dynamic Range (SFDR)
Along with the frequency of interest, harmonics of the fundamental frequency and images of these frequencies are present at the output of a DDS device. The spurious-free dynamic range (SFDR) refers to the largest spur or harmonic present in the band of interest. The wideband SFDR gives the magnitude of the largest spur or harmonic relative to the magnitude of the fundamental frequency in the 0 to Nyquist bandwidth. The narrow-band SFDR gives the attenuation of the largest spur or harmonic in a bandwidth of ±200 kHz about the fundamental frequency.

Total Harmonic Distortion (THD)
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the rms value of the fundamental. For the AD9838, THD is defined as

$$THD = 20\log\sqrt{\frac{V_2^{\,2} + V_3^{\,2} + V_4^{\,2} + V_5^{\,2} + V_6^{\,2}}{V_1}}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through sixth harmonics.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured output signal to the rms sum of all other spectral components below the Nyquist frequency. The value for SNR is expressed in decibels.

Clock Feedthrough
There is feedthrough from the MCLK input to the analog output. Clock feedthrough refers to the magnitude of the MCLK signal relative to the fundamental frequency in the output spectrum of the AD9838.

THEORY OF OPERATION

Sine waves are typically thought of in terms of their magnitude form: a(t) = sin(ωt). However, sine waves are nonlinear and not easy to generate except through piecewise construction. On the other hand, the angular information is linear in nature; that is, the phase angle rotates through a fixed angle for each unit of time. The angular rate depends on the frequency of the signal by the traditional rate of $\omega = 2\pi f$.

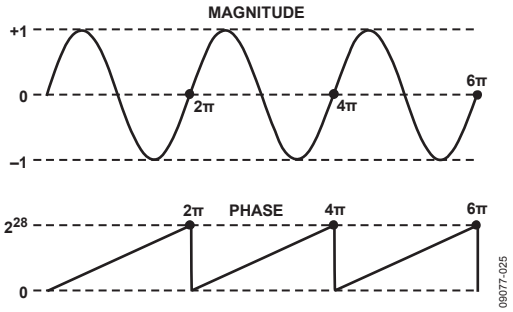


Figure 20. Sine Wave

Knowing that the phase of a sine wave is linear and given a reference interval (clock period), the phase rotation for that period can be determined as follows:

$$\Delta Phase = \omega \Delta t \quad (1)$$

Solving for ω,

$$\omega = \Delta Phase/\Delta t = 2\pi f \quad (2)$$

Solving for f and substituting the reference clock frequency for the reference period ($1/f_{MCLK} = \Delta t$),

$$f = \Delta Phase \times f_{MCLK}/2\pi \quad (3)$$

The AD9838 builds the output based on this simple equation. A simple DDS chip can implement this equation with three major subcircuits: numerically controlled oscillator (NCO) plus phase modulator, SIN ROM, and digital-to-analog converter (DAC). Each subcircuit is described in the Circuit Description section.

CIRCUIT DESCRIPTION

The AD9838 is a fully integrated direct digital synthesis (DDS) chip. The chip requires one reference clock, one low precision resistor, and eight decoupling capacitors to provide digitally created sine waves up to 8 MHz. In addition to the generation of this RF signal, the chip is fully capable of a broad range of simple and complex modulation schemes. These modulation schemes are fully implemented in the digital domain, allowing accurate and simple realization of complex modulation algorithms using DSP techniques.

The internal circuitry of the AD9838 consists of the following main sections: a numerically controlled oscillator (NCO), frequency and phase modulators, SIN ROM, a digital-to-analog converter, a comparator, and a regulator.

NUMERICALLY CONTROLLED OSCILLATOR PLUS PHASE MODULATOR

The AD9838 consists of two frequency select registers, a phase accumulator, two phase offset registers, and a phase offset adder. The main component of the NCO is a 28-bit phase accumulator. Continuous time signals have a phase range of 0 to 2π. Outside this range of numbers, the sinusoid functions repeat themselves in a periodic manner. The digital implementation is no different. The accumulator simply scales the range of phase numbers into a multibit digital word. The phase accumulator in the AD9838 is implemented with 28 bits. Therefore, in the AD9838, $2\pi = 2^{28}$. Likewise, the ΔPhase term is scaled into this range of numbers:

$$0 < \Delta Phase < 2^{28} - 1$$

With these substitutions, Equation 3 becomes

$$f = \Delta Phase \times f_{MCLK}/2^{28} \quad (4)$$

where $0 < \Delta Phase < 2^{28} - 1$.

The input to the phase accumulator can be selected from either the FREQ0 register or the FREQ1 register and is controlled by the FSELECT pin or the FSEL bit in the control register. NCOs inherently generate continuous phase signals, thus avoiding any output discontinuity when switching between frequencies.

Following the NCO, a phase offset can be added to perform phase modulation using the 12-bit phase registers. The contents of one of these phase registers is added to the MSBs of the NCO. The AD9838 has two phase registers; their resolution is 2π/4096.

SIN ROM

To make the output from the NCO useful, it must be converted from phase information into a sinusoidal value. Because phase information maps directly to amplitude, the SIN ROM uses the digital phase information as an address to a lookup table and converts the phase information into amplitude.

Although the NCO contains a 28-bit phase accumulator, the output of the NCO is truncated to 12 bits. Using the full resolution of the phase accumulator is impractical and unnecessary because a lookup table of 2^{28} entries would be required. It is only necessary to have sufficient phase resolution such that the errors due to truncation are smaller than the resolution of the 10-bit DAC. Therefore, the SIN ROM must have two bits of phase resolution more than the 10-bit DAC.

The SIN ROM is enabled using the OPBITEN and MODE bits (Bit D5 and Bit D1) in the control register (see Table 19).

DIGITAL-TO-ANALOG CONVERTER (DAC)

The AD9838 includes a high impedance, current source, 10-bit DAC capable of driving a wide range of loads. The full-scale output current can be adjusted for optimum power and external load requirements using a single external resistor (R_{SET}).

The DAC can be configured for single-ended or differential operation. The IOUT and IOUTB pins can be connected through equal external resistors to AGND to develop complementary output voltages. The load resistors can be of any value required, as long as the full-scale voltage developed across them does not exceed the output compliance range. Because full-scale current is controlled by R_{SET}, adjustments to R_{SET} can balance changes made to the load resistors.

COMPARATOR

The AD9838 can be used to generate synthesized digital clock signals. This is accomplished by using the on-board self-biasing comparator that converts the sinusoidal signal of the DAC to a square wave. The output from the DAC can be filtered externally before being applied to the comparator input. The comparator reference voltage is the time average of the signal applied to VIN. The comparator can accept signals in the range of approximately 100 mV p-p to 1 V p-p. The comparator input is ac-coupled; therefore, to operate correctly as a zero-crossing detector, the comparator requires a minimum input frequency of 3 MHz typical. The comparator output is a square wave with an amplitude from 0 V to DVDD.

The AD9838 provides a sampled signal with its output following Nyquist sampling theorem. Specifically, its output spectrum contains the fundamental plus aliased signals (images) that occur at multiples of the reference clock frequency and the selected output frequency. A graphical representation of the sampled spectrum, with aliased images, is shown in Figure 21.

The prominence of the aliased images depends on the ratio of f_{OUT} to MCLK. If the ratio is small, the aliased images are very prominent and of a relatively high energy level as determined by the sin(x)/x roll-off of the quantized DAC output. In fact, depending on the f_{OUT}/reference clock ratio, the first aliased image can be on the order of −3 dB below the fundamental.

A low-pass filter is generally placed between the output of the DAC and the input of the comparator to further suppress the effects of aliased images. To avoid unwanted (and unexpected) output anomalies, it is necessary to consider the relationship of the selected output frequency and the reference clock frequency.

To apply the AD9838 as a clock generator, limit the selected output frequency to <33% of the reference clock frequency. In this way, the user can prevent the generation of aliased signals that fall within, or close to, the output band of interest (generally the dc selected output frequency). This practice reduces the complexity (and cost) of the external filter requirement for the clock generator application. For more information, see the AN-837 Application Note.

To enable the comparator, the SIGN/PIB and OPBITEN bits in the control resister must be set to 1 (see Table 18).

REGULATOR

The AD9838 has separate power supplies for the analog and digital sections. AVDD provides the power supply required for the analog section, and DVDD provides the power supply for the digital section. Both supplies can have a value of 2.3 V to 5.5 V and are independent of each other. For example, the analog section can be operated at 5 V, and the digital section can be operated at 3 V, or vice versa.

The internal digital section of the AD9838 is operated at 2.5 V. An on-board regulator steps down the voltage applied at DVDD to 2.5 V. The digital interface (serial port) of the AD9838 also operates from DVDD. These digital signals are level shifted within the AD9838 to make them 2.5 V compatible.

If the voltage applied at the DVDD pin of the AD9838 is less than or equal to 2.7 V, the CAP/2.5V and DVDD pins should be tied together to bypass the on-board regulator.

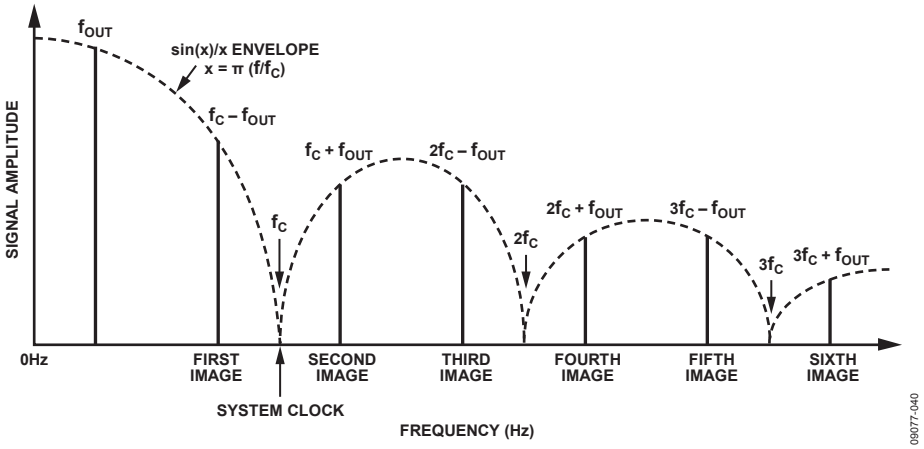


Figure 21. DAC Output Spectrum

FUNCTIONAL DESCRIPTION

SERIAL INTERFACE

The AD9838 has a standard 3-wire serial interface that is compatible with the SPI, QSPI™, MICROWIRE®, and DSP interface standards.

Data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK. The timing diagram for this operation is given in Figure 4.

FSYNC is a level triggered input that acts as a frame synchronization and chip enable input. Data can be transferred into the device only when FSYNC is low. To start the serial data transfer, FSYNC should be taken low, observing the minimum FSYNC to SCLK falling edge setup time, t_7 (see Table 2). After FSYNC goes low, serial data is shifted into the input shift register of the device on the falling edges of SCLK for 16 clock pulses. FSYNC can be taken high after the 16th falling edge of SCLK, observing the minimum SCLK falling edge to FSYNC rising edge time, t_8. Alternatively, FSYNC can be kept low for a multiple of 16 SCLK pulses and then brought high at the end of the data transfer. In this way, a continuous stream of 16-bit words can be loaded while FSYNC is held low; FSYNC goes high only after the 16th SCLK falling edge of the last word loaded.

The SCLK can be continuous, or it can idle high or low between write operations. In either case, it must be high when FSYNC goes low (t_{12}).

For an example of how to program the AD9838, see the AN-1070 Application Note on the Analog Devices, Inc., website. The AD9838 has the same register settings as the AD9833/AD9834.

LATENCY PERIOD

A latency period is associated with each operation. When the FSELECT and PSELECT pins change value, there is a pipeline delay before control is transferred to the selected register.

When the t_{11} and t_{11A} timing specifications are met (see Figure 3), FSELECT and PSELECT have latencies of eight MCLK cycles. When the t_{11} and t_{11A} timing specifications are not met, the latency is increased by one MCLK cycle.

Similarly, a latency period is associated with each asynchronous write operation. If a selected frequency or phase register is loaded with a new word, there is a delay of eight or nine MCLK cycles before the analog output changes. The delay can be eight or nine MCLK cycles, depending on the position of the MCLK rising edge when the data is loaded into the destination register.

The negative transitions of the RESET and SLEEP pins are sampled on the internal falling edge of MCLK. Therefore, they also have a latency period associated with them.

CONTROL REGISTER

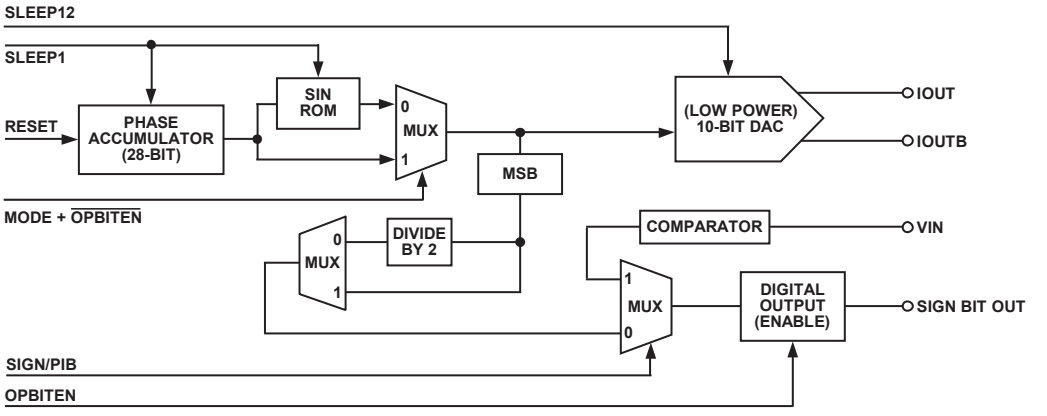
The AD9838 contains a 16-bit control register that allows the user to configure the operation of the AD9838. All control bits other than the MODE bit are sampled on the internal falling edge of MCLK.

Figure 22 illustrates the functions of the control bits. Table 7 describes the individual bits of the control register. The different functions and the various output options of the AD9838 are described in more detail in the following sections.

To inform the AD9838 that the contents of the control register will be altered, Bit D15 and Bit D14 must be set to 0, as shown in Table 6.

Table 6. Control Register Bits

D15	D14	D13 to D0
0	0	Control bits



D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	B28	HLB	FSEL	PSEL	PIN/SW	RESET	SLEEP1	SLEEP12	OPBITEN	SIGN/PIB	DIV2	0	MODE	0

09077-026

Figure 22. Function of Control Bits

Table 7. Control Register Bit Descriptions

Bit	Bit Name	Description
D13	B28	Two write operations are required to load a complete word into either of the frequency registers. B28 = 1 allows a complete word to be loaded into a frequency register in two consecutive writes. The first write contains the 14 LSBs of the frequency word, and the second write contains the 14 MSBs. The first two bits of each 16-bit word define the frequency register to which the word is loaded and should, therefore, be the same for both consecutive writes. See Table 11 for the appropriate addresses. The write to the frequency register occurs after both words have been loaded, so the register never holds an intermediate value. An example of a complete 28-bit write is shown in Table 12. Note, however, that consecutive 28-bit writes to the same frequency register are not allowed; to execute consecutive 28-bit writes, you must alternate between the frequency registers. B28 = 0 configures the 28-bit frequency register to operate as two 14-bit registers, one containing the 14 MSBs and the other containing the 14 LSBs. In this way, the 14 MSBs of the frequency word can be altered independently of the 14 LSBs, and vice versa. To alter the 14 MSBs or the 14 LSBs, a single write is made to the appropriate frequency address. Bit D12 (HLB) informs the AD9838 whether the bits to be altered are the 14 MSBs or the 14 LSBs.
D12	HLB	This control bit allows the user to continuously load the MSBs or LSBs of a frequency register while ignoring the remaining 14 bits. This is useful if the complete 28-bit resolution is not required. The HLB bit is used in conjunction with the B28 bit (Bit D13). The HLB bit indicates whether the 14 bits to be loaded are transferred to the 14 MSBs or the 14 LSBs of the addressed frequency register. Bit D13 (B28) must be set to 0 to change the MSBs or LSBs of a frequency word separately. When Bit D13 (B28) is set to 1, the HLB bit is ignored. HLB = 1 allows a write to the 14 MSBs of the addressed frequency register. HLB = 0 allows a write to the 14 LSBs of the addressed frequency register.
D11	FSEL	The FSEL bit defines whether the FREQ0 register or the FREQ1 register is used in the phase accumulator (see Table 9).
D10	PSEL	The PSEL bit defines whether the PHASE0 register data or the PHASE1 register data is added to the output of the phase accumulator (see Table 10).
D9	PIN/SW	The following functions can be implemented using either software or hardware: frequency register selection, phase register selection, reset of internal registers, and DAC power-down. The PIN/SW bit selects the source of control for these functions. PIN/SW = 1 selects the control pins to implement the register selection, reset, and DAC power-down functions. PIN/SW = 0 selects the control bits to implement the register selection, reset, and DAC power-down functions.
D8	RESET	When the PIN/SW bit is set to 0, this bit controls the reset function. RESET = 1 resets internal registers to 0, which corresponds to an analog output of midscale. RESET = 0 disables the reset function (see the Reset Function section).
D7	SLEEP1	This bit enables or disables the internal MCLK. SLEEP1 = 1 disables the internal MCLK. The DAC output remains at its present value because the NCO is no longer accumulating. SLEEP1 = 0 enables the internal MCLK (see the Sleep Function section).
D6	SLEEP12	When the PIN/SW bit is set to 0, this bit powers down the on-chip DAC. SLEEP12 = 1 powers down the on-chip DAC. This is useful when the AD9838 is used to output the MSB of the DAC data. SLEEP12 = 0 implies that the DAC is active (see the Sleep Function section).
D5	OPBITEN	This bit controls whether an output is available at the SIGN BIT OUT pin. If the user is not using the SIGN BIT OUT pin, this bit should be set to 0. OPBITEN = 1 enables the SIGN BIT OUT pin. OPBITEN = 0 places the SIGN BIT OUT output buffer into a high impedance state (no output is available at the SIGN BIT OUT pin).
D4	SIGN/PIB	This bit controls the output at the SIGN BIT OUT pin when the OPBITEN bit (Bit D5) is set to 1. SIGN/PIB = 1 connects the on-board comparator to the SIGN BIT OUT pin. After filtering the sinusoidal output from the DAC, the waveform can be applied to the comparator to generate a square waveform (see Table 18). SIGN/PIB = 0 connects the MSB (or MSB/2) of the DAC data to the SIGN BIT OUT pin. Bit D3 (DIV2) controls whether the output is the MSB or MSB/2.
D3	DIV2	DIV2 is used when the OPBITEN bit (Bit D5) is set to 1 and the SIGN/PIB bit (Bit D4) is set to 0 (see Table 18). DIV2 = 1 causes the MSB of the DAC data to be output at the SIGN BIT OUT pin. DIV2 = 0 causes the MSB/2 of the DAC data to be output at the SIGN BIT OUT pin.
D2	Reserved	This bit must be set to 0.
D1	MODE	This bit, in association with the OPBITEN bit (Bit D5), controls the output at the IOUT and IOUTB pins. This bit should be set to 0 if the OPBITEN bit is set to 1 (see Table 19). MODE = 1 bypasses the SIN ROM, resulting in a triangle output from the DAC. MODE = 0 uses the SIN ROM to convert the phase information into amplitude information, resulting in a sinusoidal signal at the output.
D0	Reserved	This bit must be set to 0.

FREQUENCY AND PHASE REGISTERS

The AD9838 contains two frequency registers and two phase registers, which are described in Table 8.

Table 8. Frequency and Phase Registers

Register	Size	Description
FREQ0	28 bits	Frequency Register 0. When the FSEL bit or FSELECT pin = 0, the FREQ0 register defines the output frequency as a fraction of the MCLK frequency.
FREQ1	28 bits	Frequency Register 1. When the FSEL bit or FSELECT pin = 1, the FREQ1 register defines the output frequency as a fraction of the MCLK frequency.
PHASE0	12 bits	Phase Offset Register 0. When the PSEL bit or PSELECT pin = 0, the contents of the PHASE0 register are added to the output of the phase accumulator.
PHASE1	12 bits	Phase Offset Register 1. When the PSEL bit or PSELECT pin = 1, the contents of the PHASE1 register are added to the output of the phase accumulator.

The analog output from the AD9838 is

$$f_{MCLK}/2^{28} \times FREQREG$$

where *FREQREG* is the value loaded into the selected frequency register.

This signal is phase shifted by

$$2\pi/4096 \times PHASEREG$$

where *PHASEREG* is the value contained in the selected phase register.

The relationship of the selected output frequency and the reference clock frequency must be considered to avoid unwanted output anomalies.

Selecting a Frequency or Phase Register

Access to the frequency and phase registers is controlled by the FSELECT and PSELECT pins or by the FSEL and PSEL control bits. If the PIN/SW control bit (Bit D9) = 1, the pins control the function; if the PIN/SW control bit = 0, the bits control the function (see Table 9 and Table 10). If the FSEL and PSEL bits are used, the pins should be held at CMOS logic high or low. Control of the frequency and phase registers is interchangeable from the pins to the bits.

Table 9. Selecting a Frequency Register

FSELECT Pin	FSEL Bit	PIN/SW Bit	Selected Register
0	X	1	FREQ0
1	X	1	FREQ1
X	0	0	FREQ0
X	1	0	FREQ1

Table 10. Selecting a Phase Register

PSELECT Pin	PSEL Bit	PIN/SW Bit	Selected Register
0	X	1	PHASE0
1	X	1	PHASE1
X	0	0	PHASE0
X	1	0	PHASE1

The FSELECT and PSELECT pins are sampled on the internal falling edge of MCLK. It is recommended that the data on these pins not change within the time window of the falling edge of MCLK (see Figure 3 for timing). If the FSELECT or PSELECT pin changes value when a falling edge occurs, there is an uncertainty of one MCLK cycle as it pertains to when control is transferred to the other frequency/phase register.

The flowcharts in Figure 26 and Figure 27 show the routine for selecting and writing to the frequency and phase registers of the AD9838.

Writing to a Frequency Register

When writing to a frequency register, Bit D15 and Bit D14 of the control register give the address of the frequency register (see Table 11).

Table 11. Frequency Register Bits

D15	D14	D13 to D0
0	1	14 FREQ0 register bits
1	0	14 FREQ1 register bits

To change the entire contents of a frequency register, two consecutive writes to the same address must be performed because the frequency registers are 28 bits wide. The first write contains the 14 LSBs, and the second write contains the 14 MSBs. For this mode of operation, the B28 control bit (Bit D13) must be set to 1. An example of a 28-bit write is shown in Table 12.

Table 12. Writing 0xFFFC000 to the FREQ0 Register

SDATA Input	Result of Input Word
0010 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 1, HLB (D12) = X
0100 0000 0000 0000	FREQ0 register write (D15, D14 = 01), 14 LSBs = 0x0000
0111 1111 1111 1111	FREQ0 register write (D15, D14 = 01), 14 MSBs = 0x3FFF

Note, however, that continuous writes to the same frequency register may result in intermediate updates during the writes. If a frequency sweep, or something similar, is required, it is recommended that users alternate between the two frequency registers.

In some applications, the user does not need to alter all 28 bits of the frequency register. With coarse tuning, only the 14 MSBs are altered; with fine tuning, only the 14 LSBs are altered. By setting the B28 control bit (Bit D13) to 0, the 28-bit frequency register operates as two 14-bit registers, one containing the 14 MSBs and the other containing the 14 LSBs. In this way, the 14 MSBs of the frequency word can be altered independently of the 14 LSBs, and vice versa. The HLB bit (Bit D12) in the control register identifies which 14 bits are being altered (see Table 13 and Table 14).

Table 13. Writing 0x3FFF to the 14 LSBs of the FREQ1 Register

SDATA Input	Result of Input Word
0000 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 0, HLB (D12) = 0, that is, LSBs
1011 1111 1111 1111	FREQ1 register write (D15, D14 = 10), 14 LSBs = 0x3FFF

Table 14. Writing 0x00FF to the 14 MSBs of the FREQ0 Register

SDATA Input	Result of Input Word
0001 0000 0000 0000	Control word write (D15, D14 = 00), B28 (D13) = 0, HLB (D12) = 1, that is, MSBs
0100 0000 1111 1111	FREQ0 register write (D15, D14 = 01), 14 MSBs = 0x00FF

Writing to a Phase Register

When writing to a phase register, Bit D15 and Bit D14 are set to 11. Bit D13 identifies the phase register that is being loaded.

Table 15. Phase Register Bits

D15	D14	D13	D12	D11 to D0
1	1	0	X	12 PHASE0 register bits
1	1	1	X	12 PHASE1 register bits

RESET FUNCTION

The reset function resets the appropriate internal registers to 0 to provide an analog output of midscale. A reset does not reset the phase, frequency, or control registers. When the AD9838 is powered up, the part should be reset (see the Powering Up the AD9838 section). To reset the AD9838, set the RESET pin or bit to 1. To take the part out of reset, set the RESET pin or bit to 0. A signal appears at the DAC output eight or nine MCLK cycles after the RESET pin or bit is set to 0.

The reset function is controlled by either the RESET pin or the RESET control bit. If the PIN/SW control bit = 0, the RESET bit controls the function; if the PIN/SW control bit = 1, the RESET pin controls the function (see Table 16).

Table 16. Applying the Reset Function

RESET Pin	RESET Bit	PIN/SW Bit	Result
0	X	1	No reset applied
1	X	1	Internal registers reset
X	0	0	No reset applied
X	1	0	Internal registers reset

The effect of asserting the RESET pin is immediately evident at the output—that is, the 0-to-1 transition of this pin is not sampled. However, the negative (1-to-0) transition of the RESET pin is sampled on the internal falling edge of MCLK.

SLEEP FUNCTION

Sections of the AD9838 that are not in use can be powered down to minimize power consumption by using the sleep function. The parts of the chip that can be powered down are the internal clock and the DAC. The DAC can be powered down using hardware or software (see Table 17).

Table 17. Applying the Sleep Function

SLEEP Pin	SLEEP1 Bit	SLEEP12 Bit	PIN/SW Bit	Result
0	X	X	1	No power-down
1	X	X	1	DAC powered down
X	0	0	0	No power-down
X	0	1	0	DAC powered down
X	1	0	0	Internal clock disabled
X	1	1	0	DAC powered down and internal clock disabled

DAC Powered Down

When the AD9838 is used to output the MSB of the DAC data only, the DAC is not required. The DAC can be powered down to reduce power consumption.

Internal Clock Disabled

When the internal clock of the AD9838 is disabled, the DAC output remains at its present value because the NCO is no longer accumulating. New frequency, phase, and control words can be written to the part when the SLEEP1 control bit is active. Because the synchronizing clock (FSYNC) remains active, the selected frequency and phase registers can also be changed either at the pins or by using the control bits. Setting the SLEEP1 bit to 0 enables the MCLK. Any changes made to the registers while SLEEP1 was active are observed at the output after a latency period (see the Latency Period section).

The effect of asserting the SLEEP pin is immediately evident at the output—that is, the 0-to-1 transition of this pin is not sampled. However, the negative (1-to-0) transition of the SLEEP pin is sampled on the internal falling edge of MCLK.

SIGN BIT OUT PIN

The AD9838 offers a variety of outputs from the chip. The digital outputs are available from the SIGN BIT OUT pin. The available outputs are the comparator output or the MSB of the DAC data. The bits controlling the SIGN BIT OUT pin are listed in Table 18.

Table 18. Outputs from the SIGN BIT OUT Pin

OPBITEN Bit	MODE Bit	SIGN/PIB Bit	DIV2 Bit	SIGN BIT OUT Pin
0	X	X	X	High impedance
1	0	0	0	DAC data MSB/2
1	0	0	1	DAC data MSB
1	0	1	0	Reserved
1	0	1	1	Comparator output
1	1	X	X	Reserved

The SIGN BIT OUT pin must be enabled before use. The OPBITEN bit (Bit D5) in the control register enables and disables this pin. When OPBITEN = 1, the SIGN BIT OUT pin is enabled. Note that if OPBITEN = 1, the MODE bit (Bit D1) in the control register should be set to 0.

Comparator Output

The AD9838 has an on-board comparator. To connect this comparator to the SIGN BIT OUT pin, the OPBITEN bit (Bit D5) and the SIGN/PIB bit (Bit D4) must be set to 1. After filtering the sinusoidal output from the DAC, the waveform can be applied to the comparator to generate a square waveform.

MSB of the DAC Data

The MSB of the DAC data can be output from the AD9838. By setting the OPBITEN bit (Bit D5) to 1 and the SIGN/PIB bit (Bit D4) to 0, the MSB of the DAC data is available at the SIGN BIT OUT pin. This output is useful as a coarse clock source. The square wave can also be divided by 2 before being output. The DIV2 bit (Bit D3) in the control register controls the frequency of this output from the SIGN BIT OUT pin.

IOUT AND IOUTB PINS

The analog outputs from the AD9838 are available from the IOUT and IOUTB pins. The available outputs are a sinusoidal output or a triangular output (see Table 19).

Note that the SLEEP pin and the SLEEP12 bit must be set to 0 (the DAC is enabled) when using the IOUT and IOUTB pins.

Table 19. Outputs from the IOUT and IOUTB Pins

OPBITEN Bit	MODE Bit	IOUT and IOUTB Pin Output
0	0	Sinusoid
0	1	Triangle
1	0	Sinusoid
1	1	Reserved

Sinusoidal Output

The SIN ROM converts the phase information from the frequency and phase registers into amplitude information, resulting in a sinusoidal signal at the output. To obtain a sinusoidal output from the IOUT and IOUTB pins, set the MODE bit (Bit D1) to 0.

Triangle Output

The SIN ROM can be bypassed so that the truncated digital output from the NCO is sent to the DAC. In this case, the output is no longer sinusoidal. The DAC produces a 10-bit linear triangular function (see Figure 23). To obtain a triangle output from the IOUT and IOUTB pins, set the MODE bit (Bit D1) to 1 and the OPBITEN bit (Bit D5) to 0.

Figure 23. Triangle Output

POWERING UP THE AD9838

The flowchart in Figure 24 shows the operating routine for the AD9838. When the AD9838 is powered up, the part should be reset. This resets the appropriate internal registers to 0 to provide an analog output of midscale. To avoid spurious DAC outputs during AD9838 initialization, the RESET pin or the RESET bit should be set to 1 until the part is ready to begin generating an output.

A reset does not reset the phase, frequency, or control registers. These registers will contain invalid data and, therefore, should be set to known values by the user. The RESET pin or bit should then be set to 0 to begin generating an output. The data appears on the DAC output eight or nine MCLK cycles after the RESET pin or bit is set to 0.

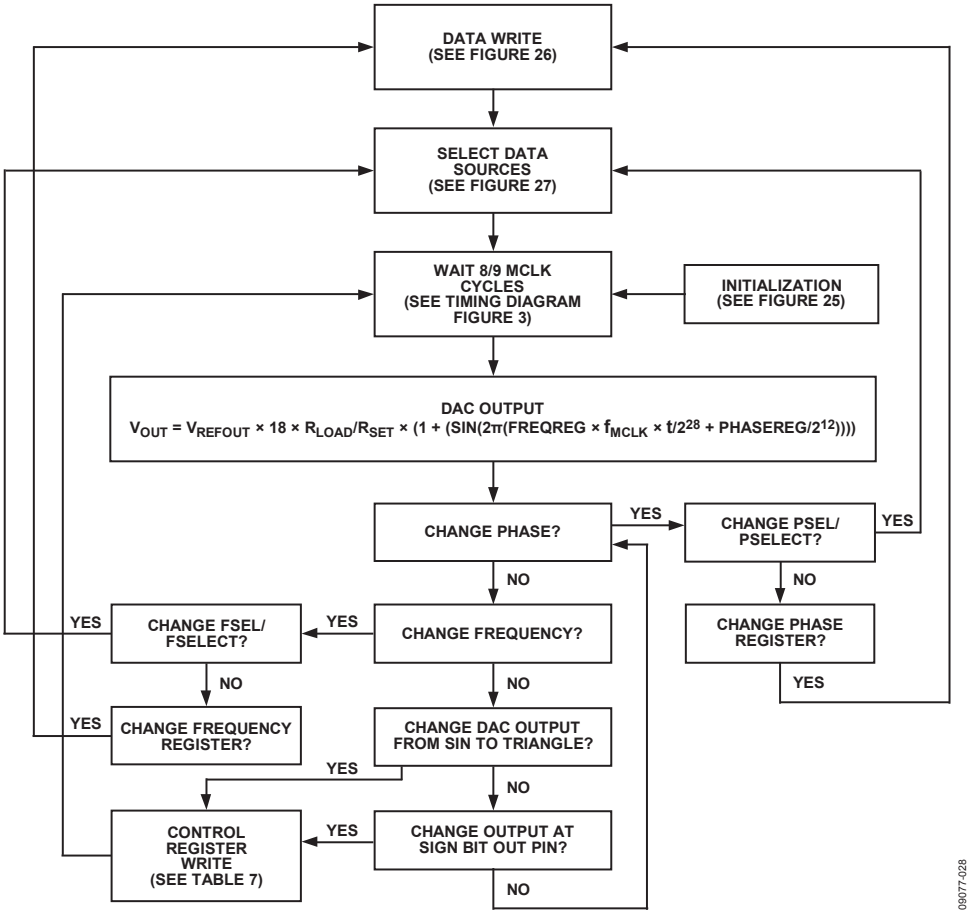


Figure 24. Flowchart for AD9838 Initialization and Operation

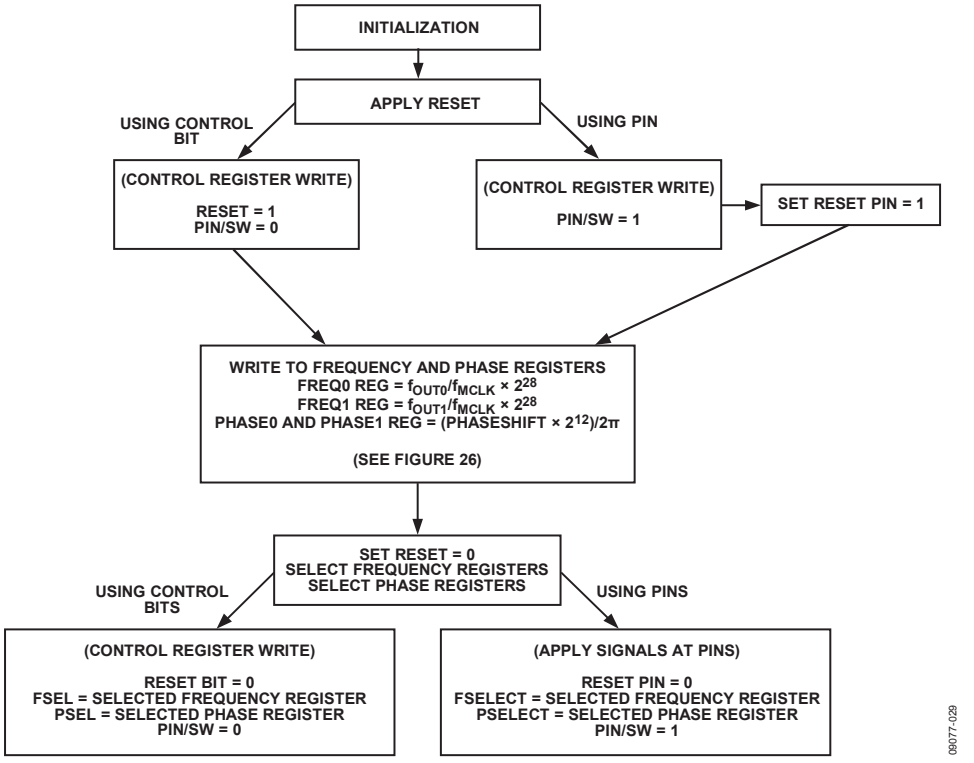


Figure 25. Flowchart for Initialization

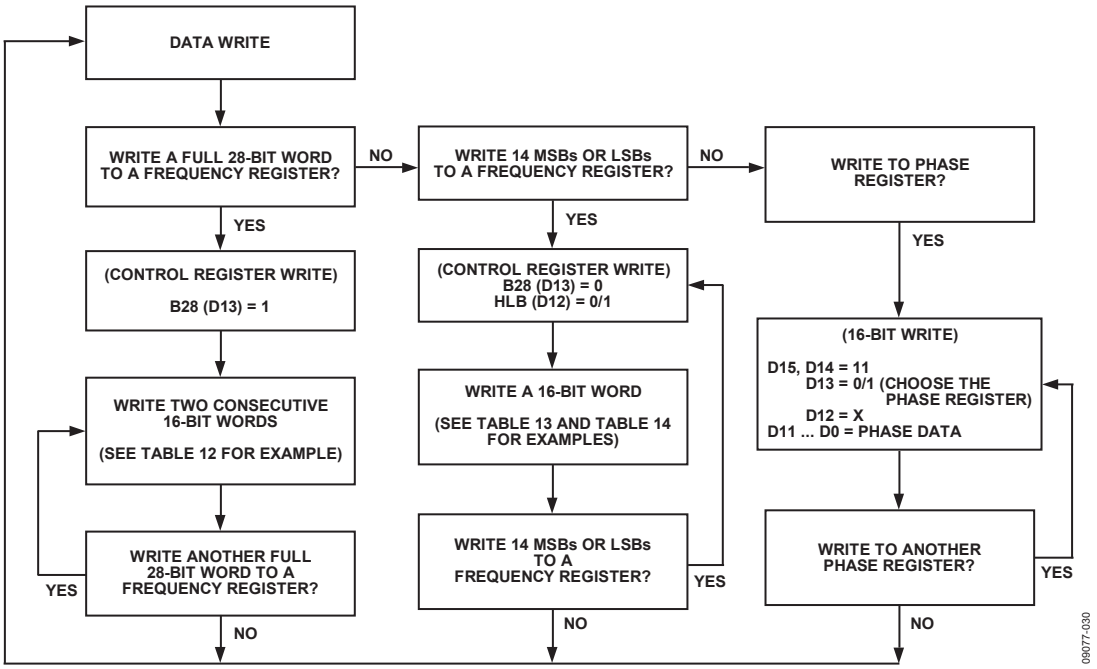


Figure 26. Flowchart for Data Writes

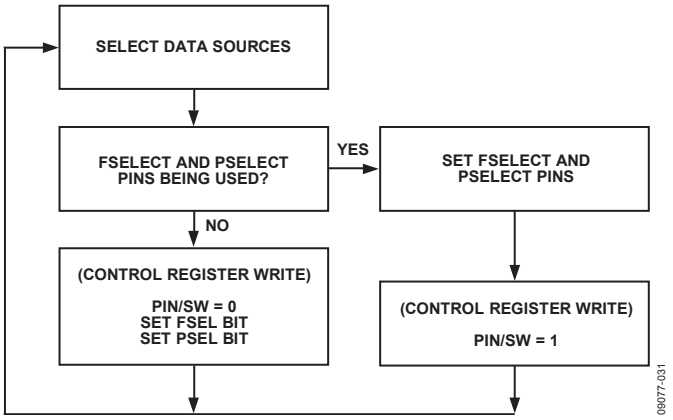


Figure 27. Flowchart for Selecting Data Sources

APPLICATIONS INFORMATION

The various output options available from the AD9838 make the part suitable for a wide variety of applications, including modulation applications. The AD9838 can be used to perform simple modulation, such as frequency shift keying (FSK). More complex modulation schemes, such as Gaussian minimum shift keying (GMSK) and quadrature phase shift keying (QPSK), can also be implemented using the AD9838.

In an FSK application, the two frequency registers of the AD9838 are loaded with different values. One frequency represents the space frequency, and the other represents the mark frequency. The digital data stream is fed to the FSELECT pin, causing the AD9838 to modulate the carrier frequency between the two values.

The AD9838 has two phase registers, enabling the part to perform phase shift keying (PSK). With PSK, the carrier frequency is phase shifted, that is, the phase is altered by an amount that is related to the bit stream input to the modulator.

The AD9838 is also suitable for signal generator applications. Using the on-board comparator, the device can be used to generate a square wave.

With its low current consumption, the part is also suitable for applications in which it can be used as a local oscillator.

GROUNDING AND LAYOUT

The printed circuit board that houses the AD9838 should be designed so that the analog and digital sections are separated and confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes because it provides the best shielding. Digital and analog ground planes should be joined in one place only. If the AD9838 is the only device that requires an AGND to DGND connection, the ground planes should be connected at the AGND and DGND pins of the AD9838. If the AD9838 is in a system where multiple devices require AGND to DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the AD9838.

Avoid running digital lines under the device; these lines couple noise onto the die. The analog ground plane should be allowed to run under the AD9838 to avoid noise coupling. The power supply lines to the AD9838 should use as large a track as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals, such as clocks, should be shielded with digital ground to avoid radiating noise to other sections of the board.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other to reduce the effects of feedthrough through the board. A microstrip technique is by far the best but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes and signals are placed on the other side.

Good decoupling is important. The analog and digital supplies to the AD9838 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. All analog and digital supplies should be decoupled to AGND and DGND, respectively, with 0.1 μF ceramic capacitors in parallel with 10 μF tantalum capacitors. To achieve the best performance from the decoupling capacitors, they should be placed as close as possible to the device, ideally right up against the device.

In systems where a common supply is used to drive both the AVDD and DVDD pins of the AD9838, it is recommended that the system's AVDD supply be used. This supply should have the recommended analog supply decoupling between the AVDD pin of the AD9838 and AGND, as well as the recommended digital supply decoupling capacitors between the DVDD pin and DGND.

Proper operation of the comparator requires good layout strategy. The layout must minimize the parasitic capacitance between V_{IN} and the SIGN BIT OUT pin by using a ground plane to add isolation. For example, in a multilayered board, the V_{IN} signal can be connected to the top layer, and the SIGN BIT OUT pin can be connected to the bottom layer. In this way, isolation is provided by the power and ground planes between V_{IN} and the SIGN BIT OUT pin.

INTERFACING TO MICROPROCESSORS

The AD9838 has a standard serial interface that allows the part to interface directly with several microprocessors. The device uses an external serial clock to write the data or control information into the device. The serial clock can have a frequency of 40 MHz maximum. The serial clock can be continuous, or it can idle high or low between write operations. When data or control information is written to the AD9838, FSYNC is taken low and is held low until the 16 bits of data are written into the AD9838. The FSYNC signal frames the 16 bits of information that are loaded into the AD9838.

AD9838 to 68HC11/68L11 Interface

Figure 28 shows the serial interface between the AD9838 and the 68HC11/68L11 microcontroller. The microcontroller is configured as the master by setting the MSTR bit in the SPCR to 1. This setting provides a serial clock on SCK; the MOSI output drives the serial data line, SDATA. Because the microcontroller does not have a dedicated frame sync pin, the FSYNC signal is derived from a port line (PC7). The setup conditions for correct operation of the interface are as follows:

- SCK idles high between write operations (CPOL = 0)
- Data is valid on the SCK falling edge (CPHA = 1)

When data is to be transmitted to the AD9838, the FSYNC line (PC7) is taken low. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data into the AD9838, PC7 is held low after the first eight bits are transferred, and a second serial write operation is performed to the AD9838. Only after the second eight bits are transferred should FSYNC be taken high again.

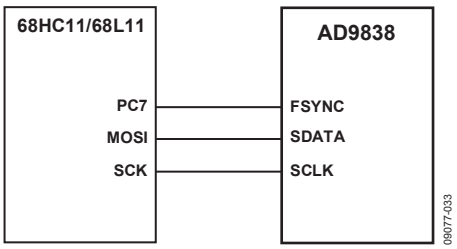


Figure 28. 68HC11/68L11 to AD9838 Interface

AD9838 to 80C51/80L51 Interface

Figure 29 shows the serial interface between the AD9838 and the 80C51/80L51 microcontroller. The microcontroller is operated in Mode 0 so that TxD of the 80C51/80L51 drives SCLK of the AD9838, and RxD drives the serial data line, SDATA. The FSYNC signal is derived from a bit programmable pin on the port (P3.3 is shown in Figure 29).

When data is to be transmitted to the AD9838, P3.3 is taken low. The 80C51/80L51 transmits data in 8-bit bytes with only eight falling SCLK edges occurring in each cycle. To load the remaining eight bits to the AD9838, P3.3 is held low after the first eight bits are transmitted, and a second write operation is initiated to transmit the second byte of data. P3.3 is taken high following the completion of the second write operation. SCLK should idle high between the two write operations.

The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD9838 accepts the MSB first (the four MSBs are the control information, the next four bits are the address, and the eight LSBs contain the data when writing to a destination register). Therefore, the transmit routine of the 80C51/80L51 must take this into account and rearrange the bits so that the MSB is output first.

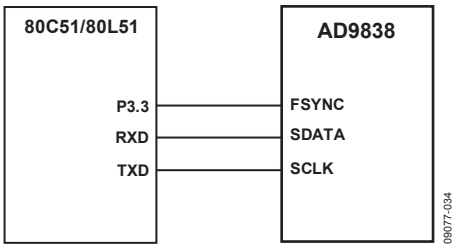


Figure 29. 80C51/80L51 to AD9838 Interface

AD9838 to DSP56002 Interface

Figure 30 shows the interface between the AD9838 and the DSP56002. The DSP56002 is configured for normal mode asynchronous operation with a gated internal clock (SYN = 0, GCK = 1, SCKD = 1). The frame sync pin is generated internally (SC2 = 1), the transfers are 16 bits wide (WL1 = 1, WL0 = 0), and the frame sync signal frames the 16 bits (FSL = 0). The frame sync signal is available on the SC2 pin, but it must be inverted before it is applied to the AD9838. The interface to the DSP56000/DSP56001 is similar to that of the DSP56002.

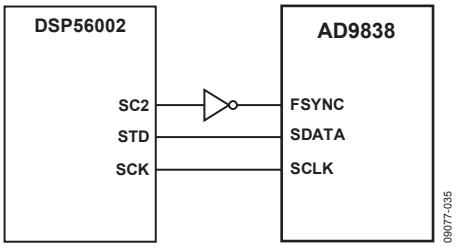


Figure 30. DSP56002 to AD9838 Interface

EVALUATION BOARD

The AD9838 evaluation board allows designers to evaluate the high performance AD9838 DDS modulator with a minimum of effort.

SYSTEM DEMONSTRATION PLATFORM

The system demonstration platform (SDP) is a hardware and software evaluation tool for use in conjunction with product evaluation boards. The SDP board is based on the Blackfin® ADSP-BF527 processor with USB connectivity to the PC through a USB 2.0 high speed port. For more information, see the SDP board product page.

Note that the SDP board is sold separately from the AD9838 evaluation board.

AD9838 TO SPORT INTERFACE

The Analog Devices SDP board has a SPORT serial port that is used to control the serial inputs to the AD9838. The connections are shown in Figure 31.

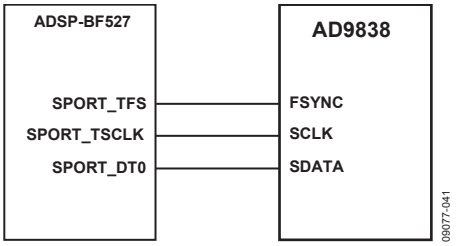


Figure 31. SDP to AD9838 Interface

EVALUATION KIT

The DDS evaluation kit includes a populated, tested AD9838 printed circuit board (PCB). The schematics of the evaluation board are shown in Figure 33 and Figure 34.

The software provided in the evaluation kit allows the user to easily program the AD9838 (see Figure 32). The evaluation software runs on any IBM-compatible PC with Microsoft® Windows® software installed (including Windows 7). The software is compatible with both 32-bit and 64-bit operating systems.

More information about the evaluation software is available on the software CD and on the AD9838 product page.

Figure 32. AD9838 Evaluation Software Interface

CRYSTAL OSCILLATOR VS. EXTERNAL CLOCK

The AD9838 can operate with master clocks up to 16 MHz. A 16 MHz oscillator is included on the evaluation board. This oscillator can be removed and, if required, an external CMOS clock can be connected to the part. Options for the general oscillator include the following:

- AEL 301-Series oscillators, AEL Crystals
- SG-310SCN oscillators, Epson Electronics

POWER SUPPLY

Power to the AD9838 evaluation board can be provided from the USB connector or externally through pin connections. The power leads should be twisted to reduce ground loops.

EVALUATION BOARD SCHEMATICS

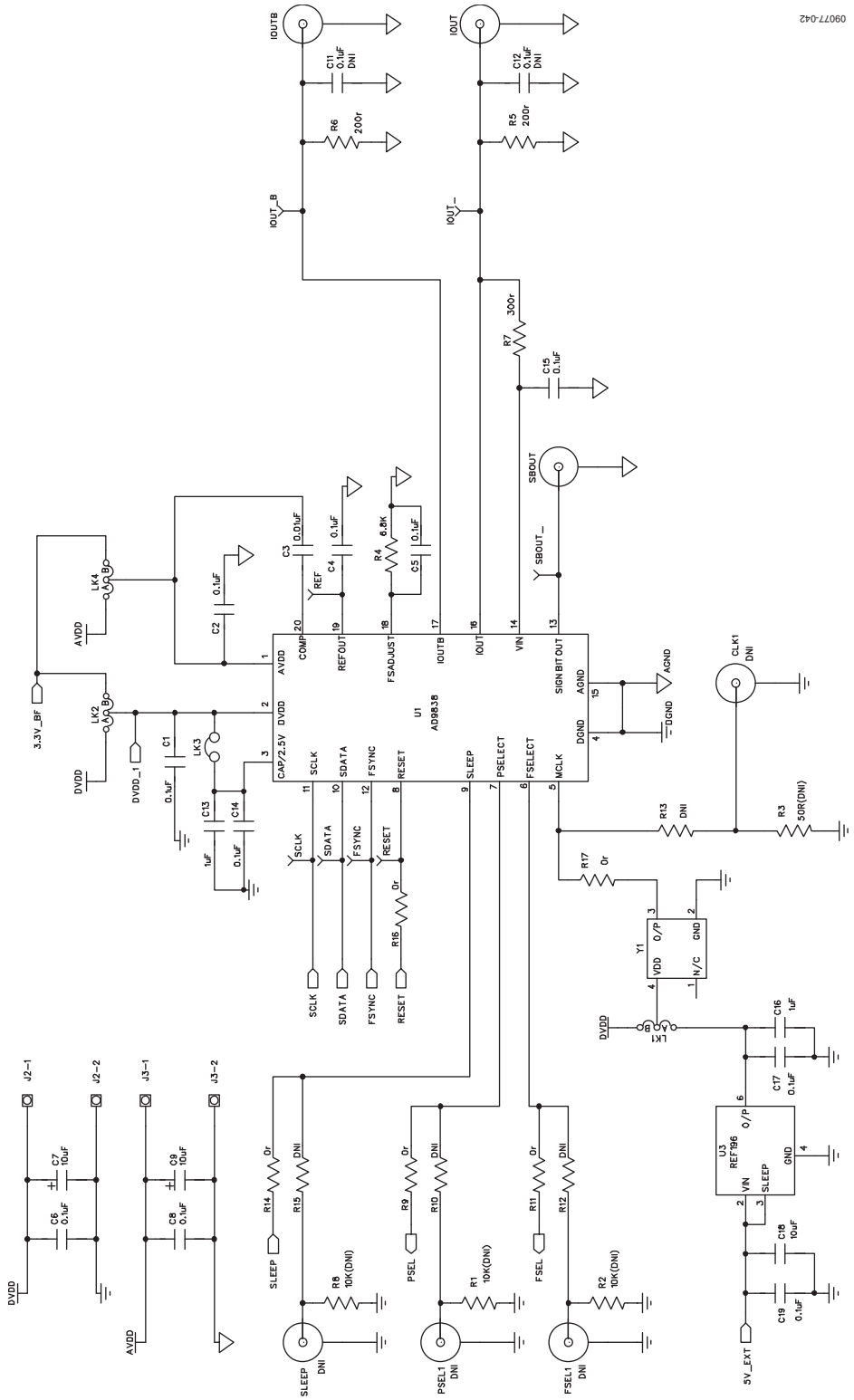


Figure 33. Evaluation Board Schematic

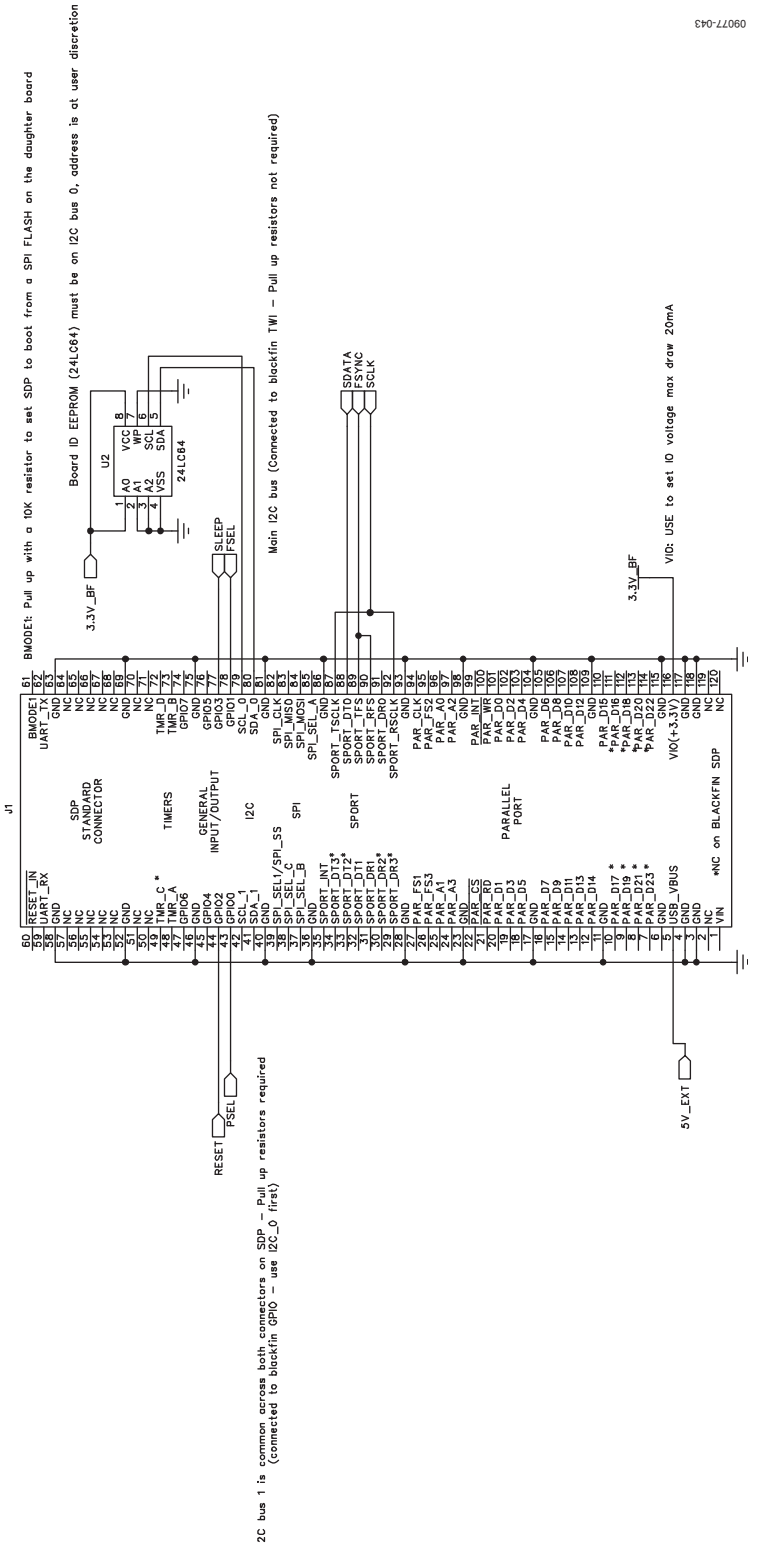


Figure 34. SDP Connector Schematic

EVALUATION BOARD LAYOUT

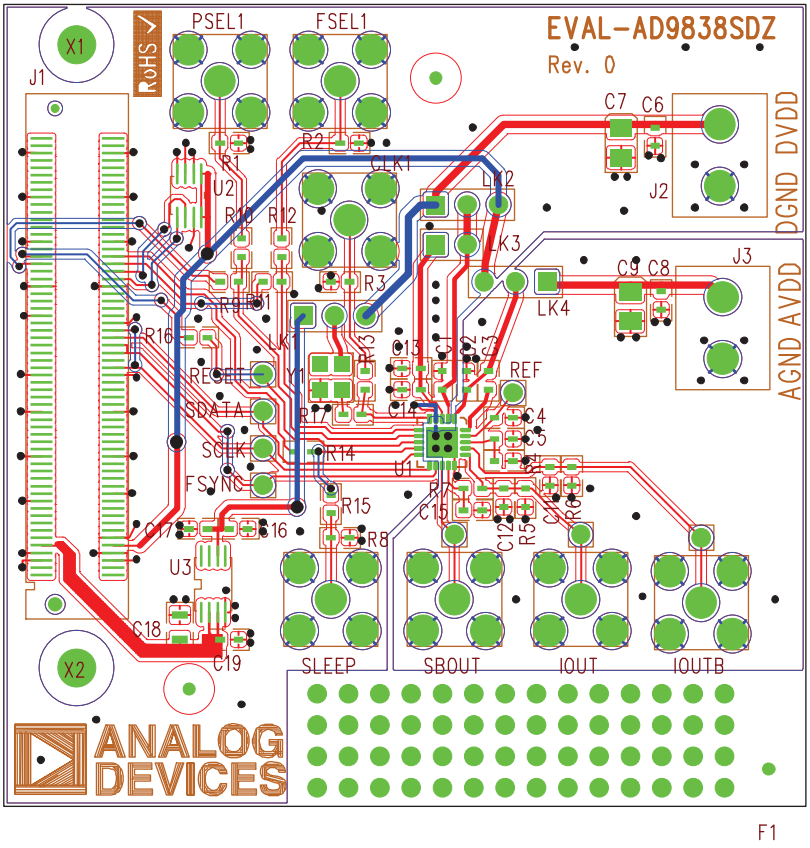


Figure 35. Evaluation Board Layout

OUTLINE DIMENSIONS

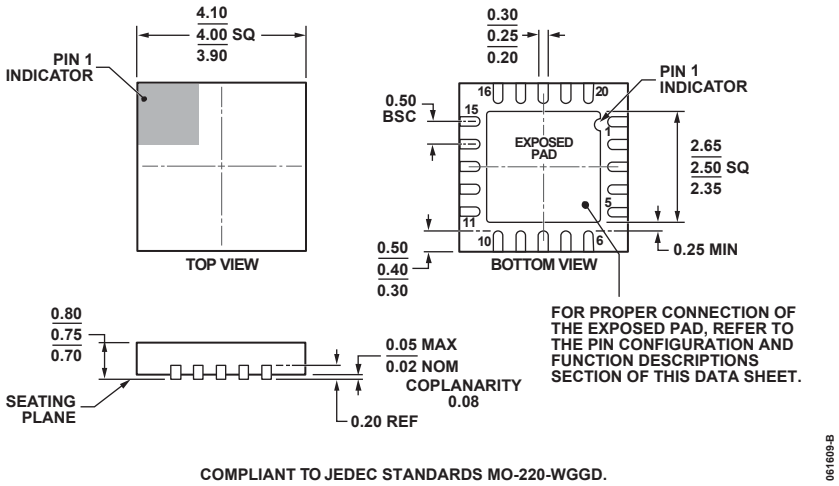


Figure 36. 20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-20-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Max MCLK	Package Description	Package Option
AD9838BCPZ-RL	−40°C to +125°C	16 MHz	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
AD9838BCPZ-RL7	−40°C to +125°C	16 MHz	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
AD9838ACPZ-RL	−40°C to +125°C	5 MHz	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
AD9838ACPZ-RL7	−40°C to +125°C	5 MHz	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-10
EVAL-AD9838SDZ			Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The evaluation board for the AD9838 requires the system demonstration platform (SDP) board, which is sold separately.

NOTES

NOTES

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