TI Panelbus™ Digital Receiver

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 3: –40°C to 85°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Supports Pixel Rates Up to 165 MHz (Including 1080p and WUXGA at 60 Hz)
- Digital Visual Interface (DVI) Specification Compliant(1)
- True-Color, 24-Bit/Pixel, 16.7M Colors at 1 or 2 Pixels per Clock
- Laser-Trimmed Internal Termination Resistors for Optimum Fixed Impedance Matching
- Skew Tolerant Up to One Pixel-Clock Cycle
- 4× Oversampling
- Reduced Power Consumption – 1.8-V Core Operation With 3.3-V I/Os and Supplies(2)
- Reduced Ground Bounce Using Time-Staggered Pixel Outputs
- Low Noise and Good Power Dissipation Using TI PowerPAD™ Packaging
- Advanced Technology Using TI 0.18-µm EPIC-5™ CMOS Process
- TFP401A-Q1 Incorporates HSYNC Jitter Immunity(3)

(1) The TFP401A-Q1 device incorporates additional circuitry to create a stable HSYNC from DVI transmitters that introduce undesirable jitter on the transmitted HSYNC signal.

(2) The TFP401A-Q1 device has an internal voltage regulator that provides the 1.8-V core power supply from the external 3.3-V supplies.

(3) The Digital Visual Interface Specification, DVI, is an industry standard developed by the Digital Display Working Group (DDWG) for high-speed digital connection to digital displays. The TFP401A-Q1 is compliant with the DVI Specification Rev. 1.0.

2 Applications

- High-Definition TV
- HD PC Monitors
- Digital Video
- HD Projectors
- DVI/HDMI Receiver

(4) HDMI video-only

3 Description

The Texas Instruments TFP401A-Q1 device is a TI Panelbus™ flat-panel display product, and is part of a comprehensive family of end-to-end DVI 1.0-compliant solutions. Targeted primarily at desktop LCD monitors and digital projectors, the TFP401A-Q1 device finds applications in any design requiring high-speed digital interface.

The TFP401A-Q1 device supports display resolutions up to 1080p and WUXGA in 24-bit true-color pixel format. It also offers design flexibility to drive one or two pixels per clock, supports TFT or DSTN panels, and provides an option for time-staggered pixel outputs for reduced ground bounce.

PowerPAD advanced packaging technology results in best-of-class power dissipation, footprint, and ultralow ground inductance.

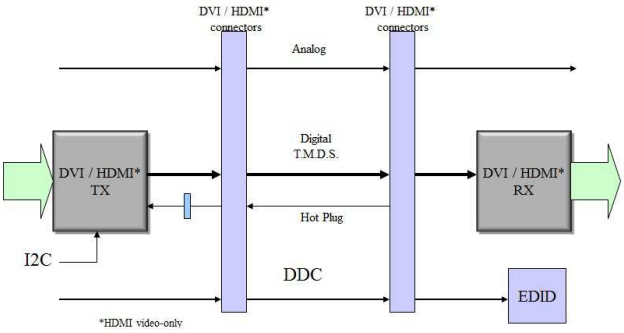
The TFP401A-Q1 combines Panelbus circuit innovation with TI's advanced 0.18-µm EPIC-5™ CMOS process technology, along with TI PowerPAD package technology to achieve a reliable, low-powered, low-noise, high-speed digital interface solution.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TFP401A-Q1	PQFP (100)	14.00 mm × 14.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

TFP401 Diagram



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4 Revision History

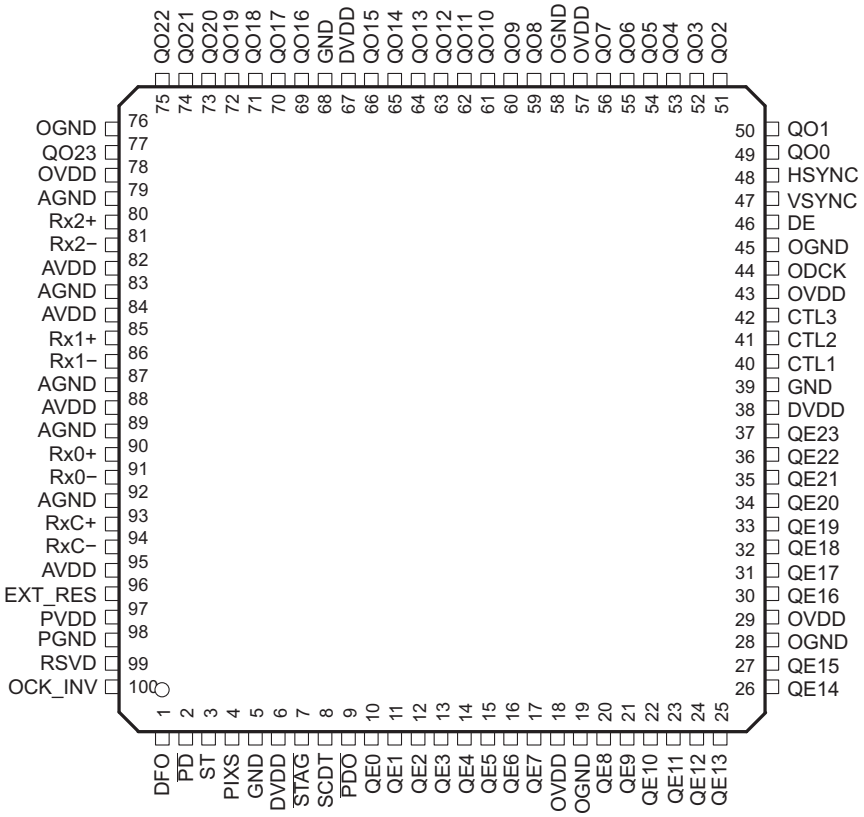
Changes from Original (November 2012) to Revision A **Page**

- Added the *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed Changed *Features* From: "Device HBM ESD Classification Level C3B" To: "Device CDM ESD Classification Level C3" ... 1
- Changed the Operating free-air temperature MIN value From: 0°C To: –40°C and the MAX value From: 70°C To: 85°C in the *Recommended Operating Conditions* ... 6
- Changed the *Thermal Information* table values ... 6

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5 Pin Configuration and Functions

PZP Package
100-Pin PQFP PowerPAD Package
(Top View)



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AGND	79, 83, 87, 89, 92	GND	Analog ground – Ground reference and current return for analog circuitry
AVDD	82, 84, 88, 95	V_{DD}	Analog VDD – Power supply for analog circuitry. Nominally 3.3 V
CTL[3:1]	42, 41, 40	DO	General-purpose control signals – Used for user-defined control. CTL1 is not powered down through PDO.
DE	46	DO	Output data enable – Used to indicate time of active video display versus non-active display or blank time. During blank, the device transmits only HSYNC, VSYNC, and CTL[3:1]. During times of active display, or non-blank, the device transmits only pixel data, QE[23:0], and QO[23:0]. High: Active display time Low: Blank time
DFO	1	DI	Output clock data format – Controls the output clock (ODCK) format for either TFT or DSTN panel support. For TFT support, the ODCK clock runs continuously. For DSTN support, ODCK only clocks when DE is high; otherwise, ODCK remains low when DE is low. High: DSTN support – ODCK held low when DE = low Low: TFT support – ODCK runs continuously.
GND	5, 39, 68	GND	Digital ground – Ground reference and current return for digital core
DVDD	6, 38, 67	V_{DD}	Digital VDD – Power supply for digital core. Nominally 3.3 V.
EXT_RES	96	AI	Internal impedance matching – The TFP401A-Q1 device has internal optimization for impedance matching at 50 Ω. An external resistor tied to this pin has no effect on device performance.
HSYNC	48	DO	Horizontal sync output

(1) DI = Digital Input; DO = Digital Output; AI = Analog Input; AO = Analog Output

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Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
RSVD	99	DI	Reserved. Tie this pin high for normal operation.
OVDD	18, 29, 43, 57, 78	V_{DD}	Output driver VDD – Power supply for output drivers. Nominally 3.3 V
ODCK	44	DO	Output data clock – Pixel clock. The device synchronizes all pixel outputs QE[23:0] and QO[23:0] (if in 2-pixels-per-clock mode), along with DE, HSYNC, VSYNC and CTL[3:1], to this clock.
OGND	19, 28, 45, 58, 76	GND	Output driver ground – Ground reference and current return for digital output drivers
OCK_INV	100	DI	ODCK polarity – Selects ODCK edge to which pixel data (QE[23:0] and QO[23:0]) and control signals (HSYNC, VSYNC, DE, CTL[3:1]) latch. Normal mode: High: Latches output data on rising ODCK edge Low: Latches output data on falling ODCK edge
$\overline{PD}$	2	DI	Power down – An active-low signal that controls the TFP401A-Q1 power-down state. During power down, all output buffers switch to a high-impedance state. The device powers down all analog circuits and disables all inputs, except for $\overline{PD}$. If leaving $\overline{PD}$ unconnected, an internal pullup defaults the TFP401A-Q1 device to normal operation. High : Normal operation Low: Power down
$\overline{PDO}$	9	DI	Output drive power down – An active-low signal that controls the power-down state of the output drivers. During output drive power down, the output drivers (except SCDT and CTL1) are driven to a high-impedance state. When $\overline{PDO}$ is left unconnected, an internal pullup defaults the TFP401A-Q1 device to normal operation. High: Normal operation; output drivers on Low: Output drive powered down
PGND	98	GND	PLL GND – Ground reference and current return for internal PLL.
PIXS	4	DI	Pixel select – Selects between 1- and 2-pixels-per-clock output modes. During the 2-pixels-per-clock mode, the device outputs both even pixels, QE[23:0], and odd pixels, QO[23:0], in tandem on a given clock cycle. During 1-pixel-per-clock mode, the device outputs even and odd pixels sequentially, one at a time, with the even pixel first, on the even-pixel bus, QE[23:0]. (The first pixel per line is pixel-0, the even pixel. The second pixel per line is pixel-1, the odd pixel). High: 2 pixels per clock Low: 1 pixel per clock
PVDD	97	V_{DD}	PLL VDD – Power supply for internal PLL
QE[8:15]	20–27	DO	Even green-pixel output – Output for even and odd green pixels when in 1-pixel-per-clock mode. Output for even-only green pixel when in 2-pixels-per-clock mode. Output data synchronizes to the output data clock, ODCK. LSB: QE8, pin 20 MSB: QE15, pin 27
QE[16:23]	30–37	DO	Even red-pixel output – Output for even and odd red pixels when in 1-pixel-per-clock mode. Output for even-only red pixel when in 2-pixels-per-clock mode. Output data synchronizes to the output data clock, ODCK. LSB: QE16, pin 30 MSB: QE23, pin 37
QO[0:7]	49–56	DO	Odd blue-pixel output – Output for odd-only blue pixel when in 2-pixels-per-clock mode. Not used, and held low, when in 1-pixel-per-clock mode. Output data synchronizes to the output data clock, ODCK. LSB: QO0, pin 49 MSB: QO7, pin 56
QO[8:15]	59–66	DO	Odd green-pixel output – Output for odd-only green pixel when in 2-pixels-per-clock mode. Not used, and held low, when in 1-pixel-per-clock mode. Output data synchronizes to the output data clock, ODCK. LSB: QO8, pin 59 MSB: QO15, pin 66
QO[16:23]	69–75, 77	DO	Odd red-pixel output – Output for odd-only red pixel when in 2-pixels-per-clock mode. Not used, and held low, when in 1-pixel-per-clock mode. Output data synchronizes to the output data clock, ODCK. LSB: QO16, pin 69 MSB: QO23, pin 77

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Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
QE[0:7]	10–17	DO	Even blue-pixel output – Output for even and odd blue pixels when in 1-pixel-per-clock mode. Output for even-only blue pixel when in 2-pixels-per-clock mode. Output data synchronizes to the output data clock, ODCK. LSB: QE0, pin 10 MSB: QE7, pin 17
RxC+	93	AI	Clock positive receiver input – Positive side of reference clock. TMDS low-voltage signal differential-input pair.
RxC–	94	AI	Clock negative receiver input – Negative side of reference clock. TMDS low-voltage signal differential-input pair.
Rx0+	90	AI	Channel-0 positive receiver input – Positive side of channel-0. TMDS low-voltage signal differential-input pair. Channel-0 receives blue pixel data in active display and HSYNC, VSYNC control signals in blank.
Rx0–	91	AI	Channel-0 negative receiver input – Negative side of channel-0. TMDS low-voltage signal differential-input pair.
Rx1+	85	AI	Channel-1 positive receiver input – Positive side of channel-1 TMDS low-voltage signal differential-input pair. Channel-1 receives green-pixel data in active display and CTL1 control signals in blank.
Rx1–	86	AI	Channel-1 negative receiver input – Negative side of channel-1 TMDS low-voltage signal differential-input pair.
Rx2+	80	AI	Channel-2 positive receiver input – Positive side of channel-2 TMDS low-voltage signal differential-input pair. Channel-2 receives red-pixel data in active display and CTL2, CTL3 control signals in blank.
Rx2–	81	AI	Channel-2 negative receiver input – Negative side of channel-2 TMDS low-voltage signal differential-input pair
SCDT	8	DO	Sync detect - Output to signal when the link is active or inactive. The link is active when DE is actively switching. The TFP401A-Q1 device monitors the state of DE to determine link activity. SCDT can be tied externally to $\overline{PDO}$ to power down the output drivers when the link is inactive. High: Active link Low: Inactive link
ST	3	DI	Output drive strength select – Selects output drive strength for high- or low-current drive. (See dc specifications for I_{OH} and I_{OL} versus the ST state). High: High drive strength Low: Low drive strength
$\overline{STAG}$	7	DI	Staggered pixel select – An active-low signal used in the 2-pixels-per-clock pixel mode (PIXS = high). Time-staggers the even and odd pixel outputs to reduce ground bounce. Normal operation outputs the odd and even pixels simultaneously. High: Normal simultaneous even-and-odd pixel output Low: Time-staggered even-and-odd pixel output
VSYNC	47	DO	Vertical sync output

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply-voltage range DVDD, AVDD, OVDD, PVDD	–0.3	4	V
Input-voltage range, logic and analog signals	–0.3	4	V
Operating ambient temperature range, T_A	–40	85	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011 — All pins	±750	
		Charged-device model (CDM), per AEC Q100-011 — Corner pins (1, 25. 26. 50. 51, 75, 76, and 100)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage (DV_{DD}, AV_{DD}, PV_{DD}, OV_{DD})	3	3.3	3.6	V
R_t	Single-ended analog-input termination resistance	45	50	55	Ω
T_A	Operating free-air temperature	–40	25	85	°C

6.4 Thermal Information

THERMAL METRIC (1)		TFP401A-Q1 PZP (PQFP) 100 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semicondictor and IC Package Thermal Metrics* application report.

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6.5 DC Digital I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level digital input voltage		2		DV_{DD}	V
V_{IL}	Low-level digital input voltage		0		0.8	V
I_{OH}	High-level output drive current	ST = high, V_{OH} = 2.4 V	5	10	16.3	mA
		ST = low, V_{OH} = 2.4 V	3	6	10.3	
I_{OL}	Low-level output drive current	ST = high, V_{OL} = 0.8 V	8	13	19	mA
		ST = low, V_{OL} = 0.8 V	4	7	11	
I_{OZ}	Hi-Z output leakage current	$\overline{PD}$ = low or $\overline{PDO}$ = low	–1		1	µA

6.6 DC Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ID}	Analog-input differential voltage(1)		75		1200	mV
V_{IC}	Analog-input common-mode voltage(1)		AV_{DD} – 300		AV_{DD} – 37	mV
$V_{I(OC)}$	Open-circuit analog input voltage		AV_{DD} – 10		AV_{DD} + 10	mV
$I_{DD(2PIX)}$	Normal 2-pixels-per-clock power-supply current(2)	ODCK = 82.5 MHz, 2 pixels per clock			370	mA
I_{PD}	Power-down current(3)	$\overline{PD}$ = low			10	mA
I_{PDO}	Output-drive power-down current(3)	$\overline{PDO}$ = low		35		mA

(1) Specified as dc characteristic with no overshoot or undershoot
(2) Alternating 2-pixel black and 2-pixel white patterns. ST = high, $\overline{STAG}$ = high, QE[23:0] and QO[23:0] C_L = 10 pF.
(3) Analog inputs are open-circuit (transmitter disconnected from the TFP401A-Q1 device).

6.7 AC Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{ID(2)}$	Differential input sensitivity(1)		150		1560	mV_{p-p}
f_{ODCK}	ODCK frequency	PIXS = low (1-PIX/CLK)	25		165	MHz
		PIXS = high (2-PIX/CLK)	12.5		82.5	
	ODCK duty-cycle		45%	60%	75%	

(1) Specified as ac parameter to include sensitivity to overshoot, undershoot, and reflection

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6.8 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ps}	Analog input intra-pair (+ to –) differential skew (1)				0.4	t_{bit} (2)
t_{ccs}	Analog input inter-pair or channel-to-channel skew (1)				1	t_{pix} (3)
t_{ijit}	Worst-case differential input-clock jitter tolerance (1)(4)		50			ps
t_{f1}	Fall time of data and control signals (5)(6)	ST = low, C_L = 5 pF			2.4	ns
		ST = high, C_L = 10 pF			1.9	
t_{r1}	Rise time of data and control signals (5)(6)	ST = low, C_L = 5 pF			2.4	ns
		ST = high, C_L = 10 pF			1.9	
t_{r2}	Rise time of ODCK clock (5)	ST = low, C_L = 5 pF			2.4	ns
		ST = high, C_L = 10 pF			1.9	
t_{f2}	Fall time of ODCK clock (5)	ST = low, C_L = 5 pF			2.4	ns
		ST = high, C_L = 10 pF			1.9	
t_{su1}	Setup time, data and control signal to falling edge of ODCK	1 pixel per clock, PIXS = low, OCK_INV = low	1.8			ns
		2 pixels per clock, PIXS = high, $\overline{STAG}$ = high, OCK_INV = low	3.8			
		2 pixels and STAG, PIXS = high, $\overline{STAG}$ = low, OCK_INV = low	0.6			
t_{h1}	Hold time, data and control signal to falling edge of ODCK	1 pixel per clock, PIXS = low, OCK_INV = low	0.6			ns
		2 pixels and STAG, PIXS = high, $\overline{STAG}$ = low, OCK_INV = low	2.5			
		2 pixels per clock, PIXS = high, $\overline{STAG}$ = high, OCK_INV = low	2.9			
t_{su2}	Setup time, data and control signal to rising edge of ODCK	1 pixels per clock, PIXS = low, OCK_INV = high	2.1			ns
		2 pixels per clock, PIXS = high, $\overline{STAG}$ = high, OCK_INV = high	4			
		2 pixels and STAG, PIXS = high, $\overline{STAG}$ = low, OCK_INV = high	1.5			
t_{h2}	Hold time, data and control signal to rising edge of ODCK	1 pixel per clock, PIXS = low, OCK_INV = high	0.3			ns
		2 pixels and STAG, PIXS = high, $\overline{STAG}$ = low, OCK_INV = high	2.4			
		2 pixels per clock, PIXS = high, $\overline{STAG}$ = high, OCK_INV = high	2.1			
t_{pix}	Pixel time (3)		6.06		40	ns

(1) Specified by Characterization.
(2) t_{bit} is 1/10 the pixel time, t_{pix}.
(3) t_{pix} is the pixel time defined as the period of the RxC clock input. The period of the output clock, ODCK, is equal to t_{pix} when in 1-pixel-per-clock mode or 2 t_{pix} when in 2-pixels-per-clock mode.
(4) Measured differentially at 50% crossing using ODCK output clock as trigger
(5) Rise and fall times measured as time between 20% and 80% of signal amplitude
(6) Data and control signals are QE[23:0], QO[23:0], DE, HSYNC, VSYNC. and CTL[3:1].

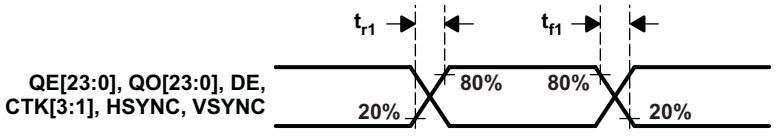


Figure 1. Rise and Fall Times of Data and Control Signals

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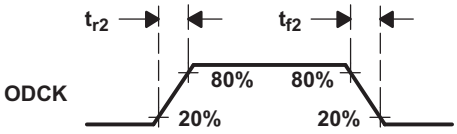


Figure 2. Rise and Fall Times of ODCK

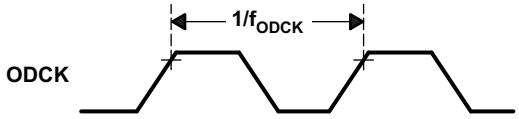


Figure 3. ODCK Frequency

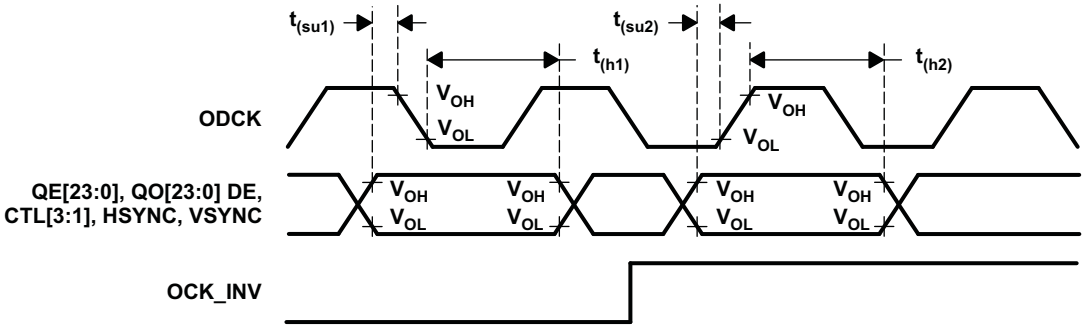


Figure 4. Data Setup and Hold Times to Rising and Falling Edges of ODCK

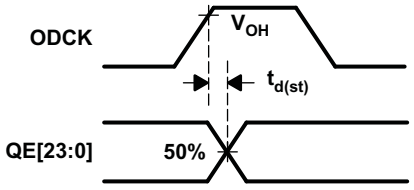


Figure 5. ODCK High to QE[23:0] Staggered Data Output

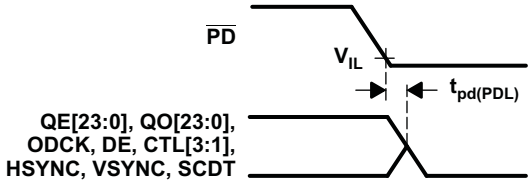


Figure 6. Delay From $\overline{PD}$ Low to Hi-Z Outputs

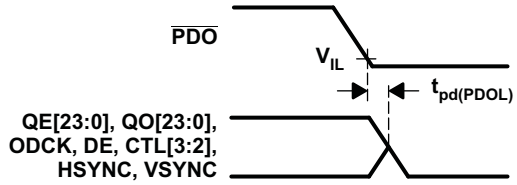


Figure 7. Delay From $\overline{PDO}$ Low to Hi-Z Outputs

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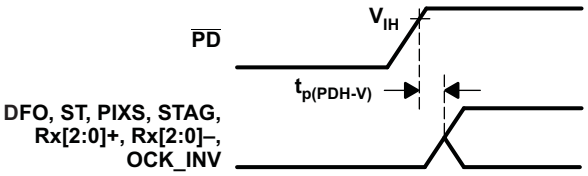


Figure 8. Delay From $\overline{PD}$ Low to High Until Inputs Are Active

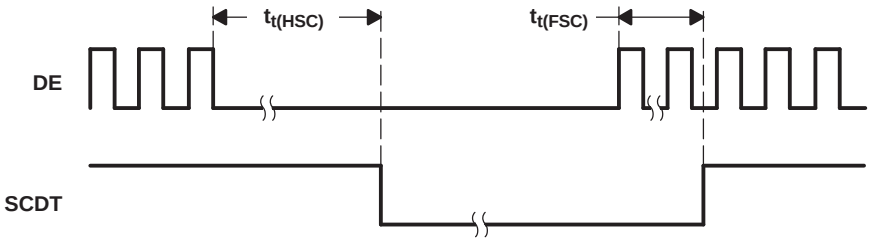


Figure 9. Time From DE Transitions to SCDT Low and SCDT High

6.9 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(PDL)}$	Propagation delay time from $\overline{PD}$ low to Hi-Z outputs				9	ns
$t_{pd(PDOL)}$	Propagation delay time from $\overline{PDO}$ low to Hi-Z outputs				9	ns
$t_{t(HSC)}$	Delay time from DE transition to SCDT low(1)			1e6		t_{pix}
$t_{t(FSC)}$	Delay time from DE transition to SCDT high(1)			1600		t_{pix}
$t_{d(st)}$	Delay time, ODCK latching edge to QE[23:0] data output	$\overline{STAG}$ = low, PIXS = high		0.25		t_{pix}

(1) Amount of time detected between DE transitions determines whether link is active or inactive. SCDT indicates link activity.

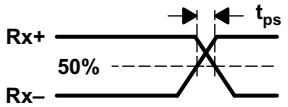


Figure 10. Analog Input Intra-Pair Differential Skew

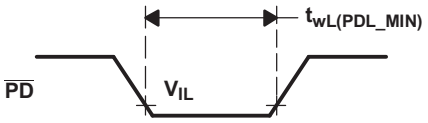


Figure 11. Minimum Time $\overline{PD}$ Low

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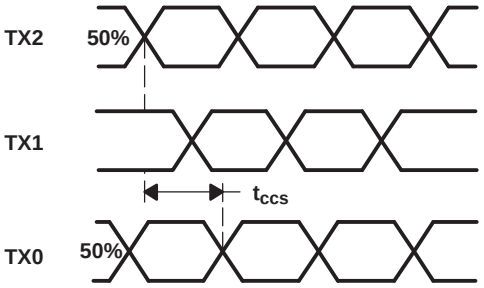


Figure 12. Analog Input Channel-to-Channel Skew

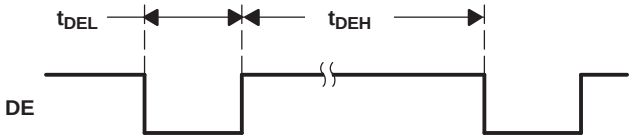


Figure 13. Minimum DE Low and Maximum DE High

6.10 Typical Characteristics

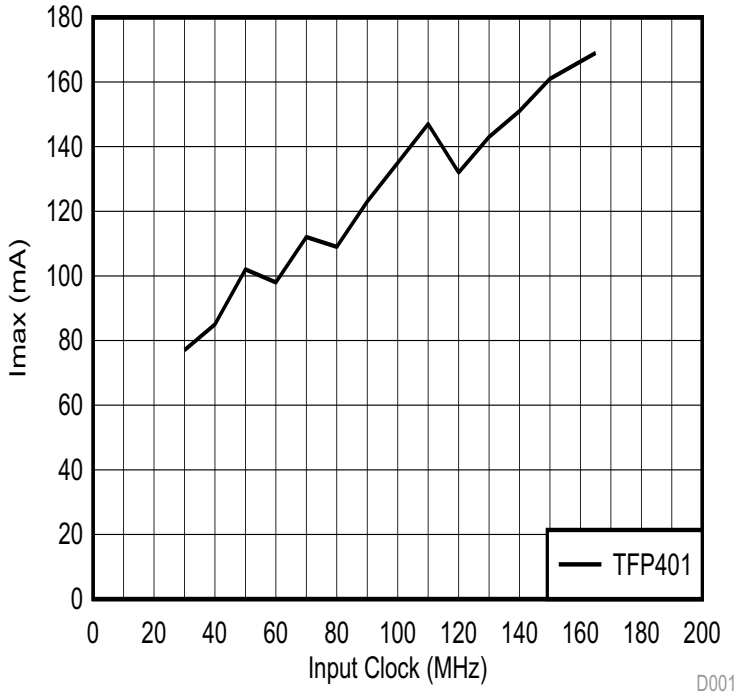


Figure 14. Imax vs Input Frequency

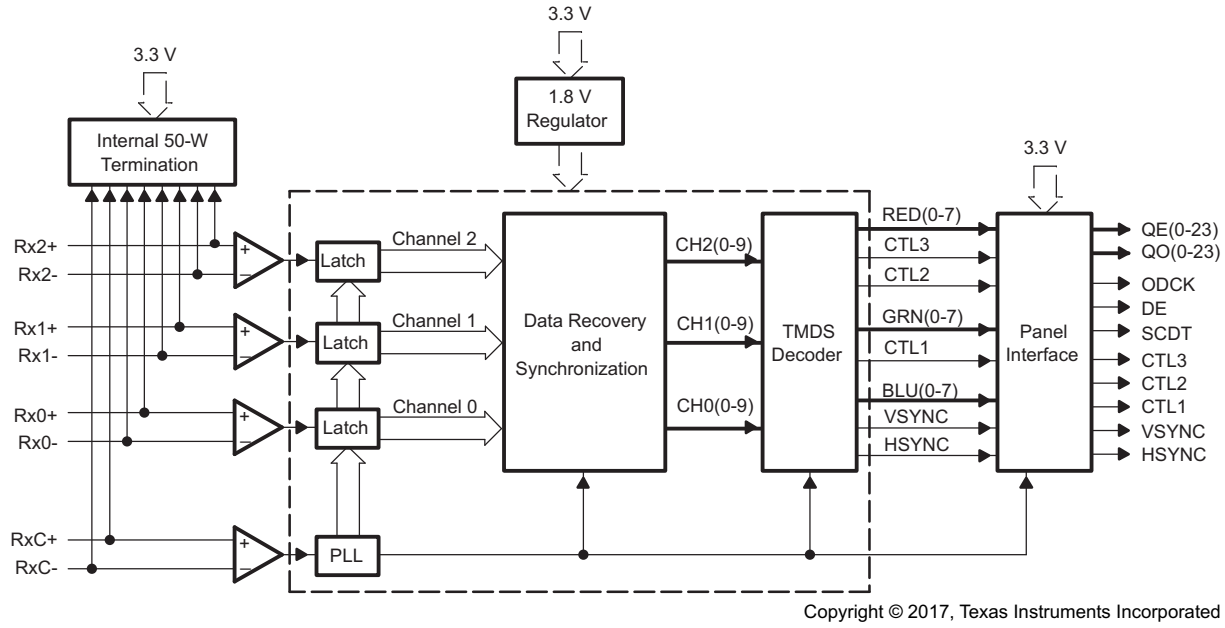
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7 Detailed Description

7.1 Overview

The TFP401A-Q1 device is a digital visual interface (DVI)-compliant TMDS digital receiver used in digital flat-panel display systems to receive and decode TMDS-encoded RGB pixel data streams. In a digital display system, a host (usually a PC or workstation) contains a TMDS-compatible transmitter that receives 24-bit pixel data along with appropriate control signals. The host encodes the data and control signals into a high-speed low-voltage differential serial bit stream (fit for transmission over a twisted-pair cable) to a display device. The display device (usually a flat-panel monitor) requires a TMDS-compatible receiver like the TI TFP401A-Q1 device to decode the serial bit stream back to the same 24-bit pixel data and control signals that originated at the host. This decoded data is then suitable for application directly to the flat-panel drive circuitry to produce an image on the display. Host and display separation distances can be up to 5 meters or more, making serial transmission of the pixel data preferable. Support of modern display resolutions up to UXGA requires a high-bandwidth receiver with good jitter and skew tolerance.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 TMDS Pixel Data and Control Signal Encoding

The device transmits only one of two possible transition-minimized differential signaling (TMDS) characters for a given pixel at a given time. The transmitter keeps a running count of the number of ones and zeros previously sent, and transmits the character that minimizes the number of transitions to approximate a dc balance of the transmission line.

Reception of RGB pixel data during active display time uses three TMDS channels, DE = high. The same three channels also receive control signals, HSYNC, VSYNC, and user-defined control signals CTL[3:1]. Reception of these control signals occurs during inactive display or blanking-time. Blanking-time is when DE = low. The following table maps the received input data to the appropriate TMDS input channel in a DVI-compliant system.

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Feature Description (continued)

Table 1. TMDS Pixel Data and Control Signal Encoding

RECEIVED PIXEL DATA ACTIVE DISPLAY DE = HIGH	INPUT CHANNEL	OUTPUT PINS (VALID FOR DE = HIGH)
Red[7:0]	Channel-2 (Rx2 ±)	QE[23:16] QO[23:16]
Green[7:0]	Channel-1 (Rx1 ±)	QE[15:8] QO[15:8]
Blue[7:0]	Channel-0 (Rx0 ±)	QE[7:0] QO[7:0]
RECEIVED CONTROL DATA BLANKING DE = LOW	**INPUT CHANNEL**	**OUTPUT PINS (VALID FOR DE = LOW)**
CTL[3:2]	Channel-2 (Rx2 ±)	CTL[3:2]
CTL[1: 0](1)	Channel-1 (Rx1 ±)	CTL1
HSYNC, VSYNC	Channel-0 (Rx0 ±)	HSYNC, VSYNC

(1) Some TMDS transmitters transmit a CTL0 signal. The TFP401A-Q1 device decodes and transfers CTL[3:1] and ignores CTL0 characters. CTL0 is not available as a TFP401A-Q1 output.

The TFP401A-Q1 device discriminates between valid pixel TMDS characters and control TMDS characters to determine the state of active display versus blanking, in effect, the state of DE.

7.3.2 TFP401A-Q1 Clocking and Data Synchronization

The TFP401A-Q1 device receives a clock reference from the DVI transmitter that has a period equal to the pixel time, t_{pix}. Another name for the frequency of this clock is the pixel rate. Because the TMDS encoded data on Rx[2:0] contains 10 bits per 8-bit pixel, it follows that the Rx[2:0] serial bit rate is 10 times the pixel rate. For example, the required pixel rate to support a UXGA resolution with 60-Hz refresh rate is 165 MHz. The TMDS serial bit rate is 10× the pixel rate, or 1.65 Gb/s. Due to the transmission of this high-speed digital bit stream, on three separate channels (or twisted-pair wires) of long distances (3–5 meters), there is no assurance of phase synchronization between the data steams and the input reference clock. In addition, skew between the three data channels is common. The TFP401A-Q1 device uses a 4× oversampling scheme of the input data streams to achieve reliable synchronization with up to 1-t_{pix} channel-to-channel skew tolerance. Accumulated jitter on the clock and data lines due to reflections and external noise sources is also typical of high-speed serial data transmission; hence, the TFP401A-Q1 design for high jitter tolerance.

A phase-locked loop (PLL) conditions the input clock of the TFP401A-Q1 device to remove high-frequency jitter from the clock. The PLL provides four 10× clock outputs of different phase to locate and sync the TMDS data streams (4× oversampling). During active display, the pixel data encoding is for transition minimization, whereas in blank, the control data encoding is for transition maximization. Transmitting in blank for a minimum period of time, 128 t_{pix}, requires a DVI-compliant transmitter to ensure sufficient time for data synchronization when the receiver sees a transition-maximized code. Synchronization during blank, when the data is transition-maximized, ensures reliable data-bit boundary detection. Phase synchronization to the data streams, maintained as long as the link remains active, is unique for each of the three input channels.

7.3.3 TFP401A-Q1 TMDS Input Levels and Input Impedance Matching

The TMDS inputs to the TFP401A-Q1 receiver have a fixed single-ended termination to AV_{DD}. A laser trim process internally optimizes the TFP401A-Q1 device to fix the impedance precisely at 50 Ω. The device functions normally with or without a resistor on the EXT_RES pin, so it remains drop-in compatible with current sockets. The fixed impedance eliminates the need for an external resistor while providing optimum impedance matching to standard 50-Ω DVI cables.

Figure 15 shows a conceptual schematic of a DVI transmitter and TFP401A-Q1 receiver connection. A transmitter drives the twisted-pair cable through a current source, usually using an open-drain type of output driver. The internal resistor, matched to the cable impedance at the TFP401A-Q1 input, provides a pullup to AV_{DD}. Naturally, with the transmitter disconnected and the TFP401A-Q1 DVI inputs left unconnected, the TFP401A-Q1 receiver inputs pull up to AV_{DD}. Figure 16 shows the single-ended differential signal and full-differential signal. The design of the TFP401A-Q1 device is for response to differential signal swings ranging from 150 mV to 1.56 V, with common-mode voltages ranging from (AV_{DD} – 300 mV) to (AV_{DD} – 37 mV).

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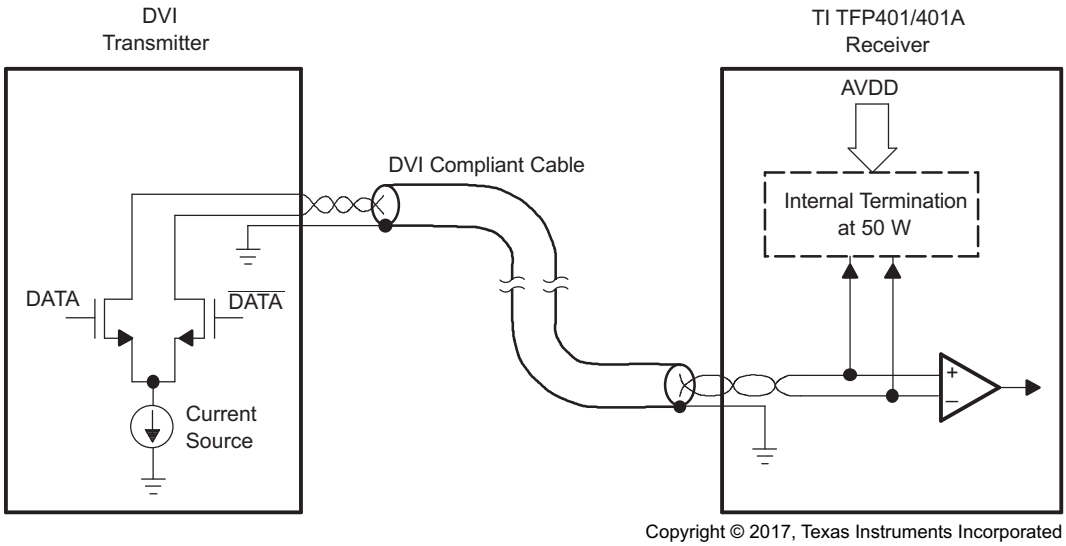


Figure 15. TMDS Differential Input and Transmitter Connection

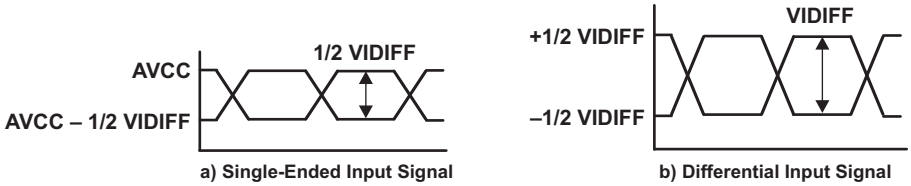


Figure 16. TMDS Inputs

7.3.4 TFP401A-Q1 Device Incorporates HSYNC Jitter Immunity

Several DVI transmitters available in the market introduce jitter on the transmitted HSYNC and VSYNC signals during the TMDS encryption process. The HSYNC signal can shift by one pixel position (one clock) from nominal in either direction, resulting in up to two cycles of HSYNC shift. This jitter carries through to the DVI receiver, and if the position of HSYNC shifts continuously, the receiver can lose track of the input timing, causing pixel noise to occur on the display. For this reason, one should use a DVI-compliant receiver with HSYNC jitter immunity in all displays that could be connected to host PCs with transmitters that have this HSYNC jitter problem.

The TFP401A-Q1 integrates HSYNC regeneration circuitry that provides a seamless interface to these noncompliant transmitters. The regeneration circuitry always fixes the position of the data enable (DE) signal in relation to data, irrespective of the location of HSYNC. The TFP401A-Q1 receiver uses the DE and clock signals to recreate stable vertical and horizontal sync signals. The circuit filters the HSYNC output of the receiver and shifts HSYNC to the nearest eighth bit boundary, producing a stable output with respect to the data, as shown in Figure 17. This ensures accurate data synchronization at the input of the display timing controller.

This HSYNC regeneration circuit is transparent to the monitor, and removal is unnecessary even if the transmitted HSYNC is stable. For example, the *PanelBus* line of DVI 1.0-compliant transmitters, such as the TFP6422 and TFP420, do not have the HSYNC jitter problem. The TFP401A-Q1 device operates correctly with either compliant or noncompliant transmitters. In contrast, the TFP401A-Q1 device is ideal for customers who have control over the transmit portion of the design, such as bundled-system manufacturers and for internal monitor use (the DVI connection between monitor and panel modules).

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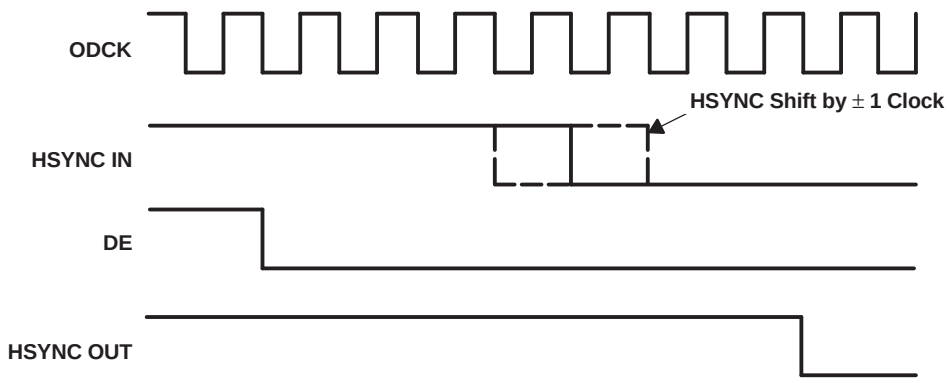


Figure 17. HSYNC Regeneration Timing Diagram

7.4 Device Functional Modes

7.4.1 TFP401A-Q1 Modes of Operation

The TFP401A-Q1 device provides system design flexibility and value by providing the system designer with configurable options or modes of operation to support varying system architectures. Table 2 outlines the various supportable panel modes, along with appropriate external control pin settings.

Table 2. Supported Panel Modes

PANEL	PIXEL RATE	ODCK LATCH EDGE	ODCK	DFO	PIXS	OCK_INV
TFT or 16-bit DSTN	1 pixel per clock	Falling	Free run	0	0	0
TFT or 16-bit DSTN	1 pixel per clock	Rising	Free run	0	0	1
TFT	2 pixels per clock	Falling	Free run	0	1	0
TFT	2 pixels per clock	Rising	Free run	0	1	1
24-bit DSTN	1 pixel per clock	Falling	Gated low	1	0	0
None	1 pixel per clock	Rising	Gated low	1	0	1
24-bit DSTN	2 pixels per clock	Falling	Gated low	1	1	0
24-bit DSTN	2 pixels per clock	Rising	Gated low	1	1	1

7.4.2 TFP401A-Q1 Output Driver Configurations

The TFP401A-Q1 device provides flexibility by offering various output driver features for use to optimize power consumption, ground bounce, and power-supply noise. The following sections outline the output driver features and their effects.

Output Driver Power Down ($\overline{PDO}$ = low): Pulling $\overline{PDO}$ low places all the output drivers, except CTL1 and SCDT, into a high-impedance state. One can tie the SCDT output, which indicates link-disabled or link-inactive, directly to the $\overline{PDO}$ input to disable the output drivers when the link is inactive or when the cable is disconnected. An internal pullup on the $\overline{PDO}$ pin defaults the TFP401A-Q1 device to the normal nonpower-down output-drive mode if left unconnected.

Drive Strength (ST = high for high drive strength, ST = low for low drive strength): The TFP401A-Q1 device allows for selectable output drive strength on the data, control, and ODCK outputs. See the *DC Electrical Characteristics* table for the values of I_{OH} and I_{OL} current drives for a given ST state. The high output-drive strength offers approximately two times the drive as the low output-drive strength.

Time-Staggered Pixel Output: This option works only in conjunction with the 2-pixels-per-clock mode (PIXS = high). Setting $\overline{STAG}$ = low time-staggers the even- and odd-pixel outputs so as to reduce the amount of instantaneous current surge from the power supply. Depending on the PCB layout and design, this can help reduce the amount of system ground bounce and power-supply noise. The time stagger is such that in 2-pixels-per-clock mode, the even pixel is delayed from the latching edge of ODCK by 0.25 t_{cip}. (t_{cip} is the period of ODCK. The ODCK period is 2 t_{pix} when in 2-pixels-per-clock mode.)

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Depending on system constraints of output load, pixel rate, panel input architecture, and board cost, the TFP401A-Q1 drive-strength and staggered-pixel options allow flexibility to reduce system power-supply noise, ground bounce, and EMI.

Power Management: The TFP401A-Q1 device offers several system power-management features.

The output-driver power down ($\overline{PDO}$ = low) is an intermediate mode which offers several uses. During this mode, all output drivers except SCDT and CTL1 go into a high-impedance state while the rest of the device circuitry remains active.

Power down ($\overline{PD}$ = low) of the TFP401A-Q1 device is a complete power down in that it powers down the digital core, the analog circuitry, and output drivers. All output drivers go into a Hi-Z state. Of all the inputs, only $\overline{PD}$ remains active. The TFP401A-Q1 device does not respond to any digital or analog inputs until $\overline{PD}$ is pulled high.

Both $\overline{PDO}$ and $\overline{PD}$ have internal pullups, so if left unconnected they default the TFP401A-Q1 device to normal operating modes.

Sync Detect: The TFP401A-Q1 device offers an output, SCDT, to indicate link activity. The TFP401A-Q1 device monitors activity on DE to determine if the link is active. When 1 million (1e6) pixel clock periods pass without a transition on DE, the TFP401A-Q1 device considers the link inactive, and drives SCDT low. While SCDT is low, if two DE transitions are detected within 1600 pixel clock periods, the device considers the link active and pulls SCDT high.

A use of SCDT is to signal a system power management circuit to initiate a system power down when the device considers the link inactive. One can also tie the SCDT directly to the TFP401A-Q1 $\overline{PDO}$ input to power down the output drivers when the link is inactive. It is not recommended to use SCDT to drive the $\overline{PD}$ input, because once in complete power-down, the analog inputs are ignored and the SCDT state does not change. An external system power-management circuit to drive $\overline{PD}$ is preferred.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TFP401A-Q1 is a DVI (Digital Visual Interface) compliant digital receiver that is used in digital flat panel display systems to receive and decode T.M.D.S. encoded RGB pixel data streams. In a digital display system a host, usually a PC or workstation, contains a DVI compliant transmitter that receives 24 bit pixel data along with appropriate control signals and encodes them into a high speed low voltage differential serial bit stream fit for transmission over a twisted-pair cable to a display device. The display device, usually a flat-panel monitor, will require a DVI compliant receiver like the TI TFP401A-Q1 to decode the serial bit stream back to the same 24 bit pixel data and control signals that originated at the host. This decoded data can then be applied directly to the flat panel drive circuitry to produce an image on the display. Since the host and display can be separated by distances up to 5 meters or more, serial transmission of the pixel data is preferred. The TFP401A-Q1 will support resolutions up to UXGA.

8.2 Typical Application



Figure 18. Typical Application

8.2.1 Design Requirements

Table 3. Design Parameters

PARAMETER	VALUE
Power supply	3.3 V-DC at 1 A
Input clock	Single-ended
Input clock frequency range	25 MHz to 165 MHz
Output format	24 bits/pixel
Input clock latching	Rising edge
I2C EEPROM support	No
De-skew	No

8.2.2 Detailed Design Procedure

8.2.2.1 Data and Control Signals

The trace length of data and control signals out of the receiver should be kept as close to equal as possible. Trace separation should be ~5X Height. As a general rule, traces also should be less than 2.8 inches if possible (longer traces can be acceptable).

Calculation:

$$\text{Delay} = 85 \times \text{SQRT er} \quad (1)$$

$$\text{er} = 4.35; \text{ relative permitivity of 50\% resin FR-4 at 1 GHz} \quad (2)$$

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Delay = 177 pS/inch (3)

Length of rising edge = Tr(picoseconds)/Delay; Tr = 3 nS (4)
= 3000 ps/177 ps per inch (5)
= 16.9 inches (6)

Length of rising edge / 6 = Max length of trace for lumped circuit (7)
16.9 / 6 = 2.8 inches (8)

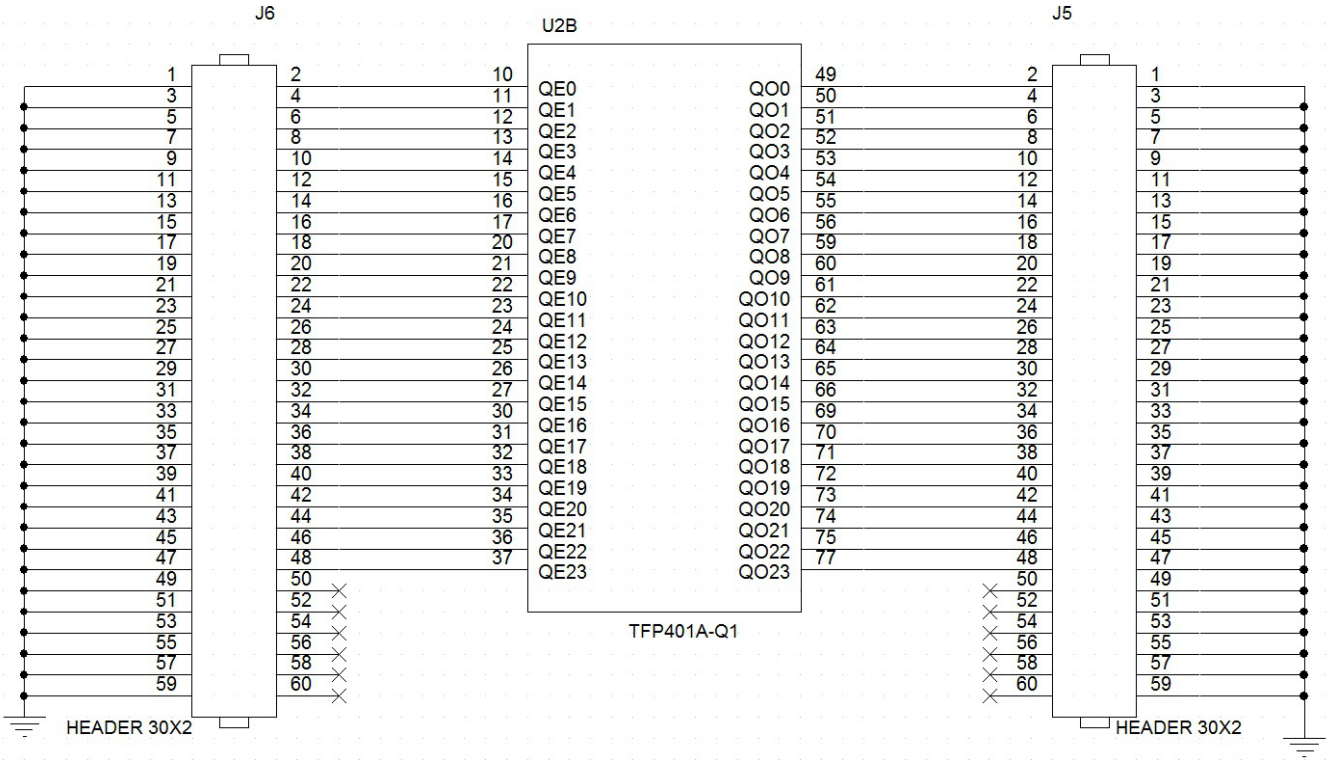


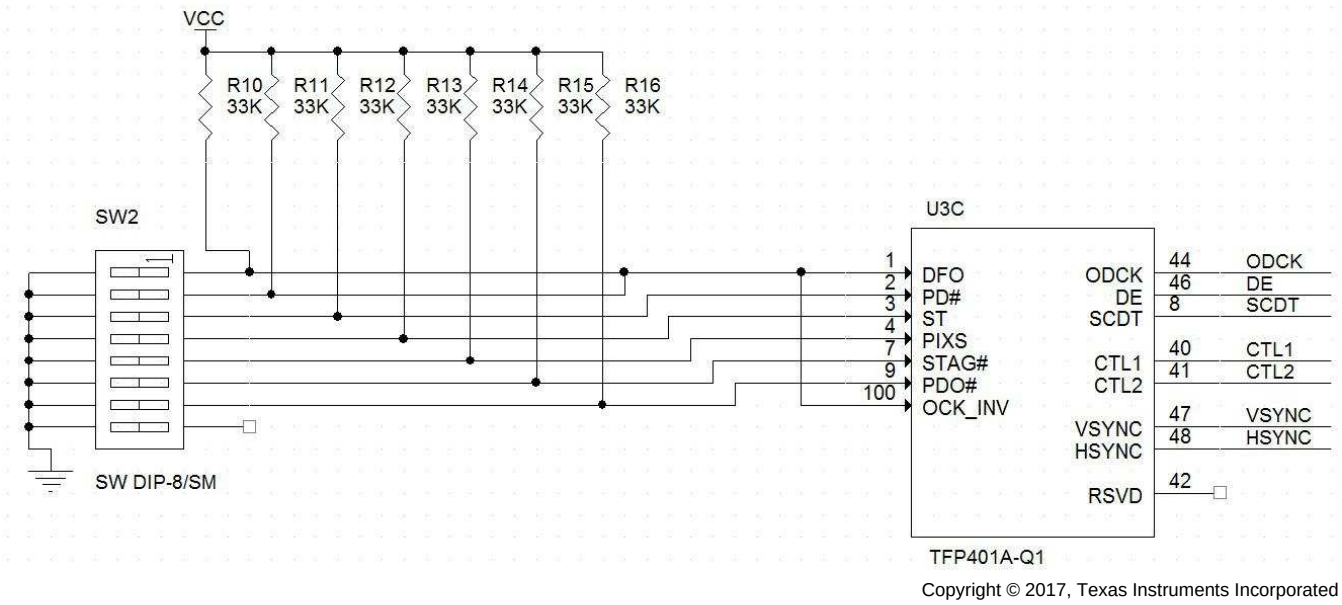
Figure 19. TFP401A-Q1 App Info Data and Control Signals

8.2.2.2 Configuration Options

The TFP401A-Q1 can be configured in several modes depending on the required output format, for example 1-byte/clock, 2-bytes/clock, falling/rinsing clock edge.

You can leave place holders for future configuration changes.

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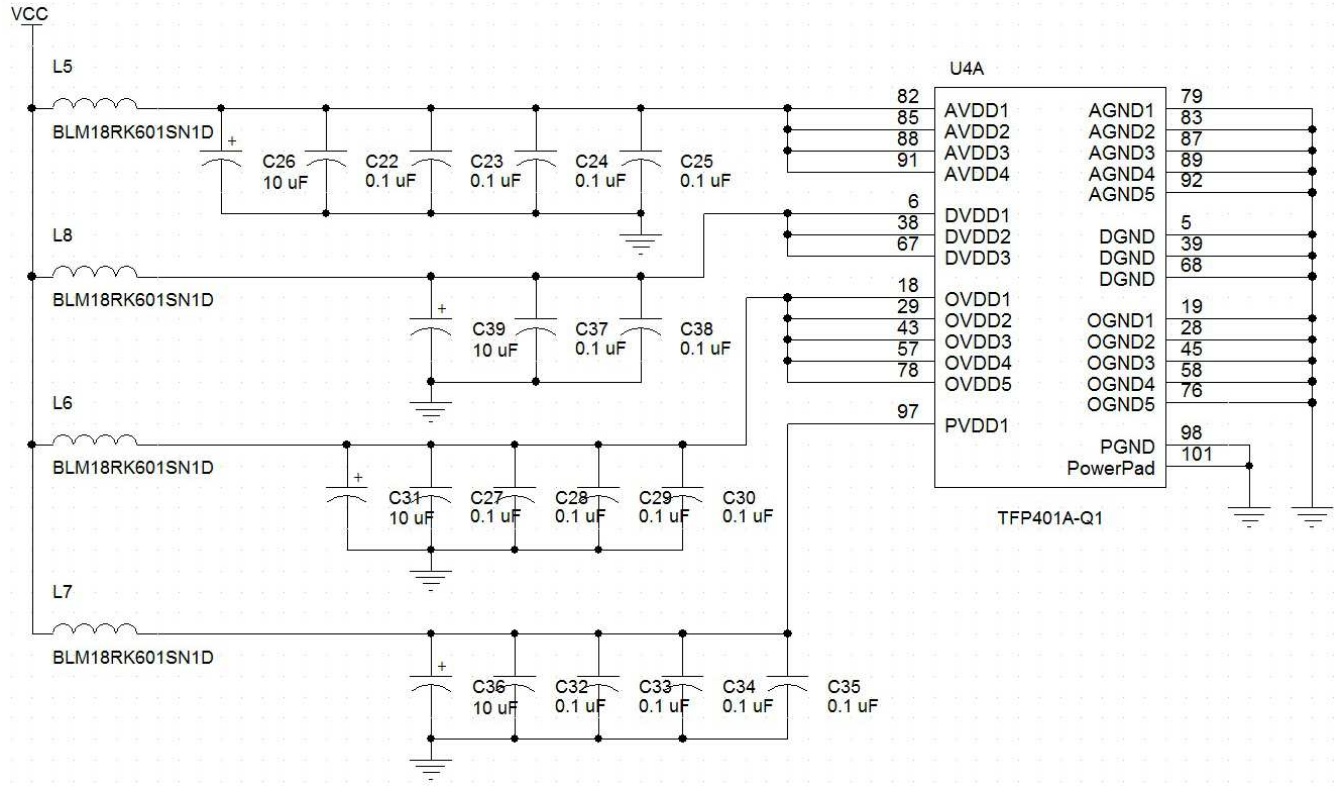


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Figure 20. TFP401A-Q1 App Info Config Options

8.2.2.3 Power Supplies Decoupling

Digital, analog and PLL supplies must be decoupled from each other to avoid electrical noise on the PLL and the core.



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Figure 21. TFP401A-Q1 App Info Power Decoupling

8.2.3 Application Curves

Sometimes the Panel does not support the same format as the GPU (graphics processor unit). In these cases the user must decide how to connect the unused bits.

The below plots show the mismatches between the 18-bit GPU and a 24-bit LCD where “x” and “y” represent the 2 LSB of the Panel.

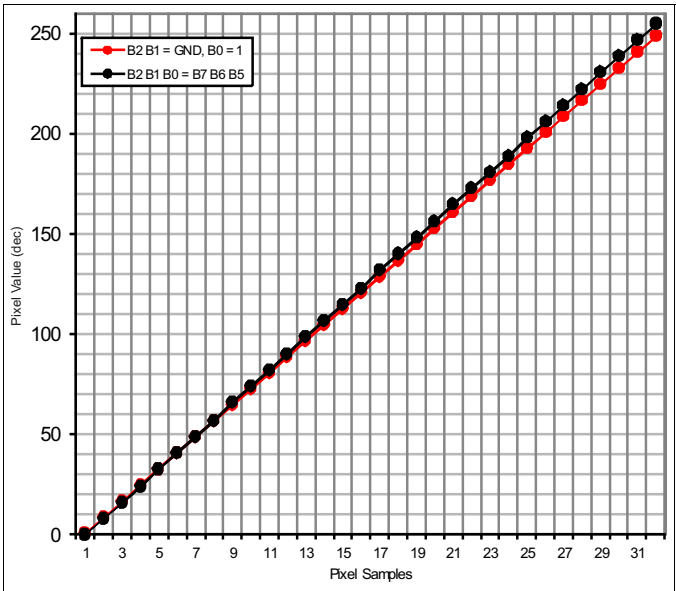


Figure 22. 16b GPU to 24b LCD

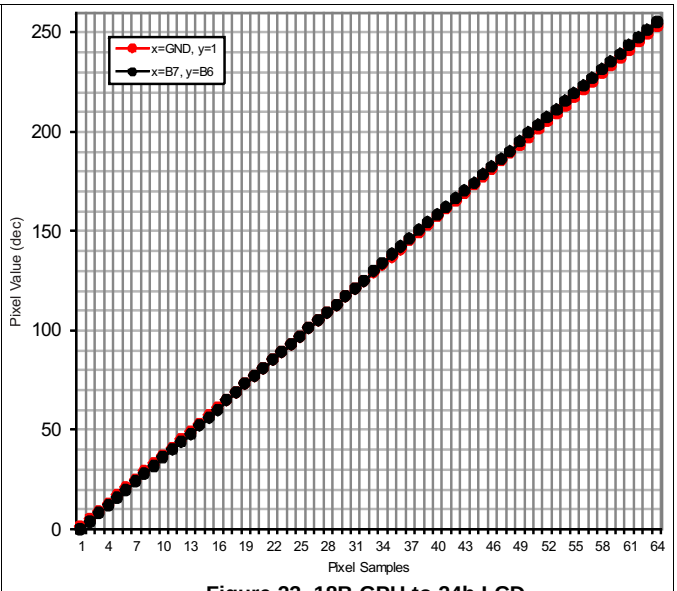


Figure 23. 18B GPU to 24b LCD

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9 Power Supply Recommendations

Use solid ground planes, tie ground planes together with as many vias as is practical. This will provide a desirable return path for current. Each supply should be on separate split power planes, where each power plane should be as large an area as possible. Connect PanelBus receiver power and ground pins and all bypass caps to appropriate power or ground plane with via. Vias should be as fat and short as practical, the goal is to minimize the inductance.

9.1 DVDD

Place one 0.01-uF capacitor as close as possible between each DVDD device pin (Pins 6, 38, 67) and ground.

9.2 OVDD

Place one 0.01-µF capacitor as close as possible between each OVDD device pin (Pins 18, 29, 43, 57, 78) and ground.

A 22-µF tantalum capacitor should be placed between the supply and 0.01-uF capacitors.

A ferrite bead should be used between the source and the 22-uF capacitor.

9.3 AVDD

Place one 0.01-uF capacitor as close as possible between each AVDD device pin (Pins 82, 84, 88, 95) and ground.

A 22-uF tantalum capacitor should be placed between the supply and 0.01-uF capacitors.

A ferrite bead should be used between the source and the 22-uF capacitor.

9.4 PVDD

Place three 0.01-µF capacitors in parallel as close as possible between the PVDD device pin (Pin 97) and ground. A 22-µF tantalum capacitor should be placed between the supply and 0.01-µF capacitors. A ferrite bead should be used between the source and the 22-uF capacitor.

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10 Layout

10.1 Layout Guidelines

10.1.1 Layer Stack

The pinout of Texas Instruments High Speed Interface (HSI) devices features differential signal pairs and the remaining signals comprise the supply rails, VCC and ground, and lower speed signals such as control pins. As an example, consider a device X which is a repeater/re-driver, so both its inputs and outputs are high-speed differential signals. These guidelines can be applied to other high-speed devices such as drivers, receivers, multiplexers, and so on.

A minimum of four layers is required to accomplish a low EMI PCB design. Layer stacking should be in the following order (top-to-bottom): high-speed differential signal layer, ground plane, power plane and control signal layer.

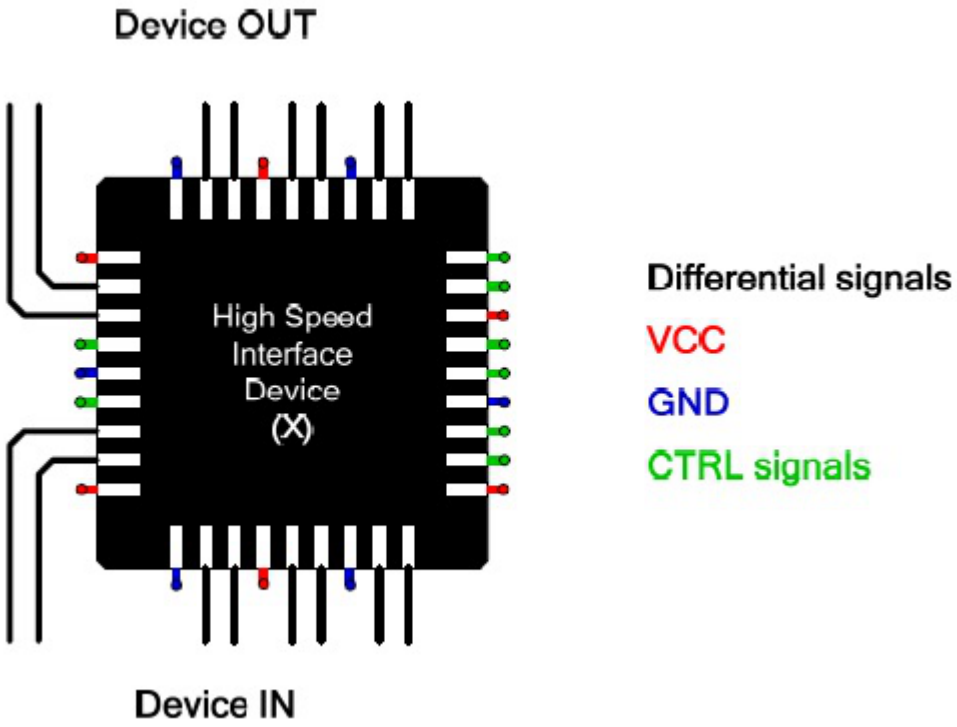


Figure 24. Layer Stack

10.1.2 Routing High-Speed Differential Signal Traces (RxC-, RxC+, Rx0-, Rx0+, Rx1-, Rx1+, Rx2-, Rx2+)

Trace impedance should be controlled for optimal performance. Each differential pair should be equal in length and symmetrical and should have equal impedance to ground with a trace separation of 2X to 4X Height. A differential trace separation of 4X Height yields about 6% cross-talk (6% effect on impedance). We recommend that differential trace routing should be side by side, though it is not important that the differential traces be tightly coupled together because tight coupling is not achievable on PCB traces. Typical ratios on PCB's are only 20-50%, 99.9% is the value of a well-balanced twisted pair cable. Each differential trace should be as short as possible (< 2 inches preferably) with no 90° angles. These high-speed transmission traces hould be on layer 1 (top layer).

RxC-, RxC+, Rx0-, Rx0+, Rx1-, Rx1+, Rx2-, Rx2+ signals all route directly from the DVI connector pins to the device, no external components are needed.

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10.2 Layout Example

- DVI connector trace matching

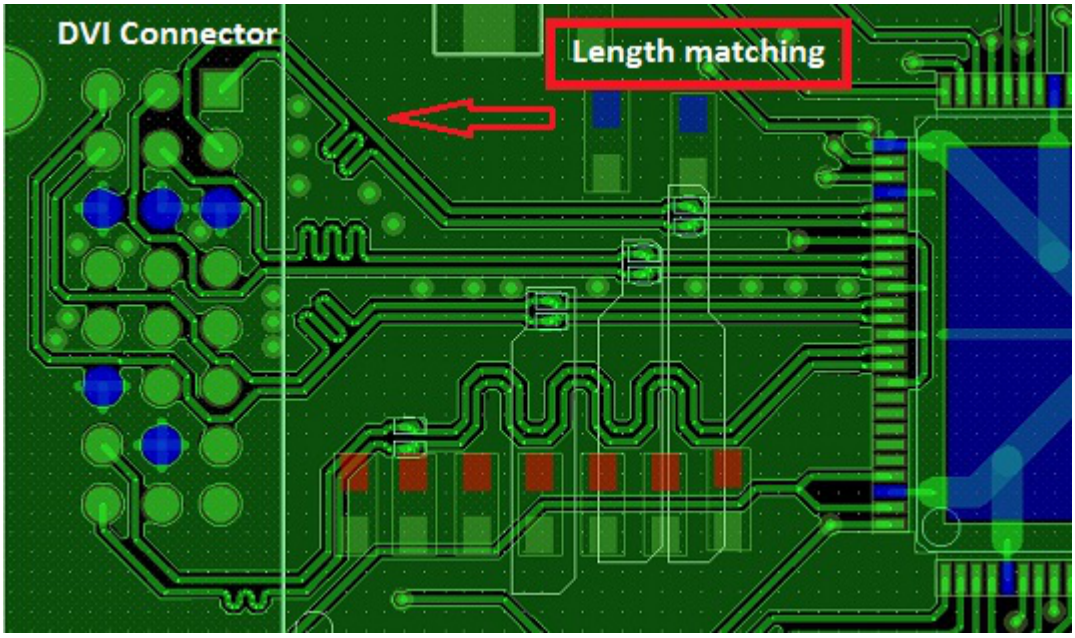


Figure 25. DVI Connector

- Keep data lines as far as possible from each other

Layout Example (continued)

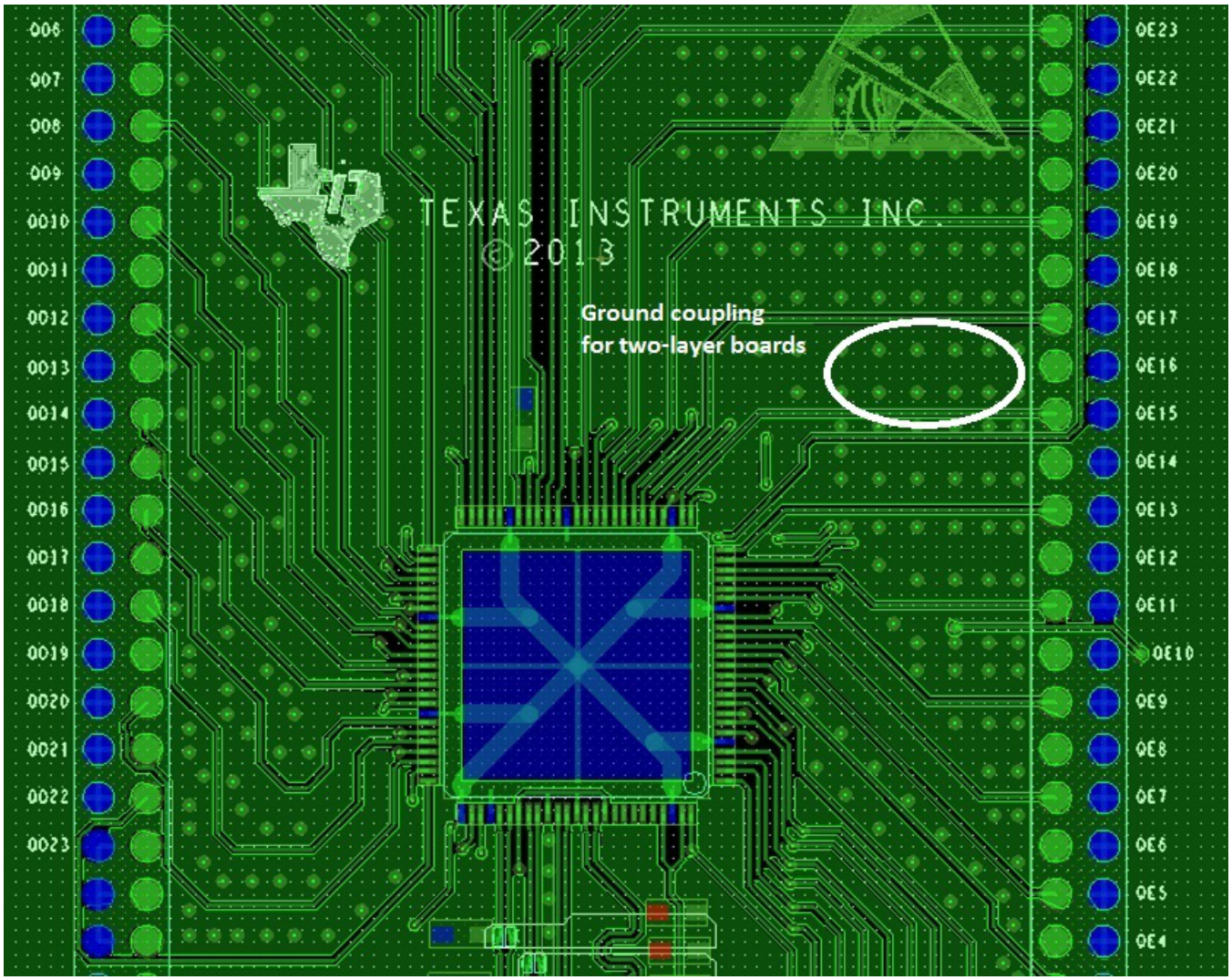


Figure 26. Data Route

- Connect the thermal pad to ground

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Layout Example (continued)

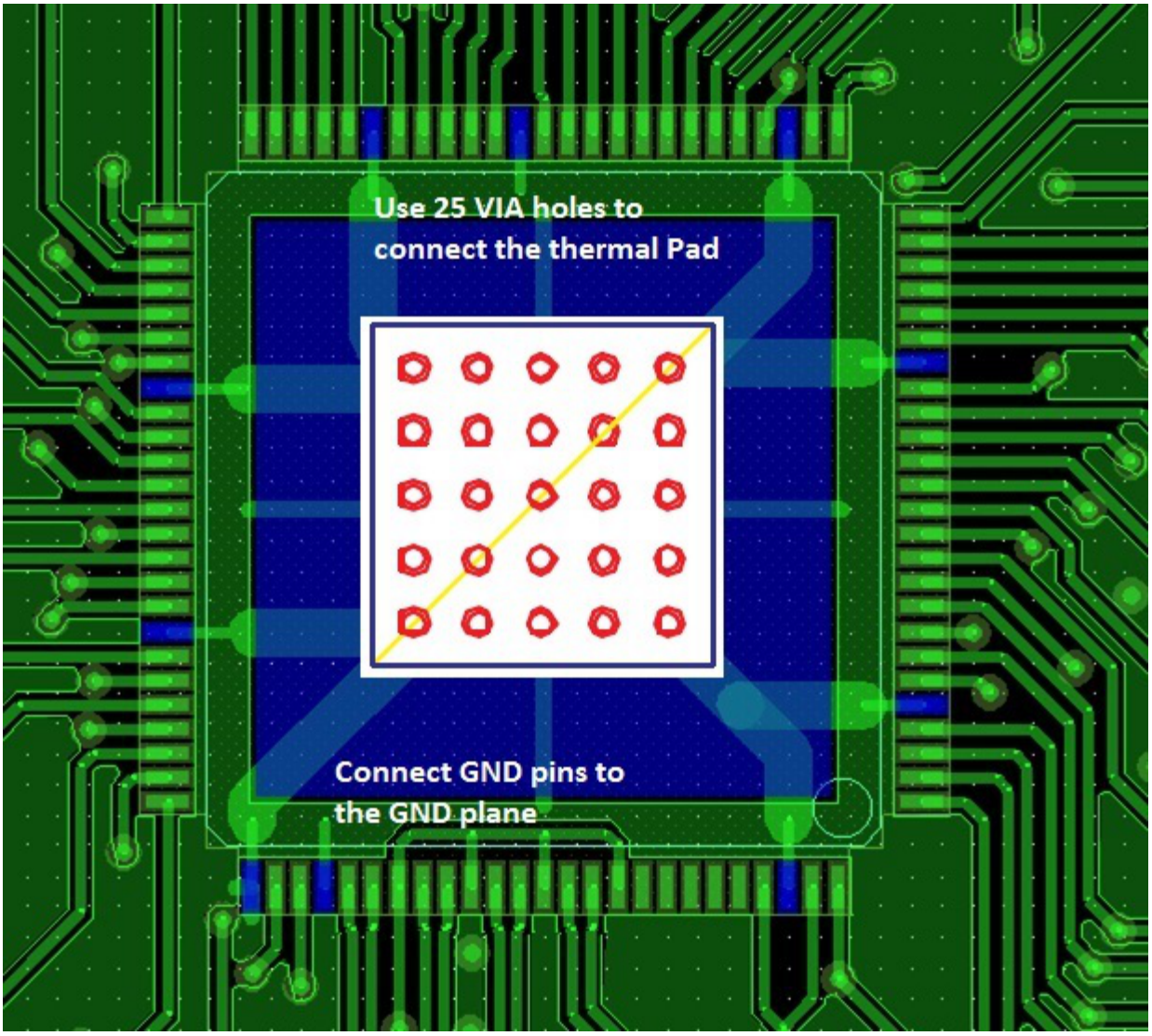


Figure 27. GND Route

10.3 TI PowerPAD 100-TQFP Package

The TFP401A-Q1 device comes in TI's thermally enhanced PowerPAD 100-TQFP package. The PowerPAD package is a 14-mm × 14-mm × 1-mm TQFP outline with 0.5-mm lead pitch. The PowerPAD package has a specially designed die mount pad that offers improved thermal capability over typical TQFP packages of the same outline. The TI 100-TQFP PowerPAD package offers a back-side solder plane that connects directly to the die mount pad for enhanced thermal conduction. There is no thermal requirement for soldering the back side of the TFP401A-Q1 device to the application board, because the device power dissipation is well within the package capability when not soldered.

Soldering the back side of the device to the PCB ground plane is recommended for electrical considerations. Connection of the PowerPAD back side to a PCB ground plane helps to improve EMI, ground bounce, and power-supply noise performance, because the die pad is electrically connected to the chip substrate and hence to chip ground.

Table 4 outlines the thermal properties of the TI 100-TQFP PowerPAD package. The 100-TQFP non-PowerPAD package is included only for reference.

Table 4. TI 100-TQFP (14 mm × 14 mm × 1 mm) With 0.5-mm Lead Pitch

PARAMETER	WITHOUT PowerPAD™ PACKAGE	PowerPAD™ PACKAGE, NOT CONNECTED TO PCB THERMAL PLANE	PowerPAD™ PACKAGE, CONNECTED TO PCB THERMAL PLANE(1)
Theta-JA(1) (2)	45°C/W	27.3°C/W	17.3°C/W
Theta-JC(1)(2)	3.11°C/W	0.12°C/W	0.12°C/W
Maximum power dissipation(1)(2)(3)	1.6 W	2.7 W	4.3 W

(1) Specified with 2-oz. (0.071 mm thick) Cu PCB plating
(2) Airflow is at 0 LFM (0 m/s) (no airflow).
(3) Measured at ambient temperature, T_A = 70°C

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11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, EPIC-5, Panelbus, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TFP401AIPZPRQ1	ACTIVE	HTQFP	PZP	100	1000	Green (RoHS & no Sb/Br)	NIPDAU	Level-3-260C-168 HR	-40 to 85	TFP401AI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TFP401A-Q1 :

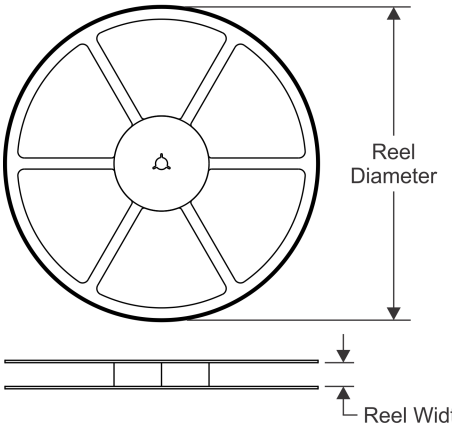
- Catalog: TFP401A
- Enhanced Product: TFP401A-EP

NOTE: Qualified Version Definitions:

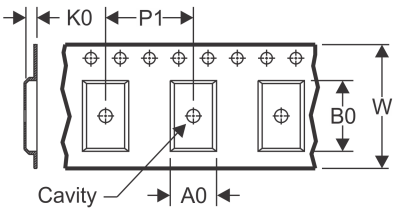
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

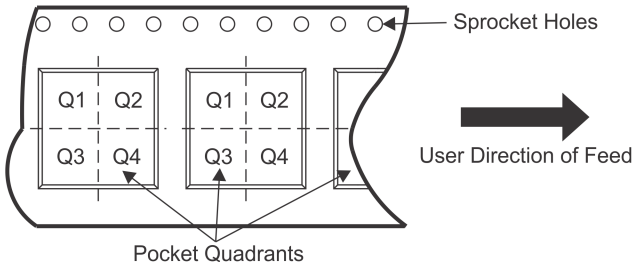


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

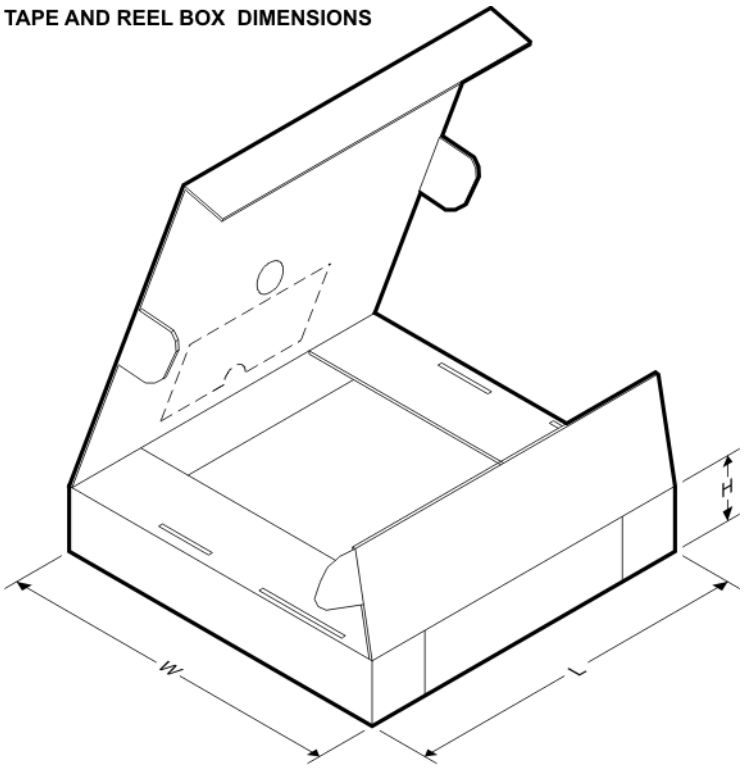
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TFP401AIPZPRQ1	HTQFP	PZP	100	1000	330.0	24.4	17.0	17.0	1.5	20.0	24.0	Q2

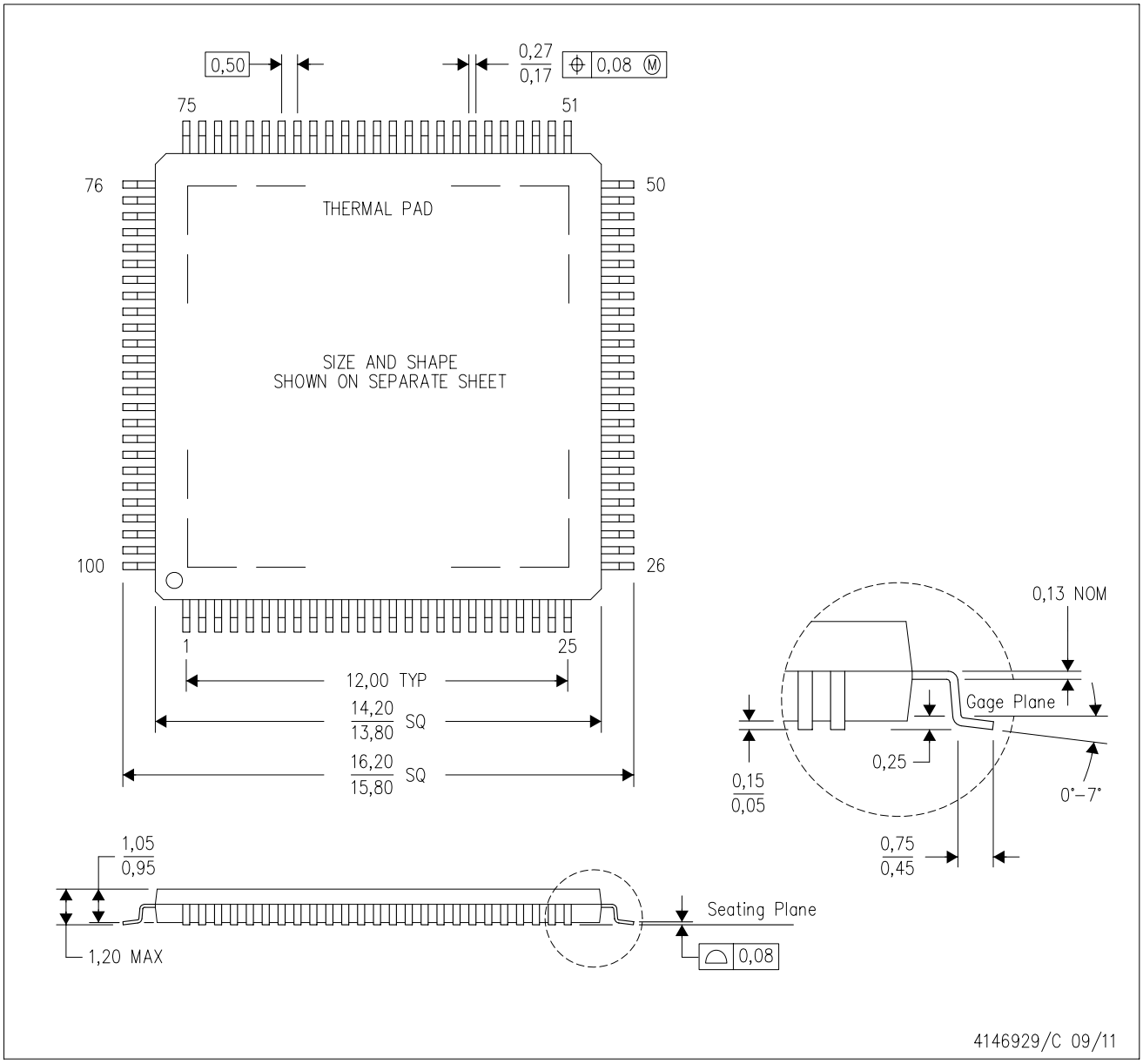
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TFP401AIPZPRQ1	HTQFP	PZP	100	1000	350.0	350.0	43.0

PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

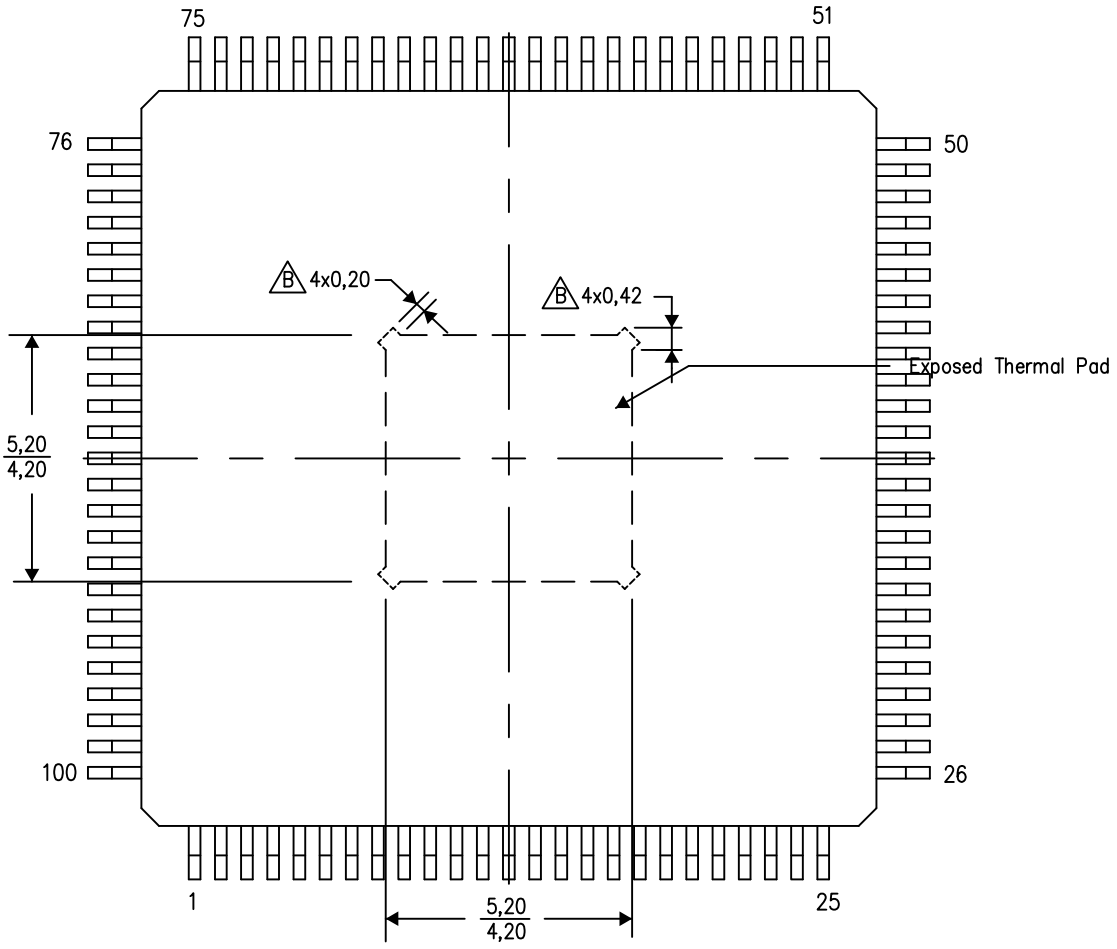
PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

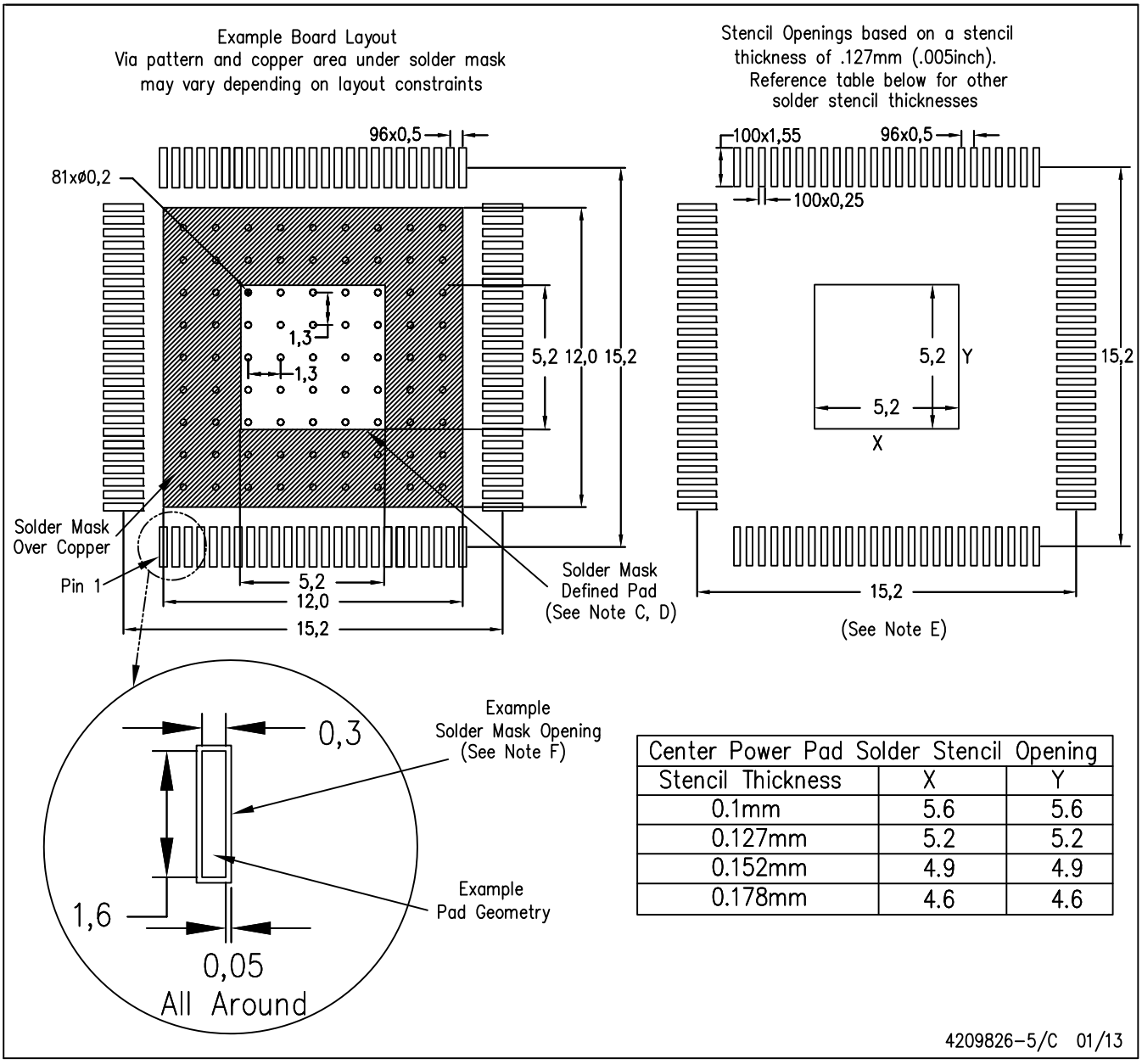
4206333–2/L 05/14

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PZP (S–PQFP–G100) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	5.6	5.6
0.127mm	5.2	5.2
0.152mm	4.9	4.9
0.178mm	4.6	4.6

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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