40A µModule Regulator with Overvoltage/ Overtemperature Protection

FEATURES

- **Overtemperature, Input/Output Overvoltage Protection**
- **Trips Upstream Power Source or Circuit Breaker**
- **Stacked Inductor Acts as Heat Sink**
- **Wide Input Voltage Range: 4.7V to 15V**
- **0.6V to 3.3V Output Voltage Range**
- **±1.3% Total DC Output Voltage Error (–40°C to 125°C)**
- **Differential Remote Sense Amplifier for Precision Regulation**
- **Current Mode Control/Fast Transient Response**
- **Frequency Synchronization**
- **Parallel Current Sharing (Up to 240A)**
- 88% Efficiency ($12V_{IN}$, $1V_{OUT}$) at 40A
- Overcurrent Foldback Protection
- Overtemperature Shutdown
- 16mm × 16mm × 7.07mm BGA Package

APPLICATIONS

- Telecom Servers and Networking Equipment
- Industrial Equipment and Medical Systems

DESCRIPTION

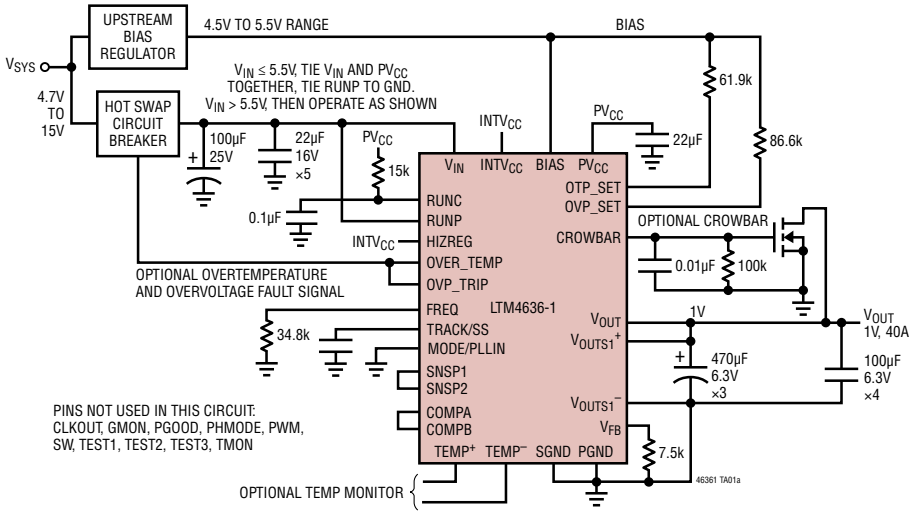
The LTM®4636-1 is a 40A step-down µModule® (power module) switching regulator with stacked inductor as a heat sink for heat dissipation and cooler operation in a small package. The LTM4636-1 detects overtemperature and input/output overvoltage conditions and can trip an upstream power supply or circuit breaker to protect itself and its load. The exposed inductor as a heat sink permits direct contact with airflow from any direction. The LTM4636-1 can deliver 40W ($12V_{IN}$, $1V_{OUT}$, 40A, 200LFM) with only 40°C rise over the ambient temperature. Full-power 40W is delivered up to 83°C ambient and half-power 20W is supported at 110°C ambient.

The LTM4636-1 operates at 92%, 90% and 88% efficiency delivering 15A, 30A and 40A, respectively, to a 1V load ($12V_{IN}$). The µModule regulator is scalable where four in current sharing deliver 160W with only 40°C rise and 88% efficiency ($12V_{IN}$, $1V_{OUT}$, 400LFM). The LTM4636-1 is offered in 16mm × 16mm × 7.07mm BGA package.

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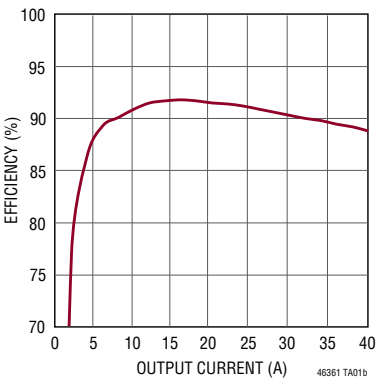
TYPICAL APPLICATION

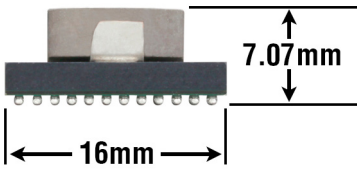
1V, 40A DC/DC µModule Regulator



See the LTM4636 for simpler circuit and fewer features.

$12V_{IN}$, $1V_{OUT}$ Efficiency at 350kHz vs Output Current



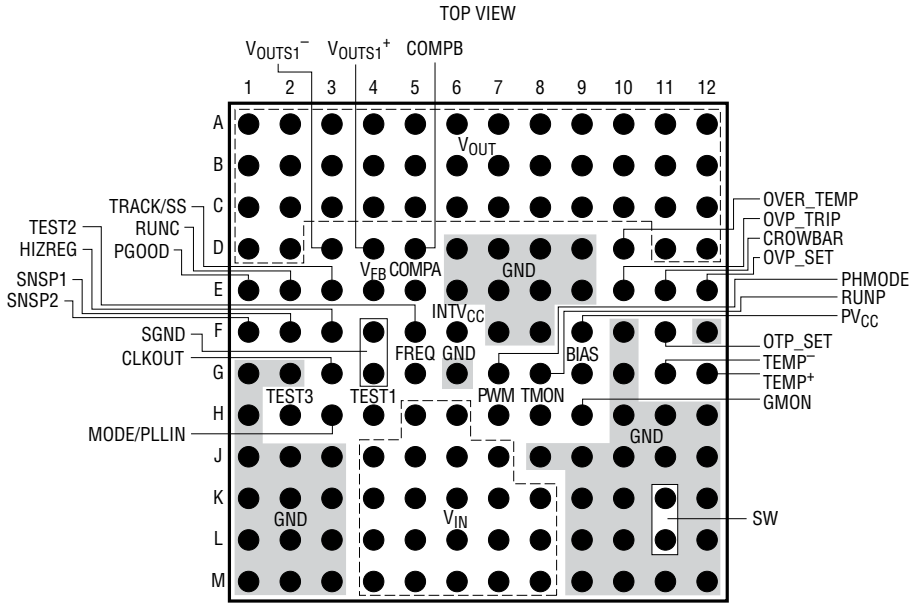


ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN}, SW, HZBREG, RUNP, OVR_TRIP, OVER TEMP ..... –0.3V to 16V
V_{OUT} ..... –0.3V to 3.5V
PGOOD, RUNC, TMON, PV_{CC}, MODE/PLLIN, PHMODE, FREQ, TRACK/SS, TEST1, TEST2, V_{OUTS1}^-, V_{OUTS1}^+, SNSP1, SNSP2, TEST3, OVP_SET, CROWBAR ..... –0.3V to $INTV_{CC}$ (5V)
V_{FB}, COMPA, COMPB (Note 6) ..... –0.3V to 2.7V
BIAS ..... –0.3V to 6V
PV_{CC} Additional Output Current ..... 0mA to 50mA
$TEMP^+$, $TEMP^-$ ..... –0.3V to 0.8V
$INTV_{CC}$ Peak Output Current (Note 6) 20mA
Internal Operating Temperature Range (Note 2) ..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Reflow (Peak Body) Temperature ..... 250°C

Note: PWM, CLKOUT, and GMON are outputs only.

PIN CONFIGURATION



BGA PACKAGE
144-LEAD (16mm × 16mm × 7.07mm)

T_{JMAX} = 125°C, θ_{JA} = 7.5°C/W, $\theta_{JCbottom}$ = 3°C/W, θ_{JCtop} = 15°C/W, θ_{JBA} = 12°C/W
θ_{JA} = DERIVED FROM 95mm × 76mm PCB WITH 6 LAYERS, WEIGHT = 3.95g
θ VALUES DETERMINED PER JESD51-12

Note: $\theta_{JA} = (\theta_{JCbottom} + \theta_{JBA}) || \theta_{JCtop}$; θ_{JBA} is Board to Ambient

ORDER INFORMATION

http://www.linear.com/product/LTM4636-1#orderinfo

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM4636-1EY#PBF	LTM4636-1EY#PBF	LTM4636-1	144-Lead (16mm × 16mm × 7.07mm) BGA	–40°C to 125°C
LTM4636-1IY#PBF	LTM4636-1IY#PBF	LTM4636-1	144-Lead (16mm × 16mm × 7.07mm) BGA	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = 12V, per the Typical Application in Figure 20.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage	$V_{IN} \le 5.5V$, Tie V_{IN} and PV_{CC} Together, Tie RUNP to GND	●	4.70		15	V
V_{OUT}	V_{OUT} Range		●	0.6		3.3	V
$V_{OUT(DC)}$	DC Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF × 5 C_{OUT} = 100µF × 4 Ceramic, 470µF POSCAP × 3 R_{FB} = 40.2k, MODE_PLLIN = GND V_{IN} = 4.70V to 15V, I_{OUT} = 0A to 40A (Note 4)	●	1.4805	1.50	1.5195	V
Input Specifications							
V_{RUNC}	RUNC Pin On Threshold	V_{RUNC} Rising		1.1	1.22	1.35	V
$V_{RUNCHYS}$	RUNC Pin On Hysteresis				150		mV
V_{RUNP}	RUNP Pin On Threshold	RUNP Pin Rising	●	0.7	0.8	0.9	V
RUNP HYS	RUNP Pin Hysteresis				60		mV
HIZREG	HIZREG Input Threshold	V_{IN} = 12V, RUNC = 5V, RUNP = V_{IN}, V_{OUT} = 1.5V			2.3		V
HIZREG HYS	HIZREG Hysteresis	V_{IN} = 12V, RUNC = 5V, RUNP = V_{IN}, V_{OUT} = 1.5V			0.8		V
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.5V, Burst Mode Operation, I_{OUT} = 0.1A V_{IN} = 12V, V_{OUT} = 1.5V, Pulse-Skipping Mode, I_{OUT} = 0.1A V_{IN} = 12V, V_{OUT} = 1.5V, Switching Continuous, I_{OUT} = 0.1A Shutdown, RUN = 0, V_{IN} = 12V			16 23 105 30		mA mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 40A V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 40A			14.7 5.66		A A
Output Specifications							
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V (Note 4)		0		40	A
$\frac{\Delta V_{OUT}\ (Line)}{V_{OUT}}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} from 4.70V to 15V I_{OUT} = 0A	●		0.02	0.06	%/V
$\frac{\Delta V_{OUT}\ (Load)}{V_{OUT}}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 40A, V_{IN} = 12V (Note 4)	●		0.2	0.35	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF × 3 Ceramic, 470µF × 3 POSCAP, V_{IN} = 12V, V_{OUT} = 1.5V			15		mV_{P-P}
$\Delta V_{OUT(START)}$	Turn-On Overshoot	C_{OUT} = 100µF × 4 Ceramic, 470µF × 3 POSCAP, V_{OUT} = 1.5V, I_{OUT} = 0A, V_{IN} = 12V, TRACK/SS = 0.1µF			5		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF × 3 Ceramic, 470µF × 3 POSCAP, No Load, TRACK/SS = 0.001µF, V_{IN} = 12V			750		µs
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load C_{OUT} = 100µF × 4 Ceramic, 470µF × 3 POSCAP, V_{IN} = 12V, V_{OUT} = 1.5V, CFF = 22pF			45		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, V_{IN} = 5V, C_{OUT} = 100µF × 4 Ceramic, 470µF × 3 POSCAP, V_{IN} = 12V, V_{OUT} = 1.5V, CFF = 22pF			25		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.5V V_{IN} = 5V, V_{OUT} = 1.5V			54 54		A A
Control Section							
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.594	0.600	0.606	V
I_{FB}	Current at V_{FB} Pin	(Note 6)			–30	–100	nA
V_{OVL}	Feedback Overvoltage Lockout	Measure at V_{OUTS1}	●	5	7.5	10	%
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V, Default 750µs Turn on with TRACK/SS Tied to $INTV_{CC}$		1.1	1.35	1.6	µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 3)			100		ns
R_{FBHI}	Resistor Between V_{OUTS1} and V_{FB} Pins				4.99		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = 12V, per the typical application in Figure 20.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Remote Sense Amplifier							
$A_{V(VFB)}$	V_{FB} Differential Gain	(Note 6)			1		V/V
GBP V_{FB} Path	Gain Bandwidth Product	(Note 5)			4		MHz
General Control or Monitor Pins							
OVP Δt	OVP to OVP_TRIP	OVP Response Time			500		ns
Crowbar Δt	OVP to CROWBAR	OVP Response Time to CROWBAR			500		ns
OVP Delay	OVP to OVER_TEMP	OVP_TEMP to OVP_TEMP Response Time			8		µs
OVP_Trip Sink	OVP_TRIP Sink Current	$V_{CE} \le 0.4V$				15	mA
OTP_Trip Sink	OVER_TEMP Sink Current	$V_{CE} \le 0.4V$				15	mA
Crowbar Source	CROWBAR Source Current	$V_{CROWBAR} \ge 3.0V$			15		mA
OTP_SET	Overtemperature Set Register				24.9		kΩ
OVP_SET	Overvoltage Set Register				24.9		kΩ
I_{TMON}		Temperature Monitor Current, T_J = 25°C Into 24.9kΩ Temperature Monitor Current, T_J = 150°C Into 24.9kΩ		38	40.3 58	44	µA µA
$I_{TMON(SLOPE)}$		Temperature Monitor Current Slope, R_{TMON} = 24.9kΩ			0.144		µA/°C
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive			 –7.5 7.5		 % %
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.2	0.4	V
t_{PGOOD}	V_{PGOOD} High-to-Low Delay				65		µs
$I_{PGOOD(OFF)}$	PGOOD Leakage Current	V_{PGOOD} = 5V		–2		2	µA
$V_{PG1(HYST)}$	PGOOD Trip Level Hysteresis				2.5		%
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage Source	6V < V_{IN} < 15V		5.3	5.5	5.7	V
V_{INTVCC} Load Reg	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 10mA			0.5		%
UVLO HYS	Controller UVLO Hysteresis	(Note 6)			0.5		V
$PV_{CC(UVLO)}$	Drivers and Power MOSFETs UVLO	PV_{CC} Rising		3.5	3.8	4.1	V
$PV_{CC(HYS)}$	PV_{CC} UVLO Hysteresis				0.45		V
PV_{CC}	Power Stage Bias	12V Input, PV_{CC} Load = 50mA			5.0		V
BIAS	External Bias for OTP and OVP Function	Range Operating		4	5.0	5.5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2), otherwise specifications are at T_A = 25°C. V_{IN} = 12V, per the typical application in Figure 20.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop							
f_{OSC}	Oscillator Frequency V_{PHSMD} = 0V	R_{FREQ} = 30.1kΩ R_{FREQ} = 47.5kΩ R_{FREQ} = 54.9kΩ R_{FREQ} = 75.0kΩ Maximum Frequency Minimum Frequency	 ● ●	210 540 625 945 1.2	250 600 750 1.05	290 660 825 1.155 0.2	kHz kHz kHz MHz MHz MHz
I_{FREQ}	FREQ Pin Output Current	V_{FREQ} = 0.8V		19	20	21	µA
$R_{MODE/PLLIN}$	MODE_PLLIN Input Resistance				250		kΩ
$V_{MODE/PLLIN}$	PLLIN Input Threshold	$V_{MODE/PLLIN}$ Rising $V_{MODE/PLLIN}$ Falling			2 1.2		V V
V_{CLKOUT}	Low Output Voltage High Output Voltage	Verified Levels Measurements on CLKOUT			0.2 5.2		V V
PWM-CLKOUT	PWM to Clockout Phase Delay	V_{PHMODE} = 0V V_{PHMODE} = 1/4 $INTV_{CC}$ V_{PHMODE} = Float V_{PHMODE} = 3/4 $INTV_{CC}$ V_{PHMODE} = $INTV_{CC}$			90 90 120 60 180		Deg Deg Deg Deg Deg
PWM/PWMEN Outputs							
PWM	PWM Output High Voltage	I_{LOAD} = 500µA		5.0			V
	PWM Output Low Voltage	I_{LOAD} = –500µA				0.5	V
Temperature Diode							
Diode V_F	Diode Forward Voltage	I = 100µA, $TEMP^+$ to $TEMP^-$			0.598		V
TC	Temperature Coefficient		●		–2.0		mV/°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4636-1 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4636-1E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the full –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4636-1I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The minimum on-time condition is specified for a peak-to-peak inductor ripple current of ~40% of I_{MAX} Load. (See the Applications Information section)

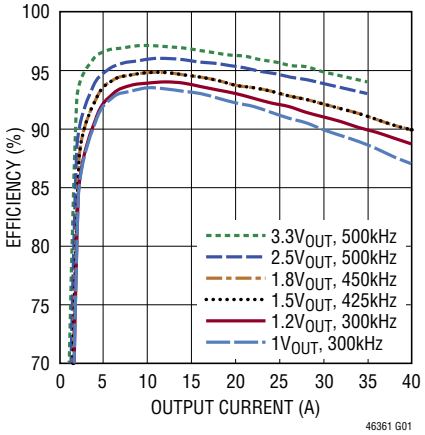
Note 4: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

Note 5: Guaranteed by design.

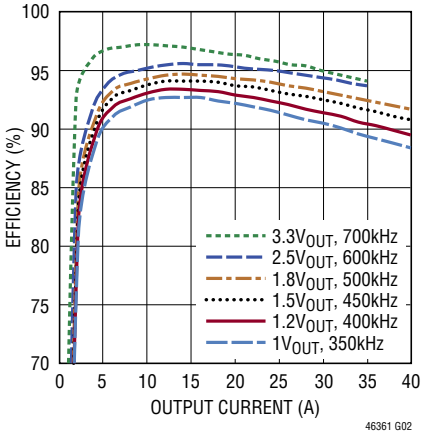
Note 6: 100% tested at wafer level.

TYPICAL PERFORMANCE CHARACTERISTICS

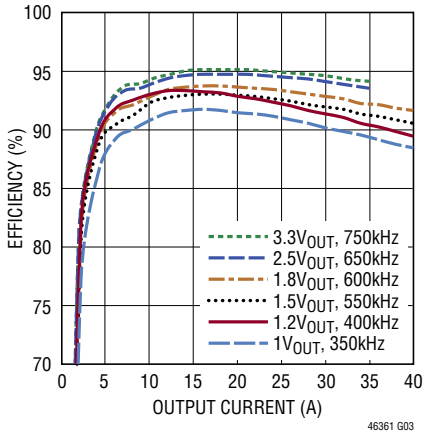
Efficiency vs Load Current with $5V_{IN}$



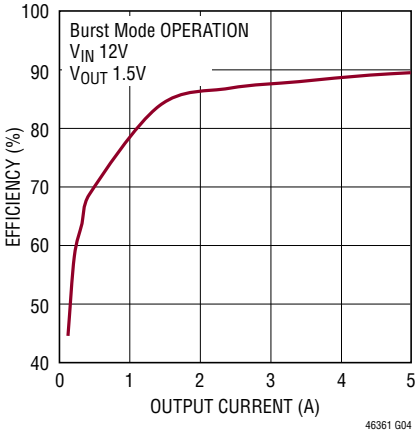
Efficiency vs Load Current with $8V_{IN}$



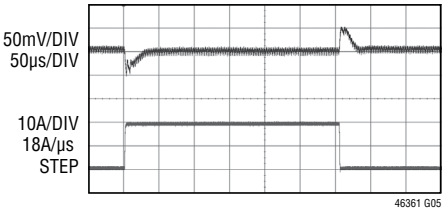
Efficiency vs Load Current with $12V_{IN}$



Burst Mode Efficiency vs Load Current

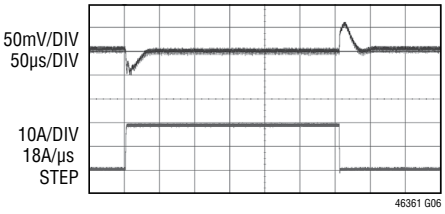


1V Transient Response



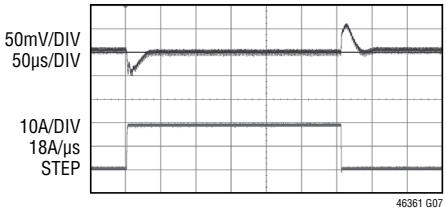
12V TO 1V TRANSIENT RESPONSE
C_{OUT} = 4 × 100µF CERAMIC, 3 × 470µF 2.5V POSCAP 5mΩ
C_{FF} = 22pF, SW FREQ = 400kHz

1.2V Transient Response



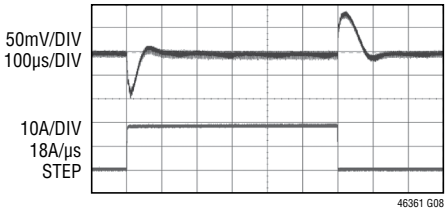
12V TO 1.2V TRANSIENT RESPONSE
C_{OUT} = 4 × 100µF CERAMIC, 3 × 470µF 2.5V POSCAP 5mΩ
C_{FF} = 22pF, SW FREQ = 400kHz
C_{COMP} = 100pF

1.5V Transient Response



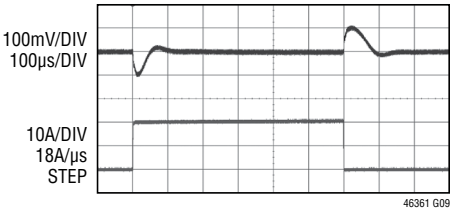
12V TO 1.5V TRANSIENT RESPONSE
C_{OUT} = 4 × 100µF CERAMIC, 3 × 470µF 2.5V POSCAP 5mΩ
C_{FF} = 22pF, SW FREQ = 425kHz
C_{COMP} = 100pF

1.8V Transient Response



12V TO 1.8V TRANSIENT RESPONSE
C_{OUT} = 6 × 100µF CERAMIC, 2 × 470µF 4V POSCAP 5mΩ
C_{FF} = 22pF, SW FREQ = 500kHz
C_{COMP} = 100pF

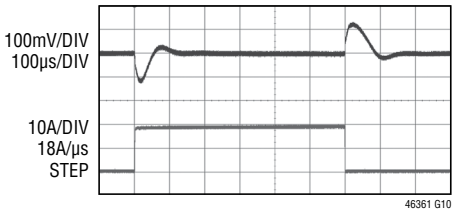
2.5V Transient Response



12V TO 2.5V TRANSIENT RESPONSE
C_{OUT} = 6 × 100µF CERAMIC, 2 × 470µF 4V POSCAP 5mΩ
C_{FF} = 22pF, SW FREQ = 650kHz
C_{COMP} = 100pF

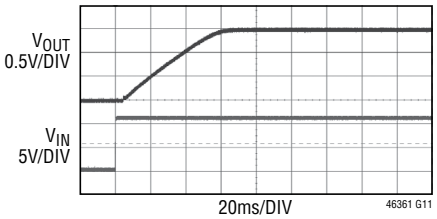
TYPICAL PERFORMANCE CHARACTERISTICS

3.3V Transient Response



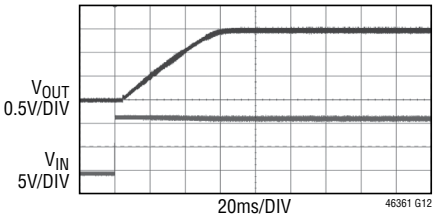
12V TO 3.3V TRANSIENT RESPONSE
C_{OUT} = 6 × 100µF CERAMIC, 2 × 470µF 4V POSCAP 5mΩ
C_{FF} = 22pF, SW FREQ = 750kHz
C_{COMP} = 100pF

Start-Up with Soft-Start No-Load



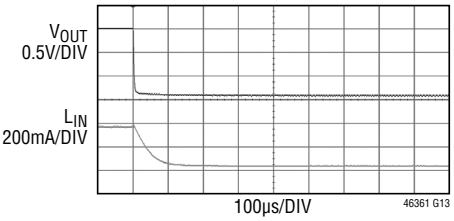
RUN PIN CAPACITOR = 0.1µF
TRACK/SS CAPACITOR = 0.1µF
C_{OUT} = 4 × 100µF CERAMIC AND 3 × 470µF POSCAP

Start-Up with Soft-Start Full Load

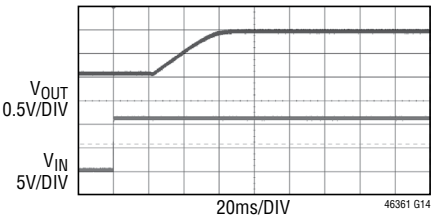


RUN PIN CAPACITOR = 0.1µF
TRACK/SS CAPACITOR = 0.1µF
C_{OUT} = 4 × 100µF CERAMIC AND 3 × 470µF POSCAP

40A Load Short-Circuit

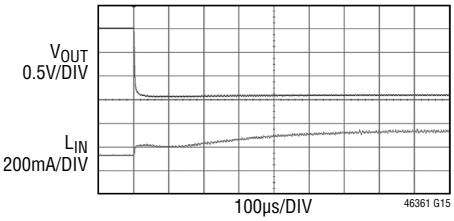


Start-Up with 0.5V Output Pre-Bias



RUN PIN CAPACITOR = 0.1µF
TRACK/SS CAPACITOR = 0.1µF
C_{OUT} = 4 × 100µF CERAMIC AND 3 × 470µF

No-Load Short-Circuit



PIN FUNCTIONS

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{OUT} (A1-A12, B1-B12, C1-C12, D1-D2, D11-D12): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance between these pins and GND pins. Review Table 4.

MODE_PLLIN (H3): Forced Continuous Mode, Burst Mode Operation, or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to $INTV_{CC}$ to enable pulse-skipping mode of operation. Connect to ground to enable forced continuous mode of operation. Floating this pin will enable Burst Mode operation. A clock on this pin will enable synchronization with forced continuous operation. See the Applications Information section.

V_{OUTS1}^- (D3): V_{OUT} Sense Ground for the Remote Sense Amplifier. This pin connects to the ground remote sense point. Connect to ground when not used. See the Applications Information section.

V_{OUTS1}^+ (D4): This pin should connect to V_{OUT} and is connected to V_{FB} through a 4.99k resistor. This pin is used to connect to a remote sense point of the load for accurate voltage sensing. Either connect to remote sense point or directly to V_{OUT}. See the Applications Information section for details.

COMPB (D5): Internal compensation network provided that coincides with proper stability utilizing the values in Table 5. Just connect this pin to COMPA for internal compensation. In parallel operation with other LTM4636-1 devices, connect COMPA and COMPB pins together for internal compensation, then connect all COMPA pins together.

GND (D6-D9, E6-E9, F7, F8, F10, F12, G1-G2, G6 G10, H1, H10-H12, J1-J3, J8-J12, K1-K3, K9-K10, K12, L1-L3, L9-L10, L12, M1-M3, M9-M12): Ground Pins for Both Input and Output Returns.

PGOOD (E1): Output Voltage Power Good Indicator. Open-drain logic output is pulled to ground when the output voltage exceeds a ±7.5% regulation window.

RUNC (E2): Run Control Pin. A voltage above 1.35V will turn on the control section of the module. A 10k resistor to ground is internal to the module for setting the RUN pin threshold with a resistor to 5V, and allowing a pull-up resistor to PV_{CC} for enabling the device. See Figure 1 Block Diagram.

TRACK/SS (E3): Output Voltage Tracking Pin and Soft-Start Inputs. The pin has a 1.25µA pull-up current source. A capacitor from this pin to ground will set a soft-start ramp rate. In tracking, the regulator output can be tracked to a different voltage. The different voltage is applied to a voltage divider then to the slave output's track pin. This voltage divider is equal to the slave output's feedback divider for coincidental tracking. Default soft-start of 750µs with TRACK/SS pin connected to $INTV_{CC}$ pin. See the Applications Information section. In PolyPhase® applications tie the TRACK/SS pins together.

V_{FB} (E4): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUTS1} with a 4.99k precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and V_{OSNS}^-. In PolyPhase operation, tying the V_{FB} pins together allows for parallel operation. See the Applications Information section.

COMPA (E5): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Tie all COMPA pins together for parallel operation. This pin allows external compensation. See the Applications Information section.

OVP_TRIP (E10): This open-drain pin can be used to trip off and retry an input circuit breaker or alert the system to an output overvoltage programmed on the OVP_SET pin. See the Applications Information section.

CROWBAR (E11): This pin can be optionally used to clamp the output voltage in an overvoltage condition to protect the load to tighter control of overvoltage. See the Applications Information section.

SNSP2 (F1): Current Sense Signal Path. Connect this pin to SNSP1 (F2).

SNSP1 (F2): Current Sense Signal Path. Connect this pin to SNSP2 (F1). Both pins are used to calibrate current sense matching and current limit at final test.

PIN FUNCTIONS

HIZREG (F3): When this pin is pulled low the power stage is disabled into high impedance. Tie this pin to V_{IN} or $INTV_{CC}$ for normal operation.

OVER_TEMP (D10): This overtemperature protection is programmable with an internal monitor that is referenced to the TMON pin and the OTP_SET pin. The OVER_TEMP pin can be used to alert the system if the module regulator overheats, and this signal can be used to trip off and retry an electronic circuit breaker in a fault condition. The pin is an open collector that pulls active low in response to OVER_TEMP. The OVER_TEMP pin can be left floating if not used. See the Applications Information section for details.

SGND (F4, G4): Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to the output capacitor GND in the application. See layout guidelines in Figure 18.

$INTV_{CC}$ (F6): Internal 5.5V LDO for Driving the Control Circuitry in the LTM4636-1. $INTV_{CC}$ is controlled and enabled when RUNC is activated high.

FREQ (G5): A resistor can be applied from this pin to ground to set the operating frequency. This pin sources 20µA. See the Applications Information section.

PHMODE (G7): This pin can be voltage programmed to change the phase relationship of the CLKOUT pin with reference to the internal clock or an input synchronized clock. The $INTV_{CC}$ (5.5V) output can be voltage divided down to the PHASMD pin to set the particular phase. The Electrical Characteristics show the different settings to select a particular phase. See the Applications Information section.

RUNP (G8): This pin enables the PV_{CC} supply. This pin can be connected to V_{IN}, or tie to ground when connecting PV_{CC} to $V_{IN} \leq 5.5V$. RUNP needs to sequence up before RUNC. A 15k resistor from PV_{CC} to RUNC with a 0.1µF capacitor will provide enough delay. In parallel operation with multiple LTM4636-1s, the resistor can be reduced in value by N times and the 0.1µF can be increased N times. See Applications Information section. RUNP can be used to set the minimum UVLO with a voltage divider. See Figure 1.

PV_{CC} (F9): 5V Power Output and Power for Internal Power MOSFET Drivers. The regulator can power 50mA of external sourcing for additional use. Place a 22µF ceramic filter capacitor on this pin to ground. When $V_{IN} < 5.5V$, tie V_{IN} and PV_{CC} together. Then tie RUNP to GND. If $V_{IN} > 5.5V$ then operate PV_{CC} regulator as normal. See the Typical Application examples.

OVP_SET (E12): This pin is used to set the output overvoltage trip point. This pin has a 24.9kΩ resistor on it to ground. See the Applications Information section. Float is not used.

BIAS (G9): This pin is used to power the OTP and OVP circuitry independently of the main power feed. See the Applications Information section.

$TEMP^+$ (G12): Temperature Monitor. An internal diode connected NPN transistor. See the Applications Information section.

OTP_SET (F11): This pin is used to set the overtemperature set point. The pin has a 24.9k resistor on it to ground. See Applications Information section. Float if not used.

$TEMP^-$ (G11): Low Side of the Internal Temperature Monitor.

CLKOUT (G3): Clock out signal that can be phase selected to the main internal clock or synchronized clock using the PHASMD pin. CLKOUT can be used for multiphase applications. See the Applications Information section.

TEST1 (H4), TEST2 (F5), TEST3 (H2), GMON (H9): These are test pins used in the final production test of the part. Leave floating.

V_{IN} (H5-H6, J4-J7, K4-K8, L4-L8, M4-M8): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} and GND pins.

PWM (H7): PWM output that drives the power stage. Primarily used for test, but can be monitored in debug or testing.

TMON (H8): Temperature Monitor Pin. Internal temperature monitor, varies from 1.0V at 25°C to 1.44V at 150°C, disables power stage at >150°C. The OTP_Trip signal is set to trip off at a value lower than 150°C. If the temperature monitor feature is not desired, then tie the TMON pin to GND.

SW (L11, K11): These are pin connections to the internal switch node for test evaluation and monitoring. An R-C snubber can be placed from the switch pins to GND to eliminate any high frequency ringing. See the Applications Information section.

BLOCK DIAGRAM

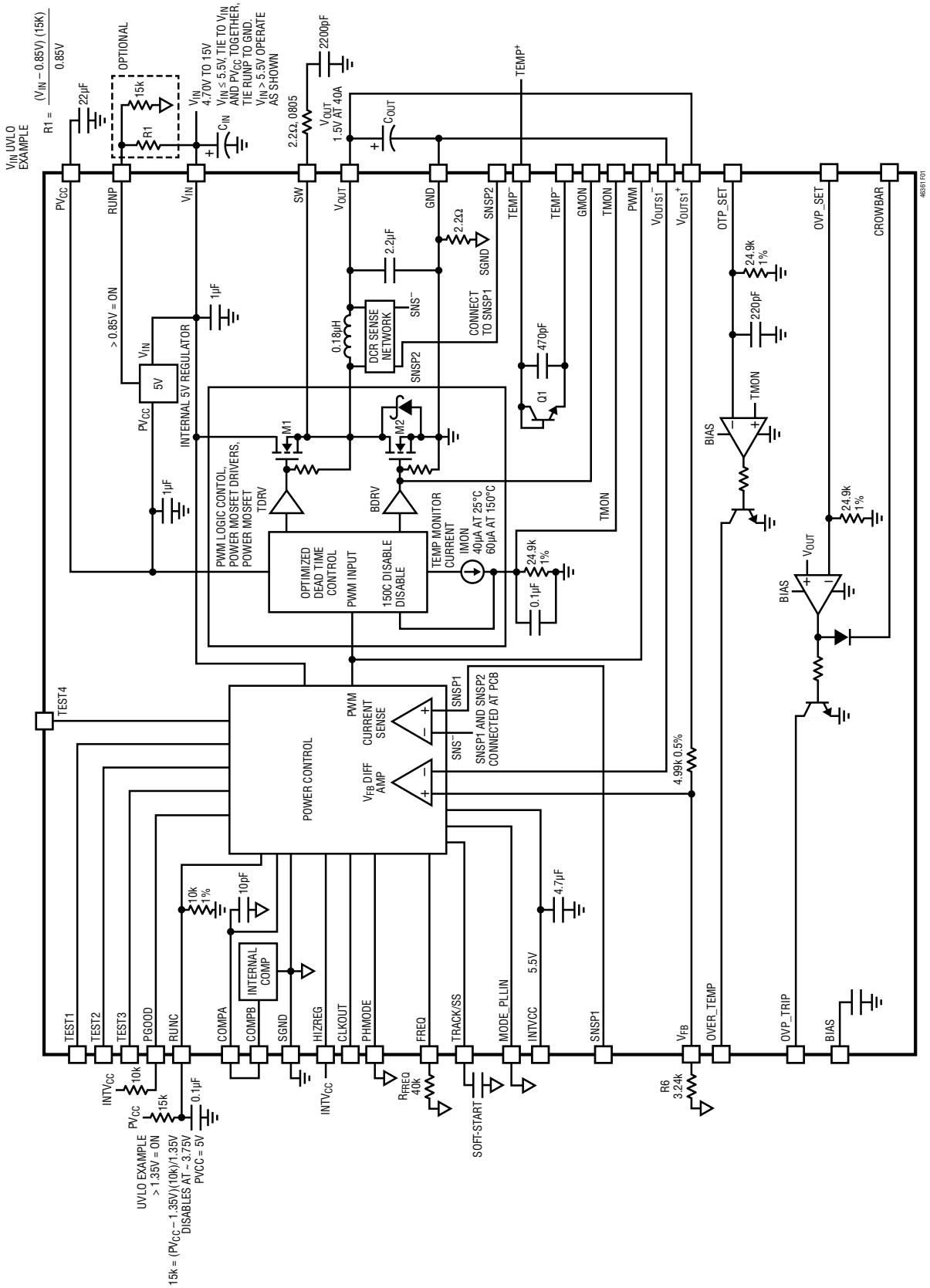


Figure 1. Simplified LTM4636-1 Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4.70V to 16V, V_{OUT} = 1.5V)	I_{OUT} = 40A, 6 × 22µF Ceramic X7R Capacitors (See Table 4)	100			µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 4.70V to 16V, V_{OUT} = 1.5V)	I_{OUT} = 40A (See Table 4)		1000		µF

OPERATION

Power Module Description

The LTM4636-1 is a high efficiency regulator that can provide a 40A output with few external input and output capacitors. This module provides precisely regulated output voltages programmable via external resistors from 0.6V DC to 3.3V DC over a 4.70V to 15V input range. The Typical Application schematic with protection is shown in Figure 20.

The LTM4636-1 has an integrated constant-frequency current mode regulator, power MOSFETs, 0.18µH inductor, protection circuitry, 5V regulator and other supporting discrete components. The switching frequency range is from 250kHz to 770kHz, and the typical operating frequency is 400kHz. For switching noise-sensitive applications, it can be externally synchronized from 250kHz to 800kHz, subject to minimum on-time limitations and limiting the inductor ripple current to less than 40% of maximum output current.

A single resistor is used to program the frequency. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4636-1 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors. An option has been provided for external loop compensation. LTpowerCAD™ can be used to optimize the external compensation option. See the Applications Information section.

Current mode control provides cycle-by-cycle fast current limit in an overcurrent condition. An internal overvoltage monitor feedback pin referred will attempt to protect the output voltage in the event of an overvoltage >10%. The top MOSFET is turned off and the bottom MOSFET is turned on until the output is cleared.

Pulling the RUNC pin below 1.1V forces the regulator controller into a shutdown state. The TRACK/SS pin is used for programming the output voltage ramp and voltage tracking during start-up. See the Applications Information section.

Optional internal overvoltage protection and overtemperature functions can be used to protect from power MOSFET failures, input and output overvoltage and overtemperature conditions. These two features can be used to trip off and retry an input circuit breaker in the event of either/or both an overvoltage and overtemperature fault. The OVP_TRIP, OVER_TEMP, TMON, OVP_SET, CROWBAR and OTP_SET pins are all used to support these two features. These features can be implemented along with an input circuit breaker to protect expensive systems boards, processors and FPGA devices from damage. See the Applications Information section.

The LTM4636-1 is internally compensated to be stable over all operating conditions. Table 5 provides a guideline for input and output capacitances for several operating conditions. LTpowerCAD is available for transient and stability analysis. This tool can be used to optimize the regulators loop response.

A remote sense amplifier is provided for accurately sensing output voltages at the load point.

Multiphase operation can be easily employed with the internal clock source or a synchronization clock applied to the MODE/PLLIN input using an external clock source, and connecting the CLKOUT pins. See the Applications Information section. Review Figure 4.

High efficiency at light loads can be accomplished with selectable Burst Mode operation using the MODE_PLLIN pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section.

OPERATION

A TEMP+ and TEMP– pins are provided to allow the internal device temperature to be monitored using an onboard diode connected NPN transistor.

High efficiency at light loads can be accomplished with selectable Burst Mode operation using the MODE_PLLIN pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section.

APPLICATIONS INFORMATION

The typical LTM4636-1 application circuit is shown in Figure 20. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 5 for specific external capacitor requirements for particular applications.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the V_{IN} to V_{OUT} step-down ratio that can be achieved for a given input voltage. The maximum duty cycle is 94% typical at 500kHz operation. The V_{IN} to V_{OUT} minimum dropout is a function of load current and operation at very low input voltage and high duty cycle applications. At very low duty cycles the minimum 100ns on-time must be maintained. See the PLL, Frequency Adjustment and Synchronization section and temperature derating curves.

Output Voltage Programming

The PWM controller has an internal 0.6V ±1% reference voltage. As shown in the Block Diagram, a 4.99k internal feedback resistor connects the V_{OUTS1} and V_{FB} pins together. When the remote sensing is used, then V_{OUTS1}^+ and V_{OUTS1}^- are connected to the remote V_{OUT} and GND points. If no remote sense the V_{OUTS1}^+ connects to V_{OUT}. The output voltage will default to 0.6V with no feedback resistor. Adding a resistor R_{FB} from V_{FB} to ground programs the output voltage:

$$V_{OUT} = 0.6V \bullet \frac{4.99k + R_{FB}}{R_{FB}}$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT} (V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3
R_{FB} (k)	Open	7.5	4.99	3.24	2.49	1.58	1.1

For parallel operation of N LTM4636-1s, the following equation can be used to solve for R_{FB}:

$$R_{FB} = \frac{4.99k / N}{\frac{V_{OUT}}{0.6V} - 1}$$

Or use V_{OUTS1} on one channel and connect all feedback pins together utilizing a single feedback resistor.

Tie the V_{FB} pins together for each parallel output. The COMP pins must be tied together also. See the Typical Applications section examples.

Input Capacitors

The LTM4636-1 module should be connected to a low AC-impedance DC source. Additional input capacitors are needed for the RMS input ripple current rating. The $I_{CIN(RMS)}$ equation which follows can be used to calculate the input capacitor requirement. Typically 22µF X7R ceramics are a good choice with RMS ripple current ratings of ~4A each. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

APPLICATIONS INFORMATION

Without considering the inductor ripple current, for each output the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

where $\eta\%$ is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated aluminum electrolytic capacitor or a Polymer capacitor.

Output Capacitors

The LTM4636-1 is designed for low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, low ESR Polymer capacitor or ceramic capacitors. The typical output capacitance range is from 400µF to 1000µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 5 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 15A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 5 matrix, and LTpowerCAD is available for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. LTpowerCAD can be used to calculate the output ripple reduction as the number of implemented phases increases by N times. External loop compensation can be used for transient response optimization.

Burst Mode Operation

The LTM4636-1 is capable of Burst Mode operation in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. To enable Burst Mode operation, simply float the MODE_PLLIN pin. During Burst Mode operation, the peak current of the inductor is set to approximately 30% of the maximum peak current value in normal operation even though the voltage at the COMPA pin indicates a lower value. The voltage at the COMPA pin drops when the inductor's average current is greater than the load requirement. As the COMPA voltage drops below 0.5V, the burst comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current. The load current is now being supplied from the output capacitors. When the output voltage drops, causing COMPA to rise, the internal sleep line goes low, and the LTM4636-1 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4636-1 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE_PLLIN pin to $INTV_{CC}$ enables pulse-skipping operation. With pulse-skipping mode at light load, the internal current comparator may remain tripped for several cycles, thus skipping operation cycles. This mode has lower ripple than Burst Mode operation and maintains a higher frequency operation than Burst Mode operation.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE_PLLIN pin to ground. In this mode, inductor current is allowed to reverse during low output loads, the COMPA voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4636-1's output voltage is in regulation.

APPLICATIONS INFORMATION

Multiphase Operation

For outputs that demand more than 40A of load current, multiple LTM4636-1 devices can be paralleled to provide more output current without increasing input and output ripple voltage. The MODE_PLLIN pin allows the LTM4636-1 to be synchronized to an external clock and the internal phase-locked loop allows the LTM4636-1 to lock onto input clock phase as well. The FREQ resistor is selected for normal frequency, then the incoming clock can synchronize the device over the specified range.

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used. See Application Note 77.

The LTM4636-1 device is an inherently current mode controlled device, so parallel modules will have good current sharing. This will balance the thermals in the design.

Tie the COMPA to COMPB and then tie the COMPA pins together, tie V_{FB} pins of each LTM4636-1 together to share the current evenly. Figure 21 shows a schematic of the parallel design. For external compensation and parallel operation only tie COMP A pins together with external compensation.

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases (see Figure 2).

PLL, Frequency Adjustment and Synchronization

The LTM4636-1 switching frequency is set by a resistor (R_{FREQ}) from the FREQ pin to signal ground. A 20µA current (I_{FREQ}) flowing out of the FREQ pin through R_{FREQ} develops a voltage on the FREQ pin. R_{FREQ} can be calculated as:

$$R_{FREQ} = \frac{FREQV}{20\mu A}$$

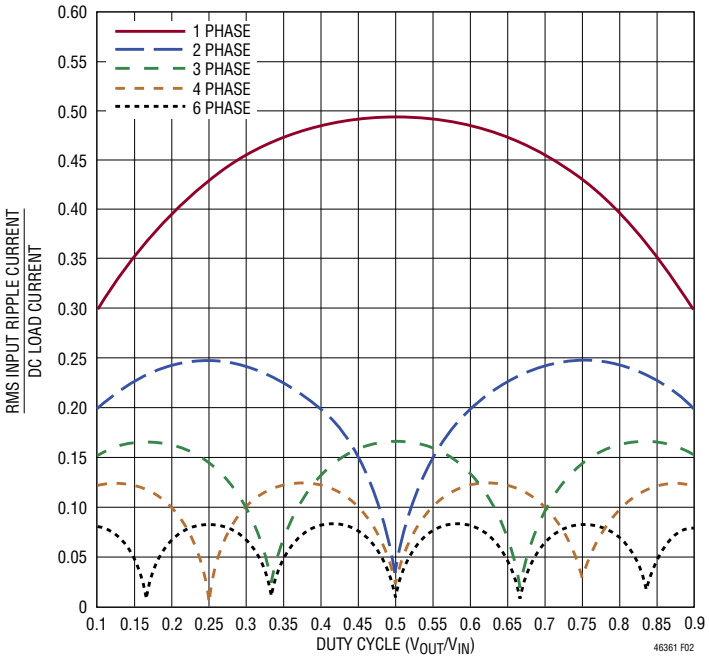


Figure 2. Normalized Input RMS Ripple Current vs Duty Cycle for One to Six µModule Regulators (Phases)

APPLICATIONS INFORMATION

The relationship of FREQV voltage to switching frequency is shown in Figure 3. For low output voltages from 0.6V to 1.2V, 350kHz operation is an optimal frequency for the best power conversion efficiency while maintaining the inductor current to about 45% of maximum load current. For output voltages from 1.5V to 1.8V, 500kHz is optimal. For output voltages from 2.5V to 3.3V, 700kHz is optimal. See efficiency graphs for optimal frequency set point. Limit the 2.5V and 3.3V outputs to 35A.

The LTM4636-1 can be synchronized from 200kHz to 1200kHz with an input clock that has a high level above 2V and a low level below 1.2V. See the Typical Applications section for synchronization examples. The LTM4636-1 minimum on-time is limited to approximately 100ns. The on-time can be calculated as:

$$t_{ON(MIN)} = \frac{1}{FREQ} \bullet \left(\frac{V_{OUT}}{V_{IN}} \right)$$

The LTM4636-1's CLKOUT pin phase difference from V_{OUT} can be programmed by applying a voltage to the PHMODE pin. This voltage can be programmed using the 5.5V $INTV_{CC}$ pin. Most of the phase selections can be programmed by either grounding, floating, or tying this pin to $INTV_{CC}$. The 60 degree phase shift will require 3/4 $INTV_{CC}$ and can be programmed with a voltage divider from the $INTV_{CC}$ pin. See Figure 4 for phase programming and the 2 to 6 phase connections. See Figure 21 for example design.

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The LTM4636-1 uses

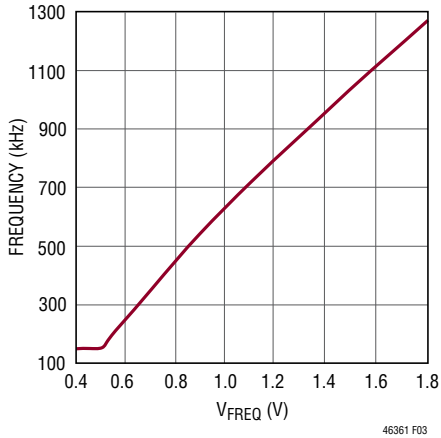


Figure 3. FREQ Voltage to Switching Frequency

APPLICATIONS INFORMATION

an accurate 4.99k resistor internally for the top feedback resistor. Figure 5 shows an example of coincident tracking.

$$V_{OUT(SLAVE)} = \left(1 + \frac{4.99k}{R_{TA}}\right) \bullet V_{TRACK}$$

V_{TRACK} is the track ramp applied to the slave's track pin. V_{TRACK} has a control range of 0V to 0.6V, or the internal reference voltage. When the master's output is divided down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point (see Figure 6). Voltage tracking is disabled when V_{TRACK} is more than 0.6V. R_{TA} in Figure 5 will be equal to R_{FB} for coincident tracking.

The TRACK/SS pin of the master can be controlled by an external ramp or the soft-start function of that regulator can be used to develop that master ramp. The LTM4636-1 can be used as a master by setting the ramp rate on its track pin using a soft-start capacitor. A 1.25µA current source is used to charge the soft-start capacitor. The following equation can be used:

$$t_{SOFT\text{-}START} = 0.6V \bullet \left(\frac{C_{SS}}{1.25\mu A}\right)$$

PHASE SELECTION

V_{OUT} PHASE	CLKOUT PHASE	PHMODE (V)
0	90	0
0	90	1/4 $INTV_{CC}$
0	120	FLOAT
0	60	3/4 $INTV_{CC}$
0	180	$INTV_{CC}$

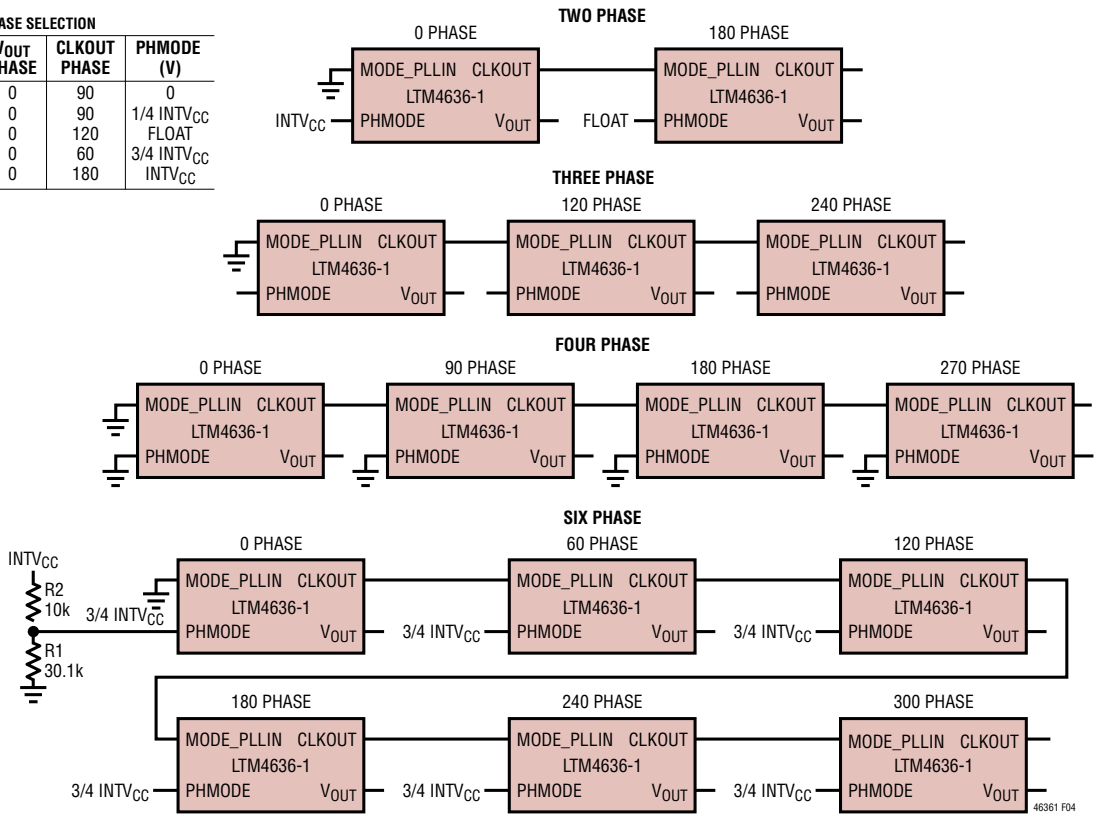
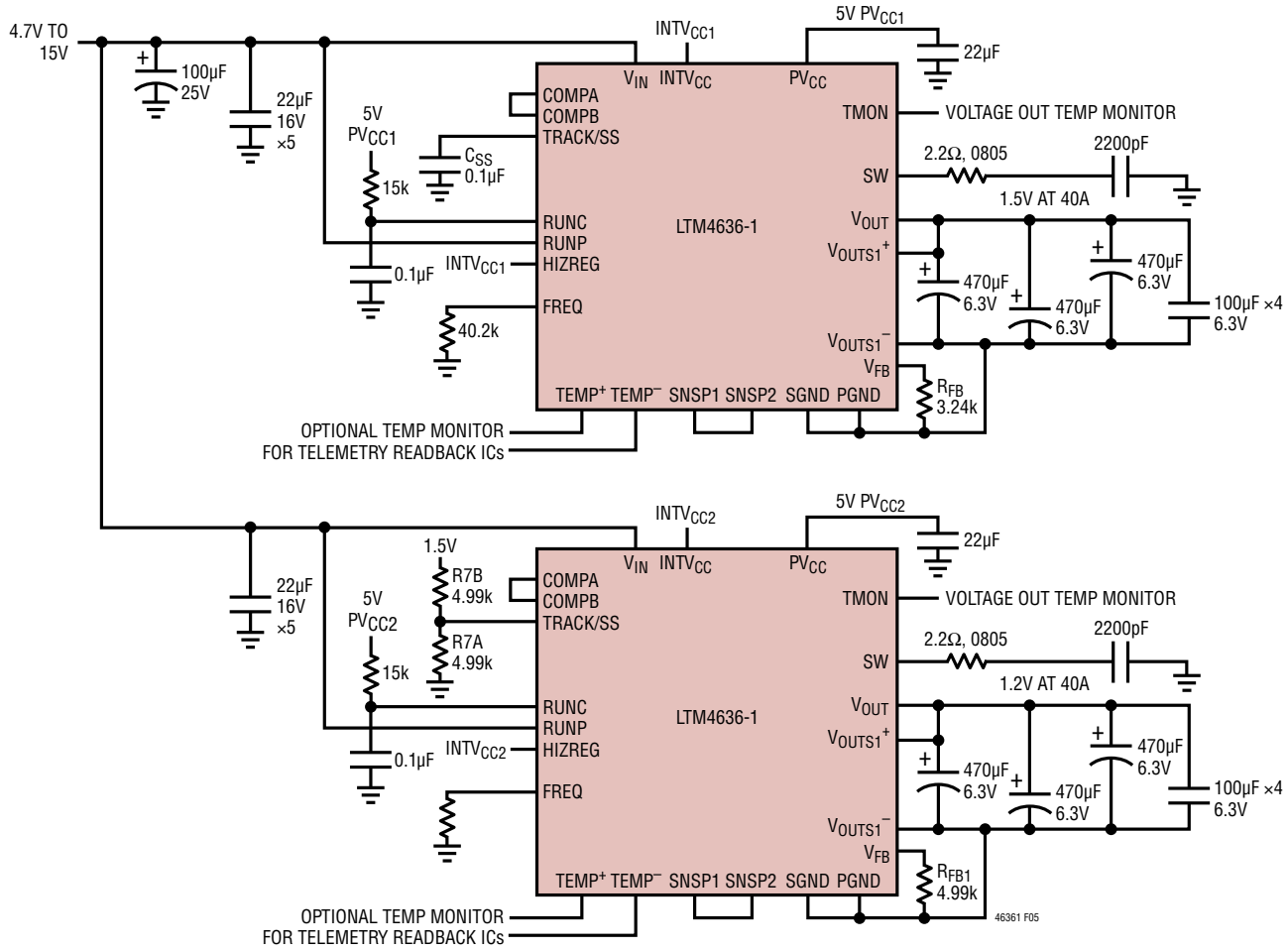


Figure 4. Phase Selection Examples

APPLICATIONS INFORMATION



PINS NOT USED IN THIS CIRCUIT:
CLKOUT, GMON, MODE/PLLIN, PGOOD, OTP_SET, CROWBAR, OVP_TRIP, OVP_SET, BIAS, OVER_TEMP, PHMODE, PWM, TEST1, TEST2, TEST3

Figure 5. Dual Outputs (1.5V and 1.2V) with Tracking

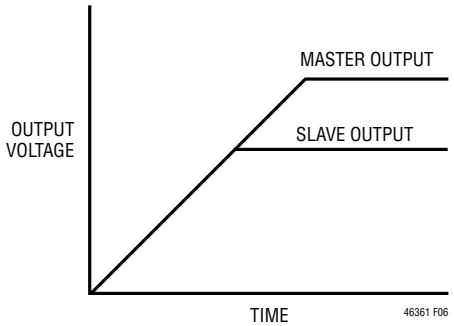


Figure 6. Output Voltage Coincident Tracking Characteristics

APPLICATIONS INFORMATION

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's TRACK/SS pin. As mentioned above, the TRACK/SS pin has a control range from 0V to 0.6V. The master's TRACK/SS pin slew rate is directly equal to the master's output slew rate in volts/time. The equation:

$$\frac{MR}{SR} \bullet 4.99k = R_{TB}$$

where MR is the master's output slew rate and SR is the slave's output slew rate in volts/time. When coincident tracking is desired, then MR and SR are equal, thus R_{TB} is equal to 60.4k. R_{TA} is derived from equation:

$$R_{TA} = \frac{0.6V}{\frac{V_{FB}}{4.99k} + \frac{V_{FB}}{R_{FB1}} - \frac{V_{TRACK}}{R_{TB}}}$$

where V_{FB} is the feedback voltage reference of the regulator, and V_{TRACK} is 0.6V. Since R_{TB} is equal to the 4.99k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then R_{TA} is equal to R_{FB} with $V_{FB} = V_{TRACK}$. Therefore R_{TB} = 4.99k, and R_{TA} = 4.99k in Figure 5.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R_{TB} can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach its final value before the master output.

For example, MR = 1.5V/ms, and SR = 1.2V/ms. Then R_{TB} = 6.19k. Solve for R_{TA} to equal 4.22k.

For applications that do not require tracking or sequencing, simply tie the TRACK/SS pin to $INTV_{CC}$ to let RUN control the turn on/off. When the RUN pin is below its threshold or the V_{IN} undervoltage lockout, then TRACK/SS is pulled low.

Default Overcurrent and Overvoltage Protection

The LTM4636-1 has overcurrent protection (OCP) in a short circuit. The internal current comparator threshold folds back during a short to reduce the output current. An overvoltage condition (OVP) above 10% of the regulated output voltage will force the top MOSFET off and the bottom MOSFET on until the condition is cleared. Foldback current limiting is disabled during soft-start or tracking start-up.

Temperature Monitoring

Measuring the absolute temperature of a diode is possible due to the relationship between current, voltage and temperature described by the classic diode equation:

$$I_D = I_S \bullet e\left(\frac{V_D}{\eta \bullet V_T}\right)$$

or

$$V_D = \eta \bullet V_T \bullet \ln\frac{I_D}{I_S}$$

where I_D is the diode current, V_D is the diode voltage, η is the ideality factor (typically close to 1.0) and I_S (saturation current) is a process dependent parameter. V_T can be broken out to:

$$V_T = \frac{k \bullet T}{q}$$

where T is the diode junction temperature in Kelvin, q is the electron charge and k is Boltzmann's constant. V_T is approximately 26mV at room temperature (298K) and scales linearly with Kelvin temperature. It is this linear temperature relationship that makes diodes suitable temperature sensors. The I_S term in the previous equation is the extrapolated current through a diode junction when the diode has zero volts across the terminals. The I_S term varies from process to process, varies with temperature, and by definition must always be less than I_D. Combining all of the constants into one term:

$$K_D = \frac{\eta \bullet k}{q}$$

where $K_D = 8.62^{-5}$, and knowing $\ln(I_D/I_S)$ is always positive because I_D is always greater than I_S, leaves us with the equation that:

$$V_D = T(KELVIN) \bullet K_D \bullet \ln\frac{I_D}{I_S}$$

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where V_D appears to increase with temperature. It is common knowledge that a silicon diode biased with a current source has an approximate –2mV/°C temperature relationship (Figure 7), which is at odds with the equation. In fact, the I_S term increases with temperature, reducing the $\ln(I_D/I_S)$ absolute value yielding an approximate –2mV/°C composite diode voltage slope.

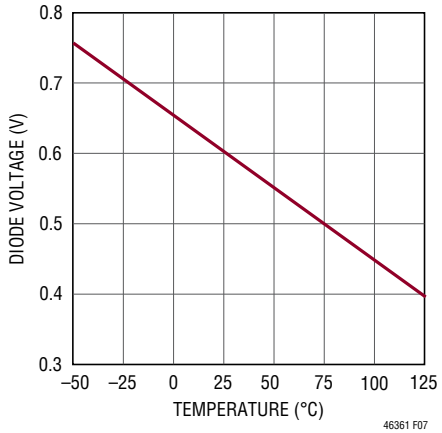


Figure 7. Diode Voltage V_D vs Temperature T(°C)

To obtain a linear voltage proportional to temperature we cancel the I_S variable in the natural logarithm term to remove the I_S dependency from the equation 1. This is accomplished by measuring the diode voltage at two currents I_1, and I_2, where $I_1 = 10 \bullet I_2$) and subtracting we get:

$$\Delta V_D = T(KELVIN) \bullet K_D \bullet IN\frac{I_1}{I_S} - T(KELVIN) \bullet K_D \bullet IN\frac{I_2}{I_S}$$

Combining like terms, then simplifying the natural log terms yields:

$$\Delta V_D = T(KELVIN) \bullet K_D \bullet IN(10)$$

and redefining constant

$$K_D' = K_D \bullet IN(10) = \frac{198\mu V}{K}$$

yields

$$\Delta V_D = K'_D \bullet T(KELVIN)$$

Solving for temperature:

$$T(KELVIN) = \frac{\Delta V_D}{K_D'} (°CELSIUS) = T(KELVIN) - 273.15$$

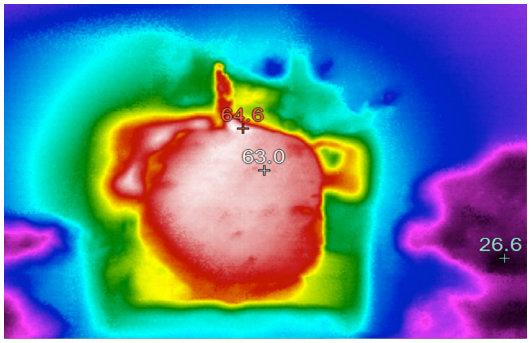
where

300°K = 27°C

means that is we take the difference in voltage across the diode measured at two currents with a ratio of 10, the resulting voltage is 198µV per Kelvin of the junction with a zero intercept at 0 Kelvin.

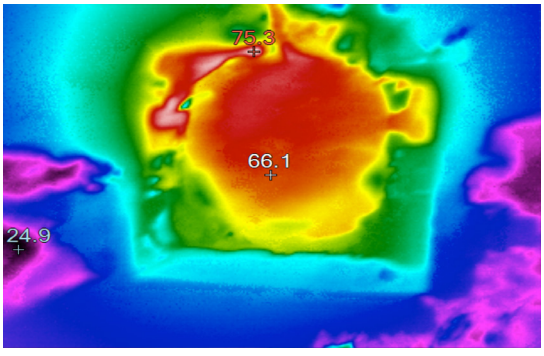
The diode connected NPN transistor at the TEMP pin can be used to monitor the internal temperature of the LTM4636-1.

V_{IN}	V_{OUT}	I_{OUT}	AIR FLOW
12	1	40	200 LFM



(8a)

V_{IN}	V_{OUT}	I_{OUT}	AIR FLOW
12	3.3	35	200 LFM



(8b)

Figure 8. The Two Images Show the LTM4636-1 Operating at 1V at 40A and 3.3V at 35A from a 12V Input. Both Images Reflect Only a 40°C to 45°C Rise Above Ambient at Full Load Current with 200LPM

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Enhanced Overvoltage OVP and Overtemperature Protection OTP

The LTM4636-1 has two enhanced protection features that can be used to detect overtemperature and overvoltage.

The BIAS pin is supplied to power the protection circuitry off of an auxiliary supervisory supply separate from the high power circuit breaker path. This is required to properly bias the protection circuitry with the proper headroom at power up, and circuit breaker retry. This separate bias supply needs to supply 1mA per module, and 6mA per module during an overvoltage and overtemperature event. If the CROWBAR signal is used then an instantaneous current will be need to drive the crow bar mosfets. This is current is ~ 50mA. The bias voltage can be used to program the OTP and OVP set points.

The TMON pin voltage varies from 1.0V at 25°C up to 1.45V at 150°C. The TMON pin can be compared to a programmable set point utilizing the 24.9k resistor to ground on the OTP_SET pin. See the block diagram. By adding an external resistor from this pin to the BIAS pin, an OTP trip point can be set below the 150°C (1.45V) level as an overtemperature detection, and the OVER_TEMP open-collector pin will pull low to provide a system alert, or can be used to trip off power. This feature can be ignored by floating the OVER_TEMP and OTP_SET pins.

The equation:

$$R_{OTP} = 24.9k \bullet \left[\left(\frac{BIAS}{OTP_SET}\right) - 1\right];$$

$$OTP_SET = 1.0V(25°C) + 3.52mV/°C \bullet 105°C$$

For 130°C, OTP_SET = 1.37V

Where BIAS is the voltage applied to BIAS pin, Ex: 5V. OTP_SET is the voltage equivalent to temperature on the TMON pin. For example, BIAS = 5V, and the overtemperature trip point is set to 130°C. TMON has a range of 440mV from 25°C to 150°C, therefore the TMON pin moves 3.52mV/°C above 25°C. 130°C minus 25°C = 105°C rise.

The ROTP resistor calculates out to a close 1% value of 66.5k.

The BIAS supply can be between 4V to 5.5V, the OTP_SET trip point depends on the BIAS supply voltage to be accurate, otherwise a more accurate reference can be derived from the BIAS supply to be utilized to program the set point. See application schematics.

The LTM4636-1 controller has overvoltage protection feedback voltage referred that trips at ~7.5% above V_{OUT}. This feature will try to correct an overvoltage transient issue, but does not protect for a shorted input power source in the event of a top power switch short while the bottom switch is on trying to protect the load. The input source has a direct path to ground in this condition. Neither will this feature protect an overvoltage issue caused by an open feedback path. The enhanced overvoltage protection consists of a fast comparator that compares V_{OUT} to a programmed value set at the OVP_SET pin. An OVP_TRIP point can be set using the BIAS supply and an external resistor (R_{OVP}) with the internal 24.9k resistor. The equation:

$$R_{OVP} = 24.9k \bullet \left[\left(\frac{BIAS}{OVP_TRIP}\right) - 1\right]$$

where OVP_TRIP is the maximum overvoltage level set point. The OVP_TRIP open-collector output pulls low and can be used to trip off a circuit breaker or alert the system of an OVP fault. The CROWBAR output drive can be used to drive an external N-channel power MOSFET to clamp the output voltage and discharge the inductor stored energy. Depending on the power design, the OVP trip point and the output capacitance, the CROWBAR clamp may not be needed. Testing will need to be performed to characterize the behavior of the clamping with and without the crowbar. Proper crowbar power MOSFET SOA (safe operating area) selection will be required to make sure the MOSFET can handle the discharge current. A small surface mount resistor can be placed in series from V_{OUT} to the drain of the CROWBAR FET to limit the CROWBAR but still clamp the output. To disable the function, float the OVP_SET, OVP_TRIP and CROWBAR pins.

The BIAS supply can be between 4.0V to 5.5V, while the OVP_TRIP point depends on the BIAS supply voltage accuracy. Otherwise an accurate reference can be derived from the BIAS supply.

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RUNP and RUNC Enable

The RUNP pin is used to enable the 5V PV_{CC} supply that powers the power driver stage and enables the power stage ~1ms later. The RUNC pin is used to enable the control section that drives the power stage. The RUNP needs to be enabled first, and then RUNC. RUNP has a 0.85V threshold and can be connected to the input voltage and RUNC has a 1.35V threshold and a 10k resistor to ground. See the Block Diagram for details. A 0.1µF capacitor from the RUNC pin to ground is used to set the delay for RUNC enable.

$INTV_{CC}$ and PV_{CC} Regulators

The LTM4636-1 has an internal low dropout regulator from V_{IN} called $INTV_{CC}$. This regulator output has a 4.7µF ceramic capacitor internal. This regulator powers the control section. The PV_{CC} 5V regulator supplies power to the power MOSFET driver stage. An additional 50mA can be used from this 5V PV_{CC} supply for other needs. The input supply source resistance needs to be very low in order to minimize IR drops when operating from a 5V input source. Depending on the output voltage and current, the input supply can source large current,and PV_{CC} 5V regulator needs a minimum 4.7V supply. Additional input capacitance maybe needed for 5V inputs to limit the input droop.

Stability Compensation

The LTM4636-1 has already been internally compensated when COMPB is tied to COMPA for all output voltages. Table 5 is provided for most application requirements. For specific optimized requirements, disconnect COMPB from COMPA, and use LTpowerCAD to perform specific control loop optimization. Then select the desired external compensation and output capacitance for the desired optimized response.

SW Pins

The SW pins are generally for testing purposes by monitoring these pins. These pins can also be used to dampen out switch node ringing caused by LC parasitic in the switched current paths. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor. If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First the SW pin can be monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance Z can be calculated:

$$Z(L) = 2\pi fL,$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by: $Z(C) = 1/(2\pi fC)$. These values are a good place to start with. Modification to these components should be made to attenuate the ringing with the least amount of power loss. A recommended value of 2.2Ω in series with 2200pF to ground should work for most applications. See Figure 19 for layout guidelines. The 2.2Ω resistor should be an 0805 size.

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board. The motivation for providing these thermal coefficients in found in JESD51-12 (“Guidelines for Reporting and Using Electronic Package Thermal Information”).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to predict the µModule regulator’s thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are, in and of themselves, not relevant to providing guidance of thermal performance; instead, the derating

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curves provided in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a 95mm × 76mm PCB with four layers.

2. $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

3 θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4 θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule package and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and a portion of the board. The board temperature is measured a specified distance from the package.

A graphical representation of the aforementioned thermal resistances is given in Figure 9; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through the bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

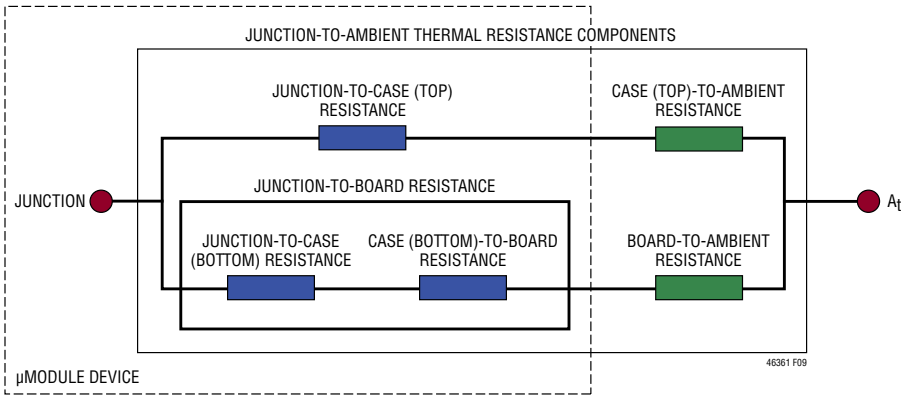


Figure 9. Graphical Representation of JESD51-12 Thermal Coefficients

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Within the LTM4636-1, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4636-1 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4636-1 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves shown in this data sheet.

The power loss curves in Figure 10 to Figure 12 can be used in coordination with the load current derating curves in Figure 13 to Figure 18 for calculating an approximate θ_{JA} thermal resistance for the LTM4636-1 with various airflow conditions. The power loss curves are taken at room temperature and can be increased with a multiplicative factor according to the junction temperature, which is ~1.4 for 120°C. The derating curves are plotted with the output current starting at 40A and the ambient temperature increased. The output voltages are 1V, 2.5V and 3.3V. These are chosen to include the lower, middle and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at ~125°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 125°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example, in Figure 14 the load current is derated to ~30A at ~94°C with no air flow and the power loss for the 12V to 1.0V at 30A output is about 4.2W. The 4.2W loss is calculated with the ~3W room temperature loss from the 12V to 1.0V power loss curve at 30A, and the 1.4 multiplying factor at 125°C junction. If the 94°C ambient temperature is subtracted from the 125°C junction temperature, then the difference of 31°C divided by 4.2W equals a 7.4°C/W θ_{JA} thermal resistance. Table 2 specifies a 7.2°C/W value which is very close. Tables 2, 3, and 4 provide equivalent thermal resistances for 1V, 1.5V and 3.3V outputs with and without airflow and heat sinking. The derived thermal resistances in Tables 2 thru 4 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss curves are provided in Figure 10 through Figure 12. The printed circuit board is a 1.6mm thick six layer board with two ounce copper for all layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm.

Safety Considerations

The LTM4636-1 does not provide galvanic isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

The fuse or circuit breaker should be selected to limit the current to the regulator during overvoltage in case of an internal top MOSFET fault. If the internal top MOSFET fails, then turning it off will not resolve the overvoltage, thus the internal bottom MOSFET will turn on indefinitely trying to protect the load. Under this fault condition, the

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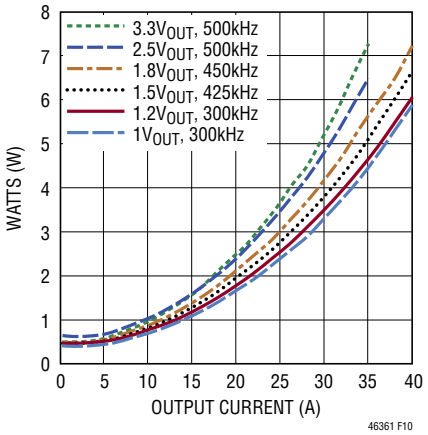


Figure 10. 5V Input Power Loss Curves

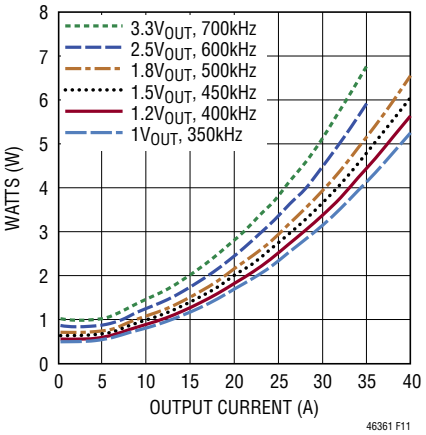


Figure 11. 8V Input Power Loss Curves

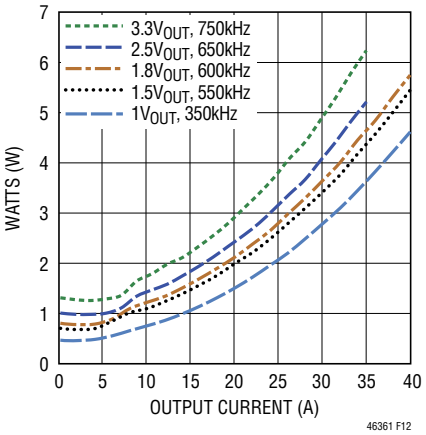


Figure 12. 12V Input Power Loss Curves

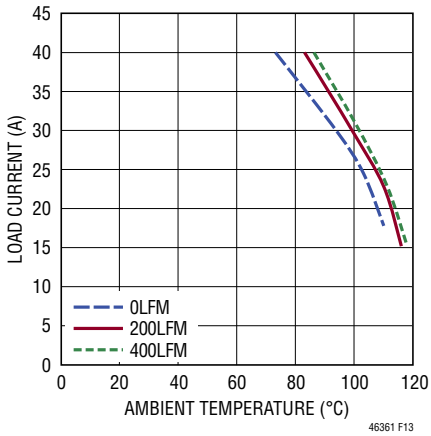


Figure 13. $5V_{IN}$, $1V_{OUT}$ Derate Curve

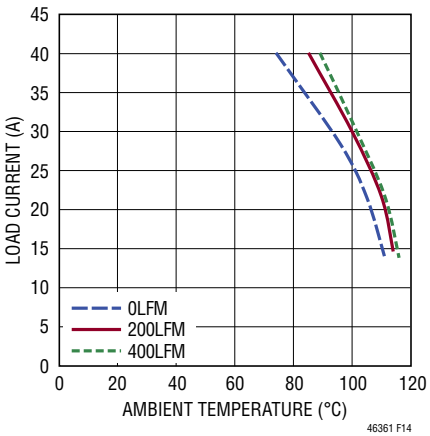


Figure 14. $12V_{IN}$, $1V_{OUT}$ Derate Curve

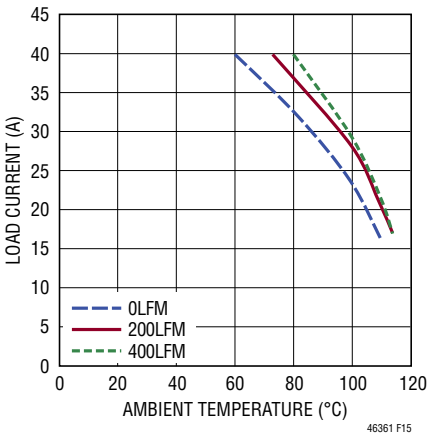


Figure 15. $5V_{IN}$, $1.5V_{OUT}$ Derate Curve

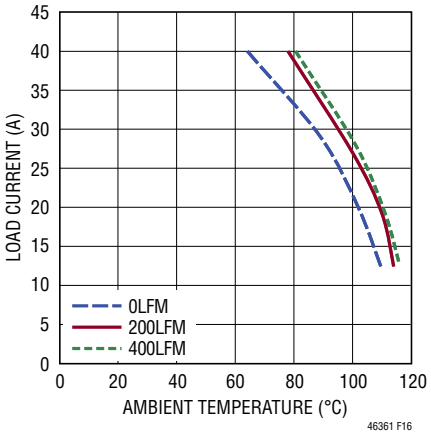


Figure 16. $12V_{IN}$, $1.5V_{OUT}$ Derate Curve

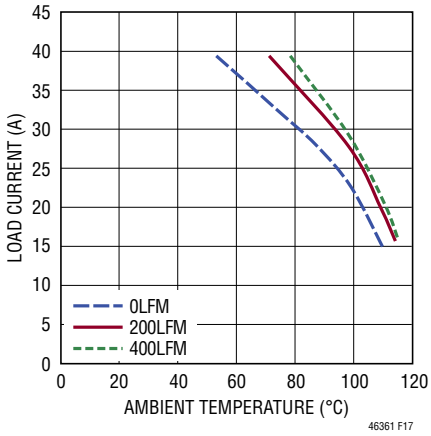


Figure 17. $5V_{IN}$, $3.3V_{OUT}$ Derate Curve

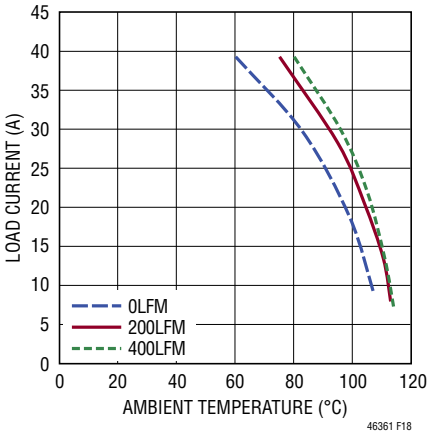


Figure 18. $12V_{IN}$, $3.3V_{OUT}$ Derate Curve

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Table 2. 1V Output

DERATING CURVE	V_{IN}	POWER LOSS CURVE	AIRFLOW (LFM)	θ_{JA} (°C/W)
Figures 13, 14	5V, 12V	Figure 10, 12	0	7.2
Figures 13, 14	5V, 12V	Figure 10, 12	200	5.4
Figures 13, 14	5V, 12V	Figure 10, 12	400	4.8

Table 3. 1.5V Output

DERATING CURVE	V_{IN}	POWER LOSS CURVE	AIRFLOW (LFM)	θ_{JA} (°C/W)
Figures 15, 16	5V, 12V	Figure 10, 12	0	7.4
Figures 15, 16	5V, 12V	Figure 10, 12	200	5.0
Figures 15, 16	5V, 12V	Figure 10, 12	400	4.5

Table 4. 3.3V

DERATING CURVE	V_{IN}	POWER LOSS CURVE	AIRFLOW (LFM)	θ_{JA} (°C/W)
Figures 17, 18	12V	Figure 10, 12	0	7.4
Figures 17, 18	12V	Figure 10, 12	200	5.0
Figures 17, 18	12V	Figure 10, 12	400	4.4

Table 5. LTM4636-1 Capacitor Matrix, All Below Parameters are Typical and are Dependent on Board Layout

Taiyo Yuden	22µF, 25V	C3216X7S0J226M	Panasonic SP	470µF 2.5V	EEFGX0E471R	Sanyo	20SEP100M	100µF 20V
Murata	22µF, 25V	GRM31CR61C226KE15L	Panasonic POSCAP	470µF 2R5	2R5TPD470M5			
Murata	100µF, 6.3V	GRM32ER60J107M	Panasonic POSCAP	470µF 6.3V	6TPD470M5			
AVX	100µF, 6.3V	18126D107MAT						
Taiyo Yuden	220µF, 4V							
Murata	220µF, 4V							

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V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)	C_{OUT1} (CERAMIC) AND C_{OUT2} (CERAMIC AND BULK)	C_{FF}* (pf)	C_{COMP} (pf)	V_{IN} (V)	DROOP (mV)	PEAK-TO-PEAK DEVIATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A/µs)	R_{FB} (kΩ)	FREQ (kHz)
0.9	22µF × 5	100µF	100µF × 8, 470µF × 3	22	100	5,12	38	76	40	15	10	350
0.9	22µF × 5	100µF	220µF × 6, 470µF × 2	68	100	5,12	40	80	30	15	10	350
0.9	22µF × 5	100µF	220µF × 10, 470µF	None	220	5,12	40	80	30	15	10	350
1	22µF × 5	100µF	100µF × 4, 470µF × 3	None	100	5,12	40	80	30	15	7.5	350
1	22µF × 5	100µF	100µF × 6, 470µF × 2	None	100	5,12	50	100	30	15	7.5	350
1	22µF × 5	100µF	100µF × 8, 470µF × 2	None	150	5,12	55	105	30	15	7.5	350
1.2	22µF × 5	100µF	100µF × 4, 470µF × 3	None	100	5,12	45	90	35	15	4.99	350
1.2	22µF × 5	100µF	100µF × 6, 470µF × 2	None	100	5,12	45	90	35	15	4.99	400
1.2	22µF × 5	100µF	220µF × 4, 470µF	None	100	5,12	50	104	30	15	4.99	400
1.5	22µF × 5	100µF	100µF × 4, 470µF × 3	None	100	5,12	60	120	35	15	3.24	425
1.5	22µF × 5	100µF	100µF × 4, 470µF × 2	None	100	5,12	56	110	35	15	3.24	425
1.5	22µF × 5	100µF	100µF × 3, 470µF	None	100	5,12	75	150	25	15	3.24	425
1.8	22µF × 5	100µF	100µF × 3, 470µF	None	220	5,12	90	180	25	15	2.49	500
1.8	22µF × 5	100µF	100µF, 470µF	None	220	5,12	95	197	24	15	2.49	500
1.8	22µF × 5	100µF	220µF × 2, 470µF	None	220	5,12	90	180	20	15	2.49	500
2.5	22µF × 5	100µF	100µF × 2, 470µF	None	220	5,12	120	220	30	15	1.58	650 (12V) 500 (5V)
2.5	22µF × 5	100µF	100µF × 6, 470µF	22	220	5,12	87	174	40	15	1.58	650 (12V) 500 (5V)
3.3	22µF × 5	100µF	100µF × 4	220	220	5,12	130	260	25	15	1.1	750 (12V) 500 (5V)
3.3	22µF × 5	100µF	100µF, 470µF	None	220	5,12	140	280	30	15	1.1	750 (12V) 500 (5V)

* C_{FF} is a capacitor from V_{OUT} to V_{FB}.

Table 6. Enhanced External Compensation, Lower Voltage Transition During Transient. Careful Power Integrity Layout Required

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)†	C_{OUT1} (CERAMIC) AND C_{OUT2} (CERAMIC AND BULK)	C_{FF} (pf)	C_{COMP} (pf)	V_{IN} (V)	DROOP (mV)	PEAK-TO-PEAK DEVIATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A/µs)	R_{FB} (kΩ)	FREQ (kHz)	R_{COMP} (k)	C_{COMP} (pF)
0.9	22µF × 5	100µF	220µF × 10, 470µF	47	100	5, 12	25	50	26	15	10	350	15	1000
1	22µF × 5	100µF	220µF × 10, 470µF	47	100	5, 12	28	55	25	15	7.5	350	15	1000
1.2	22µF × 5	100µF	220µF × 10, 470µF	47	100	5, 12	33	66	30	15	4.99	350	15	1000

† Bulk capacitance is optional if V_{IN} has very low input impedance

APPLICATIONS INFORMATION

input voltage will source very large currents to ground through the failed internal top MOSFET and enabled internal bottom MOSFET. This can cause excessive heat and board damage depending on how much power the input voltage can deliver to this system. A fuse or circuit breaker can be used as a secondary fault protector in this situation. The LTM4636-1 has the enhanced over temperature protection discussed earlier and schematic applications will be shown at the end of the data sheet.

Layout Checklist/Example

The high integration of the LTM4636-1 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pad, unless they are capped or plated over.
- Place test points on signal pins for testing.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the COMP and V_{FB} pins together. Use an internal layer to closely connect these pins together.
- Add R_{SNUB} (2.2Ω) and C_{SNUB} (2200pF) to dampen switch ringing.

Figure 19 gives a good example of the recommended layout.

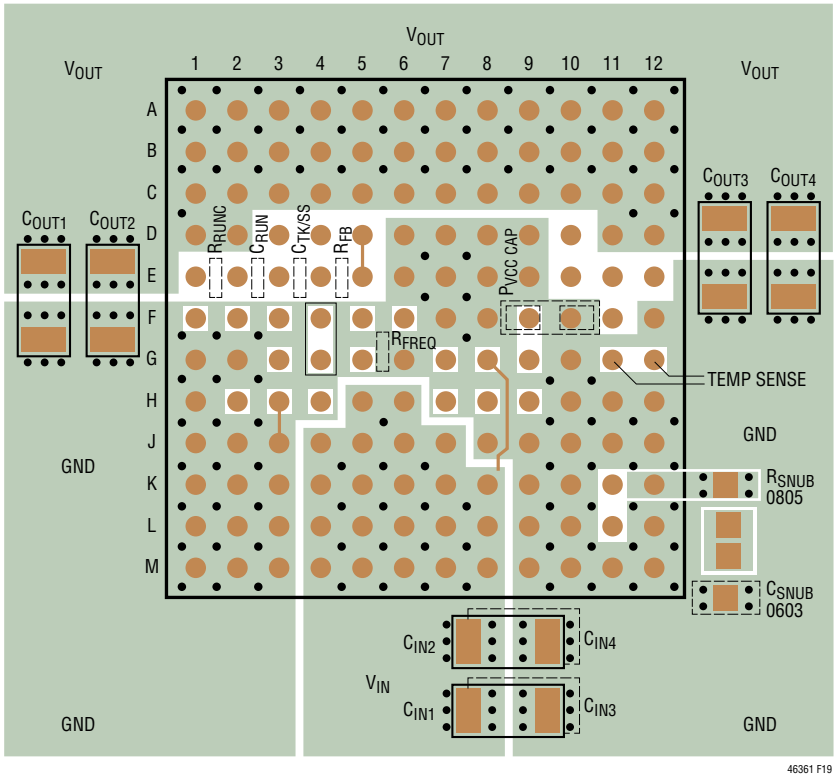


Figure 19. Recommended PCB Layout

TYPICAL APPLICATIONS

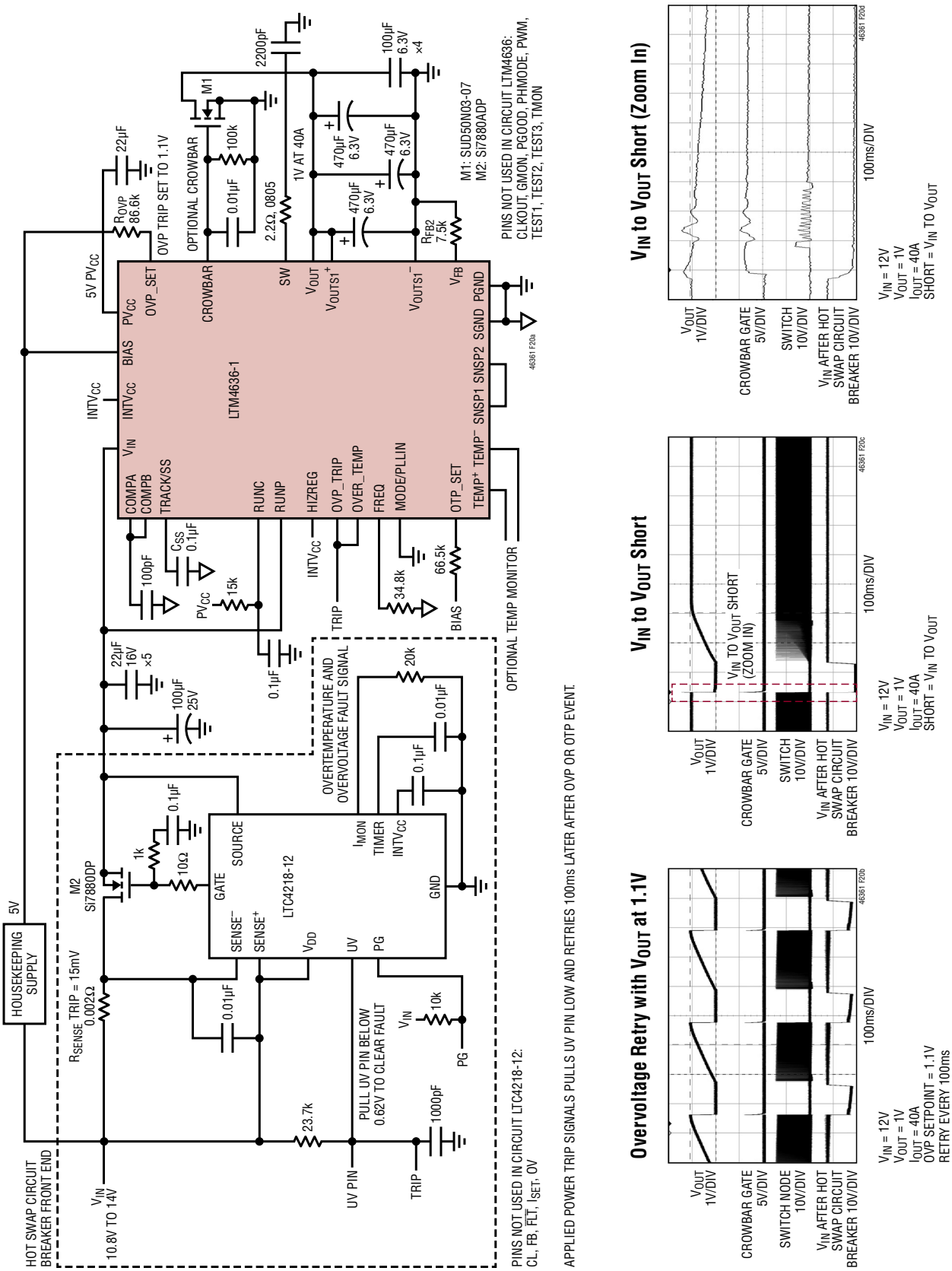
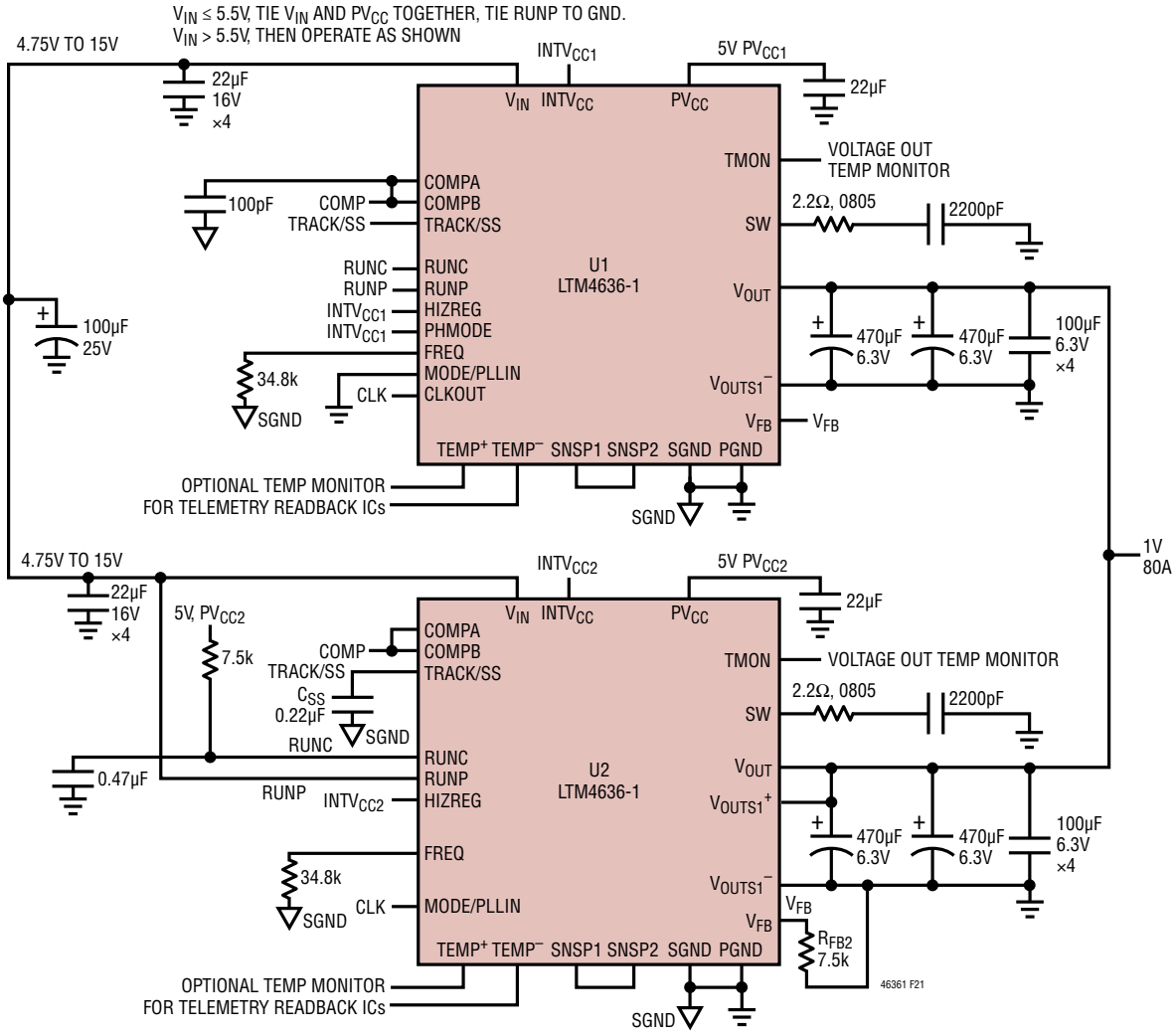


Figure 20. 10.8V to 14V, 1V at 40A Design with Protection

TYPICAL APPLICATIONS



PINS NOT USED IN CIRCUIT LTM4636-1 U1:
GMON, PGOOD, PWM, TEST1, TEST2, TEST3, V_{OSNS1}^+, CROWBAR, OTP_SET, OVP_SET, BIAS, OVP_TRIP, OVER_TEMP

PINS NOT USED IN CIRCUIT LTM4636-1 U2:
GMON, PGOOD, PHMODE, PWM, TEST1, TEST2, TEST3, CROWBAR, OTP_SET, OVP_SET, BIAS, OVP_TRIP, OVER_TEMP

Figure 21. 2-Phase 1V, 80A Regulator Design

TYPICAL APPLICATIONS

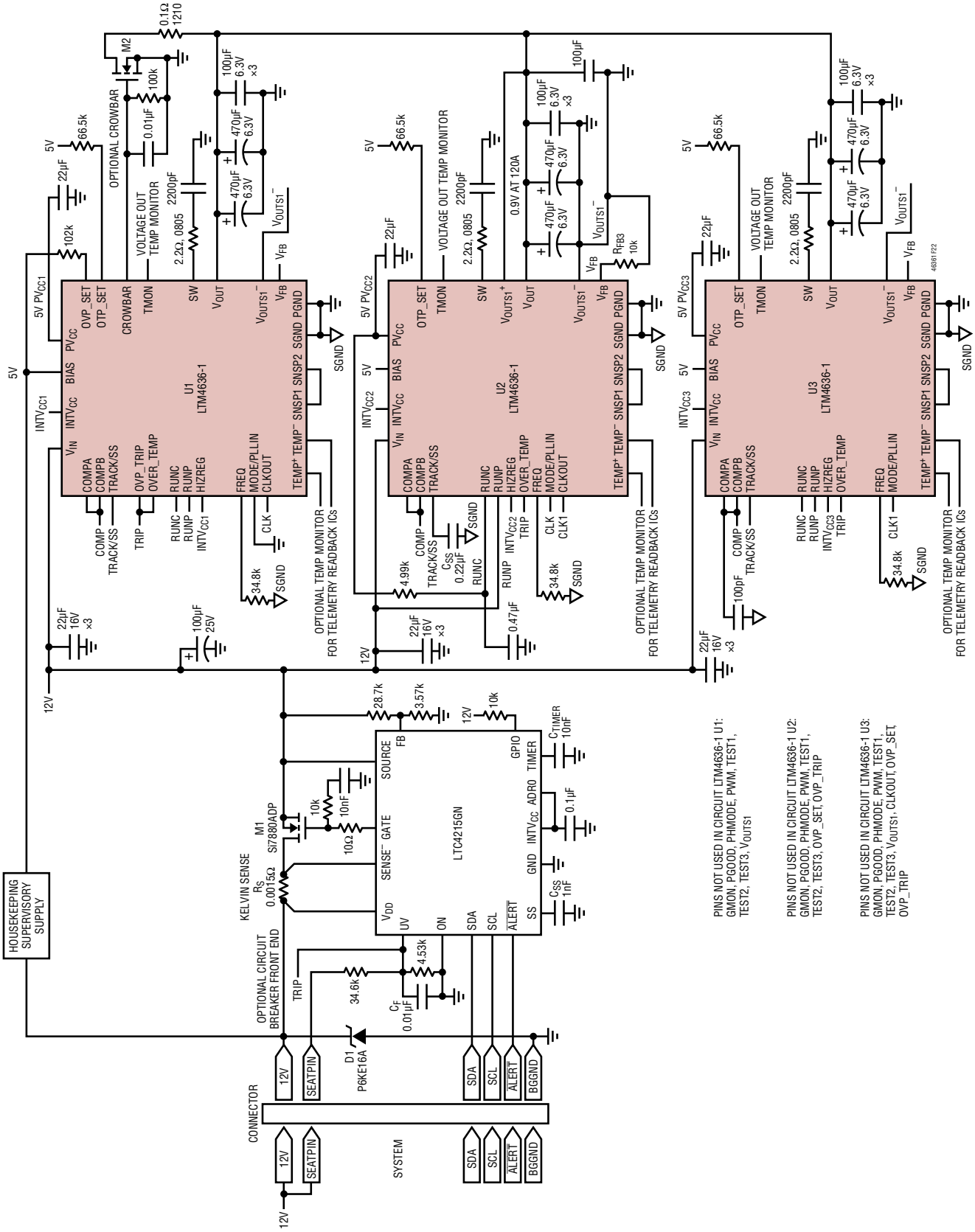


Figure 22. 3-Phase 0.9V at 120A with Overtemperature and Overvoltage Protection

TYPICAL APPLICATIONS

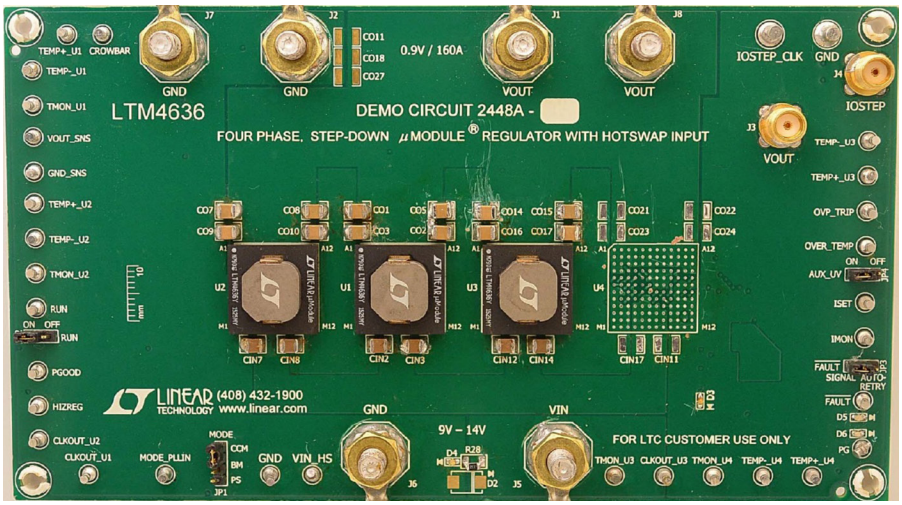


Figure 23. DC2448A Demo Board

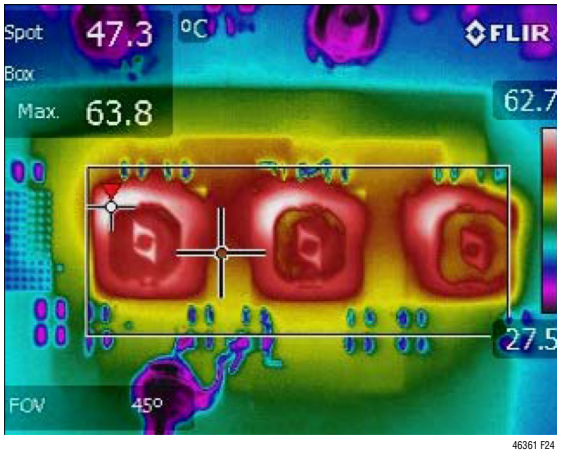


Figure 24. Thermal Plot, 12V to 0.9V at 120A, 400LFM Air Flow

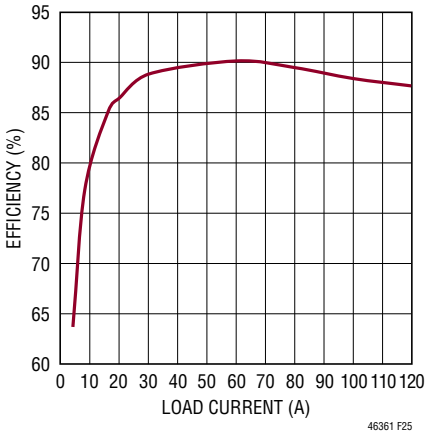
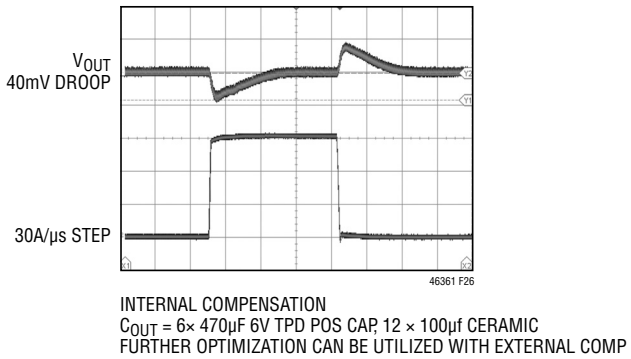


Figure 25. Efficiency, 12V to 0.9V at 120A



INTERNAL COMPENSATION
C_{OUT} = 6× 470µF 6V TPD POS CAP, 12 × 100µf CERAMIC
FURTHER OPTIMIZATION CAN BE UTILIZED WITH EXTERNAL COMP

Figure 26. 12V to 0.9V 30A/µs Load Step

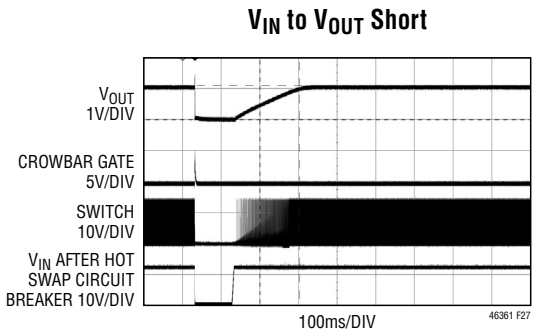


Figure 27. 12V to 0.9V Overvoltage Trip

TYPICAL APPLICATIONS

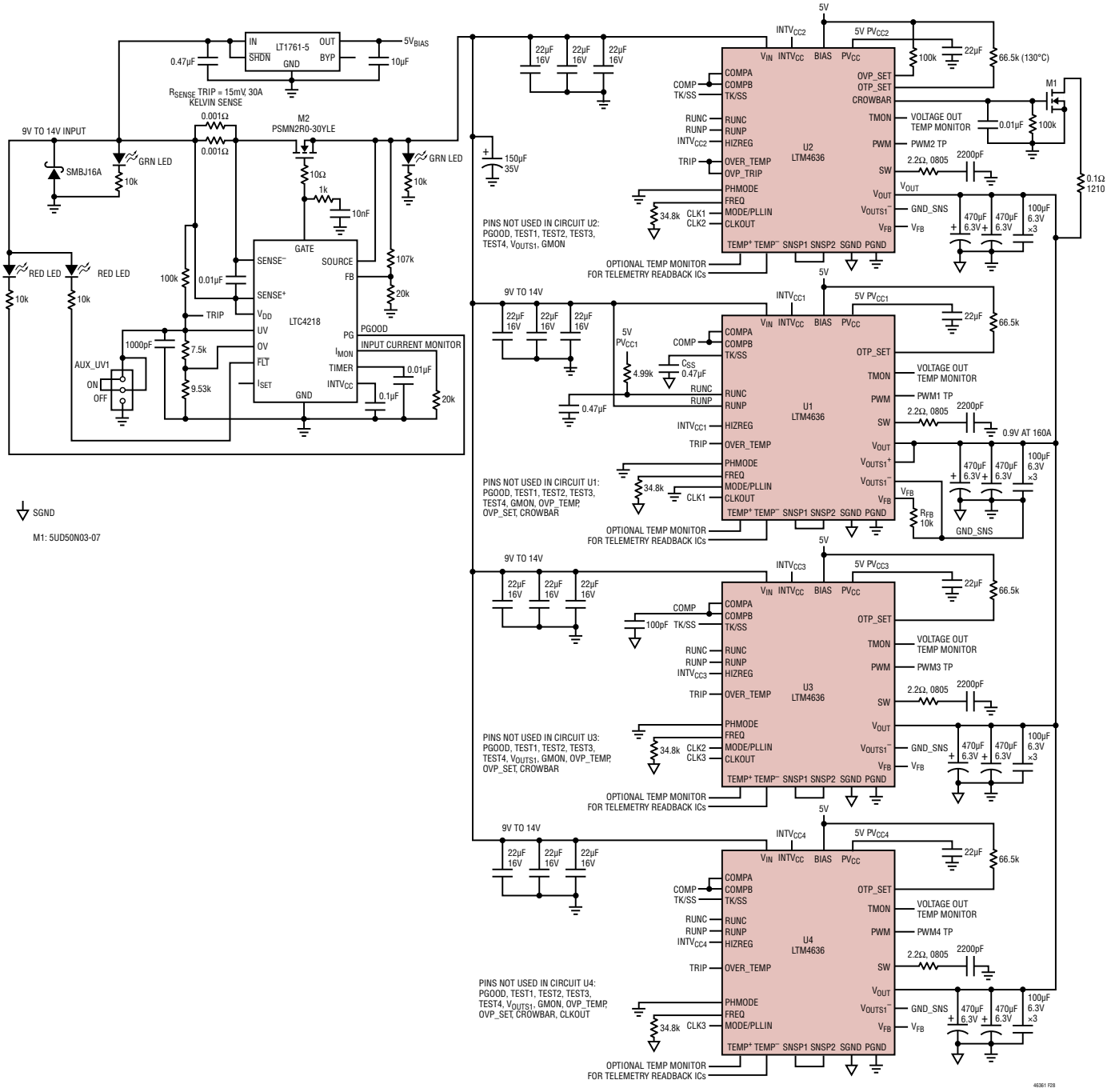


Figure 28. 12V to 0.9V, A1/60A with Circuit Breaker Front End and Overtemperature and Overvoltage Protection

TYPICAL APPLICATIONS

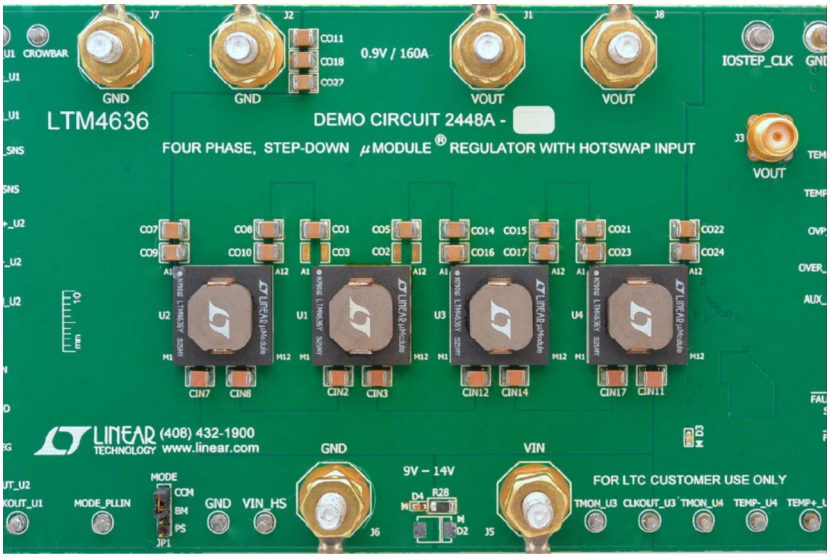


Figure 29. DC2448A Demo Board

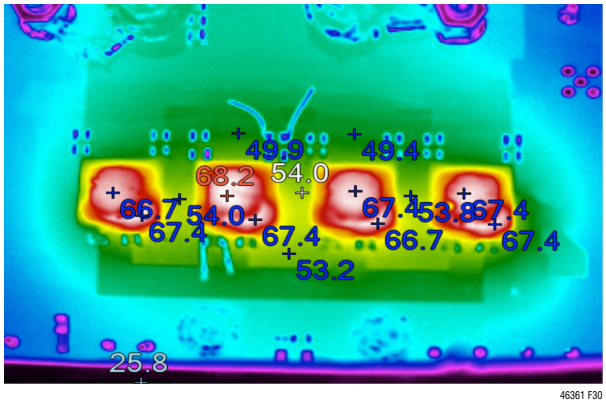


Figure 30. Thermal Plot, 12V to 0.9V at 160A, 400LFM Air Flow

V_{IN} to V_{OUT} Short

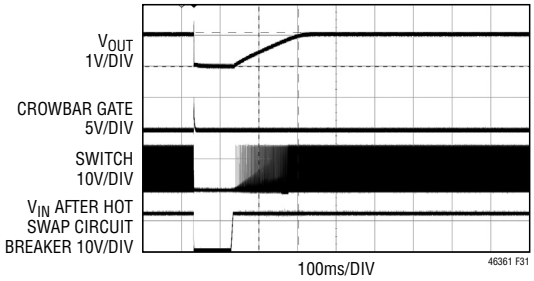


Figure 31. 12V to 0.9V Overvoltage Trip

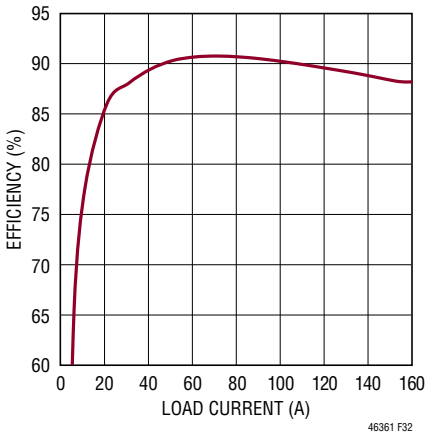
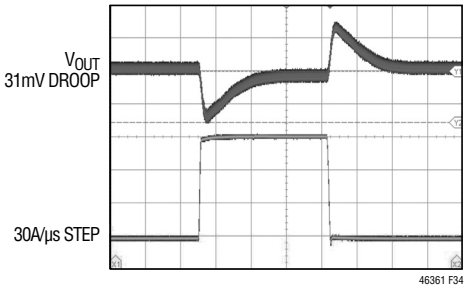


Figure 32. Efficiency, 12V to 0.9V at 160A



INTERNAL COMPENSATION
C_{OUT} = 8X 470µF 6V TPD POS CAP, 16 × 100µF CERAMIC
FURTHER OPTIMIZATION CAN BE UTILIZED WITH EXTERNAL COMP

Figure 33. 12V to 0.9V 30A/µs Load Step

PACKAGE DESCRIPTION

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

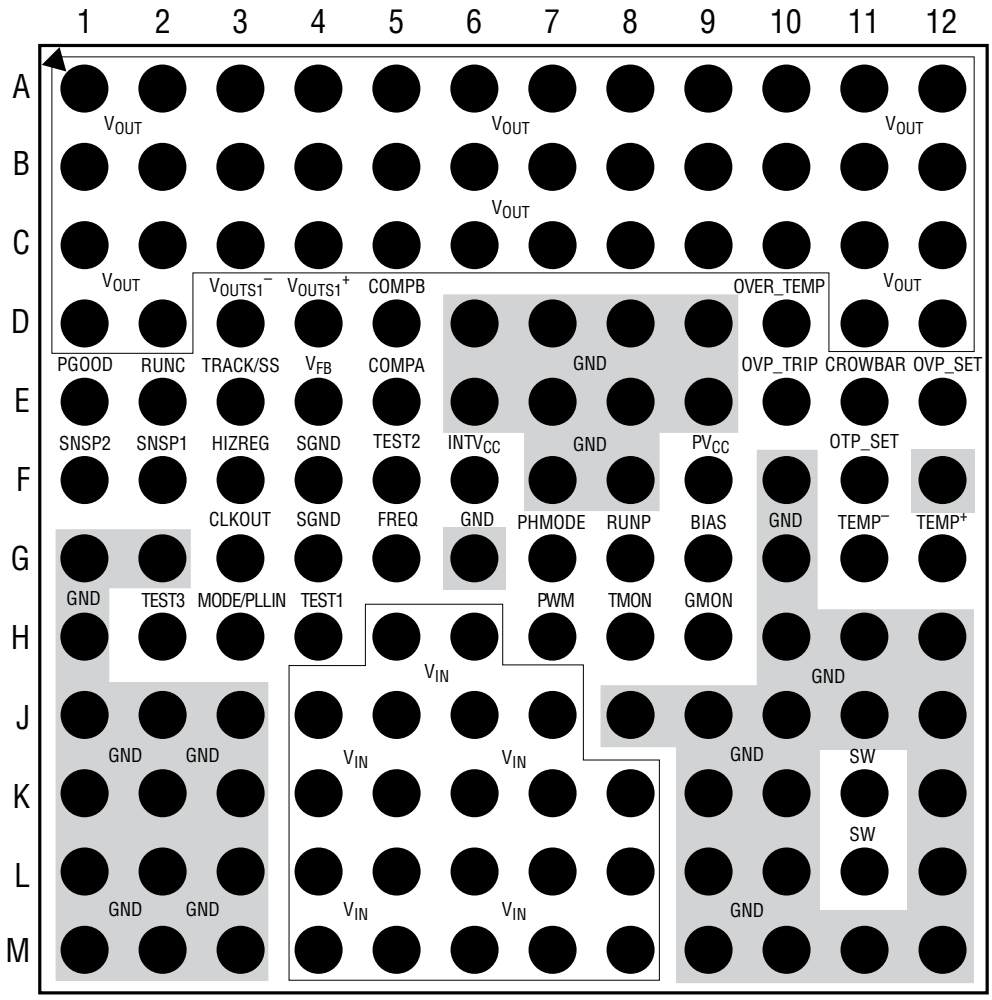
Pin Assignment Table (Arranged by Pin Number)

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT}	B1	V_{OUT}	C1	V_{OUT}	D1	V_{OUT}	E1	PGOOD	F1	SNSP2
A2	V_{OUT}	B2	V_{OUT}	C2	V_{OUT}	D2	V_{OUT}	E2	RUNC	F2	SNSP1
A3	V_{OUT}	B3	V_{OUT}	C3	V_{OUT}	D3	V_{OUTS1}^-	E3	TRACK/SS	F3	HIZREG
A4	V_{OUT}	B4	V_{OUT}	C4	V_{OUT}	D4	V_{OUTS1}^+	E4	V_{FB}	F4	SGND
A5	V_{OUT}	B5	V_{OUT}	C5	V_{OUT}	D5	COMPB	E5	COMPA	F5	TEST2
A6	V_{OUT}	B6	V_{OUT}	C6	V_{OUT}	D6	GND	E6	GND	F6	$INTV_{CC}$
A7	V_{OUT}	B7	V_{OUT}	C7	V_{OUT}	D7	GND	E7	GND	F7	GND
A8	V_{OUT}	B8	V_{OUT}	C8	V_{OUT}	D8	GND	E8	GND	F8	GND
A9	V_{OUT}	B9	V_{OUT}	C9	V_{OUT}	D9	GND	E9	GND	F9	PV_{CC}
A10	V_{OUT}	B10	V_{OUT}	C10	V_{OUT}	D10	OVER_TEMP	E10	OVP_TRIP	F10	GND
A11	V_{OUT}	B11	V_{OUT}	C11	V_{OUT}	D11	V_{OUT}	E11	CROWBAR	F11	OTP_SET
A12	V_{OUT}	B12	V_{OUT}	C12	V_{OUT}	D12	V_{OUT}	E12	OVP_SET	F12	GND

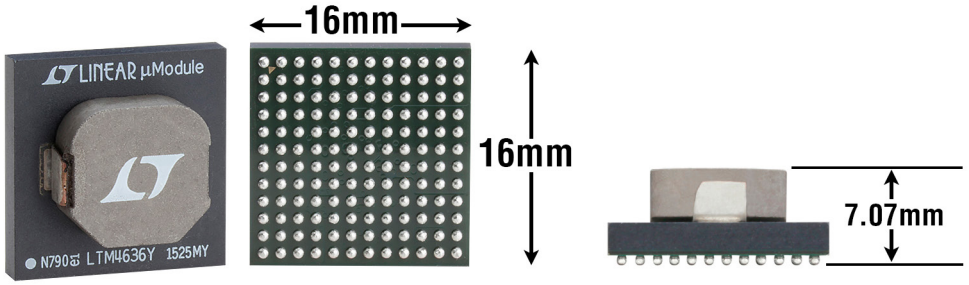
PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	GND	J1	GND	K1	GND	L1	GND	M1	GND
G2	GND	H2	TEST3	J2	GND	K2	GND	L2	GND	M2	GND
G3	CLKOUT	H3	MODE/PLLIN	J3	GND	K3	GND	L3	GND	M3	GND
G4	SGND	H4	TEST1	J4	V_{IN}	K4	V_{IN}	L4	V_{IN}	M4	V_{IN}
G5	FREQ	H5	V_{IN}	J5	V_{IN}	K5	V_{IN}	L5	V_{IN}	M5	V_{IN}
G6	GND	H6	V_{IN}	J6	V_{IN}	K6	V_{IN}	L6	V_{IN}	M6	V_{IN}
G7	PHMODE	H7	PWM	J7	V_{IN}	K7	V_{IN}	L7	V_{IN}	M7	V_{IN}
G8	RUNP	H8	TMON	J8	GND	K8	V_{IN}	L8	V_{IN}	M8	V_{IN}
G9	BIAS	H9	GMON	J9	GND	K9	GND	L9	GND	M9	GND
G10	GND	H10	GND	J10	GND	K10	GND	L10	GND	M10	GND
G11	$TEMP^-$	H11	GND	J11	GND	K11	SW	L11	SW	M11	GND
G12	$TEMP^+$	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND

PACKAGE DESCRIPTION

TOP VIEW



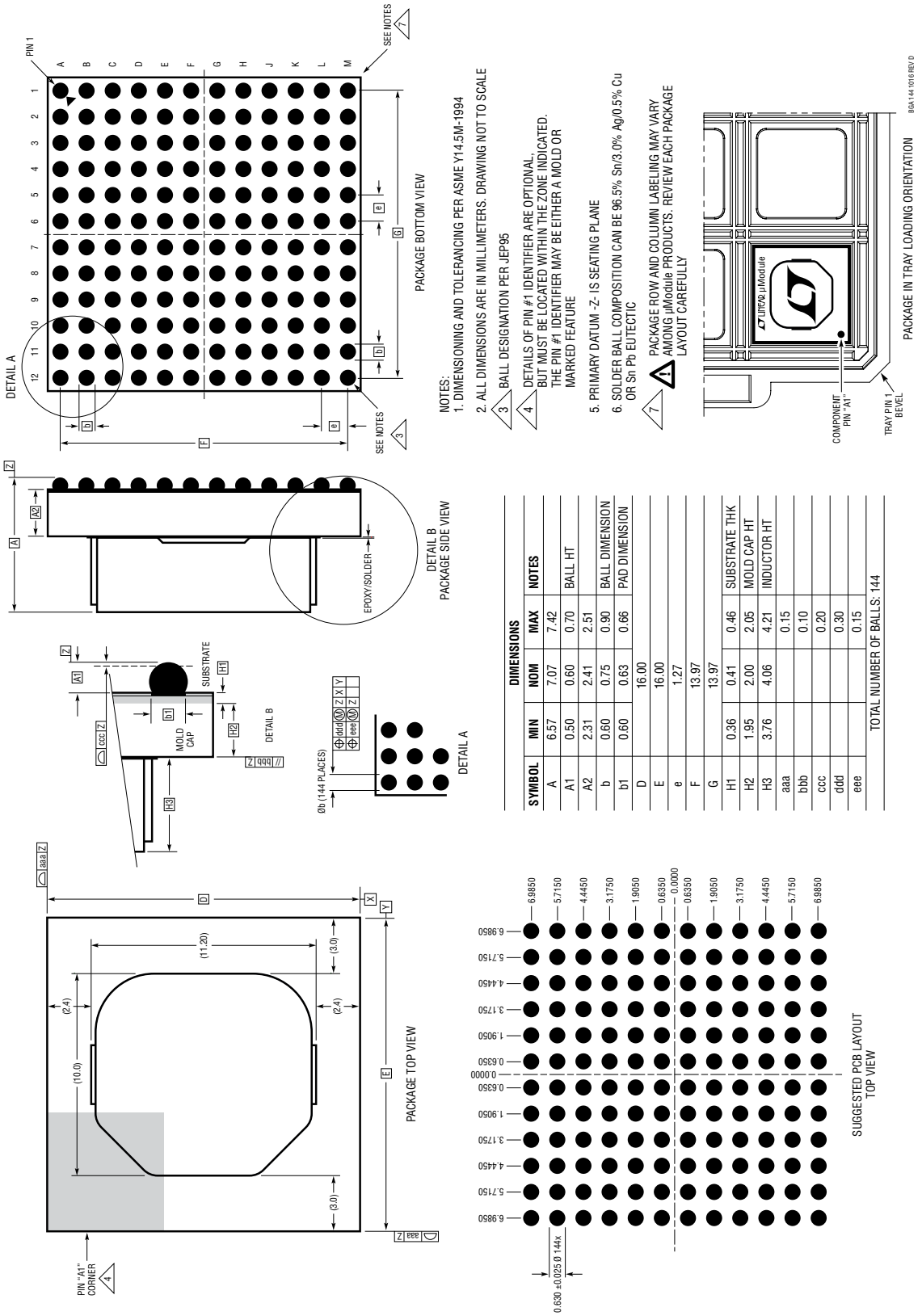
PACKAGE PHOTO



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTM4636-1#packaging for the most recent package drawings.

BGA Package
144-Lead (16mm × 16mm × 7.16mm)
(Reference LTC DWG # 05-08-1937 Rev D)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS. DRAWING NOT TO SCALE
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION CAN BE 96.5% Sn/3.0% Ag/0.5% Cu OR Sn Pb EUTECTIC
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	6.57	7.07	7.42	
A1	0.50	0.60	0.70	BALL HT
A2	2.31	2.41	2.51	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		16.00		
E		16.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.36	0.41	0.46	SUBSTRATE THK
H2	1.95	2.00	2.05	MOLD CAP HT
H3	3.76	4.06	4.21	INDUCTOR HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 144				

46361fa

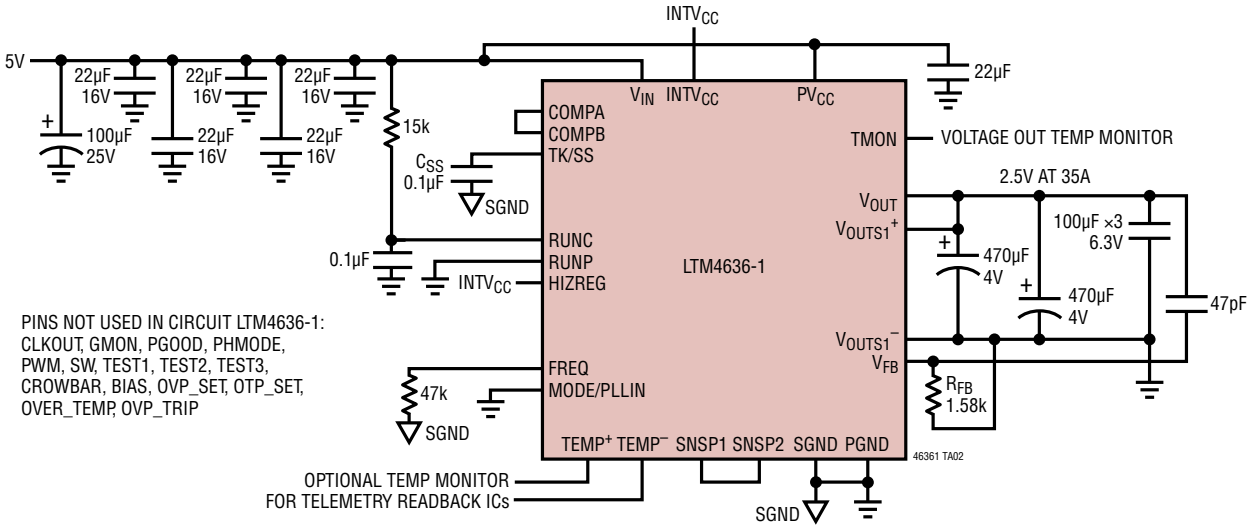
REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/17	Changed Turn-On-Time TYP from 50ms to 750µs	3

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

5V to 2.5V at 30A Design



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search Input V_{in} (Min) V V_{in} (Max) V Output V_{out} V I_{out} A Search	
TechClip Videos	Quick videos detailing how to bench test electrical and thermal performance of µModule products.	
Digital Power System Management	Linear Technology's family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4609	Buck-Boost DC/DC µModule Family	All Pin Compatible; Up to 5A; Up to 36V_{IN}, 34V_{OUT} 15mm × 15mm × 2.82mm
LTM4612	Ultralow Noise High V_{OUT} DC/DC µModule Regulator	5A, 5V ≤ V_{IN} ≤ 36V, 3.3V ≤ V_{OUT} ≤ 15V, 15mm × 15mm × 2.82mm Package
LTM4627	15A DC/DC µModule Regulator	4.5V ≤ V_{IN} ≤ 20V, 0.6V ≤ V_{OUT} ≤ 5V, LGA and BGA Packages
LTM4620	Dual 13A, Single 26A DC/DC µModule Regulator	Up to 100A with Four in Parallel, 4.5V ≤ V_{IN} ≤ 16V, 0.6V ≤ V_{OUT} ≤ 2.5V
LTM4636	LTM4636-1 without Overvoltage/Overtemperature Protection	4.75V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 3.3V, 16mm × 16mm × 7.12mm BGA

LT 1217 REV A • PRINTED IN USA
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