LM5105 100-V Half-Bridge Gate Driver With Programmable Dead Time

1 Features

- Drives Both a High-Side and Low-Side N-Channel MOSFET
- 1.8-A Peak Gate Drive Current
- Bootstrap Supply Voltage Range up to 118-V DC
- Integrated Bootstrap Diode
- Single TTL Compatible Input
- Programmable Turnon Delays (Dead Time)
- Enable Input Pin
- Fast Turnoff Propagation Delays (26 ns Typical)
- Drives 1000 pF With 15-ns Rise and Fall Time
- Supply Rail Undervoltage Lockout
- Low Power Consumption
- Package: Thermally Enhanced 10-Pin WSON (4 mm × 4 mm)

2 Applications

- Solid-State Motor Drives
- Half- and Full-Bridge Power Converters

3 Description

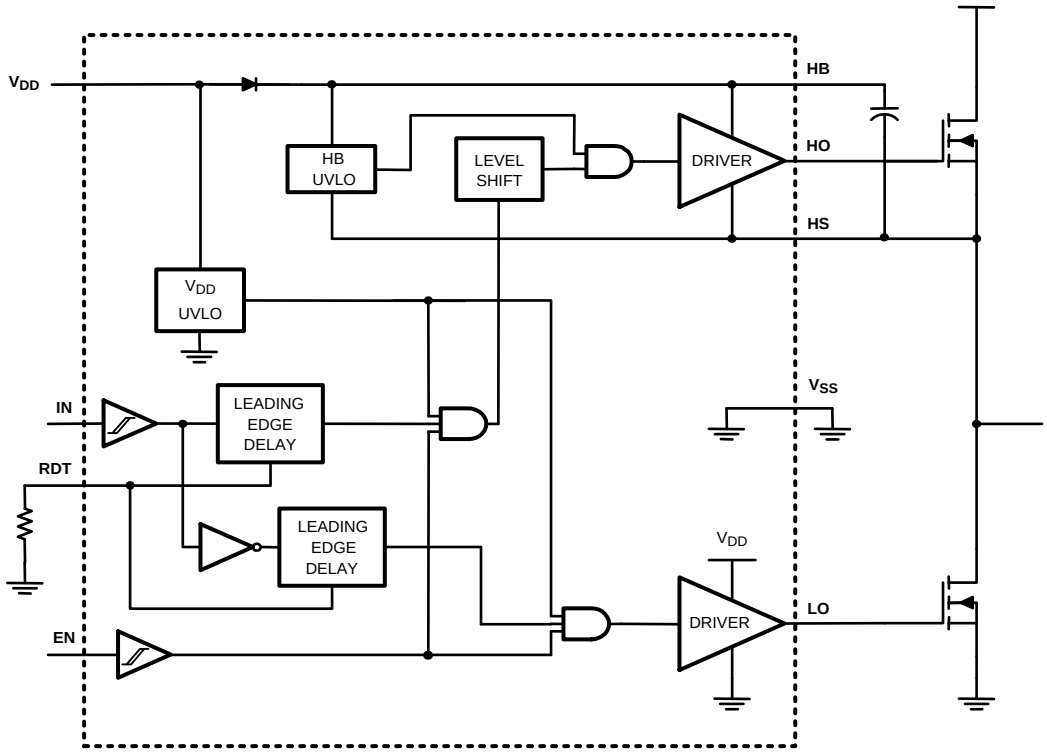
The LM5105 is a high-voltage gate driver designed to drive both the high-side and low-side N–Channel MOSFETs in a synchronous buck or half-bridge configuration. The floating high-side driver is capable of working with rail voltages up to 100 V. The single control input is compatible with TTL signal levels and a single external resistor programs the switching transition dead time through tightly matched turnon delay circuits. A high-voltage diode is provided to charge the high-side gate-drive bootstrap capacitor. The robust level shift technology operates at high speed while consuming low power and provides clean output transitions. Undervoltage lockout disables the gate driver when either the low-side or the bootstrapped high-side supply voltage is below the operating threshold. The LM5105 is offered in the thermally enhanced WSON plastic package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5105	WSON (10)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2016) to Revision E **Page**

- Updated values in the *Thermal Information* table to align with JEDEC standards ... 5

Changes from Revision C (March 2013) to Revision D **Page**

- Added *Device Information* table, *ESD Ratings*, *Detailed Description* section, *Application and Implementation* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

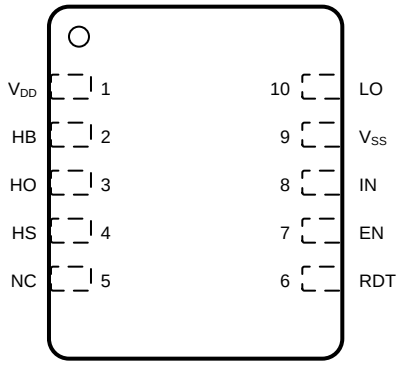
Changes from Revision B (March 2013) to Revision C **Page**

- Changed layout of National Semiconductor Data Sheet to TI format ... 13

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5 Pin Configuration and Functions

DPR Package
10-Pin WSON
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	V_{DD}	P	Positive gate drive supply. Decouple VDD to VSS using a low ESR/ESL capacitor, placed as close to the IC as possible.
2	HB	P	High-side gate driver bootstrap rail. Connect the positive terminal of bootstrap capacitor to the HB pin and connect negative terminal to HS. The Bootstrap capacitor must be placed as close to IC as possible.
3	HO	O	High-side gate driver output. Connect to the gate of high side N-MOS device through a short, low inductance path.
4	HS	P	High-side MOSFET source connection. Connect to the negative terminal of the bootstrap capacitor and to the source of the high side N-MOS device.
5	NC	—	Not connected.
6	RDT	I	Dead-time programming pin. A resistor from RDT to VSS programs the turnon delay of both the high and low side MOSFETs. The resistor must be placed close to the IC to minimize noise coupling from adjacent PCB traces.
7	EN	I	Logic input for driver disable or enable. TTL compatible threshold with hysteresis. LO and HO are held in the low state when EN is low.
8	IN	I	Logic input for gate driver. TTL compatible threshold with hysteresis. The high side MOSFET is turned on and the low side MOSFET turned off when IN is high.
9	V_{SS}	G	Ground return. All signals are referenced to this ground.
10	LO	O	Low-side gate driver output. Connect to the gate of the low side N-MOS device with a short, low inductance path.
—	Exposed Pad	—	It is recommended that the exposed pad on the bottom of the package be soldered to ground plane on the PCB to aid thermal dissipation.

(1) G = Ground, I = Input, O = Output, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
V_{DD} to V_{SS}	–0.3	18	V
HB to HS	–0.3	18	V
IN and EN to V_{SS}	–0.3	V_{DD} + 0.3	V
LO to V_{SS}	–0.3	V_{DD} + 0.3	V
HO to V_{SS}	HS – 0.3	HB + 0.3	V
HS to V_{SS}(3)	−5	100	V
HB to V_{SS}		118	V
RDT to V_{SS}	–0.3	5	V
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage generally does not exceed –1 V. However, in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} – 15 V. For example, if V_{DD} = 10 V, the negative transients at HS must not exceed –5 V.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)(1)(2)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human-body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. Pin 2, Pin 3 and Pin 4 are rated at 500 V.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}		8		14	V
HS(1)		–1		100	V
HB		HS + 8		HS + 14	V
HS	Slew rate			<50	V/ns
T_J	Junction temperature	–40		125	°C

(1) In the application the HS node is clamped by the body diode of the external lower N-MOSFET; therefore, the HS voltage generally does not exceed –1 V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently. If negative transients occur on HS, the HS voltage must never be more negative than V_{DD} – 15 V. For example, if V_{DD} = 10 V, the negative transients at HS must not exceed –5 V.

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6.4 Thermal Information

THERMAL METRIC[1]		LM5105 DPR (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise noted, V_{DD} = HB = 12 V, V_{SS} = HS = 0 V, EN = 5 V, no load on LO or HO, RDT= 100 kΩ[1]. Typical limits are for T_J = 25°C, and minimum and maximum limits apply over the operating junction temperature range (–40°C to 125°C).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{DD}	V_{DD} quiescent current	IN = EN = 0 V		0.34	0.6	mA
I_{DDO}	V_{DD} operating current	f = 500 kHz		1.65	3	mA
I_{HB}	Total HB quiescent current	IN = EN = 0 V		0.06	0.2	mA
I_{HBO}	Total HB operating current	f = 500 kHz		1.3	3	mA
I_{HBS}	HB to V_{SS} current, quiescent	HS = HB = 100 V		0.05	10	µA
I_{HBSO}	HB to V_{SS} current, operating	f = 500 kHz		0.1		mA
INPUT IN AND EN						
V_{IL}	Low-level input voltage threshold		0.8	1.8		V
V_{IH}	High-level input voltage threshold			1.8	2.2	V
R_{pd}	Input pulldown resistance pin IN and EN		100	200	500	kΩ
DEAD-TIME CONTROLS						
VRDT	Nominal voltage at RDT		2.7	3	3.3	V
IRDT	RDT pin current limit	RDT = 0 V	0.75	1.5	2.25	mA
UNDER VOLTAGE PROTECTION						
V_{DDR}	V_{DD} rising threshold		6	6.9	7.4	V
V_{DDH}	V_{DD} threshold hysteresis			0.5		V
V_{HBR}	HB rising threshold		5.7	6.6	7.1	V
V_{HBH}	HB threshold hysteresis			0.4		V
BOOT STRAP DIODE						
V_{DL}	Low-current forward voltage	I_{VDD-HB} = 100 µA		0.6	0.9	V
V_{DH}	High-current forward voltage	I_{VDD-HB} = 100 mA		0.85	1.1	V
R_D	Dynamic resistance	I_{VDD-HB} = 100 mA		0.8	1.5	Ω
LO GATE DRIVER						
V_{OLL}	Low-level output voltage	I_{LO} = 100 mA		0.25	0.4	V
V_{OHL}	High-level output voltage	I_{LO} = –100 mA, $V_{OHL} = V_{DD} - V_{LO}$		0.35	0.55	V
I_{OHL}	Peak pullup current	LO = 0 V		1.8		A
I_{OLL}	Peak pulldown current	LO = 12 V		1.6		A

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

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Electrical Characteristics (continued)

Unless otherwise noted, V_{DD} = HB = 12 V, V_{SS} = HS = 0 V, EN = 5 V, no load on LO or HO, RDT= 100 kΩ(1). Typical limits are for T_J = 25°C, and minimum and maximum limits apply over the operating junction temperature range (–40°C to 125°C).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HO GATE DRIVER						
V_{OLH}	Low-level output voltage	I_{HO} = 100 mA		0.25	0.4	V
V_{OHH}	High-level output voltage	I_{HO} = –100 mA, V_{OHH} = HB – HO		0.35	0.55	V
I_{OHH}	Peak pullup current	HO = 0 V		1.8		A
I_{OLH}	Peak pulldown current	HO = 12 V		1.6		A

6.6 Switching Characteristics

Unless otherwise noted, V_{DD} = HB = 12 , V_{SS} = HS = 0 V, no Load on LO or HO(1). Typical limits are for T_J = 25°C, and minimum and maximum limits apply over the operating junction temperature range (–40°C to 125°C).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{LPHL}	Lower turnoff propagation delay			26	56	ns
t_{HPHL}	Upper turnoff propagation delay			26	56	ns
t_{LPLH}	Lower turnon propagation delay	RDT = 100 k	485	595	705	ns
t_{HPLH}	Upper turnon propagation delay	RDT = 100 k	485	595	705	ns
t_{LPLH}	Lower turnon propagation delay	RDT = 10 k	75	105	150	ns
t_{HPLH}	Upper turnon propagation delay	RDT = 10 k	75	105	150	ns
t_{en}, t_{sd}	Enable and shutdown propagation delay			28		ns
DT1, DT2	Dead-time LO OFF to HO ON and HO OFF to LO ON	RDT = 100 k		570		ns
		RDT = 10 k		80		ns
MDT	Dead-time matching	RDT = 100 k		50		ns
t_R, t_F	Either output rise or fall time	C_L = 1000 pF		15		ns
t_{BS}	Bootstrap diode turnon or turnoff time	I_F = 20 mA, I_R = 200 mA		50		ns

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

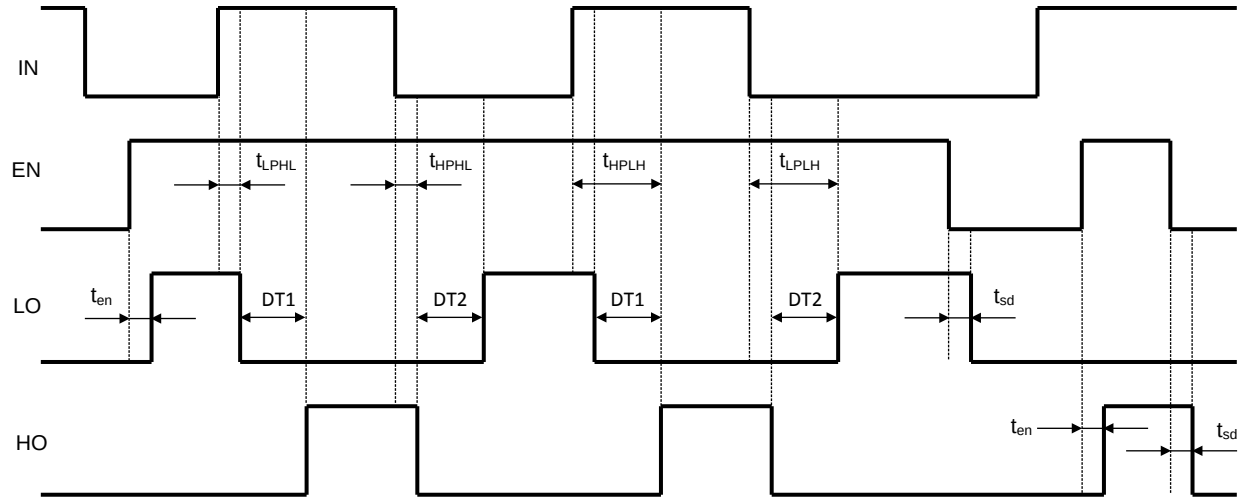


Figure 1. LM5105 Input - Output Waveforms

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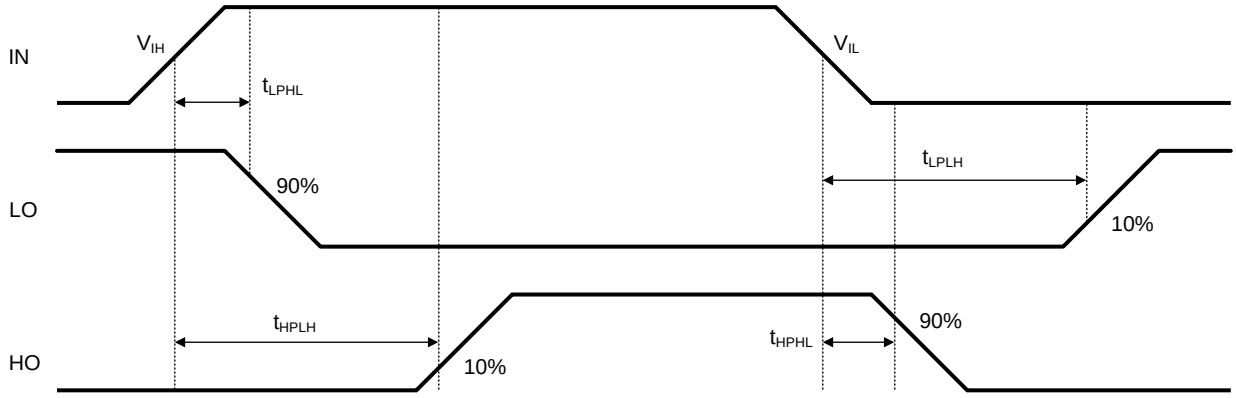


Figure 2. LM5105 Switching Time Definitions: T_{LPLH}, T_{LPHL}, T_{HPLH}, T_{HPHL}

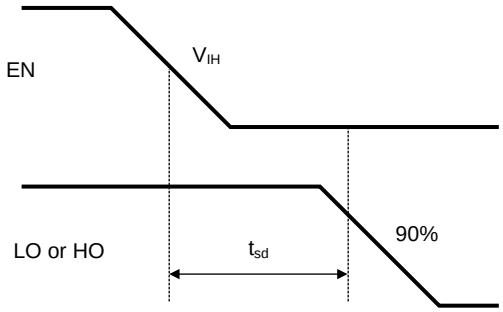


Figure 3. LM5105 Enable: T_{sd}

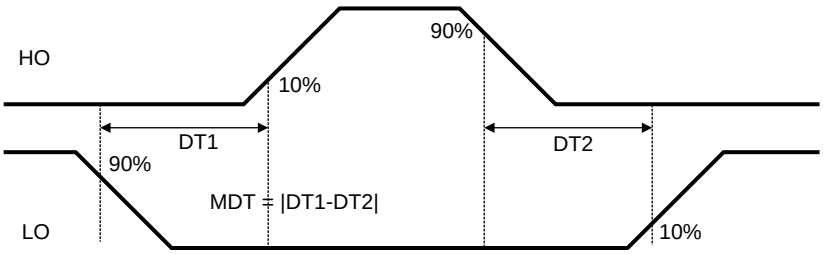


Figure 4. LM5105 Dead-Time: DT

6.7 Typical Characteristics

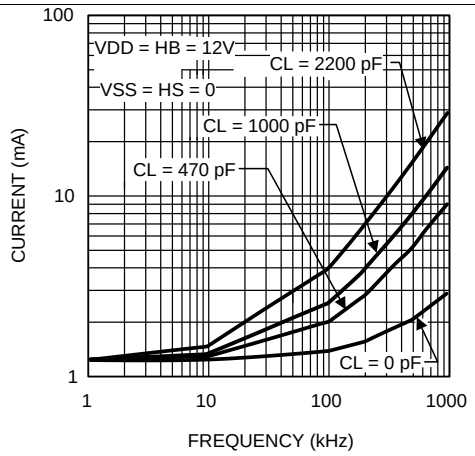


Figure 5. V_{DD} Operating Current vs Frequency

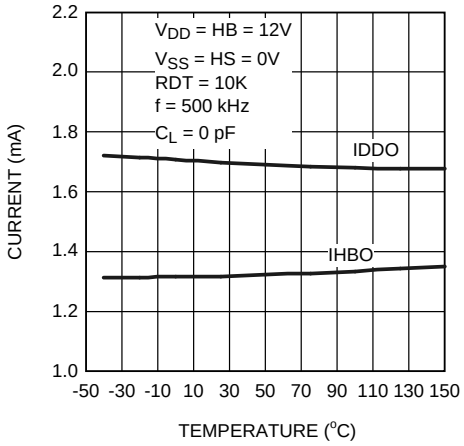


Figure 6. Operating Current vs Temperature

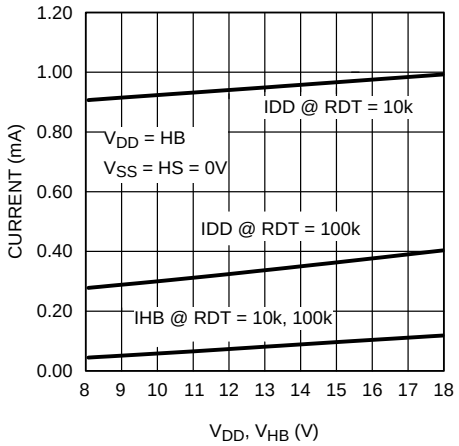


Figure 7. Quiescent Current vs Supply Voltage

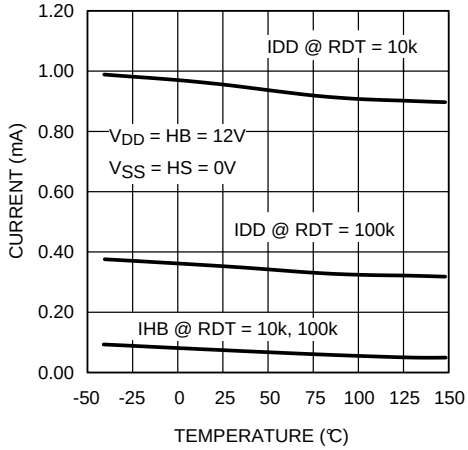


Figure 8. Quiescent Current vs Temperature

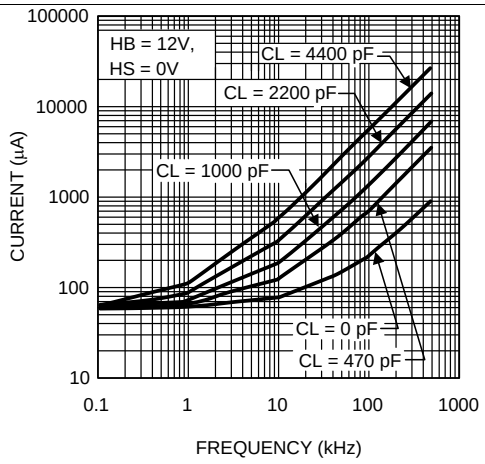


Figure 9. HB Operating Current vs Frequency

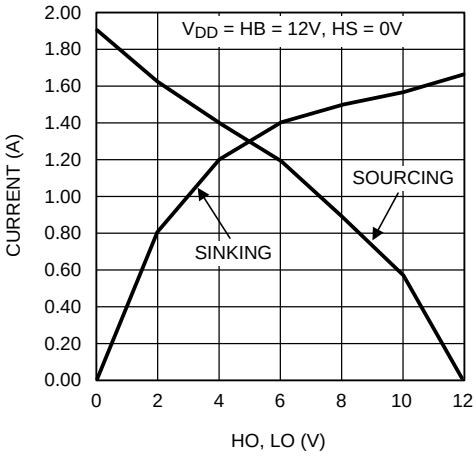


Figure 10. HO & LO Peak Output Current vs Output Voltage

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Typical Characteristics (continued)

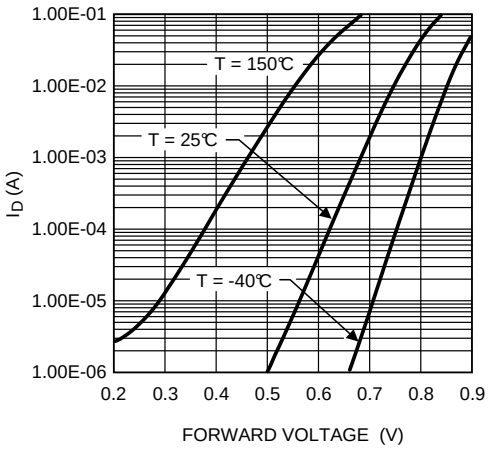


Figure 11. Diode Forward Voltage

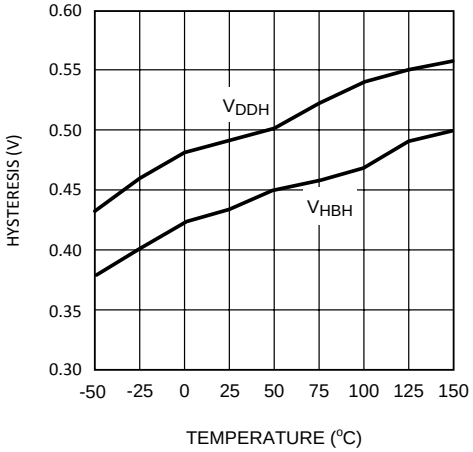


Figure 12. Undervoltage Hysteresis vs Temperature

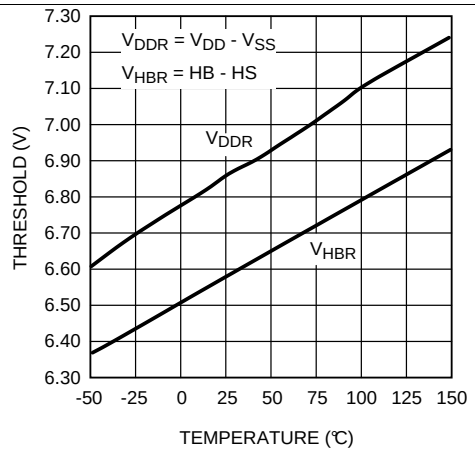


Figure 13. Undervoltage Rising Threshold vs Temperature

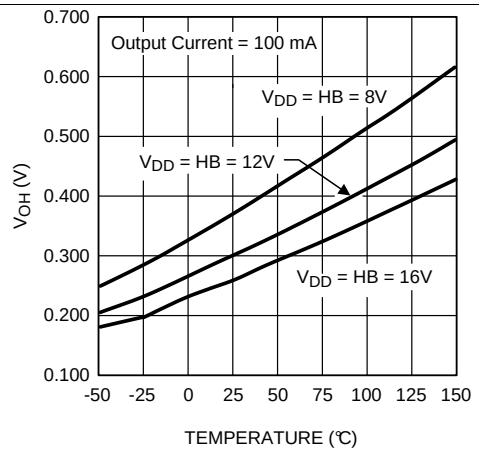


Figure 14. LO & HO High-Level Output Voltage vs Temperature

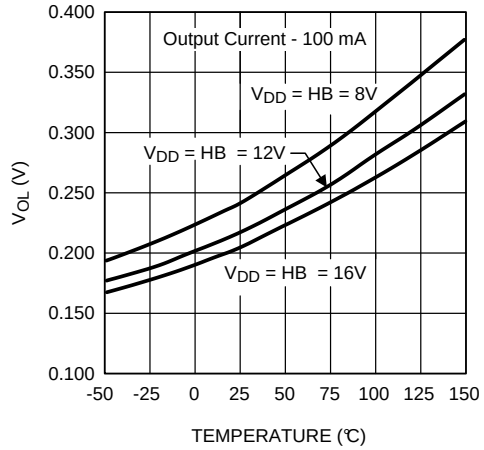


Figure 15. LO & HO Low-Level Output Voltage vs Temperature

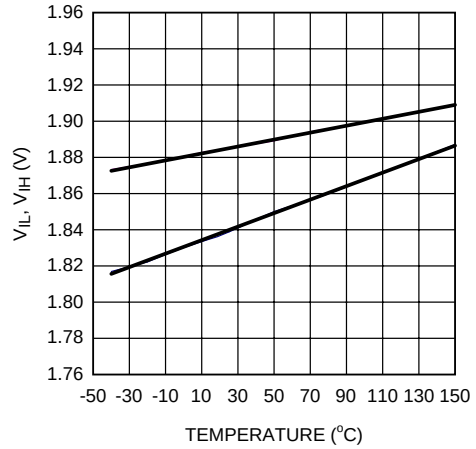


Figure 16. Input Threshold vs Temperature

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Typical Characteristics (continued)

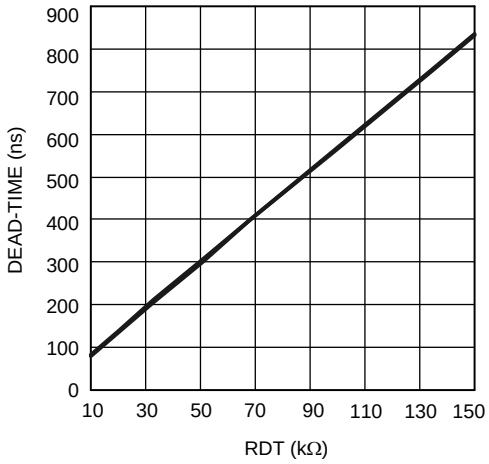


Figure 17. Dead-Time vs RT Resistor Value

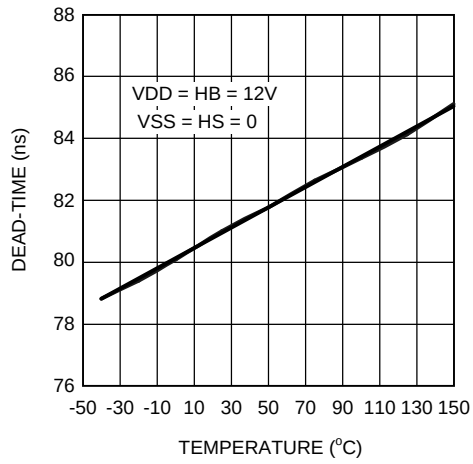


Figure 18. Dead-Time vs Temperature (RT = 10 k)

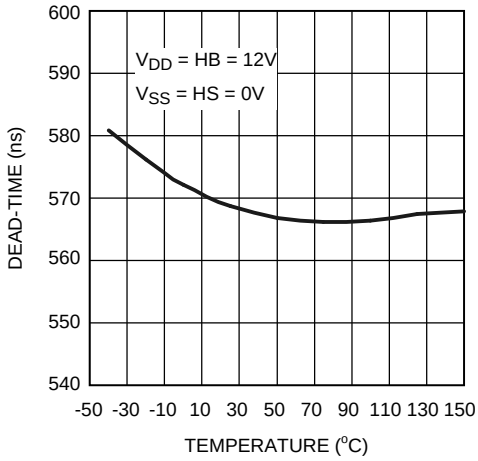


Figure 19. Dead-Time vs Temperature (RT = 100 k)

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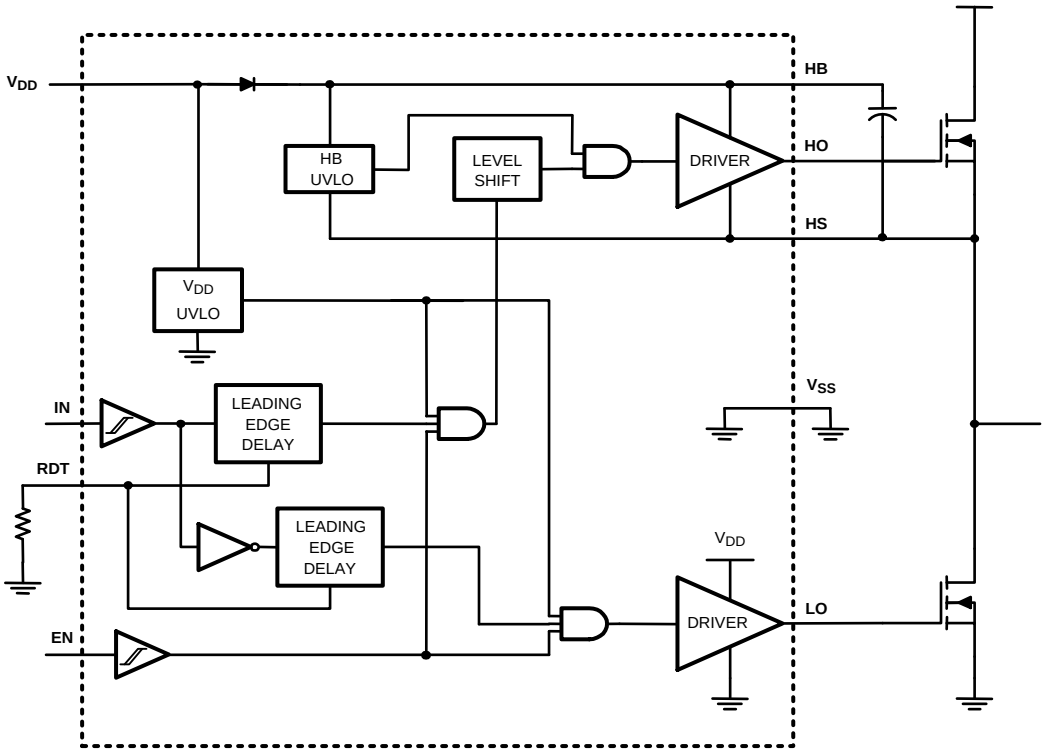
7 Detailed Description

7.1 Overview

The LM5105 is a single PWM input Gate Driver with Enable that offers a programmable dead time. The dead time is set with a resistor at the RDT pin and can be adjusted from 100 ns to 600 ns. The wide dead-time programming range provides the flexibility to optimize drive signal timing for a wide range of MOSFETS and applications.

The RDT pin is biased at 3 V and current-limited to 1-mA maximum programming current. The time delay generator accommodates resistor values from 5 k to 100 k with a dead time that is proportional to the RDT resistance. Grounding the RDT pin programs the LM5105 to drive both outputs with minimum dead time.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Start-Up and UVLO

Both top and bottom drivers include undervoltage lockout (UVLO) protection circuitry, which monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (HB – HS) independently. The UVLO circuit inhibits each driver until sufficient supply voltage is available to turn on the external MOSFETs, and the UVLO hysteresis prevents chattering during supply voltage transitions. When the supply voltage is applied to the V_{DD} pin of LM5105, the top and bottom gates are held low until V_{DD} exceeds the UVLO threshold, typically about 6.9 V. Any UVLO condition on the bootstrap capacitor disables only the high-side output (HO).

7.4 Device Functional Modes

Table 1 lists the functional modes for LM5105.

Table 1. Function Table

EN	IN PIN	LO PIN	HO PIN
L	Any	L	L
H	H	L	H
H	L	H	L

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8 Application and Implementation

NOTE

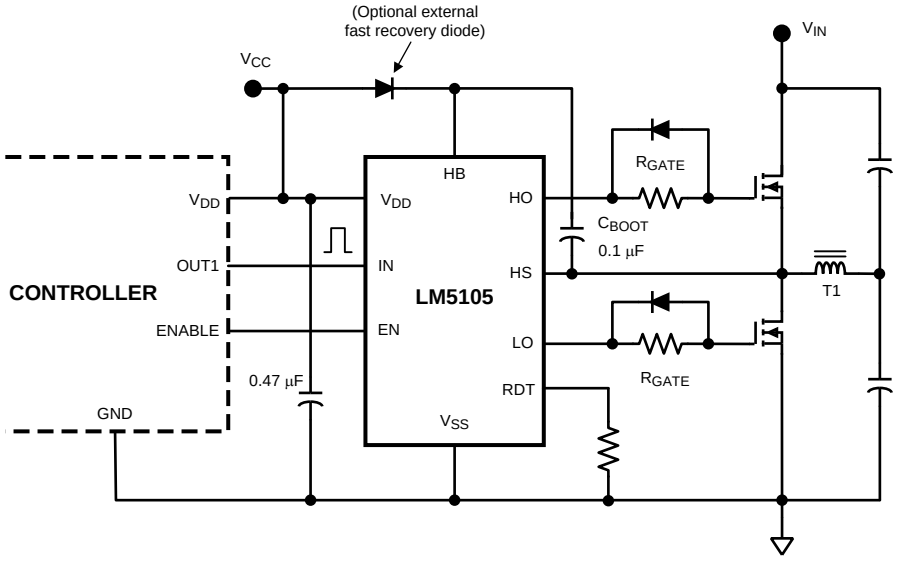
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5105 is one of the latest generation of high-voltage gate drivers which are designed to drive both the high-side and low-side N-channel MOSFETs in a half-bridge or full-bridge configuration or in a synchronous buck circuit. The floating high-side driver can operate with supply voltages up to 110 V. This allows for N-channel MOSFET control in half-bridge, full-bridge, push-pull, two-switch forward, and active clamp topologies.

The outputs of the LM5105 are controlled from a single input. The rising edge of each output can be delayed with a programming resistor.

8.2 Typical Application



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Figure 20. LM5105 Driving MOSFETS Connected in Half-Bridge Configuration

8.2.1 Design Requirements

Table 2 lists the design parameters for this application example.

Table 2. Design Parameters

PARAMETER	VALUE
Gate Drive IC	LM5105
Mosfet	CSD18531Q5A
V_{DD}	10 V
Q_{gmax}	43 nC
F_{sw}	100 kHz
D_{Max}	95%
I_{HBS}	10 µA
V_{DH}	1.1 V

Table 2. Design Parameters (continued)

PARAMETER	VALUE
V_{HBR}	7.1 V
V_{HBH}	0.4 V

8.2.2 Detailed Design Procedure

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL}$$

where

- V_{DD} = Supply voltage of the gate drive IC
- V_{DH} = Bootstrap diode forward voltage drop
- V_{gsmin} = Minimum gate source threshold voltage (1)

$$C_{BOOT} = \frac{Q_{TOTAL}}{\Delta V_{HB}} \quad (2)$$

$$Q_{TOTAL} = Q_{gmax} + I_{HBS} \times \frac{D_{Max}}{F_{SW}} \quad (3)$$

The quiescent current of the bootstrap circuit is 10 µA, which is negligible compared to the Qgs of the MOSFET.

$$Q_{TOTAL} = 43nC + 10\mu A \times \frac{0.95}{100kHz} \quad (4)$$

$$Q_{TOTAL} = 43.01\ nC \quad (5)$$

In practice the value for the C_{BOOT} capacitor should be greater than that calculated to allow for situations where the power stage may skip pulse due to load transients. In this circumstance the boot capacitor must maintain the HB pin voltage above the UVLO voltage for the HB circuit.

As a general rule the local V_{DD} bypass capacitor should be 10 times greater than the calculated value of C_{BOOT}.

$$V_{HBL} = V_{HBR} - V_{HBH} \quad (6)$$

$$V_{HBL} = 6.7\ V \quad (7)$$

$$\Delta V_{HB} = 10\ V - 1.1\ V - 6.7\ V \quad (8)$$

$$\Delta V_{HB} = 2.2\ V \quad (9)$$

$$C_{BOOT} = 43.01nc / 2.2\ V \quad (10)$$

$$C_{BOOT} = 19.6\ nF \quad (11)$$

In practice, the value of C_{Boot} is greater than the calculated value. This allows for the capacitance shift caused by the DC bias voltage and for situations where the power stage would otherwise skip pulses due to load transients. Therefore, it is recommended to include a safety-related margin in the C_{Boot} value and place it as close to the VDD and VSS pins as possible. A 50-V, 0.1-µF capacitor is chosen in this example.

The bootstrap and bias capacitors should be ceramic types with X7R dielectric. The voltage rating should be twice that of the maximum VDD to allow for loss of capacitance once the devices have a DC bias voltage across them and to ensure long-term reliability of the devices.

The resistor values, RT, for setting turnon delay can be found in Figure 17.

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8.2.3 Application Curves

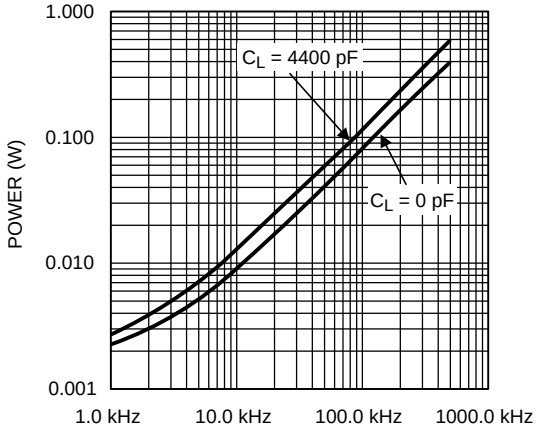


Figure 21. Diode Power Dissipation, V_{IN} = 80 V

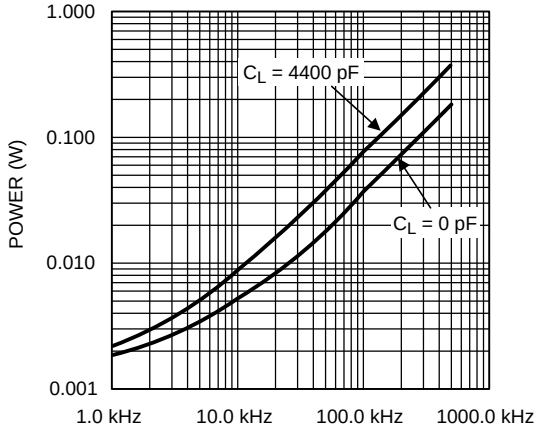


Figure 22. Diode Power Dissipation, V_{IN} = 40 V

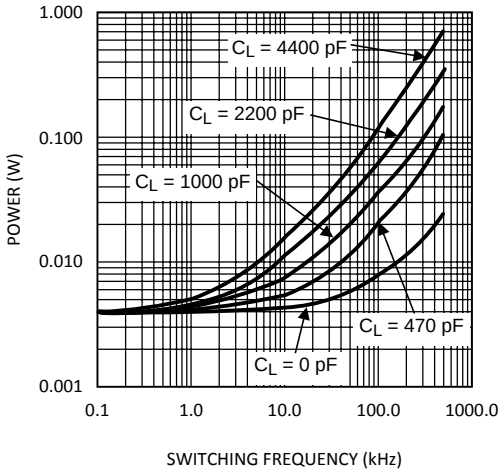


Figure 23. Gate Driver Power Dissipation (LO + HO)
V_{CC} = 12 V, Neglecting Diode Losses

9 Power Supply Recommendations

9.1 Power Dissipation Considerations

The total IC power dissipation is the sum of the gate driver losses and the bootstrap diode losses. The gate driver losses are related to the switching frequency (f), output load capacitance on LO and HO (C_L), and supply voltage (V_{DD}) and can be roughly calculated with Equation 12.

$$P_{DGATES} = 2 \times f \times C_L \times V_{DD}^2 \quad (12)$$

There are some additional losses in the gate drivers due to the internal CMOS stages used to buffer the LO and HO outputs. Figure 23 shows the measured gate driver power dissipation versus frequency and load capacitance. At higher frequencies and load capacitance values, the power dissipation is dominated by the power losses driving the output loads and agrees well with the previous equation. Figure 23 can be used to approximate the power losses due to the gate drivers.

9.2 HS Transient Voltages Below Ground

The HS node is always clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than –0.3 V below HS can activate parasitic transistors resulting in excessive current flow from the HB supply, possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible in order to be effective.
2. HB to HS operating voltage should be 14 V or less. Hence, if the HS pin transient voltage is –5 V, VDD should be ideally limited to 9 V to keep HB to HS below 14 V.
3. Low ESR bypass capacitors from HB to HS and from VCC to VSS are essential for proper operation. The capacitor should be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any inductances in series with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

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10 Layout

10.1 Layout Guidelines

The optimum performance of high- and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. Following points are emphasized.

1. A low ESR or ESL capacitor must be connected close to the IC, and between V_{DD} and V_{SS} pins and between HB and HS pins to support high peak currents being drawn from V_{DD} during turnon of the external MOSFET.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor must be connected between MOSFET drain and ground (V_{SS}).
3. To avoid large negative transients on the switch node (HS) pin, the parasitic inductances in the source of top MOSFET and in the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
   - The first priority in designing grounding connections is to confine the high peak currents from charging and discharging the MOSFET gate in a minimal physical area. This decreases the loop inductance and minimize noise issues on the gate terminal of the MOSFET. The MOSFETs must be placed as close as possible to the gate driver.
   - The second high current path includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor and low side MOSFET body diode. The bootstrap capacitor is recharged on the cycle-by-cycle basis through the bootstrap diode from the ground referenced V_{DD} bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.
5. The resistor on the RDT pin must be placed very close to the IC and separated from high current paths to avoid noise coupling to the time delay generator which could disrupt timer operation.

10.2 Layout Example

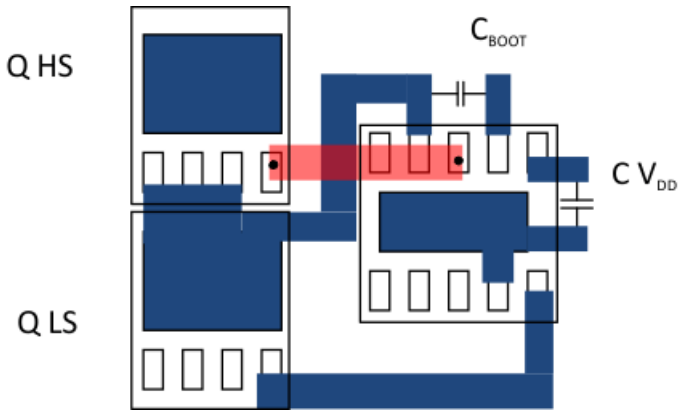


Figure 24. Component Placement

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

AN-1187 Leadless Leadframe Package (LLP) (SNOA401)

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5105SD/NOPB	ACTIVE	WSON	DPR	10	1000	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5105SD	Samples
LM5105SDX/NOPB	ACTIVE	WSON	DPR	10	4500	Green (RoHS & no Sb/Br)	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L5105SD	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

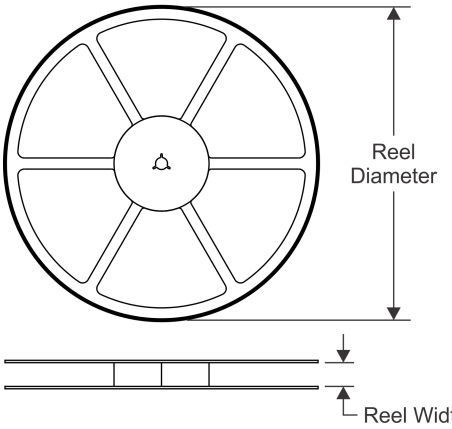
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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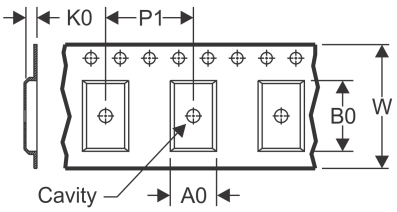
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

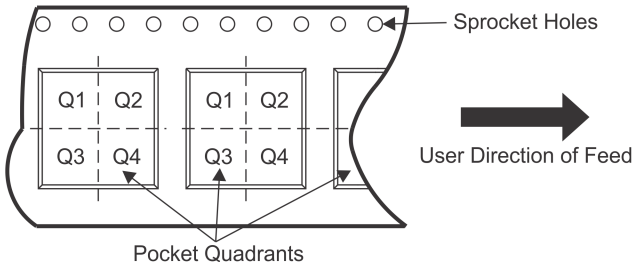


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

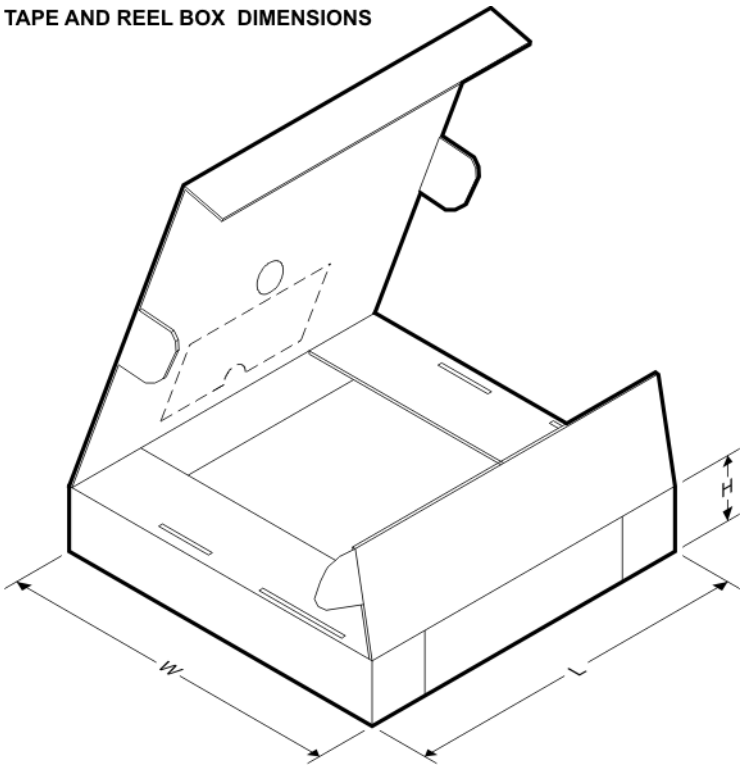
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5105SD/NOPB	WSON	DPR	10	1000	180.0	12.4	4.3	4.3	1.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5105SD/NOPB	WSON	DPR	10	1000	203.0	203.0	35.0

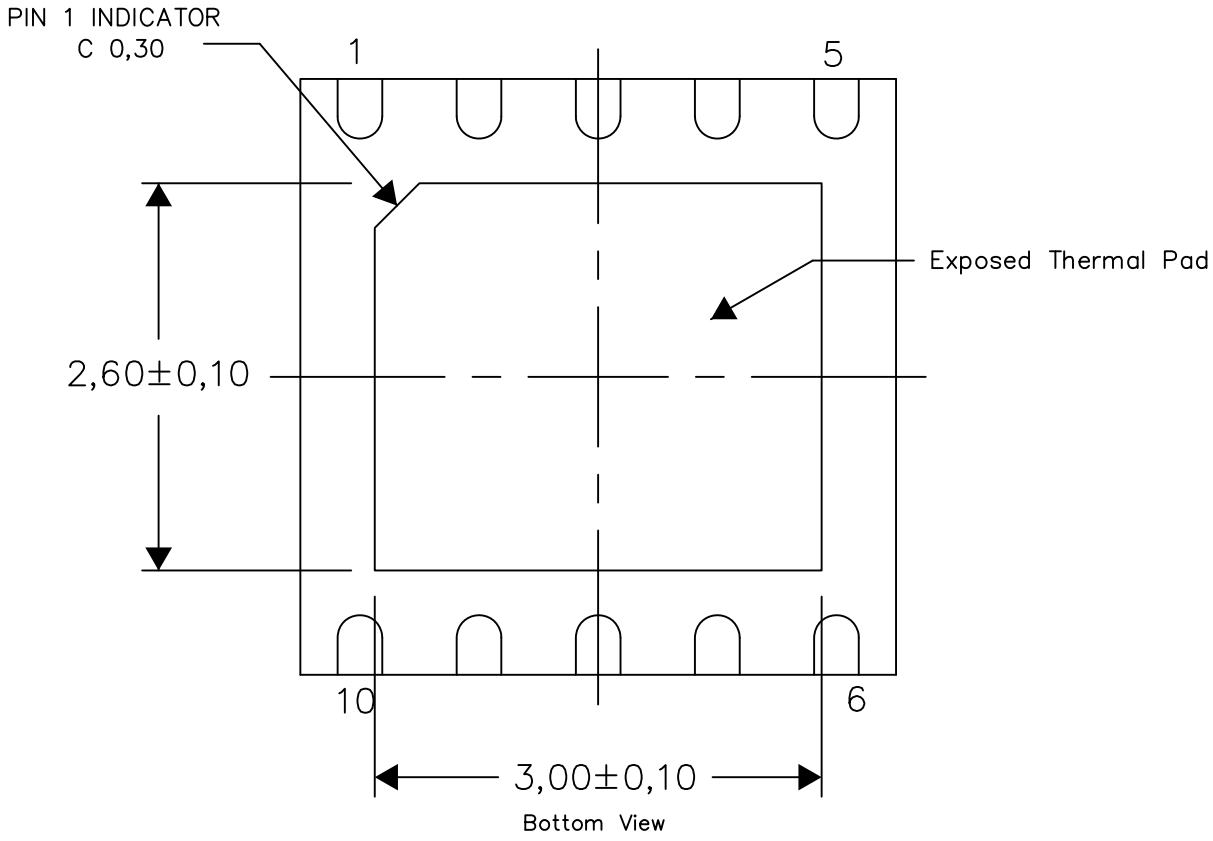
DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

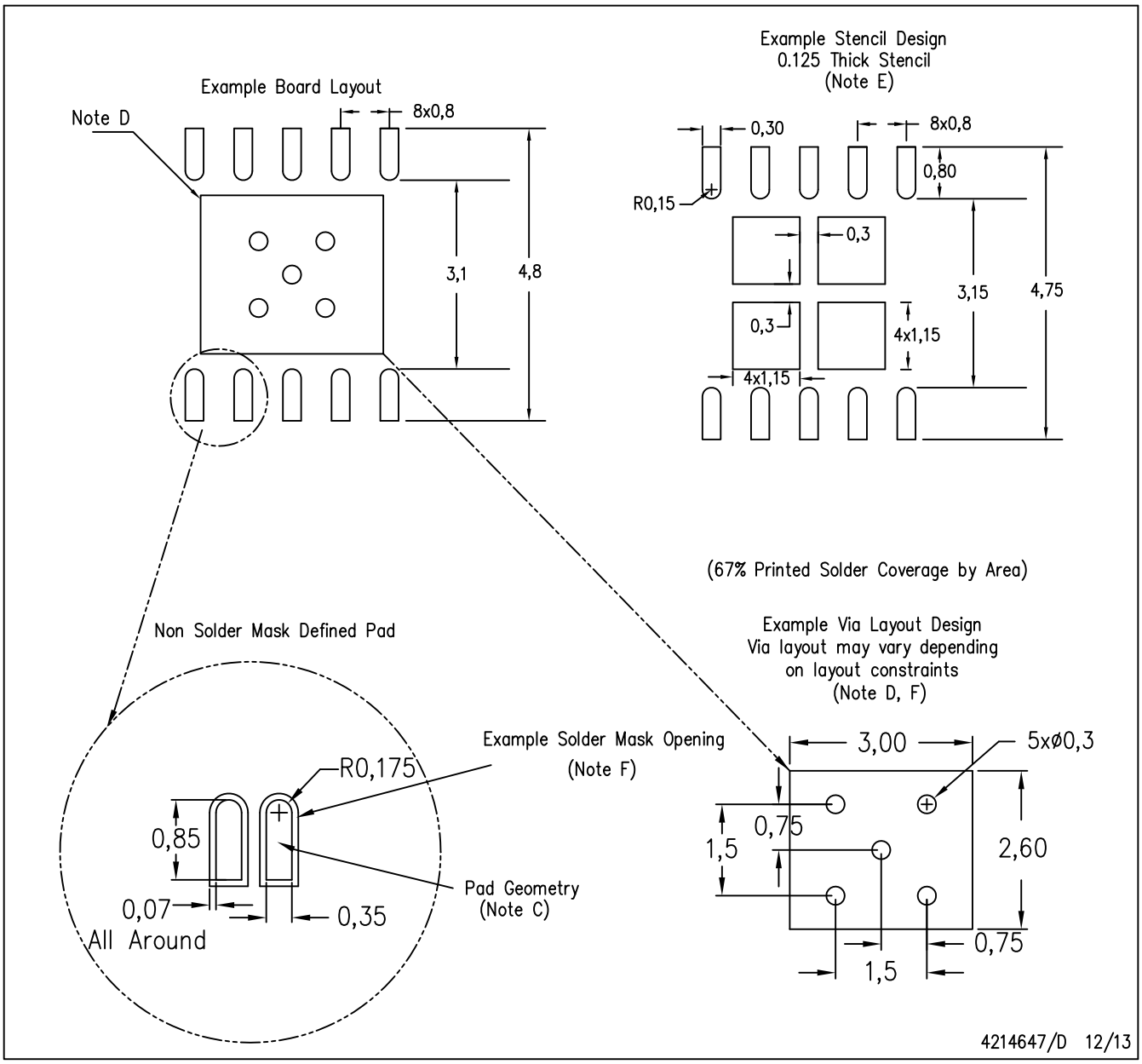


Exposed Thermal Pad Dimensions

4211551/C 12/13

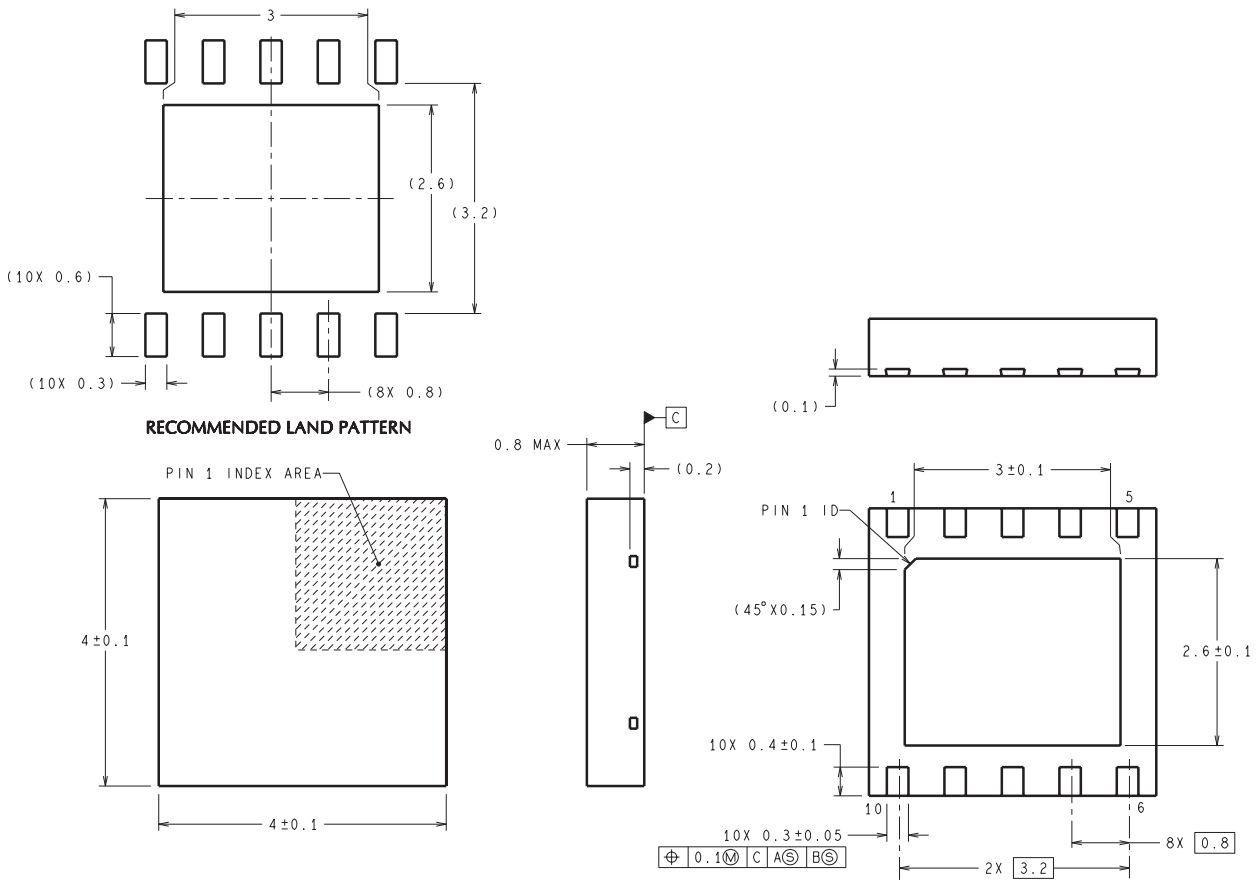
NOTES: All linear dimensions are in millimeters

DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DPR0010A



DIMENSIONS ARE IN MILLIMETERS

SDC10A (Rev A)

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