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FDY3000NZ

Dual N-Channel 2.5V Specified PowerTrench® MOSFET

General Description

This Dual N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced PowerTrench process to optimize the $R_{DS(ON)}$ @ $V_{GS} = 2.5V$.

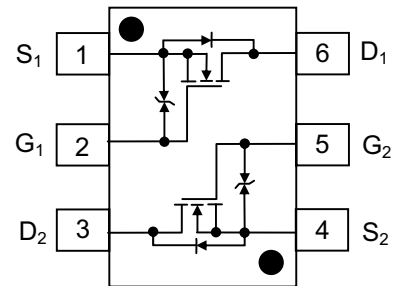
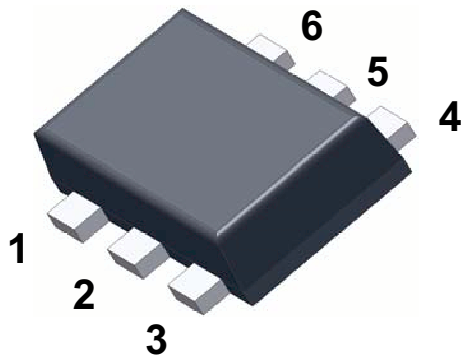
Applications

- Li-Ion Battery Pack



Features

- 600 mA, 20 V $R_{DS(ON)} = 700\text{ m}\Omega$ @ $V_{GS} = 4.5\text{ V}$
 $R_{DS(ON)} = 850\text{ m}\Omega$ @ $V_{GS} = 2.5\text{ V}$
- ESD protection diode (note 3)
- RoHS Compliant



Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous (Note 1a) – Pulsed	600	mA
		1000	
P_D	Power Dissipation (Steady State) (Note 1a) (Note 1b)	625	mW
		446	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	200	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	280	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
C	FDY3000NZ	7"	8 mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

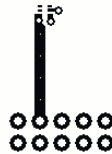
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		14		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 16 V, V _{GS} = 0 V			1	μA
I _{GSS}	Gate–Body Leakage,	V _{GS} = ± 12 V, V _{DS} = 0 V			± 10	μA
		V _{GS} = ± 4.5 V, V _{DS} = 0 V			± 1	μA
On Characteristics (Note 2)						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	0.6	1.0	1.3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		– 3		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 4.5 V, I _D = 600 mA V _{GS} = 2.5 V, I _D = 500 mA V _{GS} = 1.8 V, I _D = 150 mA V _{GS} = 4.5 V, I _D =600mA, T _J = 125°C		0.25 0.37 0.73 0.35	0.70 0.85 1.25 1.00	Ω
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 600 mA		1.8		S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 10 V, V _{GS} = 0 V, f = 1.0 MHz		60		pF
C _{oss}	Output Capacitance			20		pF
C _{rss}	Reverse Transfer Capacitance			10		pF
Switching Characteristics (Note 2)						
t _{d(on)}	Turn–On Delay Time	V _{DD} = 10 V, I _D = 1 A, V _{GS} = 4.5 V, R _{GEN} = 6 Ω		6	12	ns
t _r	Turn–On Rise Time			8	16	ns
t _{d(off)}	Turn–Off Delay Time			8	16	ns
t _f	Turn–Off Fall Time			2.4	4.8	ns
Q _g	Total Gate Charge	V _{DS} = 10 V, I _D = 600 mA, V _{GS} = 4.5 V		0.8	1.1	nC
Q _{gs}	Gate–Source Charge			0.16		nC
Q _{gd}	Gate–Drain Charge			0.26		nC
Drain–Source Diode Characteristics and Maximum Ratings						
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 150 mA (Note 2)		0.7	1.2	V
t _{rr}	Diode Reverse Recovery Time	I _F = 600 mA,		8		nS
Q _{rr}	Diode Reverse Recovery Charge	di _F /dt = 100 A/μs		1		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design



- a) 200°C/W when mounted on a 1 in^2 pad of 2 oz copper



- b) 280°C/W when mounted on a minimum pad of 2 oz copper
Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < $300\mu\text{s}$,
Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics

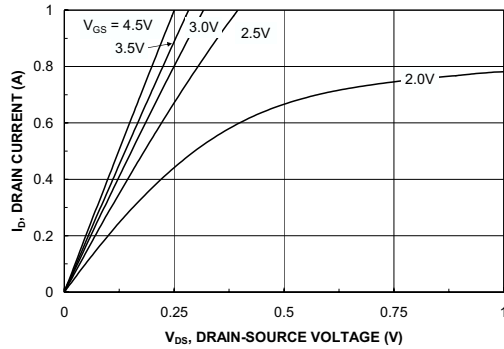


Figure 1. On-Region Characteristics.

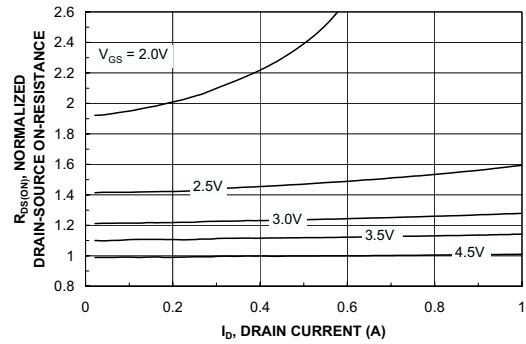


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

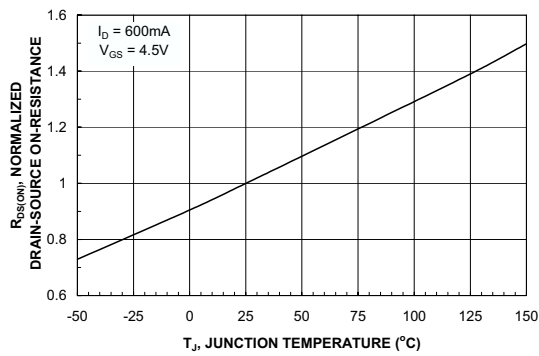


Figure 3. On-Resistance Variation with Temperature.

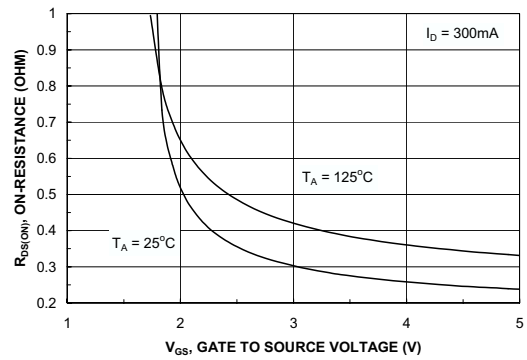


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

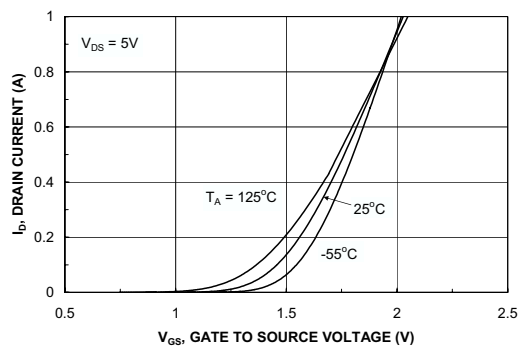


Figure 5. Transfer Characteristics.

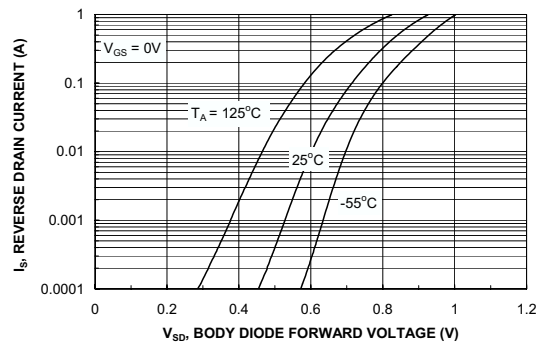


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

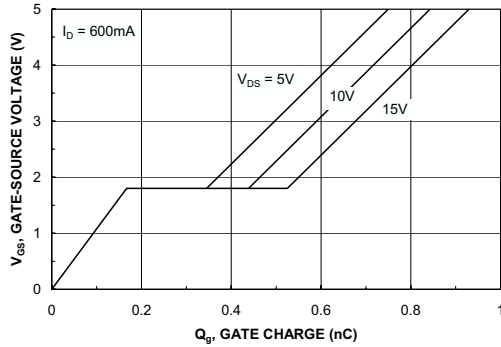


Figure 7. Gate Charge Characteristics.

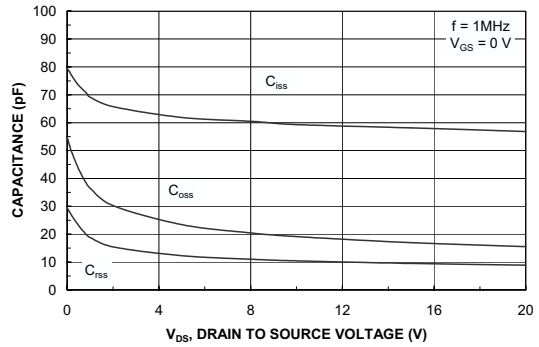


Figure 8. Capacitance Characteristics.

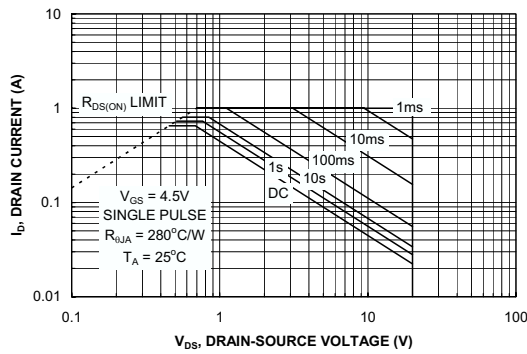


Figure 9. Maximum Safe Operating Area.

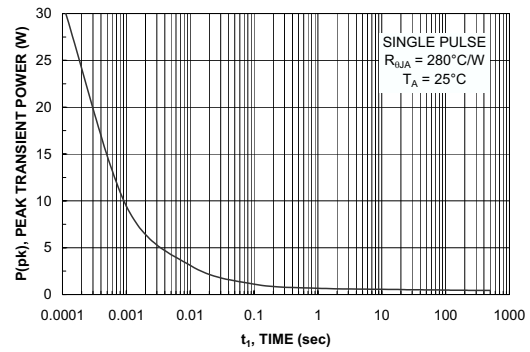


Figure 10. Single Pulse Maximum Power Dissipation.

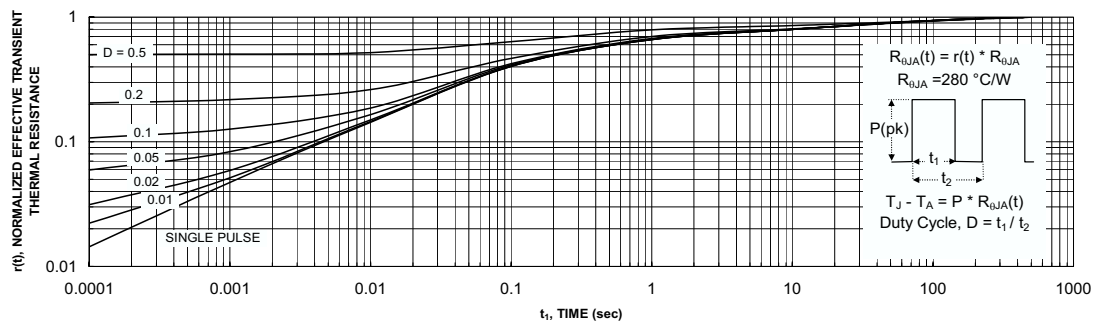
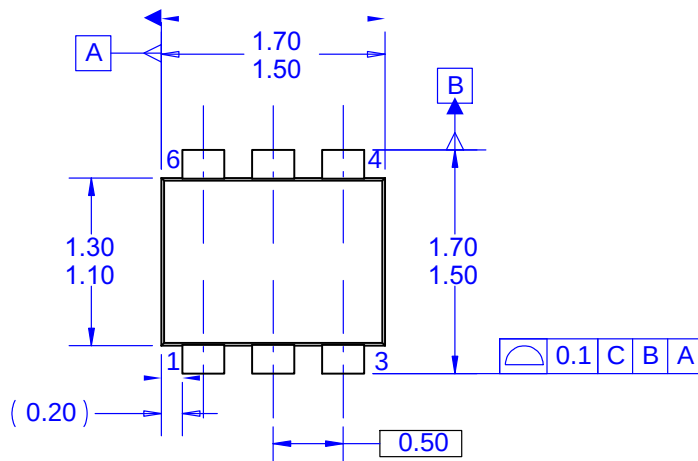


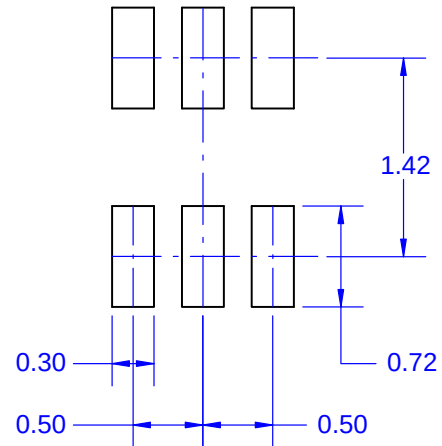
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

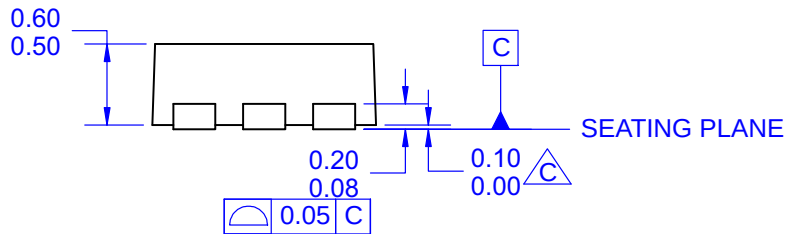
SOT-563
CASE 419BH
ISSUE O



TOP VIEW



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED.

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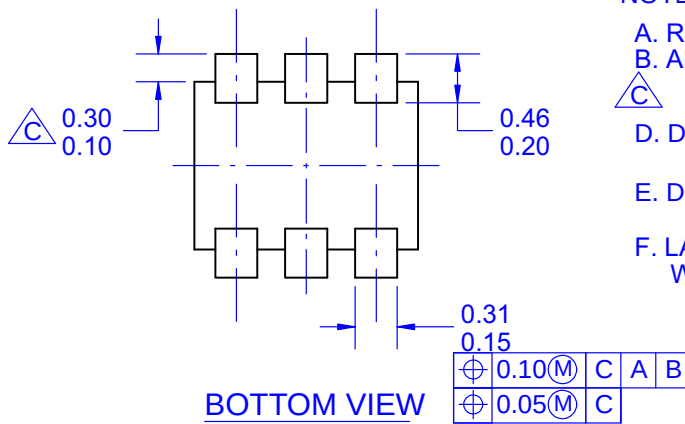
B. ALL DIMENSIONS ARE IN MILLIMETERS.

$\triangle C$ DOES NOT COMPLY JEDEC STANDARD VALUE

D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSION.

E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.

F. LANDPATTERN RECOMMENDATION GENERATED WITH IPC LANDPATTERN GENERATOR



BOTTOM VIEW

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