GaAs, pHEMT, MMIC, Single Positive Supply, DC to 10 GHz Power Amplifier

Data Sheet **ADPA9002**

FEATURES

- OP1dB: 29 dBm typical
- Gain: up to 15 dB typical
- OIP3: up to 43 dBm typical
- Self biased at V_{DD} = 12 V at 385 mA typical with an optional bias control on V_{GG1} for I_{DQ} adjustment
- 50 Ω matched input/output
- 32-lead, 5 mm × 5 mm LFCSP

APPLICATIONS

- Military and space
- Test instrumentation

FUNCTIONAL BLOCK DIAGRAM

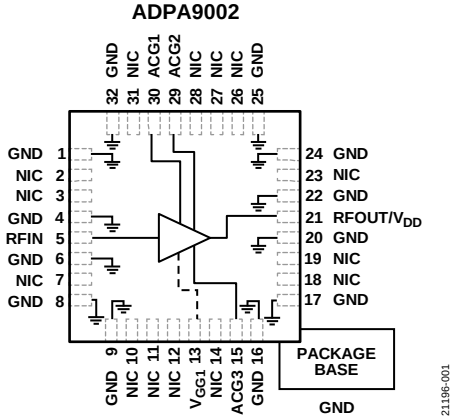


Figure 1.

GENERAL DESCRIPTION

The ADPA9002 is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), power amplifier that operates between dc and 10 GHz. The amplifier provides 15 dB of gain, 42 dBm of OIP3, and 31.5 dBm of saturated output power (P_{SAT}) while requiring 385 mA from a 12 V supply. The ADPA9002 is self biased in normal operation and has an optional bias control for supply quiescent current (I_{DQ}) adjustment. The amplifier is ideal for military and space and test equipment applications. The ADPA9002 also features inputs and outputs that are internally matched to 50 Ω, housed in a RoHS compliant, 5 mm × 5 mm LFCSP premolded cavity package, making it compatible with high volume surface-mount technology (SMT) assembly equipment.

Note that throughout this data sheet, multifunction pins, such as RFOUT/V_{DD}, are referred to either by the entire pin name or by a single function of the pin, for example, V_{DD}, when only that function is relevant.

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
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REVISION HISTORY

10/2019—Revision 0: Initial Version

SPECIFICATIONS

DC TO 2 GHz

T_A = 25°C, V_{DD} = 12 V, I_{DQ} = 385 mA, V_{GG1}= GND for nominal self biased operation, and frequency range = dc to 2 GHz, with a 50 Ω matched input and output, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		DC		2	GHz	
GAIN		12.5	14.5		dB	
Gain Variation Over Temperature			±0.01		dB/°C	
NOISE FIGURE			5		dB	
RETURN LOSS						
Input			18		dB	
Output			14		dB	
OUTPUT						
Output Power for 1 dB Compression	OP1dB	27	29		dBm	
Saturated Output Power	P_{SAT}		31		dBm	
Output Third-Order Intercept	OIP3		43		dBm	Measurement taken at output power (P_{OUT}) per tone = 14 dBm
SUPPLY						
Quiescent Current	I_{DQ}		385		mA	For external bias control, adjust V_{GG1} between −2 V and +0.5 V to achieve the desired I_{DQ}
Drain Voltage	V_{DD}	10	12	15	V	

2 GHz TO 5 GHz

T_A = 25°C, V_{DD} = 12 V, I_{DQ} = 385 mA, V_{GG1} = GND for nominal self biased operation, and frequency range = 2 GHz to 5 GHz, unless otherwise noted. 50 Ω matched input/output.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		2		5	GHz	
GAIN		13	15		dB	
Gain Variation Over Temperature			±0.008		dB/°C	
NOISE FIGURE			3		dB	
RETURN LOSS						
Input			14		dB	
Output			15		dB	
OUTPUT						
Output Power for 1 dB Compression	OP1dB	27	29		dBm	
Saturated Output Power	P_{SAT}		31.5		dBm	
Output Third-Order Intercept	OIP3		42		dBm	Measurement taken at P_{OUT} per tone = 14 dBm
SUPPLY						
Quiescent Current	I_{DQ}		385		mA	For external bias control, adjust V_{GG1} between −2 V and +0.5 V to achieve the desired I_{DQ}
Drain Voltage	V_{DD}	10	12	15	V	

5 GHz TO 10 GHz

T_A = 25°C, V_{DD} = 12 V, I_{DQ} = 385 mA, V_{GG1} = GND for nominal self biased operation, and frequency range = 5 GHz to 10 GHz, with a 50 Ω matched input and output, unless otherwise noted.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		5		10	GHz	
GAIN		13.5	15.5		dB	
Gain Variation Over Temperature			±0.016		dB/°C	
NOISE FIGURE			4		dB	
RETURN LOSS						
Input			19		dB	
Output			13		dB	
OUTPUT						
Output Power for 1 dB Compression	OP1dB	25	28		dBm	
Saturated Output Power	P_{SAT}		31		dBm	
Output Third-Order Intercept	OIP3		40.5		dBm	Measurement taken at P_{OUT}/tone = 14 dBm
SUPPLY						
Quiescent Current	I_{DQ}		385		mA	For external bias control, adjust V_{GG1} between −2 V and +0.5 V to achieve the desired I_{DQ}
Drain Voltage	V_{DD}	10	12	15	V	

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD}	16 V
V_{GG1}	−2.5 V to +1 V
RFIN	25 dBm
Continuous Power Dissipation (P_{DISS}), T = 85°C (Derate 113.64 mW/°C Above 85°C)	10.2 W
Output Load Voltage Standing Wave Ratio (VSWR)	7:1
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C
Peak Reflow (Moisture Sensitivity Level (MSL) 3)	260°C
Junction to Maintain 1 Million Hour Mean Time to Failure (MTTF)	175°C
Nominal Junction (T = 85°C, V_{DD} = 12 V)	125.7°C
ESD Sensitivity	
Human Body Model (HBM)	Class 1B, passed 500 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JC} is the junction to case thermal resistance.

Table 5. Thermal Resistance

Package	θ_{JC}	Unit
CG-32-2	8.8	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

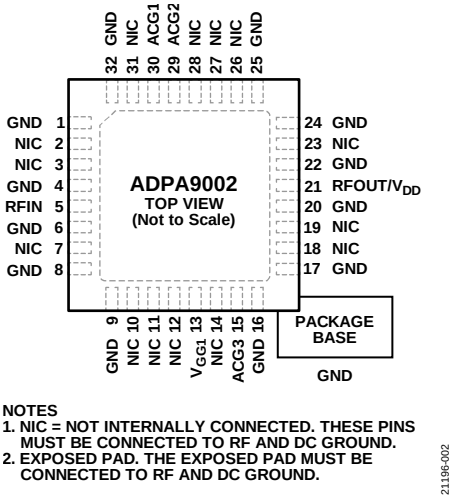


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 6, 8, 9, 16, 17, 20, 22, 24, 25, 32	GND	Ground. These pins must be connected to RF and dc ground.
2, 3, 7, 10, 11, 12, 14, 18, 19, 23, 26, 27, 28, 31	NIC	Not Internally Connected. These pins must be connected to RF and dc ground.
5	RFIN	RF Input. This pin is dc-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.
13	V_{GG1}	Gate Voltage. This pin is used for external bias operation of the device. If grounded, the amplifier runs in self biased mode at the standard current of 385 mA. Adjusting the voltage above or below the ground potential controls the drain current. External bypass capacitors are required (see Figure 62). See Figure 7 for the interface schematic.
15, 29, 30	ACG3, ACG2, ACG1	AC Ground Pins. These pins are used for low frequency termination. External bypass capacitor required (see Figure 62). See Figure 4 and Figure 5 for the interface schematics.
21	RFOUT/V_{DD}	RF Output for the Amplifier (RFOUT).
		Drain Voltage (V_{DD}). Connect the V_{DD} network to provide the drain current (I_{DD}) (see Figure 62). See Figure 5 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS



Figure 3. GND Interface Schematic

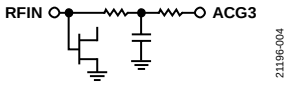


Figure 4. ACG3 Interface Schematic

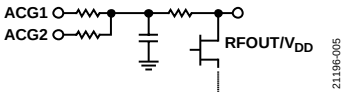


Figure 5. RFOUT/V_{DD}, ACG1, ACG2 Interface Schematic

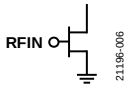


Figure 6. RFIN Interface Schematic

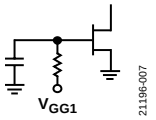


Figure 7. V_{GG1} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

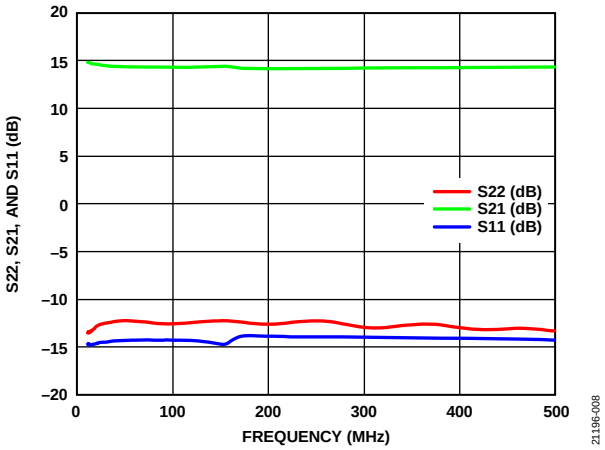


Figure 8. S22, S21, and S11 vs. Frequency, 10 MHz to 500 MHz, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

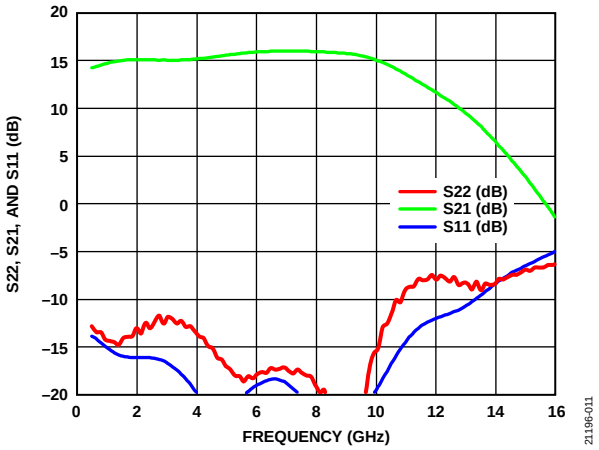


Figure 11. S22, S21, and S11 vs. Frequency, 500 MHz to 16 GHz, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

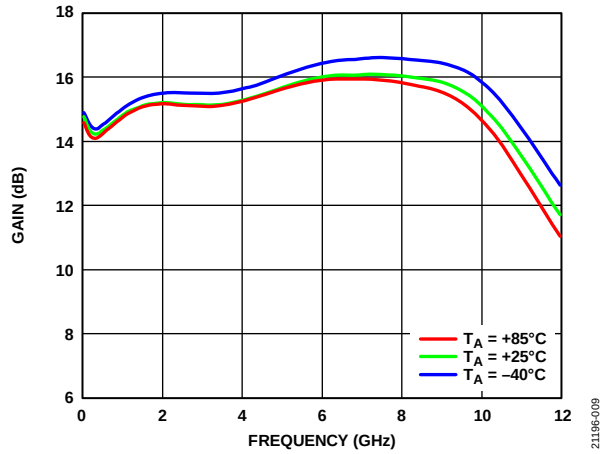


Figure 9. Gain vs. Frequency for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

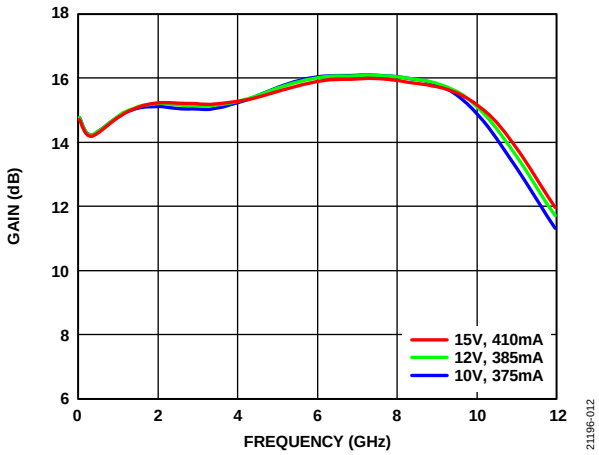


Figure 12. Gain vs. Frequency for Various V_{DD} and Quiescent Currents, Self Biased Mode, V_{GG1} = GND

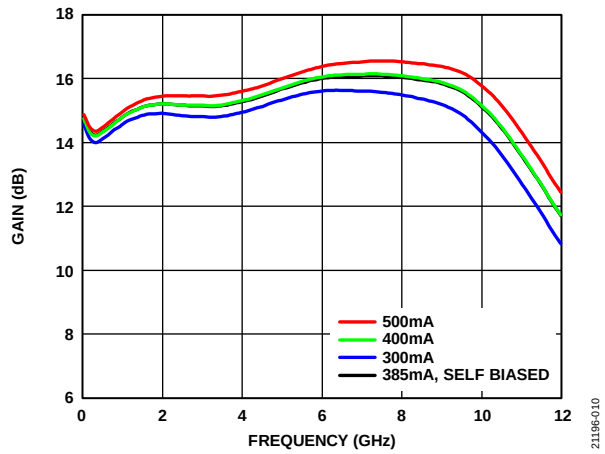


Figure 10. Gain vs. Frequency for Various I_{DQ}, Externally Biased Mode, V_{DD} = 12 V, Controlled V_{GG1}

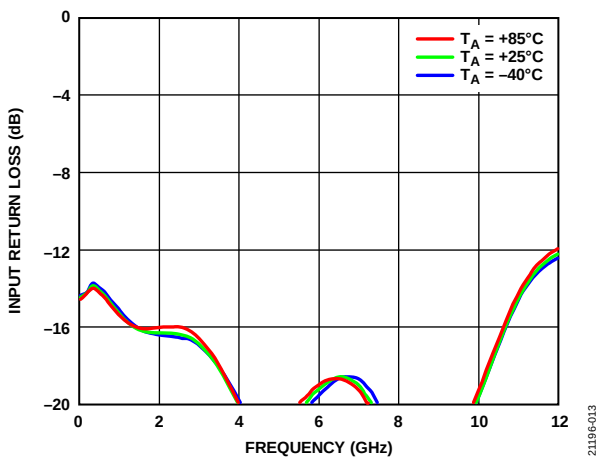


Figure 13. Input Return Loss vs. Frequency for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

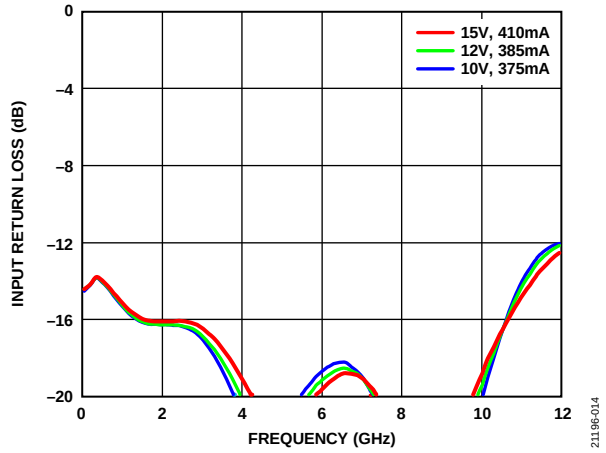


Figure 14. Input Return Loss vs. Frequency for Various V_{DD} and Quiescent Currents, Self Biased Mode, V_{GG1} = GND

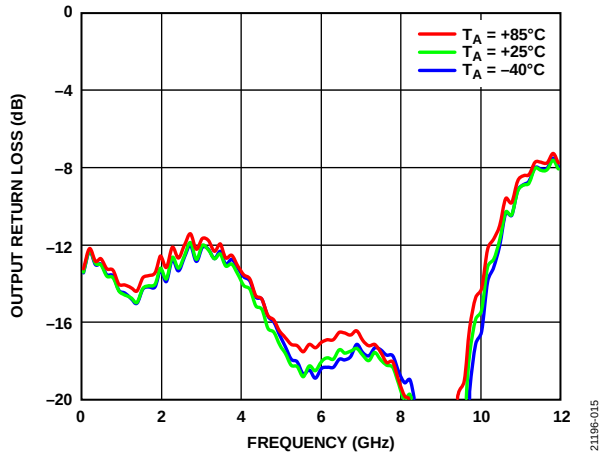


Figure 15. Output Return Loss vs. Frequency for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

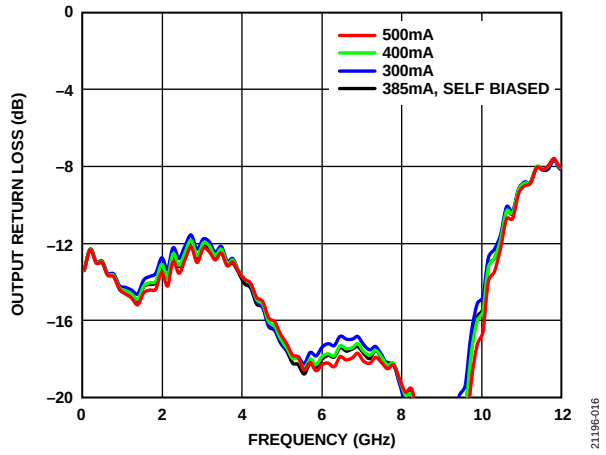


Figure 16. Output Return Loss vs. Frequency for Various I_{DQ}, External Biased Condition, V_{DD} = 12 V, Controlled V_{GG1}

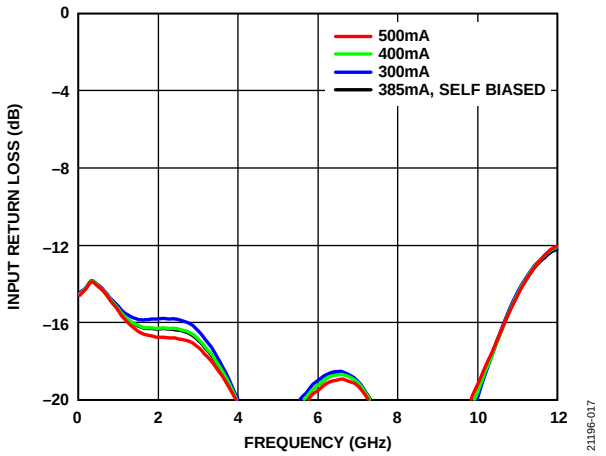


Figure 17. Input Return Loss vs. Frequency for Various I_{DQ}, Externally Biased Mode, V_{DD} = 12 V, Controlled V_{GG1}

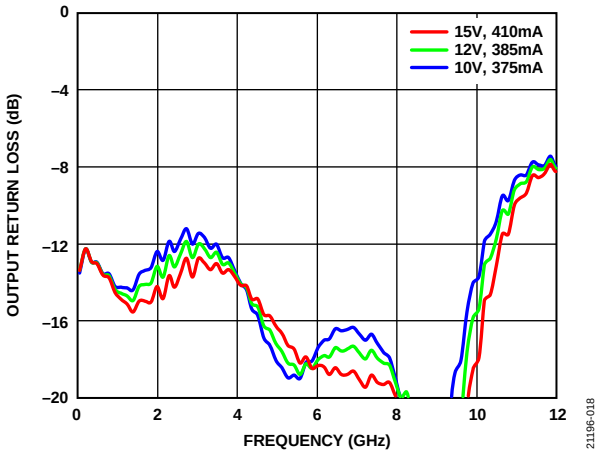


Figure 18. Output Return Loss vs. Frequency for Various V_{DD} and Quiescent Currents, Self Biased Mode, V_{GG1} = GND

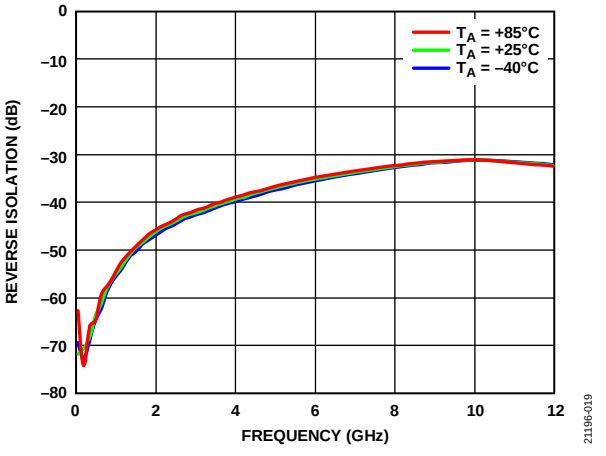


Figure 19. Reverse Isolation vs. Frequency for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

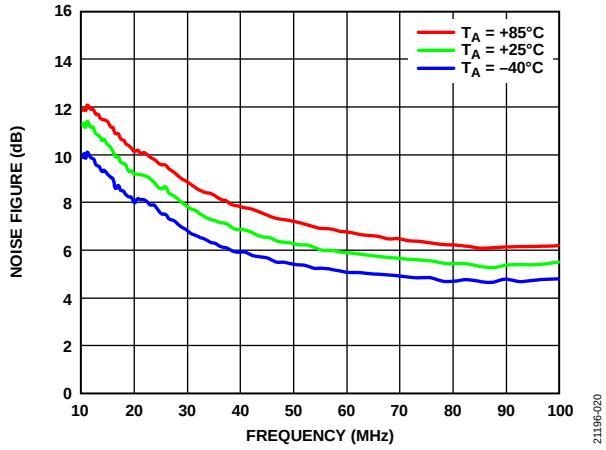


Figure 20. Noise Figure vs. Frequency, 10 MHz to 100 MHz, for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

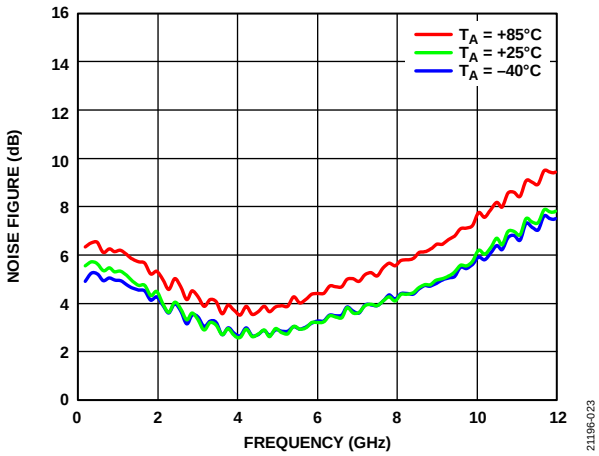


Figure 23. Noise Figure vs. Frequency, 100 MHz to 12 GHz, for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

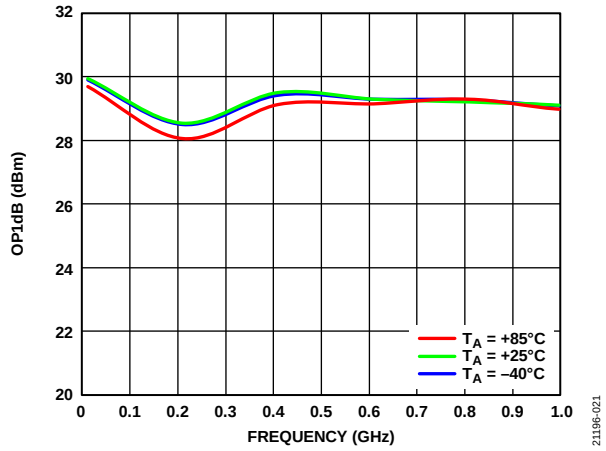


Figure 21. OP1dB vs. Frequency,10 MHz to 1 GHz for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

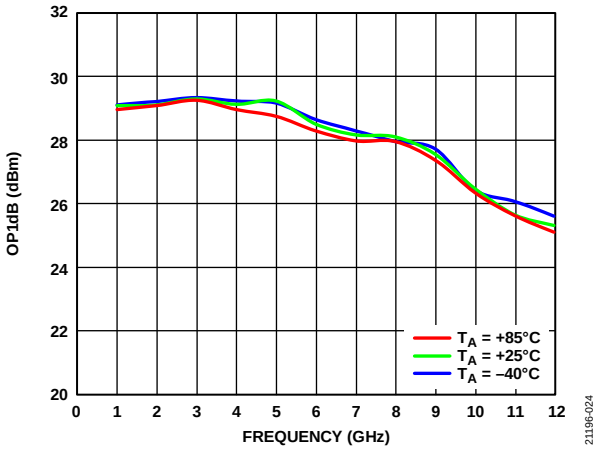


Figure 24. OP1dB vs. Frequency, 1 GHz to 12 GHz for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

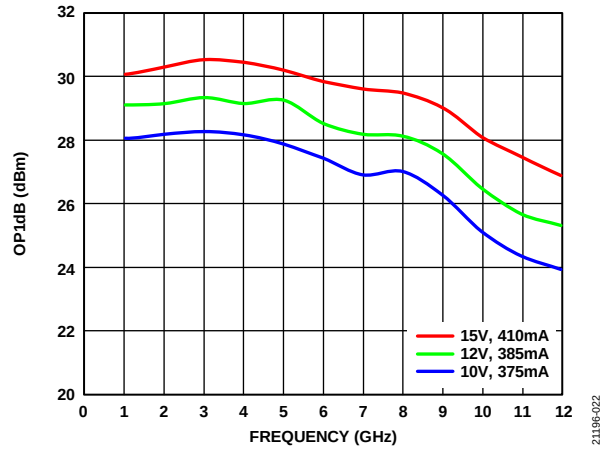


Figure 22. OP1dB vs. Frequency for Various V_{DD} and Quiescent Currents, Self Biased Mode, V_{GG1} = GND

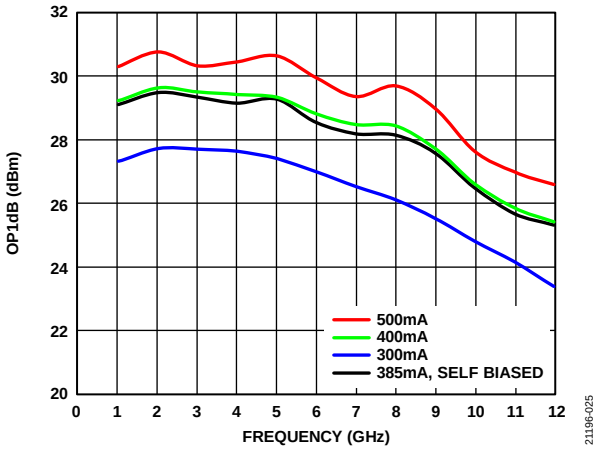


Figure 25. OP1dB vs. Frequency for Various I_{DQ}, Externally Biased Mode, V_{DD} = 12 V, Controlled V_{GG1}

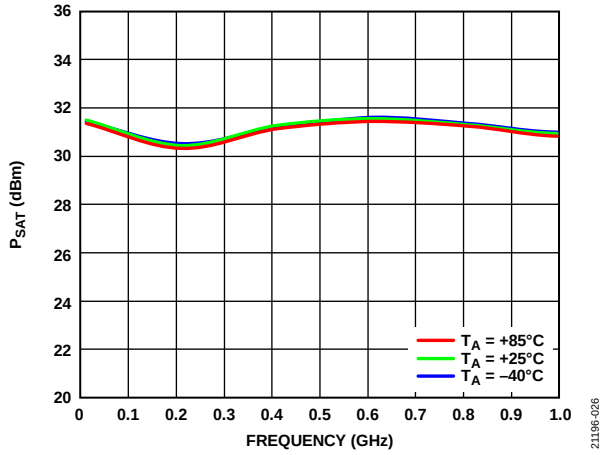


Figure 26. P_{SAT} vs. Low Frequency,10 MHz to 1 GHz for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

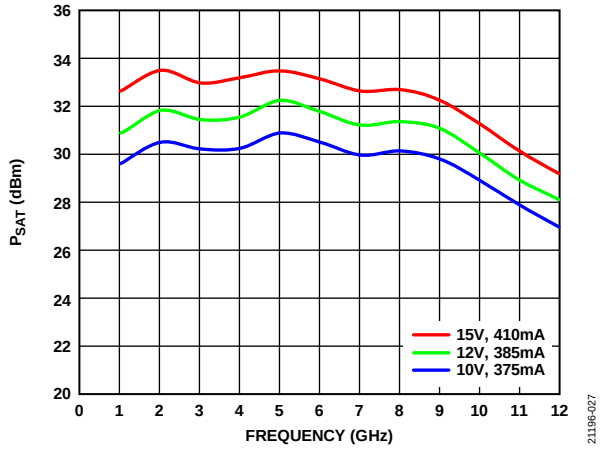


Figure 27. P_{SAT} vs. Frequency for Various V_{DD} and Quiescent Currents, Self Biased Mode, V_{GG1} = GND

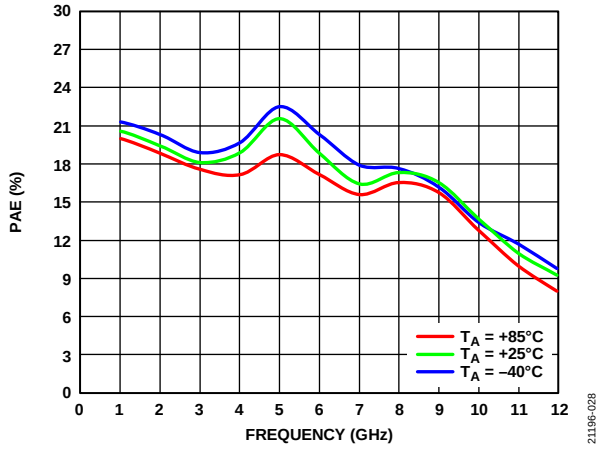


Figure 28. Power Added Efficiency (PAE) vs. Frequency for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND, PAE Measured at P_{SAT}

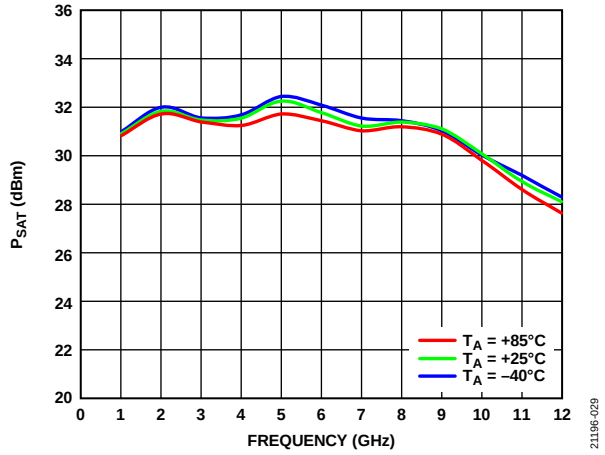


Figure 29. P_{SAT} vs. Frequency, 1 GHz to 12 GHz for Various Temperatures, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

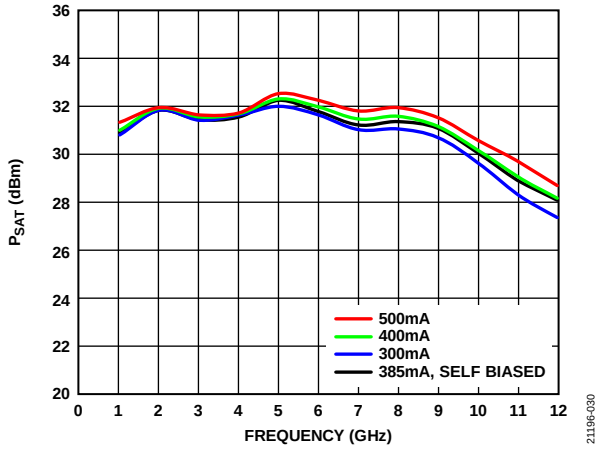


Figure 30. P_{SAT} vs. Frequency for Various I_{DQ}, Externally Biased Mode, V_{DD} = 12 V, Controlled V_{GG1}

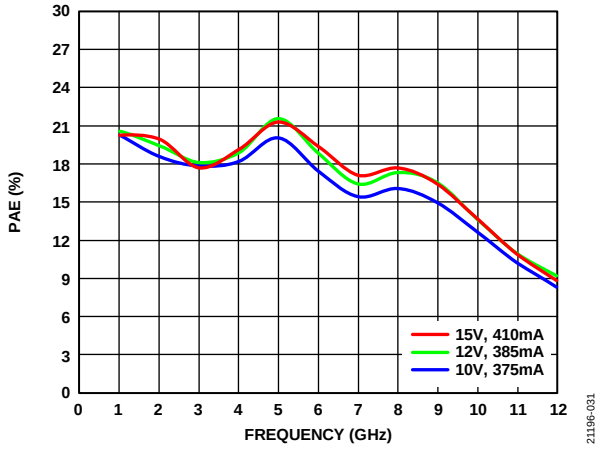


Figure 31. PAE vs. Frequency for Various V_{DD} and Quiescent Currents, Self Biased Mode, V_{GG1} = GND, PAE Measured at P_{SAT}

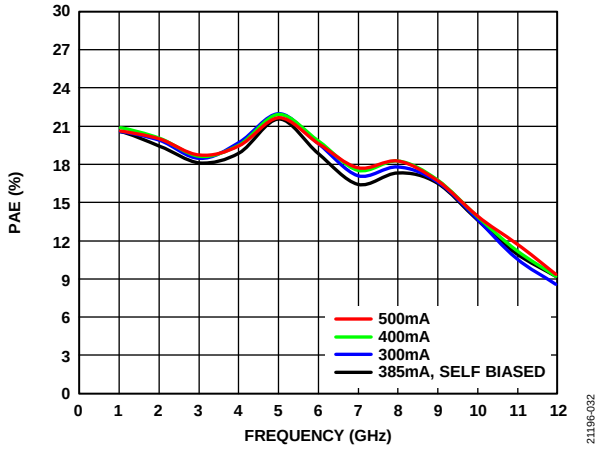


Figure 32. PAE vs. Frequency for Various I_{DQ}, Externally Biased Mode, V_{DD} = 12 V, Controlled V_{GG1}, PAE Measured at P_{SAT}

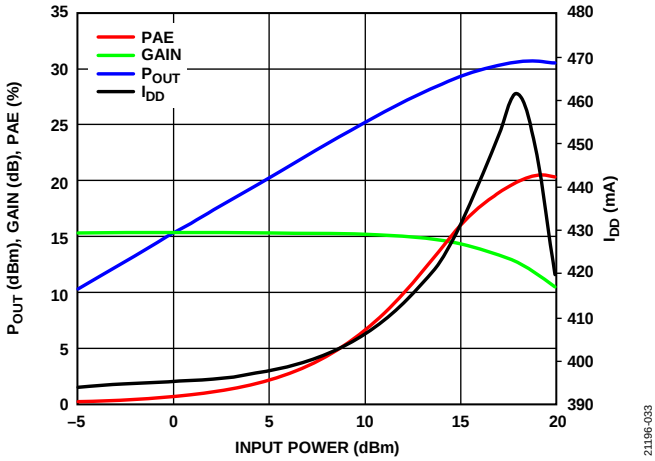


Figure 33. P_{OUT}, Gain, PAE, Supply Current (I_{DD}) vs. Input Power, 3 GHz, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

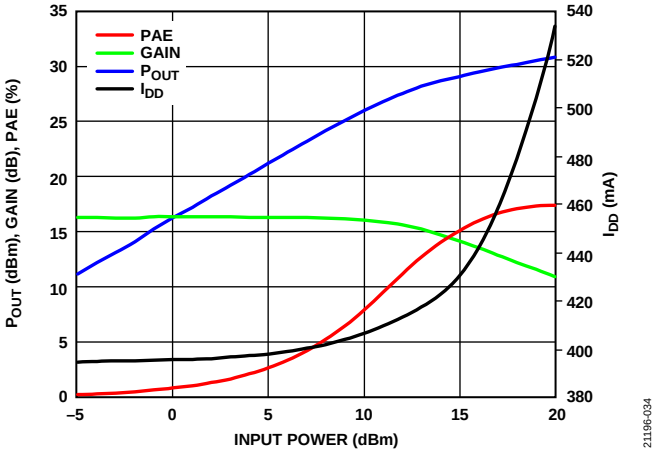


Figure 34. P_{OUT}, Gain, PAE, I_{DD} vs. Input Power, 8 GHz, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

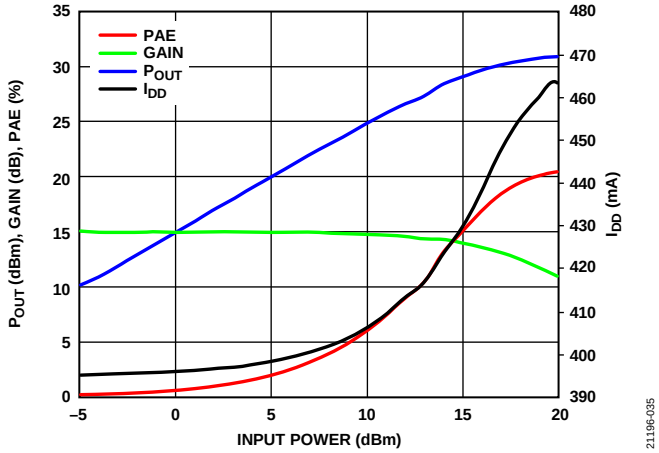


Figure 35. P_{OUT}, Gain, PAE, I_{DD} vs. Input Power, 1 GHz, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

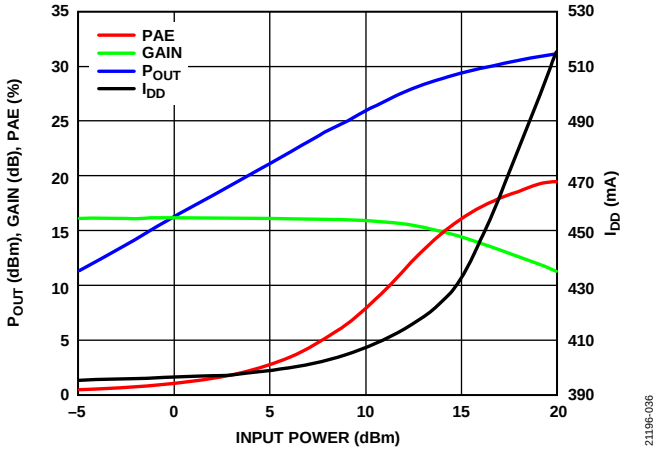


Figure 36. P_{OUT}, Gain, PAE, I_{DD} vs. Input Power, 6 GHz, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

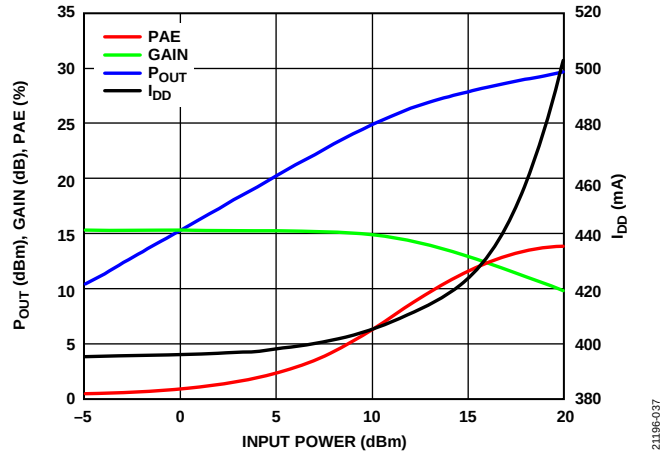


Figure 37. P_{OUT}, Gain, PAE, I_{DD} vs. Input Power, 10 GHz, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

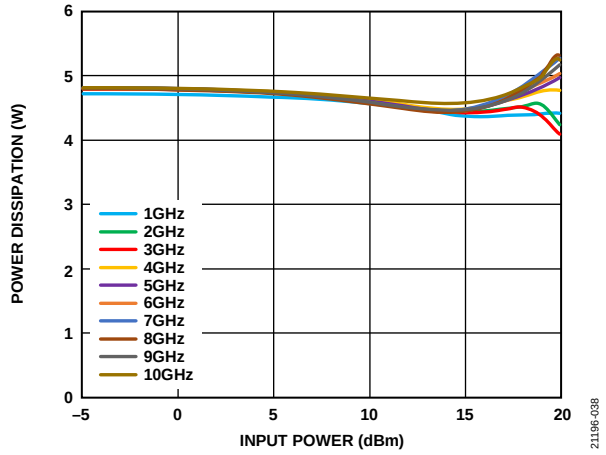


Figure 38. Power Dissipation vs. Input Power for Various Frequencies at T_A = 85°C, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

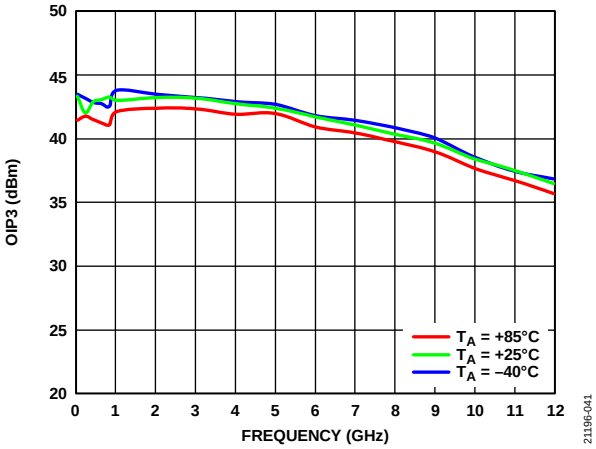


Figure 41. OIP3 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 14 dBm, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

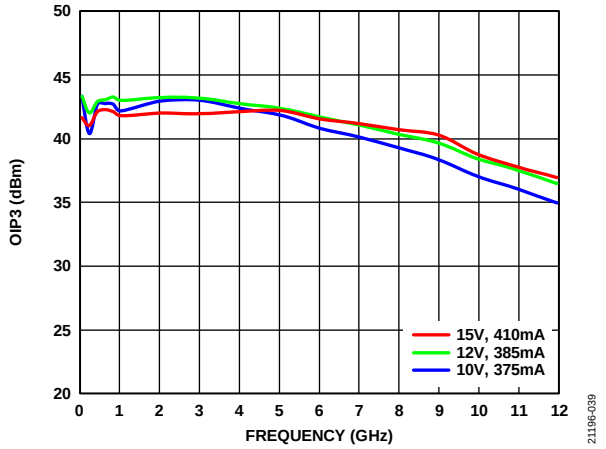


Figure 39. OIP3 vs. Frequency for Various V_{DD} and Quiescent Currents, Self Biased Mode, V_{GG1} = GND, P_{OUT} per Tone = 14 dBm

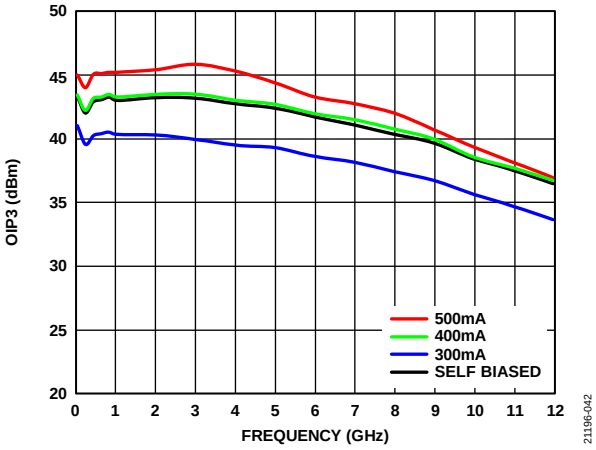


Figure 42. OIP3 vs. Frequency for Various I_{DQ}, Externally Biased Mode, V_{DD} = 12 V, Controlled V_{GG1}, P_{OUT} per Tone = 14 dBm

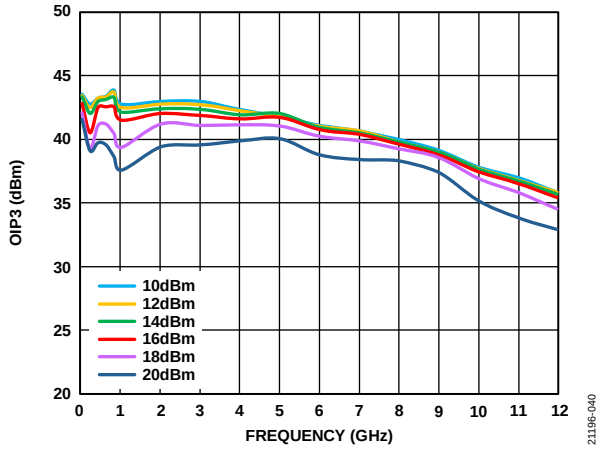


Figure 40. OIP3 vs. Frequency for Various P_{OUT} per Tone, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

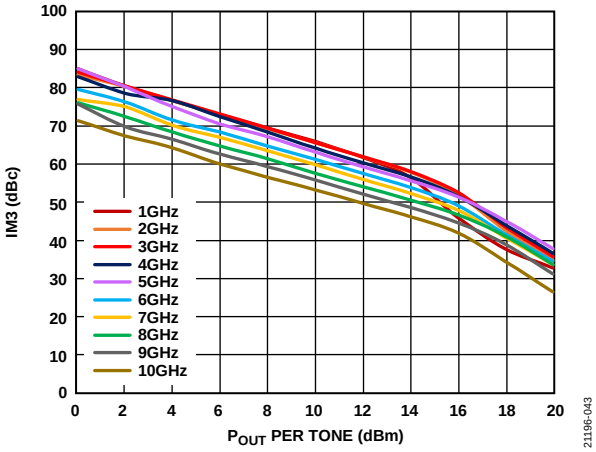


Figure 43. Third-Order Intermodulation Distortion Relative to Carrier (IM3) vs. P_{OUT} per Tone for Various Frequencies, Self Biased Mode, V_{DD} = 10 V, V_{GG1} = GND

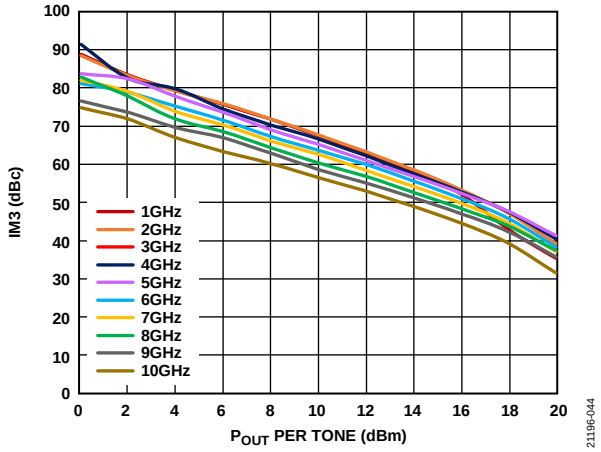


Figure 44. IM3 vs. P_{OUT} per Tone for Various Frequencies, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

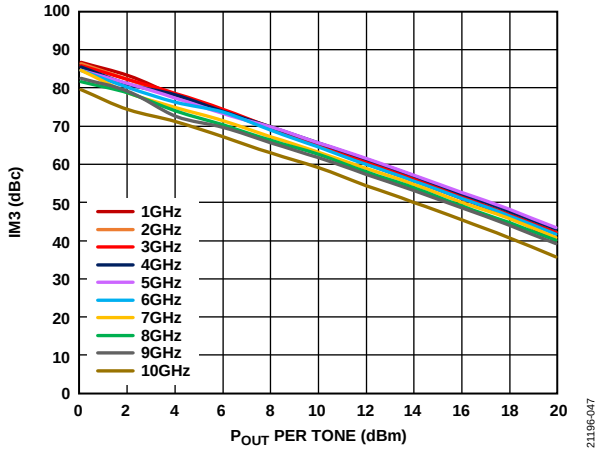


Figure 47. IM3 vs. P_{OUT} per Tone for Various Frequencies, Self Biased Mode, V_{DD} = 15 V, V_{GG1} = GND

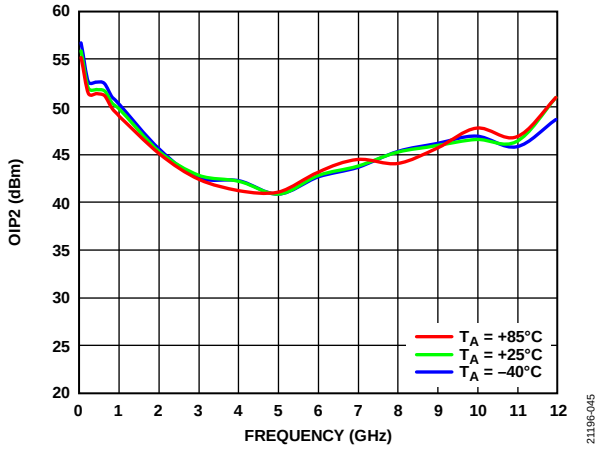


Figure 45. OIP2 vs. Frequency for Various Temperatures, P_{OUT} per Tone = 14 dBm, Self Biased, V_{DD} = 12 V, V_{GG1} = GND

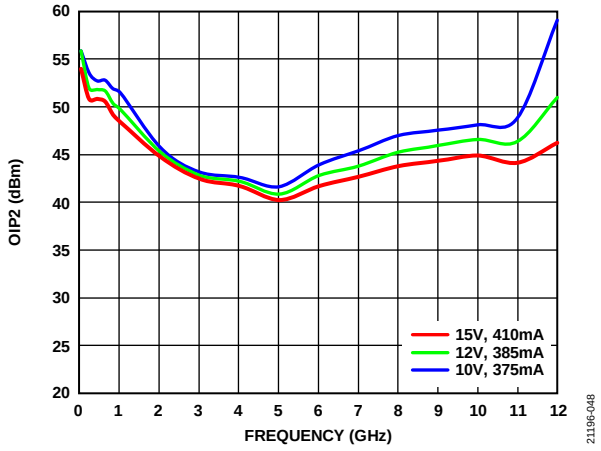


Figure 48. OIP2 vs. Frequency for Various V_{DD} and Quiescent Currents, Self Biased Mode, V_{GG1} = GND, P_{OUT} per Tone = 14 dBm

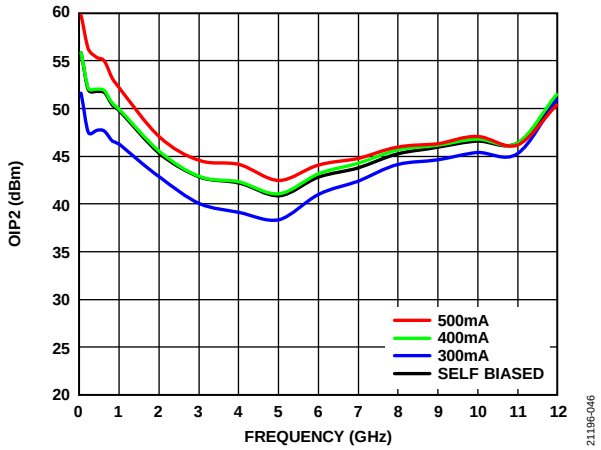


Figure 46. OIP2 vs. Frequency for Various I_{DQ}, Externally Biased Mode, V_{DD} = 12 V, Controlled V_{GG1}, P_{OUT} per Tone = 14 dBm

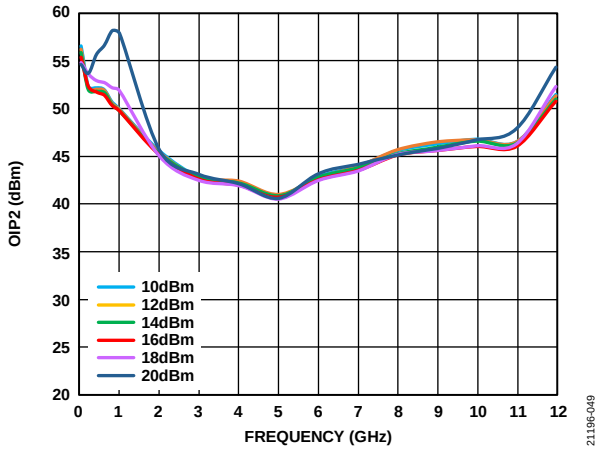


Figure 49. OIP2 vs. Frequency for Various P_{OUT} per Tone, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

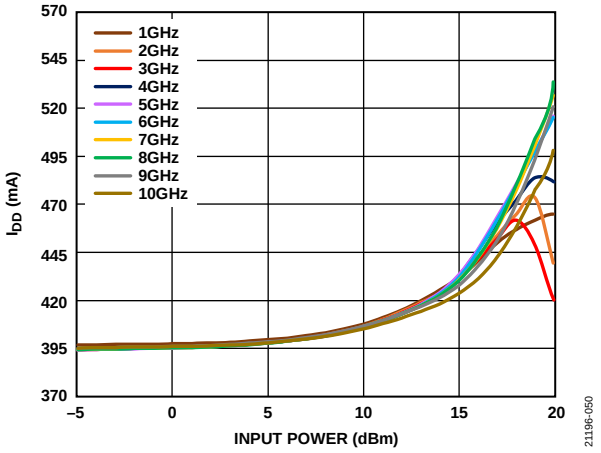


Figure 50. I_{DD} vs. Input Power for Various Frequencies, Self Biased Mode, V_{DD} = 12 V, V_{GG1} = GND

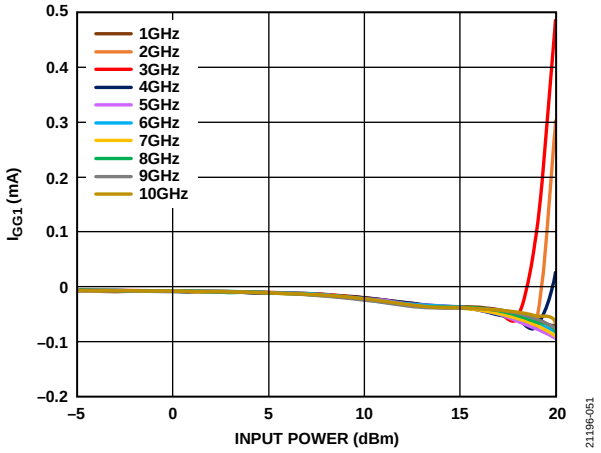


Figure 51. Gate 1 Current (I_{GG1}) vs. Input Power for Various Frequencies, V_{DD} = 12 V, I_{DQ} = 400 mA, Controlled V_{GG1}

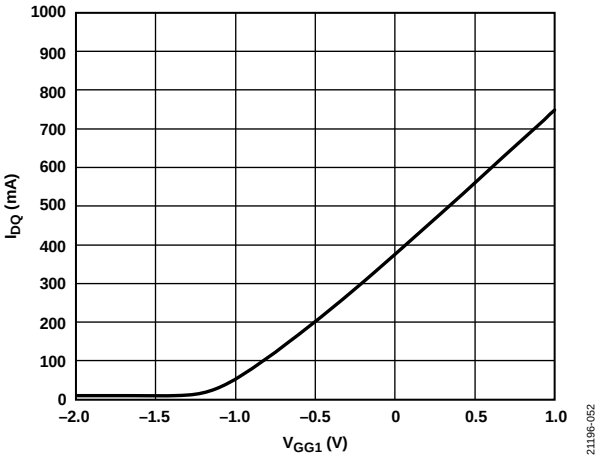


Figure 52. I_{DQ} vs. V_{GG1}, V_{DD} = 12 V, Externally Biased Mode

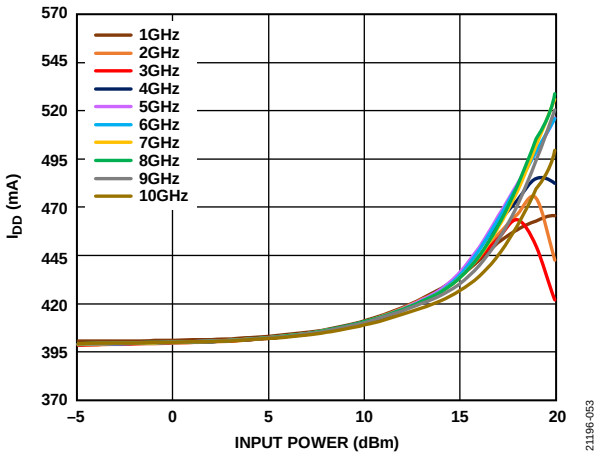


Figure 53. I_{DD} vs. Input Power for Various Frequencies, V_{DD} = 12 V, I_{DQ} = 400 mA, Controlled V_{GG1}

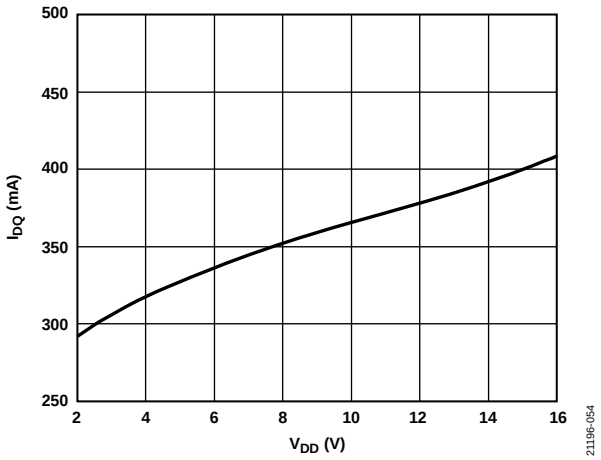


Figure 54. I_{DQ} vs. V_{DD}, V_{GG1} = GND, Self Biased Mode

CONSTANT I_{DD} OPERATION

Biased with the HMC980LP4E active bias controller for constant I_{DD} operation. T_A = 25°C, V_{DD} = 12 V, and I_{DQ} = 400 mA for nominal operation, unless otherwise noted.

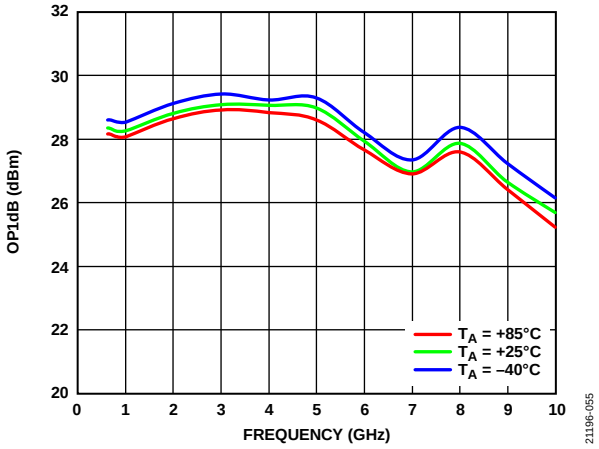


Figure 55. OP1dB vs. Frequency for Various Temperatures, V_{DD} = 12 V, Constant I_{DD} = 400 mA

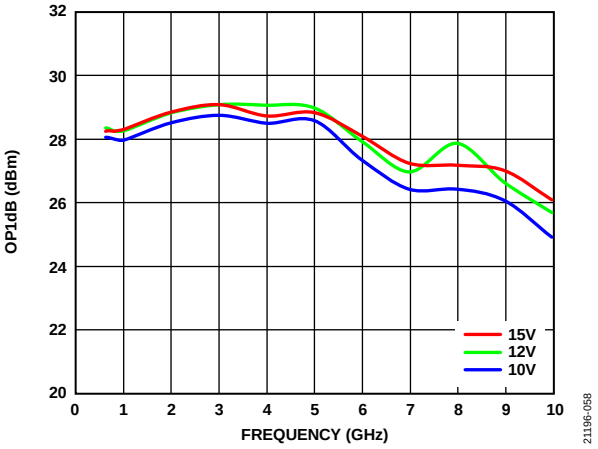


Figure 58. OP1dB vs. Frequency for Various Supply Voltages, Constant I_{DD} = 400 mA

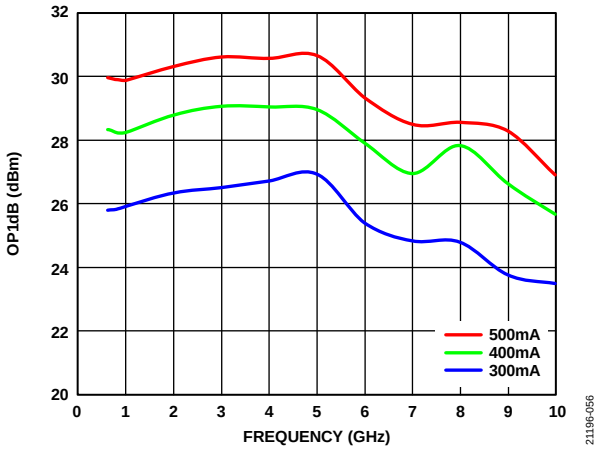


Figure 56. OP1dB vs. Frequency for Various Constant I_{DD}, V_{DD} = 12 V

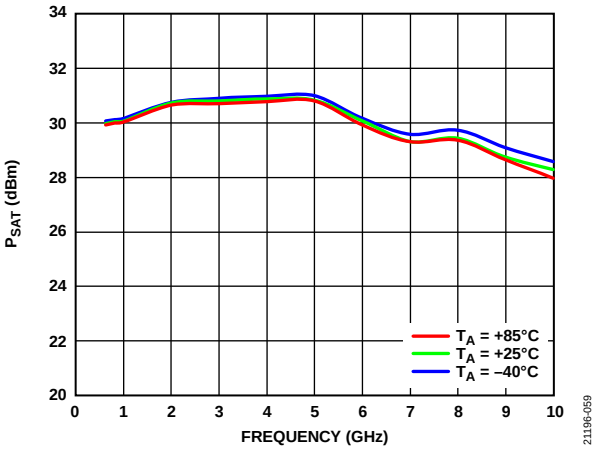


Figure 59. P_{SAT} vs. Frequency for Various Temperatures, V_{DD} = 12 V, Constant I_{DD} = 400 mA

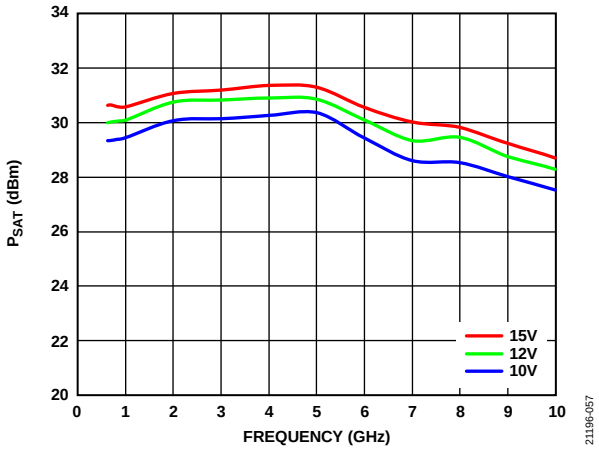


Figure 57. P_{SAT} vs. Frequency for Various Supply Voltages, Constant I_{DD} = 400 mA

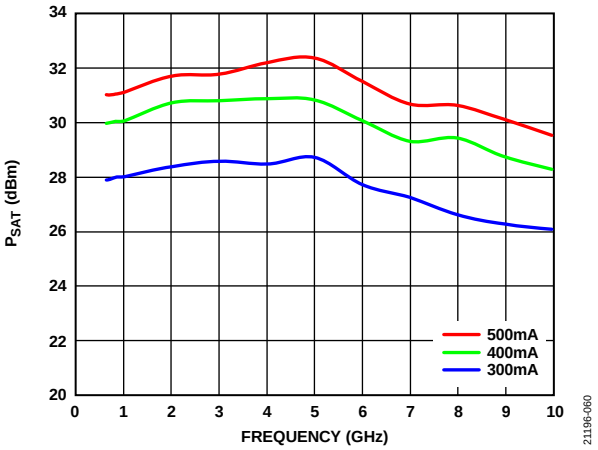


Figure 60. P_{SAT} vs. Frequency for Various Constant I_{DD}, V_{DD} = 12 V

THEORY OF OPERATION

The ADPA9002 is a GaAs, MMIC, pHEMT, cascode distributed power amplifier. The cascode distributed architecture of the ADPA9002 uses a fundamental cell consisting of a stack of two field effect transistors (FETs) with the source of the upper FET connected to the drain of the lower FET. The fundamental cell is then duplicated several times with an RFIN transmission line interconnecting the gates of the lower FETs and an RFOUT transmission line interconnecting the drains of the upper FETs.

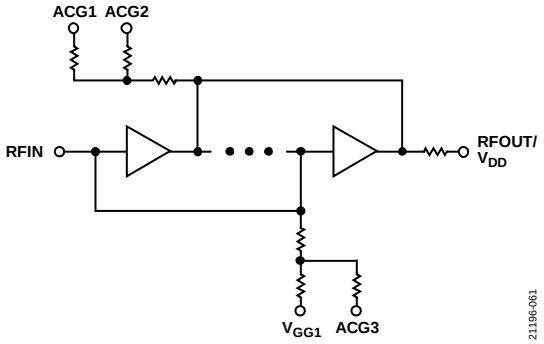


Figure 61. Simplified Schematic of the Cascode Distributed Amplifier

Additional circuit design techniques are used around each cell to optimize the overall bandwidth, output power, and noise figure. The major benefit of this architecture is that a high output level is maintained across a bandwidth far greater than a single instance of the fundamental cell provides. A simplified schematic of this architecture is shown in Figure 61.

For simplified biasing without the need for a negative voltage rail, V_{GG1} can be connected directly to GND. With V_{DD} = 12 V and V_{GG1} grounded, a quiescent drain current of 385 mA (typical) results. An externally generated V_{GG1} can optionally be applied, allowing adjustment of the quiescent drain current above and below the 385 mA nominal. As an example, Figure 52 shows that, by adjusting V_{GG1} from approximately −0.3 V to +0.3 V, quiescent drain currents from 250 mA to 450 mA can be obtained.

The ADPA9002 has single-ended input and output ports whose impedances are nominally equal to 50 Ω over the dc to 10 GHz frequency range. Consequently, the ADPA9002 can be directly inserted into a 50 Ω system with no required impedance matching circuitry. Similarly, the input and output impedances are sufficiently stable across variations in temperature and supply voltage so that no impedance matching compensation is required. The RF output port additionally functions as the V_{DD} bias, requiring an RF choke through which dc bias is applied. Though the device operates down to dc, blocking capacitors are recommended at the RF input and output ports to prevent damages on the RF stages when loading the dc bias supplies. The RF choke and blocking capacitor at the RF output together constitute a bias tee. In practice, the external RF choke and dc blocking capacitor selections limit the lowest frequency of operation.

ACG1 through ACG3 are nodes at which ac terminations (capacitors) to ground can be provided. The use of such terminations serves to roll off the gain at frequencies below 200 MHz, allowing the flattest possible gain response to be obtained over various frequencies.

It is critical to supply low inductance ground connections to the GND pins and to the package base exposed pad to ensure stable operation. To achieve optimal performance from the ADPA9002 and to prevent damage to the device, do not exceed the absolute maximum ratings.

APPLICATIONS INFORMATION

Capacitive bypassing is required for V_{DD} and V_{GG1}, as shown in Figure 62. Both the RFIN and RFOUT/V_{DD} pins are dc-coupled. Use of an external dc blocking capacitor at RFIN is recommended. Use of an external RF choke plus a dc blocking capacitor (for example, a bias tee) at the RFOUT/V_{DD} pin is required. For wideband applications, ensure that the frequency responses of the external biasing and blocking components are adequate for use across the entire frequency range of the application.

The ADPA9002 operates in either self biased or externally biased mode. Ground the V_{GG1} pin to operate the device in self biased mode. For the externally biased configuration, adjust the V_{GG1} pin within −2 V to +0.5 V to set the target drain.

The recommended bias sequence during power-up for self biased operation is as follows:

1. Connect the V_{GG1} pin to ground and ground all GND pins.
2. Set V_{DD} to 12 V.
3. Apply the RF signal to the RFIN pin.

The recommended bias sequence during power-down for self biased operation is as follows:

1. Turn off the RFIN signal.
2. Set V_{DD} to 0 V.

The recommended bias sequence during power-up for externally biased operation is as follows:

1. Connect all GND pins to ground.
2. Set the V_{GG1} pin to −2 V.
3. Set V_{DD} to 12 V.
4. Increase the V_{GG1} pin to achieve the I_{DQ}.
5. Apply the RF signal to the RFIN pin.

The recommended bias sequence during power-down for externally biased operation is as follows:

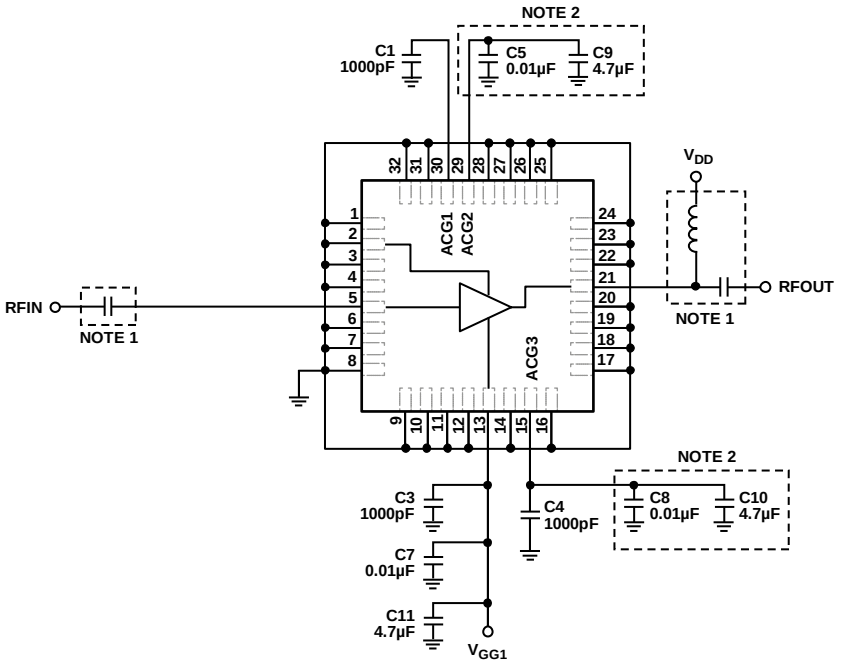
1. Turn off the RFIN signal.
2. Decrease the V_{GG1} pin to −2 V to achieve a typical I_{DQ} of 0 mA.
3. Set V_{DD} to 0 V.
4. Set the V_{GG1} pin to 0 V.

Take care to ensure adherence to the values shown in the Absolute Maximum Ratings section.

Unless otherwise noted, all measurements and data shown were taken using the typical application circuit (see Figure 62) and biased per the conditions in this section. The bias conditions described in this section are the operating points recommended to optimize the overall device performance. Operation using other bias conditions may result in performance that differs from what is shown in the Typical Performance Characteristics section. To obtain optimal performance while not damaging the device, follow the recommended biasing sequences described in this section.

TYPICAL APPLICATION CIRCUIT

In Figure 62, the drain voltage (V_{DD}) must be applied through an external broadband bias tee connected at the RFOUT/V_{DD} pin and connect an external dc block to the RFIN pin. Use optional capacitors if the device is operated below 200 MHz.



NOTES
1. DRAIN VOLTAGE (V_{DD}) MUST BE APPLIED THROUGH AN ETERNAL BIAS TEE CONNECTED AT THE RFOUT/V_{DD} PIN AND AN EXTERNAL DC BLOCK MUST BE CONNECTED AT THE RFIN PIN.
2. USE OPTIONAL CAPACITORS IF THE DEVICE IS OPERATED BELOW 200MHz.

21196-062

Figure 62. Typical Application Circuit

OUTLINE DIMENSIONS

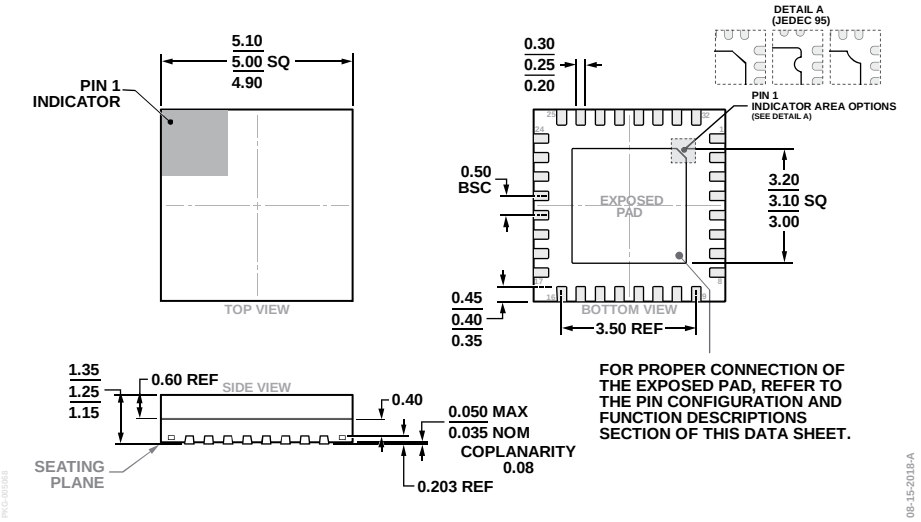


Figure 63. 32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]
5 mm × 5 mm Body and 1.25 mm Package Height
(CG-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature	MSL Rating[2]	Description[3]	Package Option
ADPA9002ACGZN	−40°C to +85°C	3	32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]	CG-32-2
ADPA9002ACGZN-R7	−40°C to +85°C	3	32-Lead Lead Frame Chip Scale Package, Premolded Cavity [LFCSP_CAV]	CG-32-2
ADPA9002-EVALZ			Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] See the Absolute Maximum Ratings section for additional information.
[3] The lead finish of the ADPA9002ACGZN and the ADPA9002ACGZN-R7 is nickel palladium gold (NiPdAu).

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