# TUSB1310
## USB 3.0 Transceiver

# Data Manual



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# USB 3.0 Transceiver

**Check for Samples: TUSB1310**

## 1 PRODUCT OVERVIEW

### 1.1 Features

- Universal Serial Bus (USB)
  - Single Port 5.0-Gbps USB 3.0 Physical Layer Transceiver
    - One 5.0-Gbps SuperSpeed Conneciton
    - One 480-Mbps HS/FS/LS Connection
  - Fully Compliant with USB 3.0 Specification
  - Supports 3+ Meters USB 3.0 Cable Length
  - Fully Adaptive Equalizer to Optimize Receiver Sensitivity
  - PIPE to Link Layer Controller
    - Supports 16-Bit SDR Mode at 250 MHz
    - Compliant With PHY Interface for the USB Architectures (PIPE), Version 3.0
  - ULPI to Link Layer Controller
    - Supports 8-Bit SDR Mode at 60 MHz
    - Supports Synchronous Mode and Low Power Mode
    - Compliant with UTMI+ Low Pin Interface (ULPI) Specification, Revision 1.1
- General Features
  - IEEE 1149.1 JTAG Support
  - IEEE 1149.6 JTAG support for the SuperSpeed Port
  - Operates on a Single Reference Clock Selectable from 20, 25, 30 or 40 MHz
  - 3.3-, 1.8-, and 1.1-V Supply Voltages
  - 1.8-V PIPE and ULPI I/O
  - Available in Lead-Free 175-Ball 12- x 12-nF BGA Package (175ZAY)

### 1.2 Target Applications

- Surveillance Cameras
- Multimedia Handset
- Smartphone
- Digital Still Camera
- Portable Media Player
- Personal Navigation Device
- Audio Dock
- Video IP Phone
- Wireless IP Phone
- Software Defined Radio

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## 1.3 Introduction

The TUSB1310 is a single port, 5.0-Gbps USB 3.0 physical layer transceiver operating off of a single crystal or an external reference clock. The reference clock frequencies are selectable from 20, 25, 30, and 40 MHz. The TUSB1310 provides a clock to USB link layer controllers. The single reference clock allows the TUSB1310 to provide a cost effective USB 3.0 solution with few external components and a minimum implementation cost.

Link controller interfaces to the TUSB1310 are via a PIPE (SuperSpeed) and a ULPI (USB2.0) interface. The 16-bit PIPE operates with a 250-MHz interface clock. The ULPI supports 8-bit operations with a 60-MHz interface clock.

USB 3.0 reduces active power and idle power by improving power management. The PIPE interface controls the TUSB1310 low power states which minimizes power consumption.

SuperSpeed USB leverages existing USB software infrastructure by keeping the existing software interfaces and software drivers. In addition the SuperSpeed USB retains backward compatibility at the Type-A connector with USB2.0 based PCs and with USB2.0 cables.

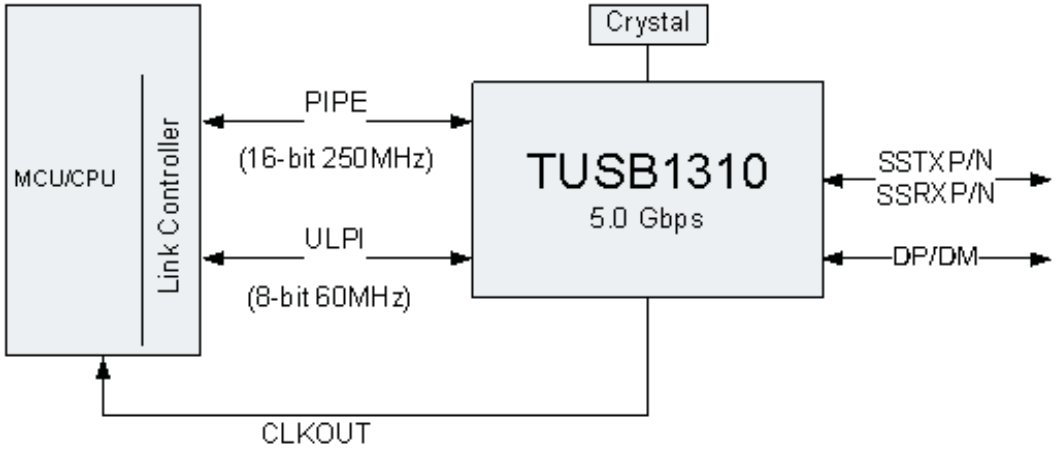



**Figure 1-1. Typical Application**

## 1.4 Functional Block Diagram

The USB physical layer handles the low level USB protocol and signaling. This includes data serialization and deserialization, 8b/10b encoding, analog buffers, elastic buffers and receiver detection. It shifts the clock domain of the data from the USB rate to one that is compatible with the link layer controller.

The SuperSpeed USB contains SSTXP/SSTXN and SSRXP/SSRXP differential pairs and uses the PIPE to communicate with the link layer controller. The Non-SuperSpeed USB has a DP/DM differential pair and communicates with the link layer controller via the ULPI. The TUSB1310 reference clock is connected to an internal crystal oscillator, spread spectrum clock and PLL which provides clocks to all blocks and to the CLKOUT pin for the link layer controller.

A JTAG interface is used for IEEE1149.1 and IEEE1149.6 boundary scan.


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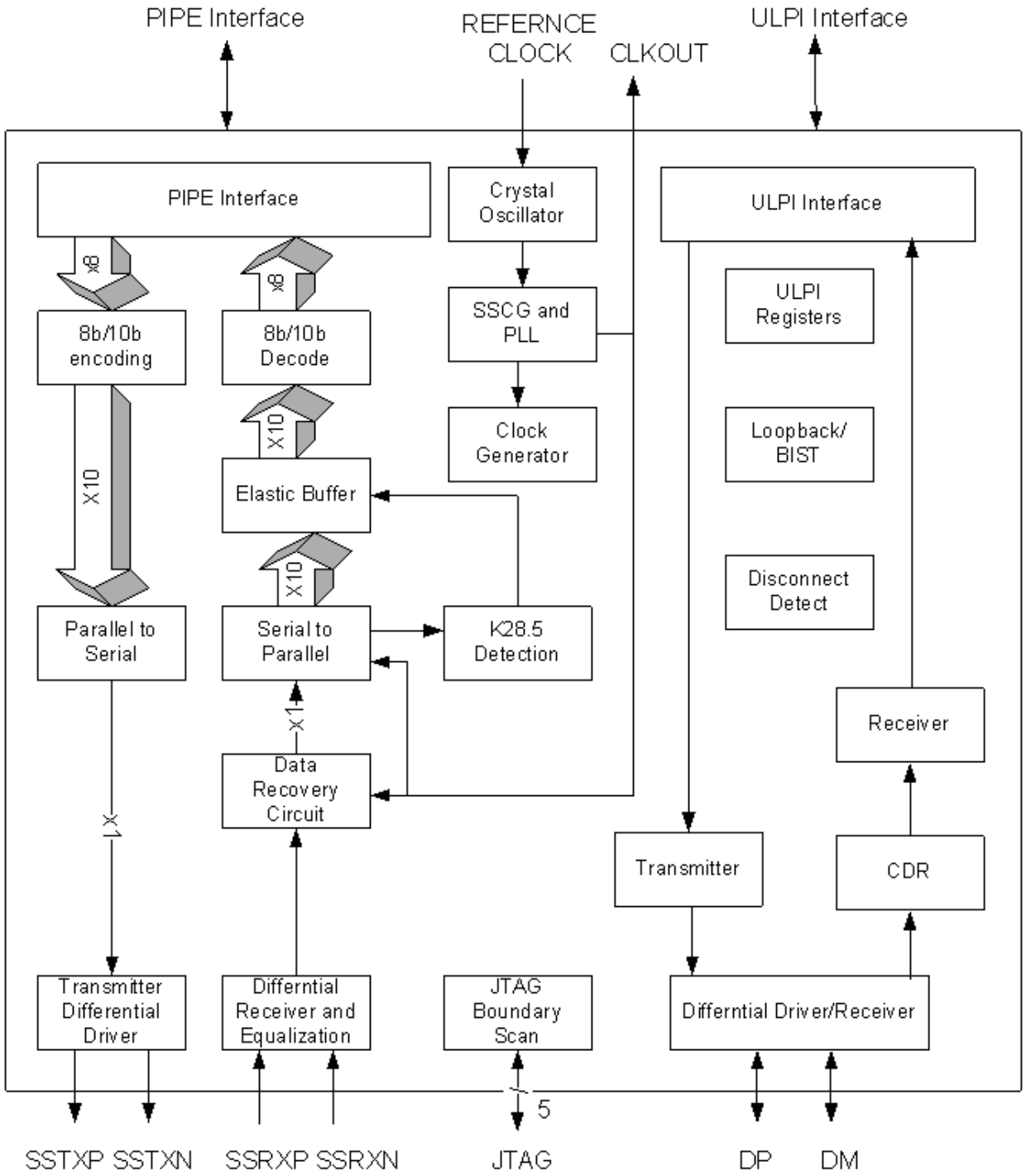



**Figure 1-2. Functional Block Diagram**

# 2 PIN DESCRIPTIONS

| TYPE | DESCRIPTION |
|---|---|
| I | Input |
| O | Output |
| I/O | Input/output |
| PD, PU | Internal pull-down / pull-up |
| S | Strapping pin |
| P | Power Supply |
| G | Ground |

## 2.1 Configuration Pins

The configuration pins are not latched by RESETN.

**Table 2-1. Configuration Pins**

| SIGNAL NAME | TYPE | PIN NO. | MODE NAME | DESCRIPTION |
|---|---|---|---|---|
| PHY_MODE1 | I, PD | H12 | USB | Must be set to 0. Operates as USB 3.0 transceiver. |
| PHY_MODE0 | I, PU | J12 | USB | Must be set to 1. Operates as USB 3.0 transceiver. |

## 2.2 PIPE

The TUSB1310 supports 16-bit SDR mode with a 250-MHz clock.

**Table 2-2. PIPE Signal Description**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| TX_CLK | I | K1 | TX_DATA and TX_DATAK clock for source synchronous PIPE. This clock frequency is the same as PCLK frequency. The rising edge of the clock is the reference for all signals. |
| TX_DATA15 | I | G2 | Parallel USB SuperSpeed data input bus.<br>The 16 bits represent 2 symbols of transmit data where TX_DATA7-0 is the first symbol to be transmitted, and TX_DATA15-8 is the second symbol. |
| TX_DATA14 | | H2 | |
| TX_DATA13 | | H1 | |
| TX_DATA12 | | J2 | |
| TX_DATA11 | | L3 | |
| TX_DATA10 | | L2 | |
| TX_DATA9 | | M2 | |
| TX_DATA8 | | M1 | |
| TX_DATA7 | | N1 | |
| TX_DATA6 | | P1 | |
| TX_DATA5 | | N2 | |
| TX_DATA4 | | P2 | |
| TX_DATA3 | | N3 | |
| TX_DATA2 | | P3 | |
| TX_DATA1 | | N4 | |
| TX_DATA0 | | P5 | |
| TX_DATAK1 | I | G1 | Data/Control for the symbols of transmit data. TX_DATAK0 corresponds to the low-byte of TX_DATA, TX_DATAK1 to the upper byte. |
| TX_DATAK0 | | J1 | |
| PCLK | O | A6 | Parallel interface data clock. All data movement across the parallel PIPE is synchronous to this clock. This clock operates at 250 MHz. The rising edge of the clock is the reference for all signals. |


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**Table 2-2. PIPE Signal Description (continued)**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| RX_DATA15 | O | B9 | Parallel USB SuperSpeed data output bus. The 16 bits represent 2 symbols of receive data where RX_DATA7-0 is the first symbol received, and RX_DATA15-8 is the second. |
| RX_DATA14 | | A9 | |
| RX_DATA13 | | A8 | |
| RX_DATA12 | | B8 | |
| RX_DATA11 | | B5 | |
| RX_DATA10 | | B4 | |
| RX_DATA9 | | A4 | |
| RX_DATA8 | | B3 | |
| RX_DATA7 | | A3 | |
| RX_DATA6 | | A2 | |
| RX_DATA5 | | B1 | |
| RX_DATA4 | | C2 | |
| RX_DATA3 | | C1 | |
| RX_DATA2 | | D1 | |
| RX_DATA1 | | D2 | |
| RX_DATA0 | | E2 | |
| RX_DATAK1 | O | B7 | Data/Control for the symbols of receive data. RX_DATAK0 corresponds to the low-byte of RX_DATA, RX_DATAK1 to the upper byte. A value of zero indicates a data byte; a value of 1 indicates a control byte. |
| RX_DATAK0 | | A7 | |
| RX_VALID | O | F1 | Active High. Indicates symbol lock and valid data on RX_DATA and RX_DATAK. |
| **CONTROL AND STATUS SIGNALS** | | | |
| PHY_RESETN | I, PU | J3 | Active Low. Resets the transmitter and receiver. This signal is asynchronous. |
| TX_DETRX_LPBK | I, PD | M6 | Active High. Used to tell the PHY to begin a receiver detection operation or to begin loopback. |
| TX_ELECIDLE | I | K3 | Active High. Forces TX output to electrical idle depending on the power state. |
| RX_ELECIDLE | S, I/O, PD | F3 | Active High. While de-asserted with the PHY in P0, P1, P2, or P3, indicates detection of LFPS. |
| RX_STATUS2 | O | C7 | Encodes receiver status and error codes for the received data stream when receiving data. |
| RX_STATUS1 | | C6 | |
| RX_STATUS0 | | C5 | |

| BIT 2 | BIT 1 | BIT 0 | DESCRIPTION |
|---|---|---|---|
| 0 | 0 | 0 | Received data OK |
| 0 | 0 | 1 | 1 SKP ordered set added |
| 0 | 1 | 0 | 1 SKP ordered set removed |
| 0 | 1 | 1 | Receiver detected |
| 1 | 0 | 0 | 8B/10B decode error |
| 1 | 0 | 1 | Elastic buffer overflow |
| 1 | 1 | 0 | Elastic buffer underflow. This error code is not used if the elasticity buffer is operating in the nominal buffer empty mode. |
| 1 | 1 | 1 | Receive disparity error |

| POWER_DOWN1 | I | G3 | Power up and down the transceiver power states. |
|---|---|---|---|
| POWER_DOWN0 | | H3 | |

| BIT 1 | BIT 0 | DESCRIPTION |
|---|---|---|
| 0 | 0 | P0, normal operation |
| 0 | 1 | P1, low recovery time latency, power saving state |
| 1 | 0 | P2, longer recovery time latency, low power state |
| 1 | 1 | P3, lowest power state |

When transitioning from P3 to P0, the signaling is asynchronous.

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**Table 2-2. PIPE Signal Description (continued)**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| PHY_STATUS | S, I/O, PD | E3 | Active High. Used to communicate completion of several PHY func-tions including power management state transitions, rate change, and receiver detection. When this signal transitions during entry and exit from P3 and PCLK is not running, then the signaling is asynchronous. |
| PWRPRESENT | O | H11 | Indicates the presence of VBUS |
| **CONFIGURATION PINS** | | | |
| TX_ONESZEROS | I, PD | M4 | Active High. Used only when transmitting USB compliance pat-terns CP7 or CP8. Causes the transmitter to transmit an alternating sequence of 50 - 250 ones and 50 - 250 zeros – regardless of the state of the TX_DATA interface. |
| TX_DEEMPH1<br>TX_DEEMPH0 | I, PD, PU | K11<br>L11 | Selects transmitter de-emphasis. When the MAC changes, the TUSB1310 starts to transmit with the new setting within 128 ns. |

| BIT 1 | BIT 0 | DESCRIPTION |
|---|---|---|
| 0 | 0 | -6 dB de-emphasis |
| 0 | 1 | -3.5 dB de-emphasis |
| 1 | 0 | No de-emphasis |
| 1 | 1 | Reserved |

TX_MARGIN2, TX_MARGIN1, TX_MARGIN0 — I, PD — M11, M10, M9 — Selects transmitter voltage levels

| BIT 2 | BIT 1 | BIT 0 | TX_SWING | DESCRIPTION |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Normal operating range<br>800 mV - 1200 mV |
| 0 | 0 | 0 | 1 | Normal operating range<br>400 mV - 700 mV |
| 0 | 0 | 1 | 0 | 800 mV - 1200 mV |
| | | | 1 | 400 mV - 700 mV |
| 0 | 1 | 0 | 0 | 700 mV - 900 mV |
| | | | 1 | 300 mV - 500 mV |
| 0 | 1 | 1 | 0 | 400 mV - 600 mV |
| | | | 1 | 200 mV - 400 mV |
| 1 | Don't care | | 0 | 200 mV - 400 mV |
| 1 | | | 1 | 100 mV - 200 mV |

| | | | |
|---|---|---|---|
| TX_SWING | I, PD | M5 | Controls transmitter voltage swing level<br>0 Full swing<br>1 Half swing |
| RX_POLARITY | I, PD | C8 | Active High. Tells PHY to do a polarity inversion on the received data. Inverted data show up on RX_DATA15-0 within 20 PCLK clocks after RX_POLARITY is asserted.<br>0 PHY does no polarity inversion.<br>1 PHY does polarity inversion. |
| RX_TERMINATION | I, PD | D3 | Controls presence of receiver terminations<br>0 Terminations removed<br>1 Terminations present |
| RATE | I, PU | L6 | Controls the link signaling rate<br>The RATE is always 1. |
| ELAS_BUF_MODE | I, PD | C9 | Selects elasticity buffer operating mode<br>0 Nominal half full buffer mode<br>1 Nominal empty buffer mode |


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## 2.3 ULPI

The ULPI (ultra low pin count interface) is a low pin count USB PHY to a link layer controller interface. The ULPI consists of the interface and the ULPI registers. The TUSB1310 is always the master of the ULPI bus.

**Table 2-3. ULPI Signal Description**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| ULPI_CLK | O | P11 | 60-MHz interface clock. All ULPI signals are synchronous to ULPI_CLK. The ULPI_CLK is always a 60-MHz output of the TUSB1310. In low power mode, the ULPI_CLK is not driven. |
| ULPI_DATA7 | S, I/O, PD | N6 | Data bus. Driven to 00h by the Link when the ULPI bus is idle.<br>8-bit data timed on rising edge of ULPI_CLK |
| ULPI_DATA6 | | P6 | |
| ULPI_DATA5 | | N7 | |
| ULPI_DATA4 | | P7 | |
| ULPI_DATA3 | | N8 | |
| ULPI_DATA2 | | P8 | |
| ULPI_DATA1 | | P9 | |
| ULPI_DATA0 | | N9 | |
| ULPI_DIR | O | M7 | Controls the direction of the ULPI_DATA bus<br>0 ULPI_DATA lines are inputs<br>1 ULPI_DATA lines are outputs |
| ULPI_STP | S, I, PU | M8 | Active High. The Link must assert ULPI_STP to signal the end of a USB transmit packet or a register write operation. The ULPI_STP signal must be asserted in the cycle after the last data byte is presented on the bus. The ULPI_STP has an internal weak pull-up to safeguard against false commands on the ULPI_DATA lines. |
| ULPI_NXT | O | N11 | Active High. The PHY asserts ULPI_NXT to throttle all data types, except register read data and the RX CMD. The PHY also asserts ULPI_NXT and ULPI_DIR simultaneously to indicate USB receive activity, if ULPI_DIR was previously low. The PHY is not allowed to assert ULPI_NXT during the first cycle of the TX CMD driven by the Link. |

### *2.3.1 ULPI Modes*

The TUSB1310 supports synchronous mode and low power mode. The default mode is synchronous mode.

The synchronous mode is a normal operation mode. The ULPI_DATA are synchronous to ULPI_CLK. The low power mode is used during power down and no ULPI_CLK. The TUSB1310 sets ULPI_DIR to output and drives LineState signals and interrupts.

**Table 2-4. ULPI Synchronous and Low Power Mode Functions**

| SYNCHRONOUS | LOW POWER |
|---|---|
| ULPI_CLK(OUT) | |
| ULPI_DATA7(I/O) | |
| ULPI_DATA6(I/O) | |
| ULPI_DATA5(I/O) | |
| ULPI_DATA4{I/O} | |
| ULPI_DATA3(I/O) | ULPI_INT (OUT) |
| ULPI_DATA2(I/O) | |
| ULPI_DATA1(I/O) | ULPI_LINESTATE1(OUT) |
| ULPI_DATA0(I/O) | ULPI_LINE_STATE0 (OUT) |
| ULPI_DIR(OUT) | |
| ULPI_STP(IN) | |
| ULPI_NXT(OUT) | |

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## 2.4 Clocking

**Table 2-5. Clock Signal Name Description**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| XI | I | A12 | Crystal Input. This pin is the clock reference input for the TUSB1310. The TUSB1310 supports either a crystal unit, or a 1.8-V clock input. Frequencies supported are 20, 25, 30, or 40 MHz. |
| XO | O | A11 | Crystal output. If a 1.8-V clock input is connected to XI, XO must be left open. |
| CLKOUT | O | D10 | OOBCLK is driven in U3 mode. |

## 2.5 JTAG Interface

The JTAG Interface is used for board-level boundary scan. All digital IO support IEEE1149.1 boundary scan and SuperSpeed differential pairs support IEEE1149.6 boundary scan.

**Table 2-6. JTAG Signal Name Description**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| JTAG_TCK | I, PU | G11 | JTAG test clock |
| JTAG_TMS | I, PU | D11 | JTAG test mode select |
| JTAG_TDI | I, PU | E11 | JTAG test data input |
| JTAG_TRSTN | I, PD | E12 | JTAG test asynchronous reset. Active Low. |
| JTAG_TDO | O | F11 | JTAG test data output |

## 2.6 Reset and Output Control Interface

**Table 2-7. Reset and Output Control Signal Description**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| RESETN | I | J11 | Active Low. Resets the transmitter and receiver. This signal is asynchronous. |
| OUT_ENABLE | I | L10 | Active High. This can be connected to a 1.8-V power on reset signal on the PCB in order to avoid static current and signal contention during power up.<br>0: Disable all driver outputs while IO powers are supplied, but internal control circuit powers are not present during power up.<br>1: Enable all driver outputs during normal operation. |

## 2.7 Strap Options

Strapping pins are latched by reset de-assertion in the TUSB1310.

**Table 2-8. Strapping Options**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| XTAL_DIS<br>(RX_ELECIDLE) | S, I/O, PD | F3 | Selects an input clock source<br>0 Crystal Input<br>1 Clock Input |
| PIPE_16BIT<br>(PHY_STATUS) | S, I/O, PD | E3 | Selects PIPE<br>0 16-bit PIPE SDR mode<br>Must be 0 at reset. |
| ISO_START<br>(ULPI_DATA7) | S, I/O, PD | N6 | Active High. Puts PIPE into isolate mode. When in the isolate mode, TUSB1310 does not respond to packet data present at TX_DATA15-0, TXDATAK1-0 inputs and presents a high imped-ance on the PCLK, RX_DATA15-0, RX_DATAK1-0, RX_VALID outputs. When in the isolate mode, the TUSB1310 will continue to respond to ULPI. Once the isolate mode bit in ULPI register is cleared, the USB interfaces will start transmitting packet data on TX_DATA15-0 and driving PCLK, RX_DATA15-0, RX_DATA1-0, and RX_VALID. |


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**Table 2-8. Strapping Options (continued)**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| ULPI_8BIT<br>(ULPI_DATA6) | S, I/O, PD | P6 | Selects ULPI data bus bit width<br>0 8-bit ULPI SDR mode<br>Must be set to 0. |
| REFCLKSEL1,<br>REFCLKSEL0<br>(ULPI_DATA5,<br>ULPI_DATA4) | S, I/O, PD | N7<br>P7 | Select input reference clock frequency for on-chip oscillator<br>00 20 MHz on XI<br>01 25 MHz on XI<br>10 30 MHz on XI<br>11 40 MHz on XI |

## 2.8 USB Interfaces

**Table 2-9. USB Interface Signal Name Descriptions**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| SSTXP<br>SSTXM | O | H14<br>J14 | USB SuperSpeed transmitter differential pair |
| SSRXP<br>SSRXM | I | E14<br>F14 | USB SuperSpeed receiver differential pair |
| DP<br>DM | I/O | P14<br>P13 | USB non-SuperSpeed differential pair |
| VBUS | I | N12 | USB VBUS pin<br>Connected through an external voltage divider. |

## 2.9 Special Connect

**Table 2-10. Special Connect Signal Descriptions**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| R1EXT | O | L14 | High precision external resistor used for calibration. The R1 value shall be 10 kΩ ±1% accuracy. |
| R1EXTRTN | I | L13 | R1 ground reference. This pin is not connected to board ground. |
| CEXT | O | M14 | Connected to an external 4.7-nF capacitor |
| CEXTSS | O | A14 | Connected to an external 4.7-nF capacitor |
| RSVD | I/O | D6<br>D5<br>C13<br>C14<br>K4<br>J4 | Must be left open. |

## 2.10 Power and Ground

**Table 2-11. Power/Ground Signal Descriptions**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| VDDA3P3 | P | P12 | Analog 3.3-V power supply |
| VDDA1P8 | P | N14<br>A13<br>C10 | Analog 1.8-V power supply |

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**Table 2-11. Power/Ground Signal Descriptions (continued)**

| SIGNAL NAME | TYPE | BALL NO. | DESCRIPTION |
|---|---|---|---|
| VDDA1P1 | P | C12<br>K14<br>G13<br>G14<br>D14<br>C11 | Analog 1.1-V power supply |
| VDD1P8 | P | B2 C3<br>D4 D7<br>D8 D9<br>E4 F4<br>G4 H4<br>L5 L4<br>M3 L7<br>L8 L9 | Digital IO 1.8-V power supply |
| VDD1P1 | P | A5 A10<br>B6 B10<br>E1 F2<br>K2 L1<br>N5 P4<br>N10 P10<br>K13 D13<br>C4 | Digital 1.1-V power supply |
| VSSA | G | B14 B13<br>J13 H13<br>F13 E13<br>K12 L12<br>G12<br>D12<br>N13<br>M12<br>M13 | Analog ground |
| VSSOSC | G | B12 | Oscillator ground<br>If using a crystal, this should not be connected to PCB ground plane.<br>See Chapter 5 for guidelines.<br>If using an oscillator, this should be connected to PCB ground. |
| VSS | G | F6 F7<br>F8 F9<br>G6 G7<br>G8 G9<br>J6 J7<br>H6 H7<br>H8 H9<br>J8 J9<br>B11 F12 | Digital ground |


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# 3 FUNCTIONAL DESCRIPTION

## 3.1 Power On and Reset

The TUSB1310 has two hardware reset pins, a chip reset RESETN and a logic reset PHY_RESETN. The RESETN is used only at Power On. The PHY_RESETN can be used as a functional reset. The ULPI register also has a software reset.

Until all power sources are supplied, the OUT_ENABLE pin can control the output driver enable. After all power sources are supplied, the chip reset RESETN and a ULPI soft reset will be asserted by the link layer. The power up sequence is described in section 3.1.4.

### *3.1.1 RESETN and PHY_RESETN – Hardware Reset*

The RESETN sets all internal states to initial values. The link layer needs to hold the PHY in reset via the RESETN until all power sources and the reference clock to the TUSB1310 are stable. All pins used for strapping options must be set before RESETN de-assertion. All strapping option pins have internal pull-up or pull-down to set default values, but if any non-default values are desired, they need to be controlled externally by the link layer controller.

**Table 3-1. Pin States in Chip Reset**

| PIPE CONTROL PIN NAME | STATE | VALUE |
|---|---|---|
| TX_DETRX_LPBK | Inactive | 0 |
| TX_ELECIDLE | Active | 1 |
| TX_COMPLIANCE | Inactive | 0 |
| RX_POLARITY | Inactive | 0 |
| POWER_DOWN | U2 | 10b |
| TX_MARGIN2-0 | Normal operating range | 000b |
| TX_DEEMP | -3.5 dB | 1 |
| RATE | 5.0 Gbps | 1 |
| TX_SWING | Full swing or half swing | 0 or 1 |
| RX_TERMINATION | Appropriate state | 0 or 1 |

### *3.1.2 ULPI Reset – Software Reset*

After power-up, the link layer controller must set the Reset bit in ULPI register. It resets the core but does not reset the ULPI interface or the ULPI registers.

During the ULPI reset, the ULPI_DIR is de-asserted. After the reset, the ULPI_DIR is asserted again and the TUSB1310 sends an RX CMD update to the link layer. During the reset, the link should ignore signals on the ULPI_DATA7-0 and must not access the TUSB1310.

### *3.1.3 OUT_ENABLE - Output Enable*

Digital IO buffers use two power supplies, core VDD1P1 and IO VDD1P8. During power up, OUT_ENABLE must be asserted low for proper operation.

### *3.1.4 Power Up Sequence*

The power up sequence is shown in Figure 3-1.

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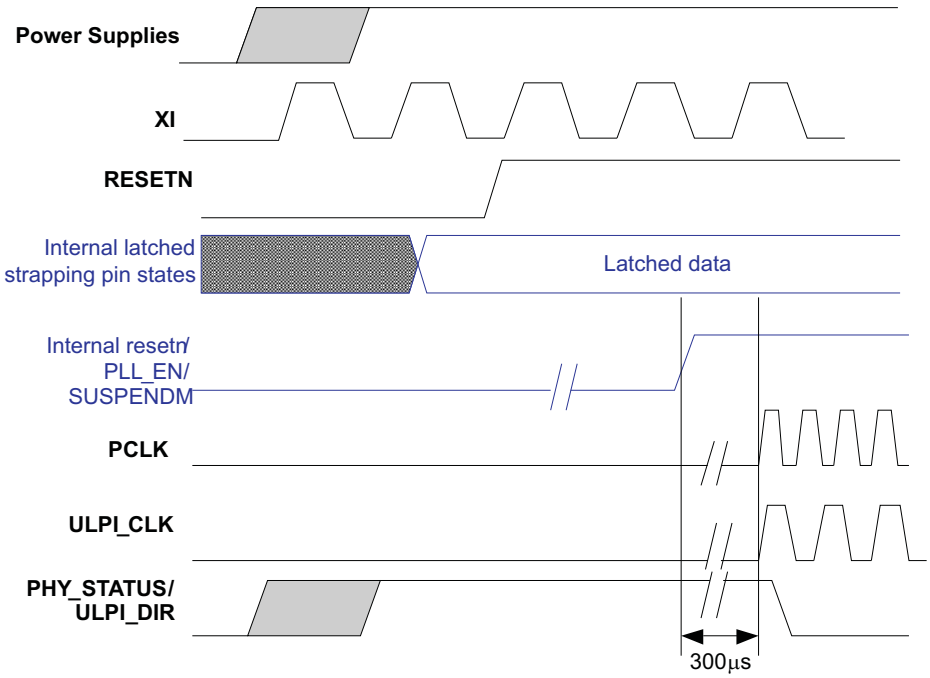



**Figure 3-1. Power Up Sequence**

After proper power supply sequencing, the reference clock on XI starts to operate. On the RESETN de-assertion, REFCLKSEL1-0 is determined depending on the PHY_MODE pins, PLL is locked and the valid ULPI_CLK and the valid PCLK are driven.

After all stable clocks are provided, the TUSB1310 allows the link layer controller to access by de-asserting the ULPI_DIR. The link layer controller sets the Reset bit in the ULPI register. At the PIPE in-terface, the PHY_STATUS changes from high to low in order to indicate the TUSB1310 is in the power state specified by the POWER_DOWN signal. After the PHY_STATUS change, the TUSB1310 is ready for PIPE transactions.

## 3.2 Clocks

### *3.2.1 Clock Distribution*

A source clock should be provided via XI/XO from an external crystal or from a square wave clock. The USB3.0 PLL provides a clock to the PIPE which drives 250 MHz. The USB2.0 PLL provides a 60-MHz clock to the ULPI.

### *3.2.2 Output Clock*

The CLKOUT is used by the link layer controller or the MAC. When ClkoutEn bit at the ULPI SS USB register is set low, a 120-MHz clock is available via the CLKOUT only in the USB U3 power state. If the ClkoutEn bit is set high, the 250-MHz clock is driven via CLKOUT in all power states.

## 3.3 Power Management

The SuperSpeed USB power state transition is controlled by the PIPE POWER_DOWN1-0 and the non-SuperSpeed USB power state is transitioned by setting suspendM bit in the ULPI Function control register via the ULPI or by asserting the ULPI_STP.


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### 3.3.1 USB Power Management

The USB 3.0 specification improves power consumption by defining 4 power states, U0, U1, U2, and U3 while the PIPE specification defines P0, P1, P2 and P3. The POWER_DOWN pin states are mapped to LTSSM states as described in Table 2-10. For all power state transitions, the link layer controller must not begin any operational sequences or further power state transitions until the TUSB1310 has indicated that the internal state transition is completed.

**Table 3-2. Power States**

| PIPE POWER STATE | USB POWER STATE | PCLK | PLL | TRANSMITTING | RECEIVING | PHY_STATUS |
|---|---|---|---|---|---|---|
| P0 | U0, all other LTSSM states | On | On | Active or Idle or LFPS | Active or Idle | A single cycle assertion |
| P1 | U1 | On | On | Idle or LFPS | Idle | A single cycle assertion |
| P2 | U2, RxDetect, SS.Inactive | On | On | Idle or LFPS or RxDetect | Idle | A single cycle assertion |
| P3 | U3, SS.disabled | Off. The PIPE is in an asynchronous mode | Off | LFPS or RxDetect | Idle | PHY_STATUS is asserted before PCLK is turned off and deasserted when PCLK is fully off. |

When the link layer controller wants to transmit LFPS in P1, P2, or P3 state, it must de-assert TX_ELECIDLE. The TUSB1310 generates valid LFPS until the TX_ELECIDLE is asserted. The link layer controller must assert TX_ELECIDLE before transitioning to P0.

When RX_ELECIDLE is de-asserted in P0, P1, P2, or P3, the TUSB1310 receiver monitors for LFPS except during reset or when RX_TERMINATION is removed for electrical idle.

When the TUSB1310 is in P0 and is actively transmitting; only RX_POLARITY can be asserted.

**Table 3-3. PIPE Control Pin Matrix**

| POWER STATE | TX_DETRX_LPBK | TX_ELECIDLE | DESCRIPTION |
|---|---|---|---|
| P0 | 0 | 0 | Transmitting data on TX_DATA |
| | 0 | 1 | Not transmitting and is in electrical idle. |
| | 1 | 0 | Goes into loopback mode |
| | 1 | 1 | Transmits LFPS signaling |
| P1 | Don't care | 0 | Transmits LFPS signaling |
| | | 1 | Not transmitting and is in electrical idle. |
| P2 | Don't care | 0 | Transmits LFPS signaling |
| | 0 | 1 | Idle |
| | 1 | 1 | Does a receiver detection operation |
| P3 | Don't care | 0 | Transmits LFPS signaling |
| | | 1 | Does a receiver detection operation |

## 3.4 Receiver Status

The TUSB1310 has an elastic buffer for clock tolerance compensation, the link partner detection, and some received data error detections. The receive data status from SSRXP/SSRXN differential pair presents on RX_STATUS2-0. If an error occurs during a SKP ordered set, the error signaling has precedence. If more than one error occurs on a received byte, the errors have the priority below.

1. 8B/10B decode error
2. Elastic buffer overflow

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3. Elastic buffer underflow (can not occur in nominal empty buffer model)
4. Disparity error

### 3.4.1 Clock Tolerance Compensation

The receiver contains an elastic buffer used to compensate for differences in frequencies between bit rates at the two ends of a link. The elastic buffer must be capable of holding enough symbols to handle worst case differences in frequency and worst case intervals between SKP ordered sets. A SKP order set is a set of symbols transmitted as a group. The SKP ordered sets allows the receiver to adjust the data stream being received to prevent the elastic buffer from either overflowing or under-flowing due to any clock tolerance differences.

The TUSB1310 supports two models, nominal half full buffer model and nominal empty buffer mode. For the nominal half full buffer model, the TUSB1310 monitors the receive data stream. When a Skip ordered set is received, the TUSB1310 adds or removes one SKP order set from each SKP to manage its elastic buffer to keep the buffer as close to half full as possible. Only full SKP ordered sets are added or removed. When a SKP order set is added, the TUSB1310 asserts an “Add SKP” code (001b) on the RX_STATUS for one clock cycle. When a SKP order set is removed, the RX_STATUS is has a “Remove SHP” code (010b).

For the nominal empty buffer model the TUSB1310 attempts to keep the elasticity buffer as close to empty as possible. When no SKP ordered sets have been received, the TUSB1310 will be required to insert SKP ordered sets into the received data stream.

**Table 3-4. RX_STATUS - SKP**

| RX_STATUS2-0 | SKP ADDITION or REMOVAL | LENGTH |
|---|---|---|
| 001b | 1 SKP ordered set added | One clock cycle |
| 010b | 1 SKP ordered set removed | |

### 3.4.2 Receiver Detection

TX_DETRX_LPBK starts a receiver detection operation to determine if there is a receiver at the other end of the link. When the receiver detect sequence completes, the PHY_STATUS is asserted for one clock and drives the RX_STATUS signals to the appropriate code. Once the TX_DETRX_LPBK signal is asserted, the link layer controller must leave the signal asserted until the PHY_STATUS pulse. When receiver detection is performed in P3, the PHY_STATUS shows the appropriate receiver detect value until the TX_DETRX_LPBK is de-asserted.

**Table 3-5. RX_STATUS - Receiver Detection**

| RX_STATUS2-0 | DETECTED CONDITION | LENGTH |
|---|---|---|
| 000b | Receiver not present | One clock cycle |
| 011b | Receiver present | |

### 3.4.3 8b/10b Decode Errors

When the TUSB1310 detects an 8b/10b decode error, it will assert an EDB (0xFE) symbol in the data on the RX_DATA where the bad byte occurred. In the same clock cycle that the EDB symbol is asserted on the RX_DATA, the 8b/10b decode error code (100b) will be asserted on the RX_STATUS. 8b/10b decoding error has priority over all other receiver error codes and could mask out a disparity error occurring on the other byte of data being clocked onto the RX_DATA with the EDB symbol.


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**Table 3-6. 8b/10b Decode Errors**

| RX_STATUS2-0 | DETECTED ERROR | LENGTH |
|---|---|---|
| 100b | 8B/10B decode error | Clock cycles during the effected byte is transferred on RX_DATA15-0 |

### 3.4.4 Elastic Buffer Errors

When the elastic buffer overflows, data is lost during the reception of the data. The elastic buffer overflow error code (101b) will be asserted on the RX_STATUS on the PCLK cycle the omitted data would have been asserted. The data asserted on the RX_DATA is still valid data, the elastic buffer overflow error code on the RX_STATUS just marks a discontinuity point in the data stream being received.

When the elastic buffer underflows, EDB (0xFE) symbols are inserted into the data stream on the RX_DATA to fill the holes created by the gaps between valid data. For every PCLK cycle a EDB symbol is asserted on the RX_DATA, an elastic buffer underflow error code (111b) is asserted on the RX_STATUS. In nominal empty buffer mode, SKP ordered sets are transferred on RX_DATA and the underflow is not signaled.

**Table 3-7. Elastic Buffer Errors**

| RX_STATUS2-0 | DETECTED ERROR | LENGTH |
|---|---|---|
| 101b | Elastic buffer overflow | Clock cycles the omitted data would have appeared |
| 110b | Elastic buffer underflow | Clock cycles during the EDB symbol presence on RX_DATA15-0 |

### 3.4.5 Disparity Errors

When the TUSB1310 detects a disparity error, it will assert a disparity error code (111b) on the RX_STATUS in the same PCLK cycle it asserts the erroneous data on the RX_DATA. The disparity code does not discern which byte on the RX_DATA is the erroneous data.

**Table 3-8. Disparity Errors**

| RX_STATUS2-0 | DETECTED ERROR | LENGTH |
|---|---|---|
| 111b | Disparity error | Clock cycles during the ef-fected byte is transferred on RX_DATA15-0 |

## 3.5 Loopback

The TUSB1310 begins an internal loopback operation from SSRXP/SSRXN differential pairs to SSTXP/SSTXN differential pairs when the TX_DETRX_LPBK is asserted while holding TX_ELECIDLE de-asserted. The TUSB1310 will stop transmitting data to the SSTXP/SSTXN signaling pair from the TX_DATA and begin transmitting on the SSTXP/SSTXN signaling pair the data received at the SSRXP/SSRXN signaling pair. This data is not routed through the 8b/10b coding/encoding paths. While in the loopback operation, the received data is still sent to the RX_DATA. The data sent to the RX_DATA is routed through the 10b/8b decoder.

The TX_DETRX_LPBK de-assertion will terminate the loopback operation and return to transmitting TX_DATA over the SSTXP/SSTXN signaling pair. The TUSB1310 only transitions out of loopback on detection of LFPS signaling by transitioning to P2 state and starting the LFPS handshake.

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# 4 REGISTERS

## 4.1 Register Definitions

**Table 4-1. Register Definitions**

| ACCESS CODE | EXPANDED NAME | DESCRIPTION |
|---|---|---|
| Rd | Read | Register can be read. Read only if this is the only mode given. |
| Wr | Write | Pattern on the data bus will be written over all bits of the register. |
| S | Set | Pattern on the data bus is OR'ed with and written into the register. |
| C | Clear | Pattern on the data bus is a mask. If a bit in the mask is set, then the corresponding register bit will be set to zero(cleared). |

## 4.2 Register Map

The TUSB1310 contains the ULPI registers consisting of an immediate register set and an extended register set.

**Table 4-2. Register Map**

| REGISTER NAME | ADDRESS (6 BITS) | | | |
|---|---|---|---|---|
| | Rd | Wr | Set | Clr |
| **IMMEDIATE REGISTER SET** | | | | |
| Vendor ID low | 00h | | | |
| Vendor ID high | 01h | | | |
| Product ID low | 02h | | | |
| Product ID high | 03h | | | |
| Function control | 04h-06h | 04h | 05h | 06h |
| Interface control | 07h-09h | 07h | 08h | 09h |
| OTG Control | 0Ah-0Ch | 0Ah | 0Bh | 0Ch |
| USB Interrupt Enable Rising | 0Dh-0Fh | 0Dh | 0Eh | 0Fh |
| USB Interrupt Enable Falling | 10h-12h | 10h | 11h | 12h |
| USB Interrupt Status | 13h | 13h | | |
| USB Interrupt Latch | 14h | 14h | | |
| Debug | 15h | | | |
| Scratch register | 16h-18h | 16h | 17h | 18h |
| Reserved | 19h-2Eh | | | |


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### 4.2.1 Vendor ID and Product ID (00h-03h)

**Table 4-3. Vendor ID and Product ID**

| ADDRESS | BITS | NAME | ACCESS | RESET | DESCRIPTION |
|---|---|---|---|---|---|
| 00h | 7:00 | Vendor ID low | Rd | 51h | Lower byte of vendor ID supplied by USB-IF |
| 01h | 7:00 | Vendor ID high | Rd | 04h | Upper byte of vendor ID supplied by USB-IF |
| 02h | 7:00 | Product ID low | Rd | 10h | Lower byte of vendor ID supplied by vendor |
| 03h | 7:00 | Product ID high | Rd | 13h | Upper byte of vendor ID supplied by vendor |

### 4.2.2 Function Control (04h-06h)

Address: 04h-06h (Read), 04h (Write), 05h (Set), 06h (Clear)

**Table 4-4. Function Control**

| BITS | NAME | ACCESS | RESET | DESCRIPTION |
|---|---|---|---|---|
| 1:00 | XcvrSelect | Rd/Wr/S/C | 1h | Selects the required transceiver speed<br>00b : Enable HS transceiver<br>01b: Enable FS transceiver<br>10b: Enable LS transceiver<br>11b: Enable FS transceiver for LS packets<br>(FS preamble is automatically pre-pended) |
| 2 | TermSelect | Rd/Wr/S/C | 0 | Controls the internal 1.5-kΩ pullup resister and 45-Ω HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown. Since low speed peripherals never support full speed or hi-speed, providing the 1.5 kΩ on DM for low speed is optional. |
| 4:03 | OpMode | Rd/Wr/S/C | 0 | Selects the required bit encoding style during transmit<br>00 : Normal operation<br>01: Non-driving<br>10: Disable bit-stuff and NRZI encoding<br>11: Do not automatically add SYNC and EOP when transmitting. Must be used only for HS packets. |
| 5 | Reset | Rd/Wr/S/C | 0 | Active High transceiver reset. After the Link sets this bit, the TUSB1310 must assert the ULPI_DIR and reset the ULPI. When the reset is completed, the PHY de-asserts the ULPI_DIR and automatically clears this bit. After de-asserting the ULPI_DIR, the PHY must re-assert the ULPI_DIR and send an RX CMD update on the link layer controller. The link layer controller must wait for the ULPI_DIR to de-assert before using the ULPI bus. Does not reset the ULPI or ULPI register set. |
| 6 | SuspendM | Rd/Wr/S/C | 1h | Active low PHY suspend. Put the TUSB1310 into low power mode. The PHY can power down all blocks except the full speed receiver, OTG comparators, and the ULPI pins. The PHY must automatically set this bit to '1' when low power mode is exited.<br>0: Low power mode<br>1: Powered |
| 7 | Reserved | Rd | 0 | Reserved |

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### 4.2.3 Interface Control (07h-09h)

Address: 07-09h (Read), 07h (Write), 08h (Set), 09h (Clear)

**Table 4-5. Interface Control**

| BITS | NAME | ACCESS | RESET | DESCRIPTION |
|---|---|---|---|---|
| 0 | Reserved | Rd | 0b | Reserved, only write a 0 to this bit. |
| 1 | Reserved | Rd | 0b | Reserved, only write a 0 to this bit. |
| 2 | Reserved | Rd | 0h | Reserved |
| 3 | ClockSuspendM | Rd/Wr/S/C | 0b | Active low clock suspend. Valid only in serial mode. Powers down the internal clock circuitry only. Valid only when SuspendM = 1. The TUSB1310 must ignore ClockSuspend when SuspendM = 0. By default, the clock will not be powered in serial mode.<br>0 : Clock will not be powered in serial mode<br>1 : Clock will be powered in serial mode |
| 6:04 | Reserved | Rd | 0h | Reserved |
| 7 | Interface protect disable | Rd/Wr/S/C | 0 | Controls internal pullups and pulldowns on the ULPI_STP and the ULPI_DATA for protecting the ULPI when the link layer controller tri-states the signals.<br>0 enables the pullup and pulldown<br>1 disables the pullup and pulldown |

### 4.2.4 OTG Control

Address: 0Ah-0Ch (Read), 0Ah (Write), 0Bh (Set), 0Ch (Clear). Controls UTMI+ OTG functions of the PHY.

**Table 4-6. OTG Control Register**

| BITS | NAME | ACCESS | RESET | DESCRIPTION |
|---|---|---|---|---|
| 0 | Reserved | Rd | 0b | This bit is not implemented and returns a 0b when read. |
| 1 | DpPulldown | Rd/Wr/S/C | 1b | Enables the 15-kΩ pull-down resistor on D+.<br>0 Pull-down resistor not connected to D+<br>1 Pull-down resistor connected to D+ |
| 2 | DmPulldown | Rd/Wr/S/C | 1h | Enables the 15-kΩ pull-down resistor on D-.<br>0 Pull-down resistor not connected to D-<br>1 Pull-down resistor connected to D- |
| 7:3 | Reserved | Rd | 0h | These bits are not implemented and return zeros when read. |

### 4.2.5 USB Interrupt Enable Rising (0Dh-0Fh)

Address: 0D-0Fh (Read), 0Dh (Write), 0Eh (Set), 0Fh (Clear)

**Table 4-7. USB Interrupt Enable Rising**

| BITS | NAME | ACCESS | RESET | DESCRIPTION |
|---|---|---|---|---|
| 0 | Hostdisconnect Rise | Rd/Wr/S/C | 1b | Generate an interrupt event notification when Hostdisconnect changes from low to high Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). |


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### 4.2.6 USB Interrupt Enable Falling (10h-12h)

Address: 10-12h (Read), 10h (Write), 11h (Set), 12h (Clear)

**Table 4-8. USB Interrupt Enable Falling**

| BITS | NAME | ACCESS | RESET | DESCRIPTION |
|---|---|---|---|---|
| 0 | Hostdisconnect Fall | Rd/Wr/S/C | 1b | Generate an interrupt event notification when Host-disconnect changes from high to low. Applicable only in host. |

### 4.2.7 USB Interrupt Status (13h)

Address: 13h (Read-only)

**Table 4-9. USB Interrupt Status**

| BITS | NAME | ACCESS | RESET | DESCRIPTION |
|---|---|---|---|---|
| 0 | Hostdisconnect Fall | Rd/Wr/S/C | 1b | Generate an interrupt event notification when Host-disconnect changes from high to low. Applicable only in host. |

### 4.2.8 USB Interrupt Latch (14h)

Address: 14h (Read-only with auto-clear)

**Table 4-10. USB Interrupt Latch**

| BITS | NAME | ACCESS | RESET | DESCRIPTION |
|---|---|---|---|---|
| 0 | Hostdisconnect Fall | Rd/Wr/S/C | 1b | Set to 1b by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode. |

### 4.2.9 Debug (15h)

Address: 15h (Read-only)

**Table 4-11. Debug**

| BITS | NAME | ACCESS | RESET | DESCRIPTION |
|---|---|---|---|---|
| 0 | LineState0 | Rd | 0 | Contains the current value of LineState0 |
| 1 | LineState1 | Rd | 0 | Contains the current value of LineState0 |
| 07:2 | Reserved | Rd | 0 | Reserved |

### 4.2.10 Scratch Register (16-18h)

Address: 16-18h (Read), 16h (Write), 17h (Set), 18h (Clear)

**Table 4-12. Scratch Register**

| BITS | NAME | ACCESS | RESET | DESCRIPTION |
|---|---|---|---|---|
| 7:0 | Scratch | Rd/Wr/S/C | 00 | Empty register byte for testing purposes. Software can read, write, set, and clear this register and the TUSB1310 functionality will not be affected. |

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# 5 DESIGN GUIDELINES

## 5.1 Chip Connection on PCB

Components should be placed close to the TUSB1310 to reduce the trace length of the interface between the components and the TUSB1310. If external capacitors can not accommodate a close placement, shielding to ground is recommended.

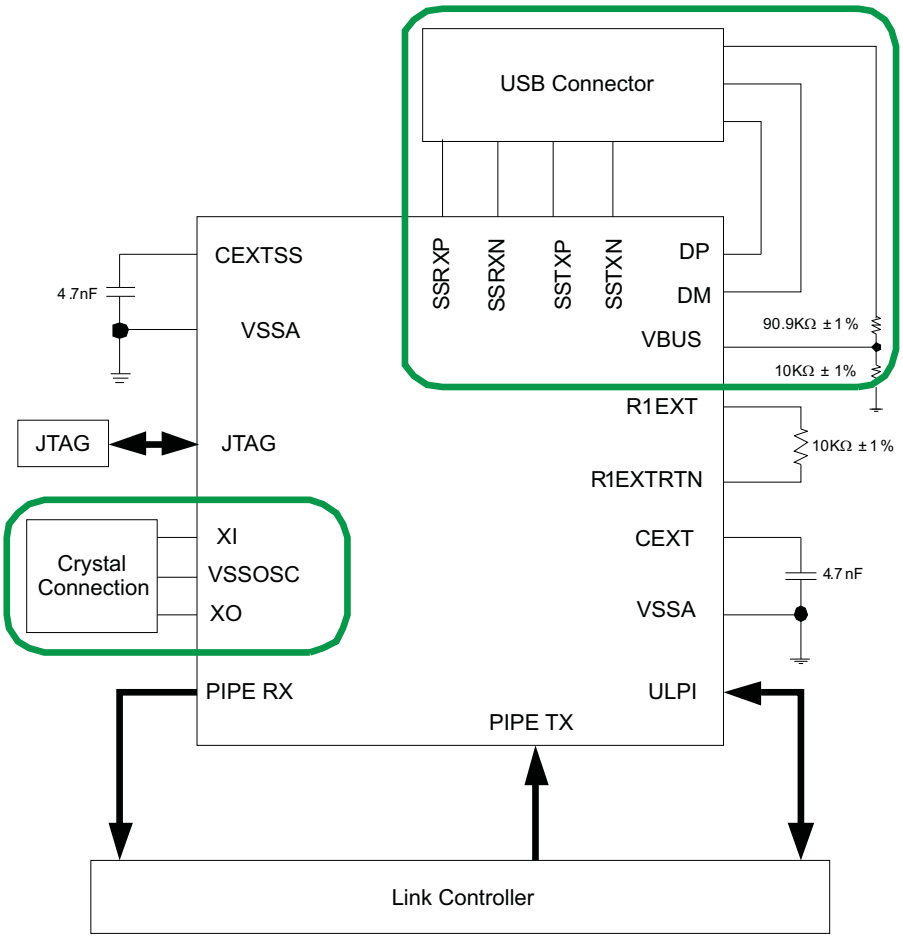


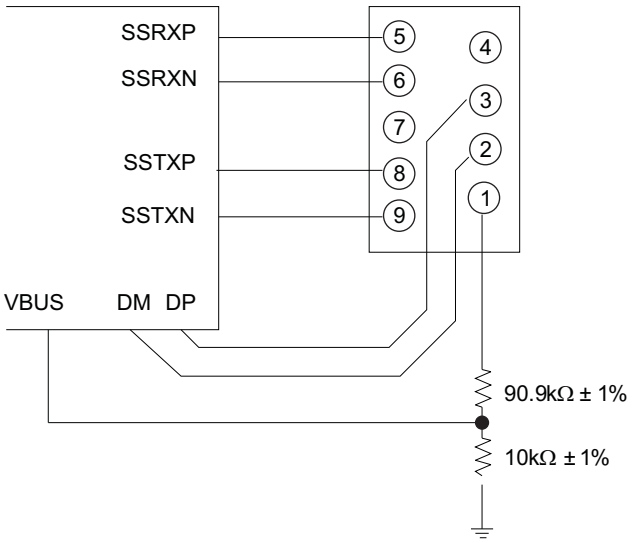

**Figure 5-1. Analog Pin Connections**

### *5.1.1 USB Connector Pins Connection*

Differential pair signals, DP/DM, SSTXP/SSTXN, SSRXP/SSRXN, should be kept as short as possible. The differential pair traces should be trace-length matched and parallelism should be maintained. They also need to minimize vias and corners and should avoid crossing plane splits and stubs.

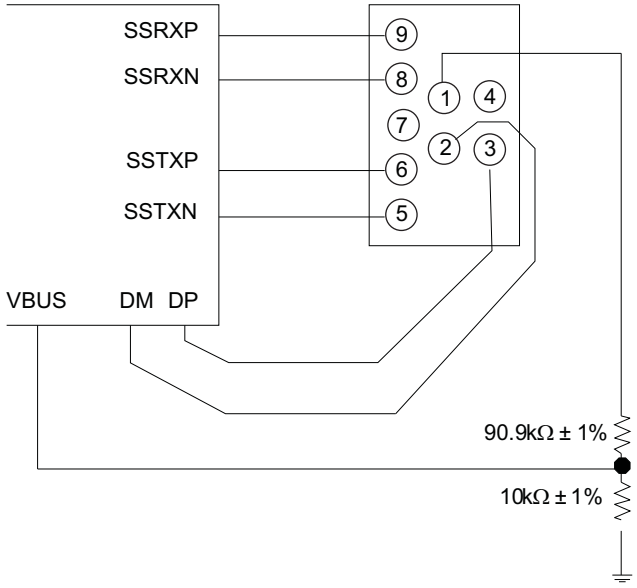
Figure 5-2 and Figure 5-3 are for visual reference only.


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| Pin# | Signal Name |
|---|---|
| 1 | VBUS |
| 2 | DM |
| 3 | DP |
| 4 | GND |
| 5 | SSRXN |
| 6 | SSRXP |
| 7 | GND_DRAIN |
| 8 | SSTXN |
| 9 | SSTXP |

**Figure 5-2. USB Standard-A Connector Pin Connection**




| Pin# | Signal Name |
|---|---|
| 1 | VBUS |
| 2 | DM |
| 3 | DP |
| 4 | GND |
| 5 | SSTXN |
| 6 | SSTXP |
| 7 | GND_DRAIN |
| 8 | SSRXN |
| 9 | SSRXP |

**Figure 5-3. USB Standard-B Connector Pin Connection**

### *5.1.2 Clock Connections*

The TUSB1310 supports an external oscillator source or a crystal unit. If a clock is provided to XI instead of a crystal, XO is left open. Otherwise, if a crystal is used, the connection needs to follow the guidelines below.

Since XI and XO are coupled to other leads and supplies on the PCB, it is important to keep them as short as possible and away from any switching leads. It is also recommended to minimize the capacitance between XI and XO. This can be accomplished by connecting the VSSOSC lead to the two external capacitors CL1 and CL2 and shielding them with the clean ground lines. The VSSOSC should not be connected to PCB ground.

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Load capacitance (Cload) of the crystal varying with the crystal vendors is the total capacitance value of the entire oscillation circuit system as seen from the crystal. It includes two external capacitors CL1 and CL2 in Figure 5-4. CVSS below is optional, but recommended for minimum jitter implementation. The trace length between the decoupling capacitors and the corresponding power pins on the TUSB1310 needs to be minimized. It is also recommended that the trace length from the capacitor pad to the power or ground plane be minimized.

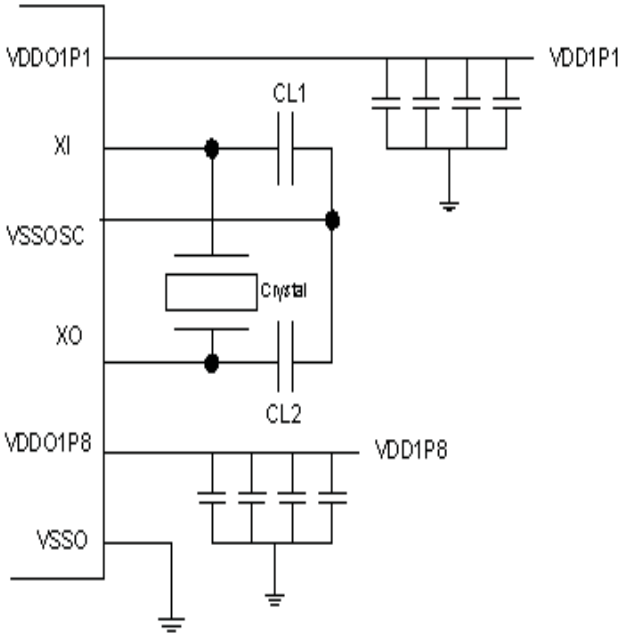



**Figure 5-4. Typical Crystal Connections**

## 5.2 Clock Source Requirements

### *5.2.1 Clock Source Selection Guide*

Reference clock jitter is an important parameter. Jitter on the reference clock will degrade both the transmit eye and receiver jitter tolerance no matter how clean the rest of the PLL is, thereby impairing sys-tem performance. Additionally, a particularly jittery reference clock may interfere with PLL lock detection mechanism, forcing the lock detector to issue an unlock signal. A good quality, low jitter reference clock is required to achieve compliance with supported USB3.0 standards. For example, USB3.0 specification requires the random jitter (RJ) component of either RX or TX to be 2.42 ps (random phase jitter calculated after applying jitter transfer function - JTF). As the PLL typically has a number of additional jitter components, the reference clock jitter must be considerably below the overall jitter budget.


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### 5.2.2 Oscillator

If an external clock source is used, XI should be tied to the clock source and XO should be left floating.

**Table 5-1. Oscillator Specification**

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Frequency tolerance | Operational temperature | | | ±50 | ppm |
| Frequency stability | 1 year aging | | | ±50 | ppm |
| Rise / Fall time | 20% - 80% | | | 6 | ns |
| Reference clock $R_J$ with JTF (1 sigma)(1)(2) | | | 0.8 | | ps |
| Reference clock $T_J$ with JTF (total p-p)(2)(3) | | | 25 | | ps |
| Reference clock jitter (absolute p-p)(4) | | | 50 | | ps |

(1) Sigma value assuming Gaussian distribution
(2) After application of JTF
(3) Calculated as 14.1 x $R_J$ + $D_J$
(4) Absolute phase jitter (p-p)

### 5.2.3 Crystal

Either a 20-MHz, 25-MHz, 30-MHz, or 40-MHz crystal can be selected. A parallel, 20-pF load crystal should be used if a crystal source is used.

**Table 5-2. Oscillator Specification**

| PARAMETER | CONDITION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Frequency tolerance | Operational temperature | | | ±50 | ppm |
| Frequency stability | 1 year aging | | | ±50 | ppm |
| Load capacitance | | 12 | 20 | 24 | pF |

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# 6 ELECTRICAL SPECIFICATIONS

## 6.1 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | UNIT |
|---|---|---|---|
| $V_{DD1P1}$ | Digital 1.1 steady-state supply voltage | -0.3 to 1.4 | V |
| $V_{DD1P8}$ | Digital IO 1.8 steady-state supply voltage | -0.3 to 2.45 | V |
| $V_{DDA1P1}$ | Analog 1.1 steady-state supply voltage | -0.3 to 1.4 | V |
| $V_{DDA1P8}$ | Analog 1.8 steady-state supply voltage | -0.3 to 2.45 | V |
| $V_{DDA3P3}$ | Analog 3.3 steady-state supply voltage | -0.3 to 3.8 | V |

## 6.2 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{DDA3P3}$ | Analog 3.3 supply voltage | | 2.97 | 3.3 | 3.63 | V |
| $V_{DDA1P8}$ | Analog 1.8 supply voltage | | 1.71 | 1.8 | 1.98 | V |
| $V_{DDA1P1}$ | Analog 1.1 supply voltage | | 1.045 | 1.1 | 1.155 | V |
| $V_{DD1P8}$ | Digital IO 1.8 supply voltage | | 1.62 | 1.8 | 1.98 | V |
| $V_{DD1P1}$ | Digital 1.1 supply voltage | | 1.045 | 1.1 | 1.155 | V |
| $V_{BUS}$ | Voltage at VBUS PAD | | 0 | | 1.21 | V |
| $T_A$ | Operating free-air temperature range | | 0 | | 70 | °C |
| $T_J$ | Operating junction temperature range | | -40 | | 105 | °C |
| ESD | | Human Body Model (HBM) | 500 | | | V |
| | | Charged Device Model (CDM) | 500 | | | |

## 6.3 DC CHARACTERISTICS FOR 1.8-V DIGITAL IO

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 0.65 x VDDS | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.35 x VDDS | V |
| $V_{OH}$ | IO = -2 mA, $V_{DDS}$ = 1.62 V to 1.98 V, driver enabled, pullup or pulldown disabled | | VDDS - 0.45 | | | V |
| | IO = -2 mA, $V_{DDS}$ = 1.4 V to 1.6 V, driver enabled, pullup or pulldown disabled | | 0.75 x VDDS | | | |
| $V_{OL}$ | IO = 2 mA, driver enabled, $V_{DDS}$ = 1.62 V to 1.98 V, pullup or pulldown disabled | | | | 0.45 | V |
| | IO = 2 mA, $V_{DDS}$ = 1.4 V to 1.6 V, driver enabled, pullup or pulldown disabled | | | | 0.25 x VDDS | |
| $V_{hys}$ | Input hysteresis | | 100 | 270 | | mV |
| $I_I$ | Any receiver, including those with a pullup or pulldown. The pullup or pulldown must be disabled. | | | | ±1 | µA |
| $I_{I(PUon)}$ | Receiver/pullup only, pullup enabled (not inhibited), $V_{PAD}$ = 0 V | | -47 to -169 | | | µA |
| | Receiver/pullup only, pullup enabled (not inhibited) | | -100 | | | |
| $I_{OZ}$ | Driver only, driver disabled | | | | ±20 | µA |
| $I_Z$ (1) | | | | | ±20 | µA |
| $V_{TX_DIFF_SS}$ | SSTXP/SSTXN Differential p-p Tx voltage swing | | 0.8 | | 1.2 | V |

(1) $I_Z$ is the total leakage current through the PAD connection of a driver/receiver combination that may include a pullup or pulldown. The driver output is disabled and the pullup or pulldown is inhibited.


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### DC CHARACTERISTICS FOR 1.8-V DIGITAL IO *(continued)*

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{TX_DIFF_DC}$ | DC differential impedance | 72 | | 120 | Ω |
| $V_{TX_RCV_DET}$ | The amount of voltage change allowed during receiver detection | | | 0.6 | V |
| $C_{AC_COUPLING}$ | AC coupling capacitor | 75 | | 200 | nF |
| $R_{RX_DC}$ | Receiver DC common mode impedance | 18 | | 30 | Ω |
| $R_{RX_DIFF_DC}$ | DC differential impedance | 72 | | 120 | Ω |
| $V_{RX_LFPS_DET}$ | LFPS detect threshold | 100 | | 300 | mV |
| $V_{CM_AC_LFPS}$ | | | | 100 | mV |
| $V_{CM_LFPS_active}$ | | | | 10 | mV |
| $V_{TX_DIFF_PP_LFPS}$ | | 800 | | 1200 | mV |

## 6.4 DEVICE POWER CONSUMPTION(1)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| VDDA3P3 power consumption | | 13 | | mW |
| VDDA1P8 power consumption | | 77 | | mW |
| VDDA1P1 power consumption | | 118 | | mW |
| VDD1P1 power consumption | | 98 | | mW |
| VDD1P8 power consumption | | 128 | | mW |

(1) Power consumption condition is transmitting and/or receiving (in U0) at 25°C and nominal voltages.

## 6.5 AC Characteristics

### *6.5.1 Power Up and Reset Timing*

The TUSB1310 does not drive signals on any strapping pins before they are latched internally.

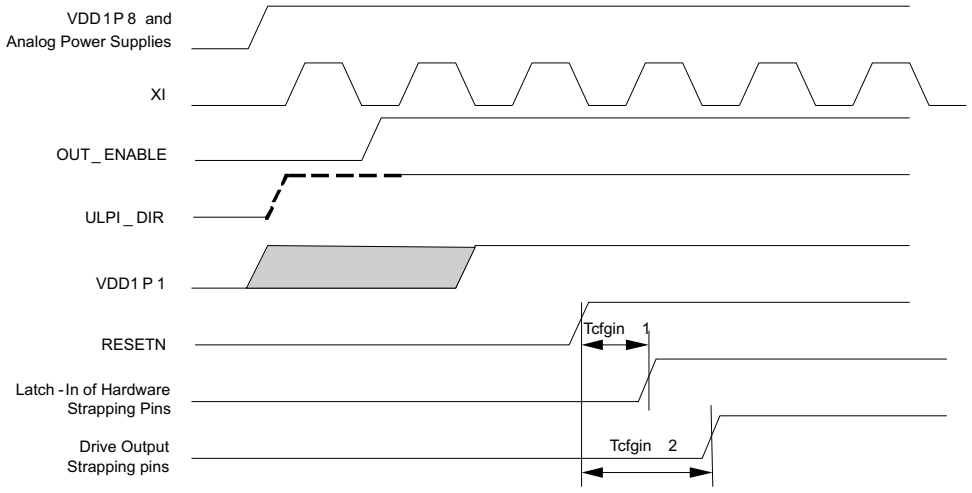



**Figure 6-1. Power Up and Reset Timing**

**Table 6-1. Power Up and Reset Timing**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Tcfgin1 | Hardware configuration latch-in time from RESETN | 0 | | | ns |
| Tcfgin2 | Time from RESETN to dDriver outputs on strapping pins | 0 | | | ns |
| | RESETN pulse width | 1 | | | µs |
| | RESETN to PHY_STATUS de-assertion | | 300 | | µs |

### 6.5.2 PIPE Transmit

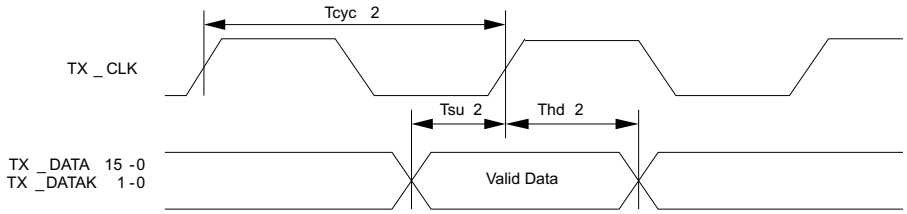



**Figure 6-2. PIPE Transmit Timing**

**Table 6-2. PIPE Transmit Timing**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Tcyc2 | TX_CLK Period | | 4 | | ns |
| Tdty2 | TX_CLK Period | | 50 | | % |
| Tsu2 | Data Setup to TX_CLK rise and TX_CLK fall (1) | 1 | | | ns |
| Thd2 | Data Hold to TX_CLK rise and TX_CLK fall (1) | 0 | | | ns |

(1) This includes TX_DATA15-0, TX_DATAK1-0, TX_ONESZEROS, RATE, TX_DEEMPTH, TX_DETRX_LPBK, TX_ELECIDLE, TX_MARGIN, TX_SWING, RX_POLARITY, POWER_DOWN1-0.

### 6.5.3 PIPE Receive

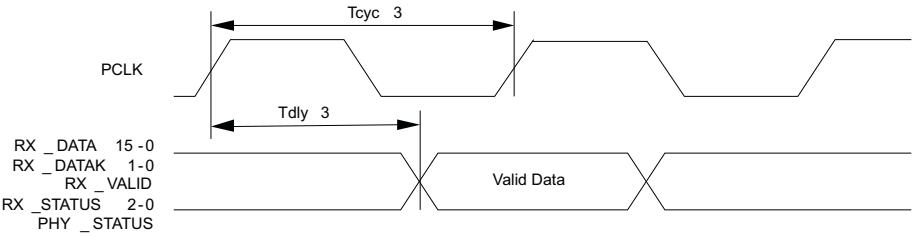



**Figure 6-3. PIPE Receive Timing**

**Table 6-3. PIPE Receive Timing**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Tcyc3 | PCLK Period | | 4 | | ns |
| Tdty3 | PCLK Duty Cycle | | 50 | | % |
| Tdly3 | PCLK rise and fall to RX_DATA15-0, RX_DATAK1-0, RX_VALID, RX_STATUS2-0, PHY_STATUS Delay (1)(2) | 1 | | 2 | ns |

(1) Output Load max = 10 pF, min = 5 pF
(2) Timing is relative to the 50% transition point, not $V_{IH}/V_{IL}$.


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### 6.5.4 ULPI Parameters

**Table 6-4. ULPI Parameters**

| DESCRIPTION | NOTES | HS | FS | LS | UNIT |
|---|---|---|---|---|---|
| RX CMD delay | PHY pipeline delays | 2-4 | 2-4 | 2-4 | clocks |
| TX start delay | | 1-2 | 1-10 | 1-10 | clocks |
| TX end delay | | 2-5 | | | clocks |
| RX start delay | | 3-8 | | | clocks |
| RX end delay | | 3-8 | 17-18 | 122-123 | clocks |
| Transmit-Transmit (host only) | Link decision times | 15-24 | 7-18 | 77-247 | clocks |
| Receive-Transmit (host or peripheral) | | 1-14 | 7-18 | 77-247 | clocks |

### 6.5.5 ULPI Clock

**Table 6-5. ULPI Clock Parameters**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Fstart_8bit | Frequency (first transition) ±10% | 54 | 60 | 66 | MHz |
| Fsteady | Frequency (steady state) ±500 ppm | 59.97 | 60 | 60.03 | MHz |
| Dstart_8bit | Duty cycle (first transition) ±10% | 40 | 50 | 60 | % |
| Dsteady | Duty cycle (steady state) ±500 ppm | 49.975 | 50 | 50.025 | % |
| Tsteady | Time to reach steady state frequency and duty cycle after first transition | | | 1.4 | ms |
| Tstart_dev | Clock startup time after deassertion of SuspemdM – Peripheral | | | 5.6 | ms |
| Tstart_host | Clock startup time after deassertion of SuspemdM – Hold | | | | ms |
| Tprep | PHY preparation time after first transition of input clock | | | | µs |
| Tjitter | Jitter | | | | ps |
| Trise/Tfall | Rise and fall time | | | | ns |

### 6.5.6 ULPI Transmit

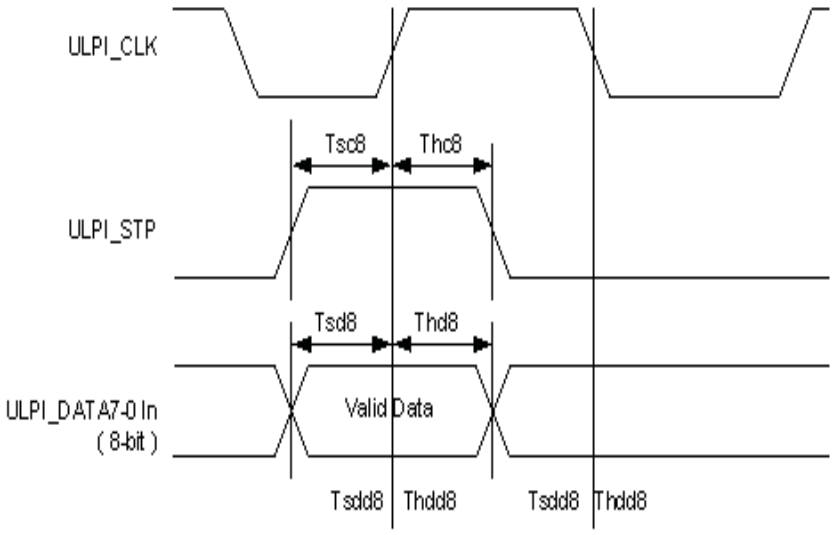



**Figure 6-4. ULPI Transmit Timing**

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**Table 6-6. ULPI Transmit Timing**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Tsc8, Tsd8 | ULPI_STP setup time | | | 6 | ns |
| Thc8, Thd8 | ULPI_STP hold time | 0 | | | ns |

### 6.5.7 ULPI Receive Timing

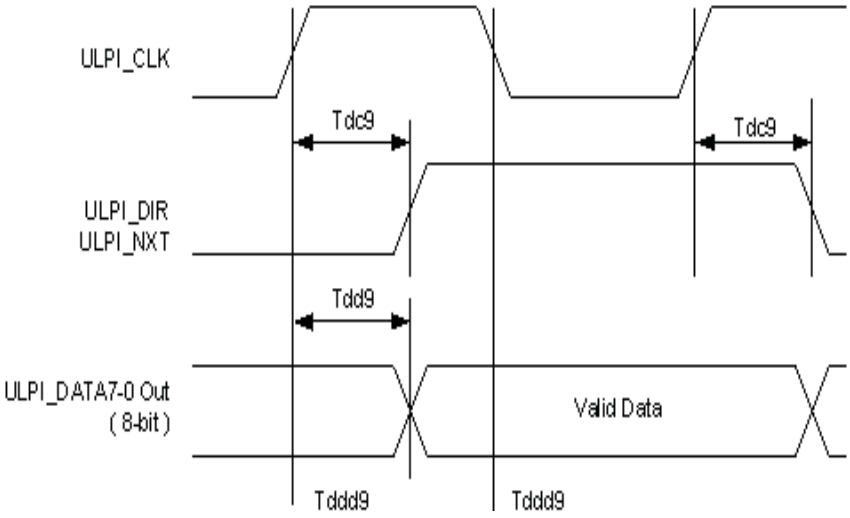



**Figure 6-5. ULPI Receive Timing**

**Table 6-7. ULPI Transmit Timing**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Tdc9, Tdd9 | ULPI_DIR/ULPI_NXT/ULPI_DATA7-0 (1) | | | 9 | ns |

(1) Output Load max = 10 pF, min = 5 pF

### 6.5.8 Power State Transition Time

The P1 to P0 transition time is the amount of time for the TUSB1310 to return to P0 state, after having been in the P1 state. This time is measured from when the MAC sets the POWER_DOWN signals to P0 until the TUSB1310 asserts PHY_STATUS. The TUSB1310 asserts PHY_STATUS when it is ready to begin data transmission and reception.

The P2 to P0 transition time is the amount of time for the TUSB1310 to return to the P0 state, after having been in the P2 state. This time is measured from when the MAC sets the POWER_DOWN signals to P0 until the TUSB1310 asserts PHY_STATUS. The TUSB1310 asserts PHY_STATUS when it is ready to begin data transmission and reception.

The P3 to P0 transition time is the amount of time for the TUSB1310 to go to P0 state, after having been in the P3 state. Time is measured from when the MAC sets the POWER_DOWN signals to P0 until the TUSB1310 deasserts PHY_STATUS. The TUSB1310 asserts PHY_STATUS when it is ready to begin data transmission and reception.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TUSB1310ZAY | NRND | NFBGA | ZAY | 175 | 160 | Green (RoHS & no Sb/Br) | SNAGCU | Level-3-260C-168 HR | 0 to 70 | TUSB1310 | |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

**(3)** MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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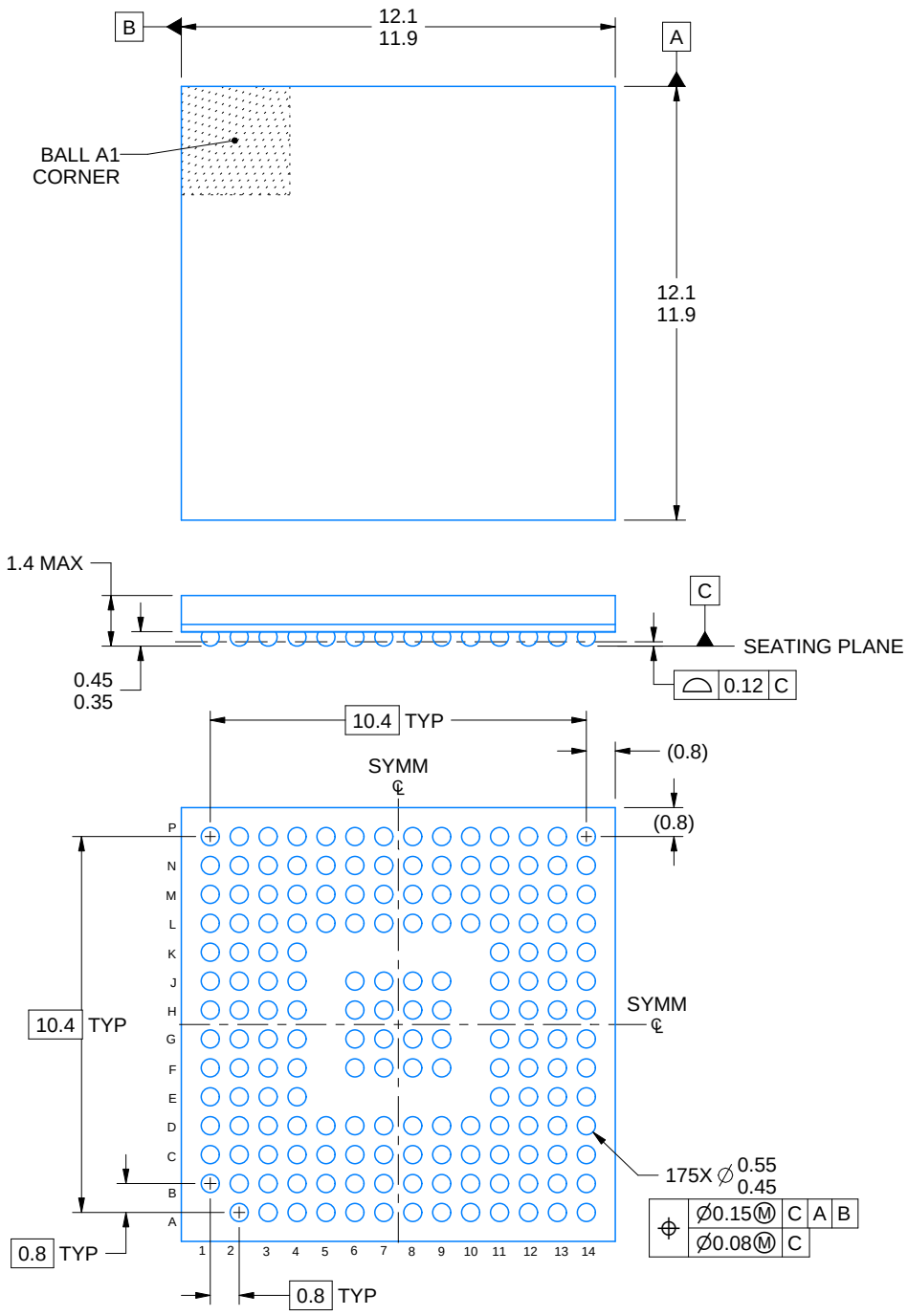
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# PACKAGE OUTLINE

## ZAY0175A

## NFBGA - 1.4 mm max height

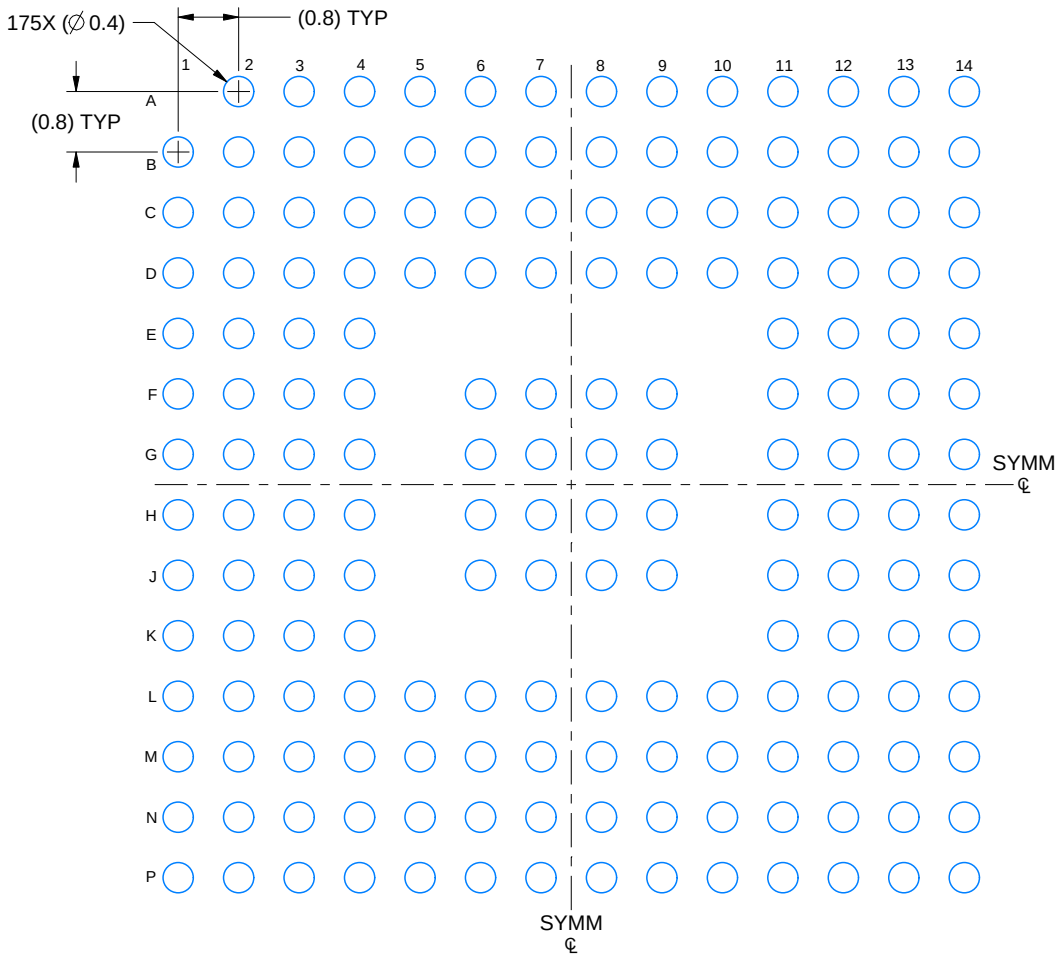
PLASTIC BALL GRID ARRAY



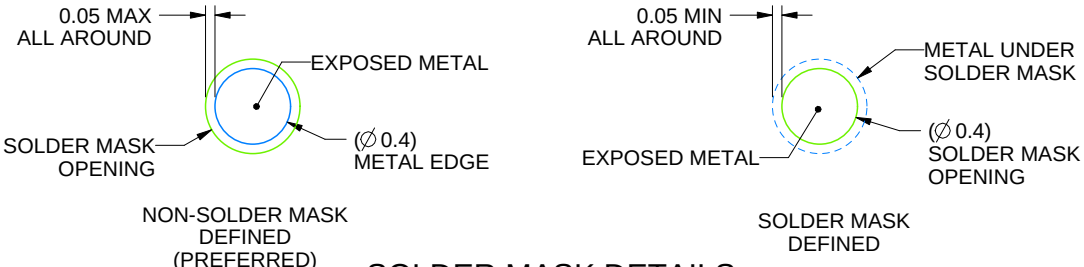

4219814/A 05/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

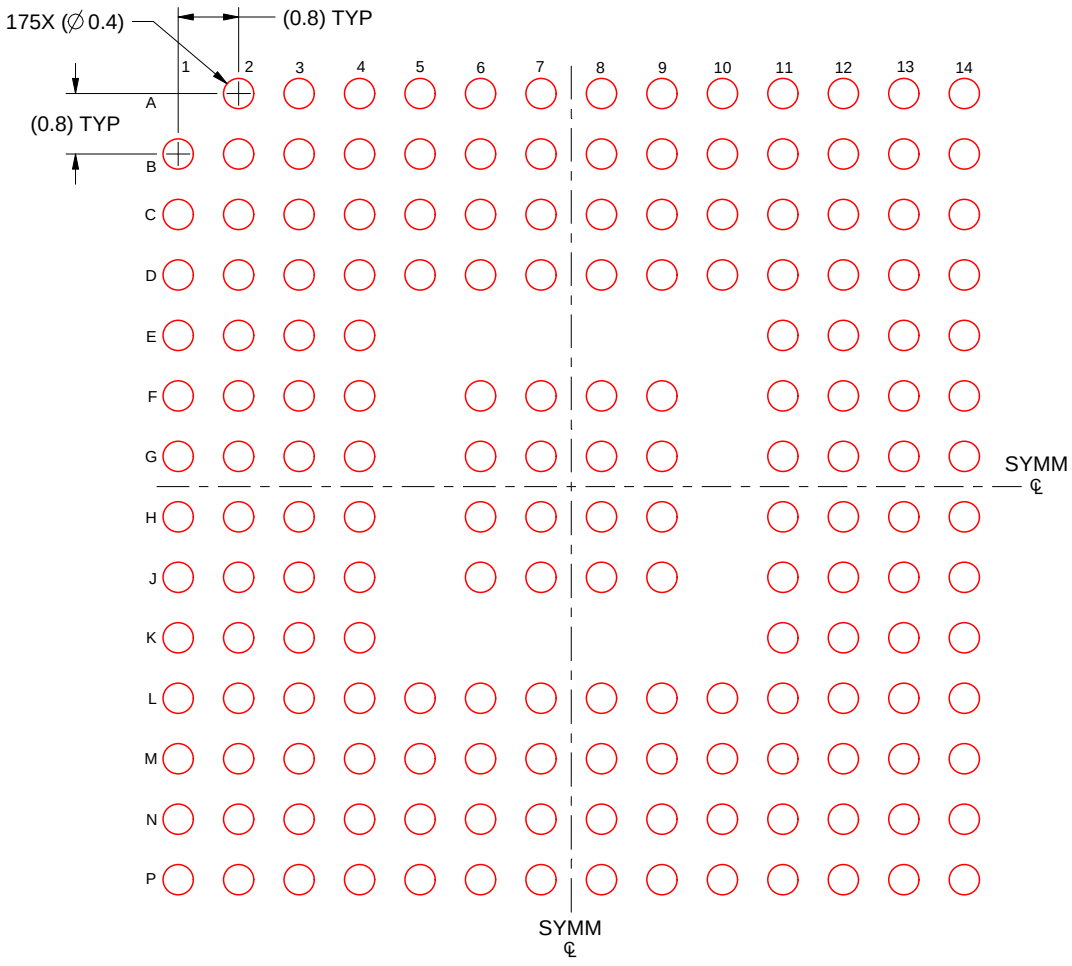



SOLDER MASK DETAILS
NOT TO SCALE

4219814/A 05/2020

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4219814/A 05/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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