TPS92410 Switch-Controlled, Direct Drive, Linear Controller for Offline LED Drivers

1 Features

- Multiplier for Good PFC, Line Regulation, and Low THD
- V_{IN} Range From 9.5 V to 450 V
- Compatible with Phase Dimmers
- Analog Dimming Input with LED Turn-Off
- Programmable Overvoltage Protection
- Precision 3-V Reference
- Thermal Foldback
- Thermal Shutdown
- No Inductor Required
- 13 Pin, High-Voltage, SOIC Package

2 Applications

- LED Drivers
- LED Light Bulb Replacement

3 Description

The TPS92410 is an advanced linear driver with high voltage start-up intended for use in low power, offline LED lighting applications. It can be used to regulate the average LED current through LEDs in conjunction with the TPS92411 direct drive switch.

The TPS92410 features a reference voltage that can be used to set the current level as well as the thermal foldback threshold. A multiplier is included to obtain excellent power factor while maintaining good line regulation. Other features include under-voltage lockout, over-voltage protection, forward phase dimmer detection with change to constant current mode, thermal foldback, and thermal shutdown.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS92410D	SOIC (13)	8.65 mm x 6.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic

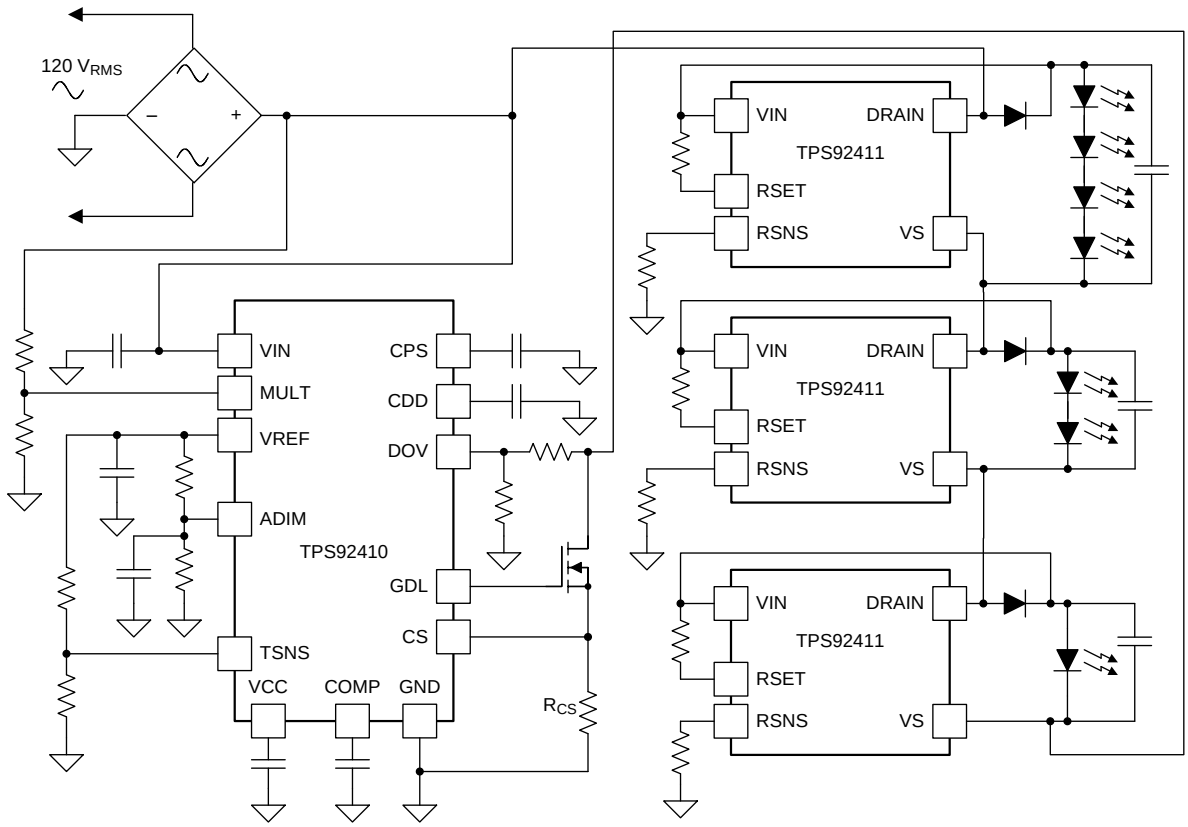


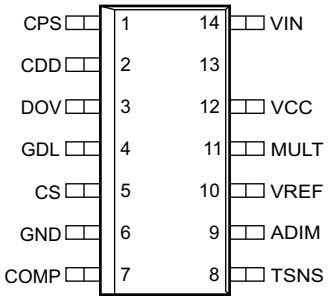
Table of Contents

4 Revision History

DATE	REVISION	NOTES
June 2014	*	Initial release.

5 Pin Configuration and Functions

SOIC HV
13 PIN
(TOP VIEW)



Pin Functions

PIN		TYPE (1)	DESCRIPTION
NAME	NO.		
ADIM	9	I	Analog input used to set the reference of the linear controller. A 0-V to 1.5-V signal on ADIM sets the current sense reference level.
CDD	2	I/O	A capacitor to ground sets the time interval for dimmer detection. Tie to GND if no phase dimmer operation is required.
COMP	7	I/O	Compensation for control loop. Connect a capacitor from the COMP pin to ground.
CPS	1	I/O	A capacitor to ground sets the length of the CDD pin charge pulse. Leave open if no phase dimmer operation is required.
CS	5	I	Current sense input used for linear regulator.
DOV	3	I	Input to monitor linear MOSFET drain voltage. A resistor divider from the DOV pin to the drain connection of the MOSFET monitors MOSFET over-voltage. Add a capacitor to GND for filtering.
GDL	4	O	Gate drive for an external linear MOSFET.
GND	6	G	Chip ground return.
MULT	11	I	AC input to the multiplier. Tap a resistor divider off the rectified line to this pin.
TSNS	8	I	Thermal sense input. Connect to a resistor and NTC thermistor for thermal foldback.
VCC	12	I/O	Pre-regulated voltage. Connect a bypass capacitor to ground.
VIN	14	P	High voltage input. Provides power to the device.
VREF	10	O	3-V voltage supply reference. Source used for TSNS input.

(1) I = Input, O = Output, P = Supply, G = Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	700	V
Output voltage	VCC	–0.3	18	V
	GDL	–0.3	18	
	MULT, VREF, ADIM, COMP, CPS, CDD, TSNS	–0.3	7.7	
	DOV	–0.3	6	
Source current	CS		1	mA
Sink current	CS		1	mA
Operating junction temperature, T_J (2)		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Maximum junction temperature is internally limited by the device.

6.2 Handling Ratings

			MIN	MAX	UNIT
T_{stg}	Storage temperature range		–65	150	°C
$V_{(ESD)}$ (1)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (2)	–1	1	kV
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (3)	–250	250	V

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.
(2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. *Terminals listed as 1000V may actually have higher performance.*
(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. *Terminals listed as 250V may actually have higher performance.*

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	9.5		450	V
V_{MULT}	Multiplier peak input voltage			3	V
V_{ADIM}	Analog dimming input voltage	0		3	V
T_J	Operating junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		TPS92410 D (13)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	39.5	
ψ_{JT}	Junction-to-top characterization parameter	8.9	
ψ_{JB}	Junction-to-board characterization parameter	39.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

–40°C ≤ T_J ≤ 125°C, V_{VIN} = 100 V, V_{ADIM} = V_{MULT} = 1 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN)						
VCC	Pre-regulator output voltage			10.15		V
VCC_{UVLO}	Supply votlage undervoltage protection	Rising threshold, V_{VIN} = V_{VCC}		8	8.3	V
		Falling threshold, V_{VIN} = V_{VCC}	5	5.85		
		Hysteresis		2.15		
I_{VIN}	Input voltage bias current	V_{VCC} = 12 V		2.5	50	µA
I_{VCC}	Supply bias current			305	500	µA
	Supply standby current	V_{VIN} = 0 V, V_{VCC} = 7 V (UVLO)		145		
I_{VCCLIM}	VCC supply current limit	V_{VCC} = 7.5 V	8		25	mA
$Tplh_{(UVLO)}$	VCC supply glitch filter rising	V_{VCC} stepped from 6.075 V to 110% of $VCC_{UVLO,rising}$		16.2		µs
MULTIPLIER (MULT)						
$V_{MULT,LINEAR}$	Multiplier linear range		0		3.5	V
$V_{COMP,LINEAR}$	COMP pin linear range		1.5		3.25	V
R_{MULT}	Input impedance		500	580	700	kΩ
A_{MULT}	Multiplier gain	V_{MULT} = 1.5 V, V_{COMP} = 2.25 V, k = V_{MULT_OUT}/[(V_{COMP}–1.5 V) × V_{MULT}]	0.95	1.43	1.85	1/V
$V_{MULT,OFFSET}$	Multiplier output offset	V_{MULT} = 0 V, V_{COMP} = 2.25 V		13.7		mV
$MULT_{OUT,mx}$	Multiplier Output Clamp Voltage	V_{ADIM} = V_{TSNS} = open; V_{COMP} = 4 V, V_{MULT} = 3.5 V	2.25	2.43	2.65	V
VOLTAGE REFERENCE (VREF)						
V_{VREF}	Reference voltage	I_{VREF} = 100 µA	2.85	3	3.15	V
$VREF_{LINE}$	Line regulation	8.5 V ≤ V_{VIN} ≤ 100 V			1%	
$VREF_{LOAD}$	Load regulation	10 µA ≤ I_{REF} ≤ 200 µA			1%	
TRANSCONDUCTANCE AMPLIFIER (ADIM, COMP)						
$ADIM_{LIM}$	ADIM operating voltage limit		1.425	1.5	1.575	V
I_{ADIM}	Pull-up current			0.5	1	µA
$ADIM_{SD}$	ADIM linear shutdown threshold	Falling	18	40	70	mV
$ADIM_{SD,HYS}$	ADIM shutdown hysteresis			20		mV
g_M	Transconductance			43.3		µS
V_{OFFSET}	Input offset voltage	V_{ADIM} = 0.5 V	-20		20	mV
$I_{OUT,SOURCE}$	Output source current	V_{COMP} = 2.25 V, V_{MULT} = 0V, V_{ADIM} = V_{TSNS} = 2 V		65		µA
$I_{OUT,SINK}$	Output sink current	V_{COMP} = 2.25 V, V_{TSNS} = 0 V		75		
I_{START}		V_{COMP} = 0 V, V_{ADIM} = 0 V		485		
DIMMER DETECT (MULT, CPS, CDD)						
I_{CPS}	Charge current for CPS pin		6.7	10	13.3	µA
$I_{CDD,c}$	Charge current for CDD pin		5.7	10	13.3	
$I_{CDD,d}$	Discharge current for CDD pin		0.67	1	1.33	
Dv/Dt	Maximum detection threshold	V_{MULT} stepped from 0 V to 1 V, minimum slew rate required		1/100		V/µs
V_{OFFSET}	Detector offset voltage			0.41		V
$V_{TH,CDD}$	CDD threshold			1.5		
$V_{TH,CPS}$	CPS threshold			1.5		
R_{CSP}	Pull down $R_{DS(on)}$			314		Ω

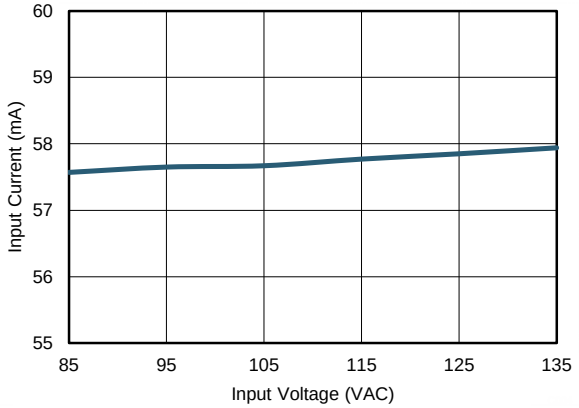
Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, V_{VIN} = 100 V, V_{ADIM} = V_{MULT} = 1 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRAIN OVER-VOLTAGE (DOV)						
$V_{TH,DOV}$	Drain over-voltage threshold		1.38	1.5	1.62	V
$V_{HYS,DOV}$	Internal DOV hysteresis			20		mV
$I_{HYS,DOV}$	Drain over-voltage source current	V_{DOV} = 1.5 V, Device in over-voltage mode	0.7	1	1.5	µA
$V_{REF,DOV}$	Linear CS reference during over-voltage	V_{DOV} = 1.75 V		0.1		V
THERMAL FOLDBACK (TSNS)						
$TSNS_{LIM}$	TSNS operating voltage limit		1.425	1.5	1.575	V
		V_{ADIM} = V_{TSNS} = 1 V, Measure reference to the linear error amplifier		2.1		mV
		V_{TSNS} = 0 V, Measure reference to the linear error amplifier		3.6		
I_{TSNS}	Pull-up current			0.5	1	µA
LINEAR CURRENT SENSE (CS)						
$V_{CS(max)}$	CS voltage level (CC dimming mode)	2.5 V = V_{ADIM} = V_{TSNS}	1.425	1.5	1.575	V
$V_{CS(max)}$	CS voltage level (PFC mode)	2.5 V = V_{ADIM} = V_{TSNS}	1.125	1.291	1.425	
V_{IO}	Input offset voltage	VREF = 1 V	–17	2.57	17	mV
$V_{CMR–}$	Minimum input common mode range			0		V
GATE DRIVER (GDL)						
V_{OH}	High-level output voltage, GDL	I_{LOAD} = –1 mA	6.5	8.2		V
V_{OL}	Low-level output voltage, GDL	I_{LOAD} = 1 mA		0.152	0.45	
$I_{OUT(src)}$	Output source current	V_{GDL}= 4 V	2.5	8.1		mA
$I_{OUT(snk)}$	Output sink current	V_{GDL}= 4 V	2.5	11.9		
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown			175		°C
	Thermal shutdown hysteresis			10		

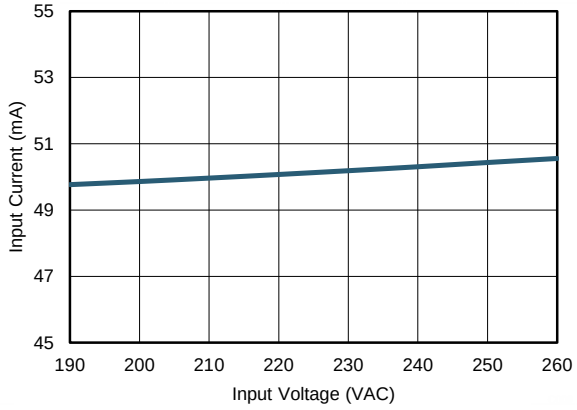
6.6 Typical Characteristics

Unless otherwise stated, –40°C ≤ T_A = T_J ≤ +125°C. All characterization circuits are fully EMI compliant and phase dimmable.



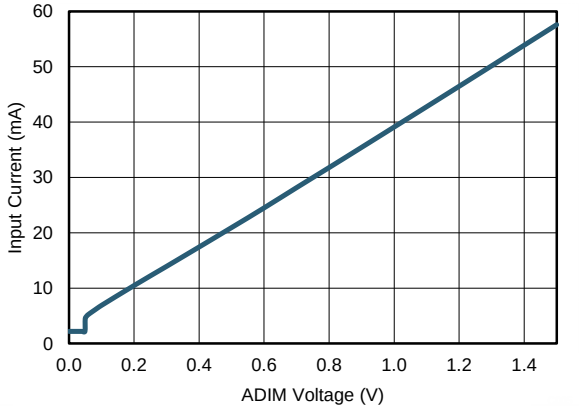
120VAC 6.8 W Input Top stack = 80 V
Middle stack = 40 V Bottom stack= 20 V V_{ADIM} = 1.5 V

Figure 1. System Input Current vs Input Voltage



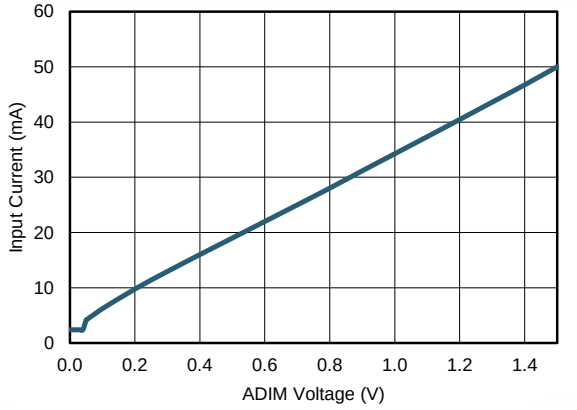
230 VAC 11.2 W Input Top stack = 160 V
Middle stack = 80 V Bottom stack= 40 V V_{ADIM} = 1.5 V

Figure 2. System Input Current vs Input Voltage



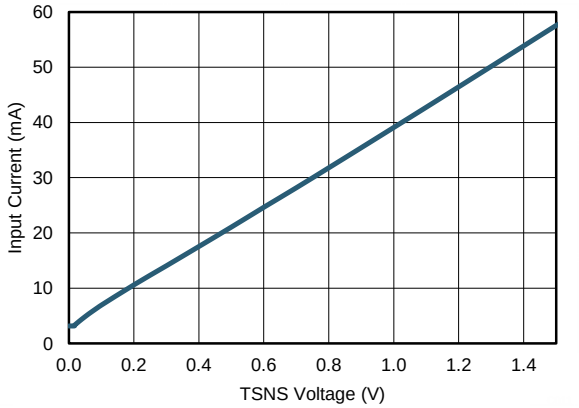
120VAC 6.8 W Input Top stack = 80 V
Middle stack = 40 V Bottom stack= 20 V

Figure 3. System Input Current vs ADIM Voltage



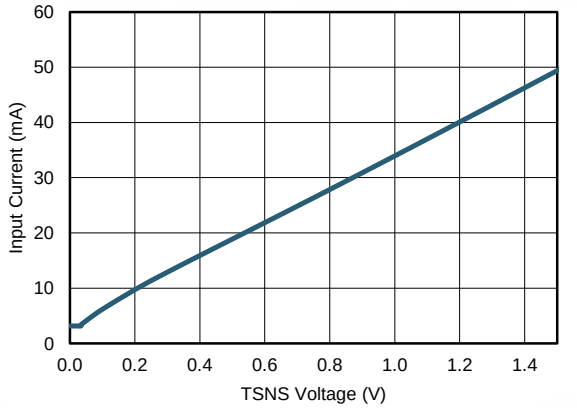
230 VAC 11.2 W Input Top stack = 160 V
Middle stack = 80 V Bottom stack= 40 V

Figure 4. System Input Current vs ADIM Voltage



120VAC 6.8 W Input Top stack = 80 V
Middle stack = 40 V Bottom stack= 20 V V_{ADIM} = 1.5 V

Figure 5. System Input Current vs TSNS Voltage



230 VAC 11. W Input Top stack = 160 V
Middle stack = 80 V Bottom stack= 40 V V_{ADIM} = 1.5 V

Figure 6. System Input Current vs TSNS Voltage

Typical Characteristics (continued)

Unless otherwise stated, –40°C ≤ T_A = T_J ≤ +125°C. All characterization circuits are fully EMI compliant and phase dimmable.

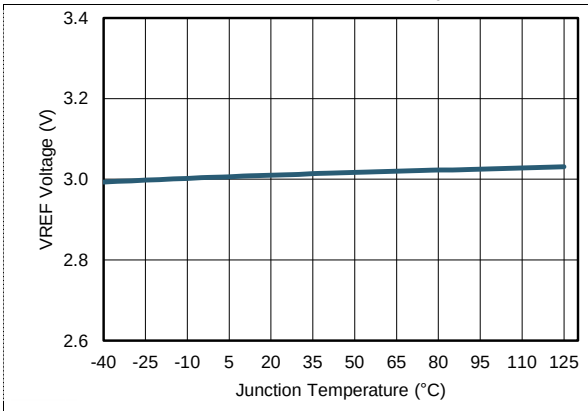


Figure 7. VREF Voltage vs Temperature

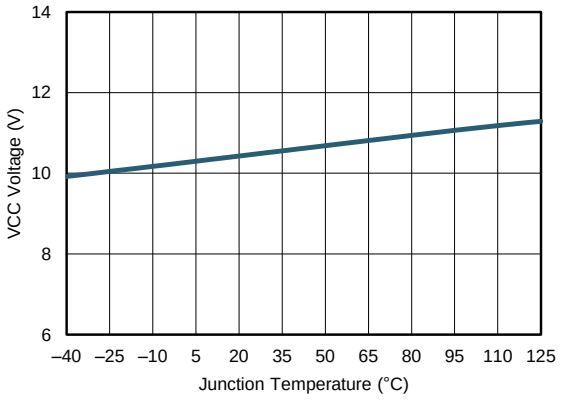


Figure 8. VCC Voltage vs Temperature

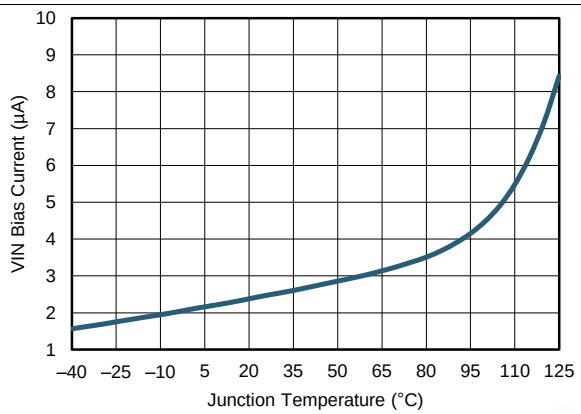


Figure 9. VIN Bias Current vs Temperature

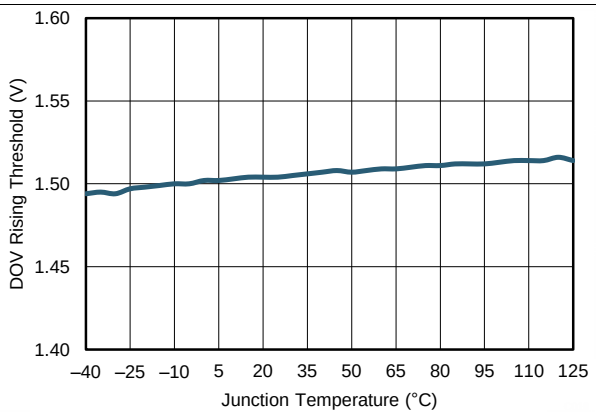


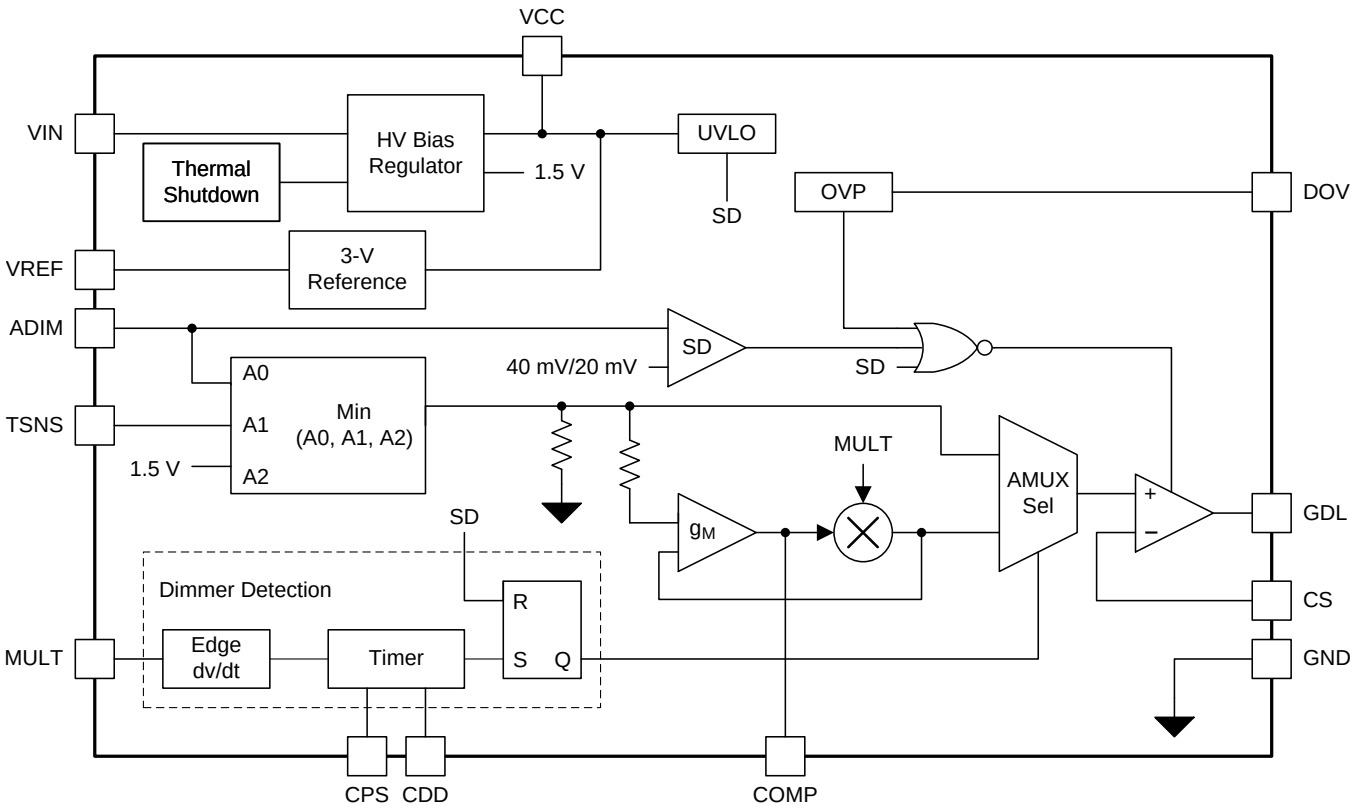
Figure 10. Over-voltage Threshold vs Temperature

7 Detailed Description

7.1 Overview

The TPS92410 device is a high-voltage linear regulator driver that can be used for offline LED drivers. It includes a feature that forces the regulator current to follow the rectified AC voltage to achieve high power-factor and low total harmonic distortion (THD). When the device detects multiple forward phase dimmer edges, the regulator current changes to a DC level to maintain a DC current draw to provide for a triac dimmer's hold current requirements. The TPS92410 device also includes linear MOSFET over-voltage protection to protect the MOSFET if the LEDs are shorted. It includes a thermal foldback feature to protect the entire circuit in the event it becomes overheated. Analog dimming capability allows light output to be controlled by a microcontroller or a 0 V to 10 V dimmer. The device also includes a precision voltage reference.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Setting the Linear Regulator Current/Input Power (CS)

The input power (P_{IN}) can be set with a resistor from the CS pin to ground. Calculate the value of the R_{CS} resistor using the following equation (see Figure 11):

$$R_{CS} = \frac{V_{IN\,(rms)} \times 1.428}{P_{IN}} \quad (1)$$

where

- $V_{IN(rms)}$ is the nominal rms input voltage to the circuit

This sets the input power level due to the linear regulator for a standard application with V_{ADIM} and V_{TSNS} greater than or equal to 1.5 V. If either pin is pulled below 1.5 V the input power scales accordingly to the ratio of $V_{TSNS/ADIM}$/1.5 V. The actual input power of the circuit is higher due to variables such as VIN bias current, resistor, diode, and other losses. When using forward phase dimmers there can be a significant current spike through the MOSFET and R_{CS} depending on the dv/dt of the dimmer edge. The magnitude and duration of this current spike should be measured in any application and a resistor should be chosen that is rated for the peak current required in any final design.

7.3.2 Over-Voltage Protecton (DOV)

The DOV pin can be used to set an over-voltage protection threshold for the external linear MOSFET. During normal operation DOV is not active, but in the event that the LEDs become shorted resulting in excessive voltage and power dissipation in the MOSFET over-voltage protection becomes active. During an over-voltage event, the CS pin regulation voltage defaults to 100 mV to reduce power dissipation in the MOSFET but still provide some light with the remaining LEDs. For this reason it is recommended to use a nominal value for CS for normal operation higher than 100 mV. A resistor divider to DOV between the MOSFET drain and system ground sets this over-voltage level as shown in Figure 11. During an over-voltage event the DOV pin sources 1 µA to provide some hysteresis. The level and hysteresis can be set using the following equations:

$$R_{DRAIN} = R_{GROUND} \times \frac{V_{OVP} - 1.5\ V}{1.5\ V} \quad (2)$$

$$V_{HYS\text{-}DOV} = 20\ \mu A \times R_{DRAIN} \quad (3)$$

where

- V_{OVP} is the desired maximum drain voltage
- R_{DRAIN} is the resistor from DOV to the drain
- R_{GROUND} is the resistor from DOV to system ground

Include a capacitor from the DOV pin to system ground to prevent the circuit from transitioning into over-voltage protection mode during the start-up sequence. A recommended value for the R_{GND} resistor is 121 kΩ in parallel with a 4.7-µF capacitor for most applications. R_{DRAIN} can then be calculated. To calculate the values of RGND and CGND for a particular application you need to set the time constant to be longer than it takes to charge up the highest voltage LED string capacitor to prevent a false trip of the over-voltage protection during start-up. This time constant and the resulting RC can be found using the following equations:

$$dt = \frac{C_{UPPER} \times V_{UPPER}}{I_{UPPER}} \quad (4)$$

$$R_{GND} \times C_{GND} = 5 \times dt \quad (5)$$

where

- dt is the time constant to charge the LED capacitor
- C_{UPPER} is the highest voltage LED string capacitor
- V_{UPPER} is the highest string voltage
- I_{UPPER} is the highest voltage LED string current

Choose R_{GND} to be in the 100 kΩ to 150 kΩ range and calculate C_{GND}. Then R_{DRAIN} can be calculated. Over-voltage protection should be adjusted for the minimum string voltages for analog dimming applications or simply disabled by connecting DOV to ground.

Feature Description (continued)

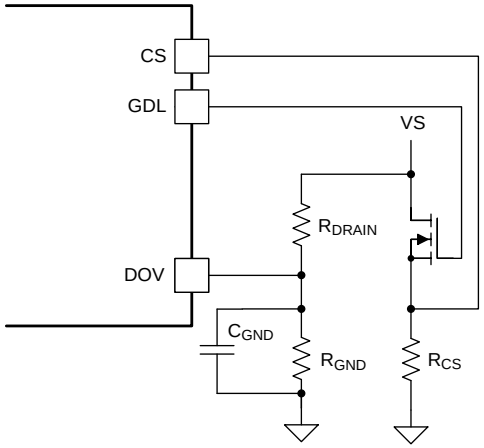


Figure 11. CS and DOV Over-voltage Connections

7.3.3 Input Undervoltage Lockout (UVLO)

The TPS92410 device includes input UVLO protection. This protection prevents the device from operating until a voltage on the VIN pin exceeds 8.0 V. The circuit has 2.15 V of hysteresis to prevent false triggering.

7.3.4 Reference Voltage (VREF)

The TPS92410 includes a 3-V reference feature which can be used to set the DC level on the ADIM pin. It can also source current for the TSNS divider for the thermal foldback circuitry using the TSNS pin. The VREF pin can supply a maximum current of approximately 3 mA but should be limited to less than 200 µA to minimize power dissipation. All current sourced from VREF is supplied by VIN so power dissipation can become significant when sourcing higher currents.

7.3.5 Forward Phase Dimmer Detection (CPS, CDD)

An edge-detect circuit senses when a forward phase dimmer is connected to the input. This detection feature allows the device to operate with a wide variety of dimmers that operate in either forward or reverse phase. The C_{CPS} and C_{CDD} capacitors assist in this function while preventing a false dimmer detect caused by line glitches and spikes in applications without a phase dimmer. Connect a 0.1-µF capacitor between CPS to GND and a 1-µF capacitor from CDD to GND for most applications to use this feature. This results in a time constant of 15 ms for CPS and 150 ms for CDD. If this feature is not required leave CPS open and ground CDD.

The dimmer detect function operates by applying a 10 µA charging current to both the CPS and CDD capacitors. If no edges are detected the CPS capacitor charges to a 1.5 V threshold at which point the CDD pin switches from sourcing 10 µA to sinking 1 µA. This prevents the CDD pin from charging to the 1.5-V threshold that switches the device to dimmer detect mode. When a forward phase dimmer is present the edge is detected at the MULT pin. Each time an edge is detected the CPS pin is discharged and then begins charging again. When enough consecutive edges are present to keep the CPS pin below 1.5 V for longer than the CDD time constant the CDD pin reaches 1.5 V and the device switches to dimmer detect mode. The current regulation level between constant current dimmer detect mode and standard PFC operation can be different depending on dimmer angle. A time constant too long can result in a mild light difference at turn-on due to a slightly different light level between PFC mode at turn-on and dimmer detect mode. A time constant too short could result in unintentionally switching to dimmer detect mode on noisy lines. The easiest way to implement a dimmer detect circuit is to use a CPS time constant just a bit longer than T_{PER}, the period of half of the sine wave input voltage. But other time constants may be used if required. To change the time constants use the following equations:

$$dt_{CPS} = \frac{C_{CPS} \times 1.5\ V}{10\ \mu A} \quad (6)$$

$$dt_{CDD} = \text{infinite} \ \ (\text{for } dt_{CPS} < \frac{T_{PER}}{11}) \quad (7)$$

Feature Description (continued)

$$dt_{CDD} = \frac{C_{CDD} \times 1.5\ V}{(11\ \mu A \times dt_{CPS}) - (1\ \mu A \times T_{PER})} \quad \left(for\ \frac{T_{PER}}{11} < dt_{CPS} < T_{PER}\right) \tag{8}$$

$$dt_{CDD} = \frac{C_{CDD} \times 1.5\ V}{10\ \mu A} \quad (for\ dt_{CPS} > T_{PER}) \tag{9}$$

7.3.6 Analog Dimming Input and Setting V_{CS} (ADIM)

If a default CS voltage of lower than 1.291 V is required, it can be set using the ADIM pin. A resistor divider from the reference sets ADIM to any voltage lower than 1.5 V. During normal operation, the CS voltage is equal to 0.86 times the voltage applied to ADIM. The ADIM pin can also be used for analog dimming using a variable voltage between 40 mV and 1.5 V to dynamically change the CS voltage. If the device pulls the ADIM pin below 40 mV, the device pulls the linear MOSFET gate low to shut off the LEDs. Tie an unused ADIM pin to VREF with a 200-kΩ resistor. If a larger analog dimming range is required, use the TSNS pin for analog dimming because it does not disable the linear regulator when the voltage drops below 40 mV. The ADIM and TSNS pins function identically with the exception of the GDL disable threshold on the ADIM pin.

7.3.7 Thermal Foldback (TSNS)

The thermal foldback function of the TPS92410 device behaves similarly to the ADIM function. However, rather than using a resistor divider, a NTC thermistor connects TSNS to system ground. Calculate the temperature at which the circuit begins to reduce current by determining the temperature at which the the TSNS pin drops below 1.5 V (when the ADIM pin is 1.5 V or higher). With a valid external voltage on the ADIM pin (< 1.5 V), the current begins to reduce when the TSNS voltage drops lower than the ADIM voltage. As described in the *Analog Dimming Input and Setting V_{CS} (ADIM)* section, the TSNS pin and the ADIM pin may be used interchangeably. If the TSNS pin is used for analog dimming, the ADIM pin may be used for thermal foldback.

7.3.8 Internal Regulator (VCC)

The VCC pin functions as the output of the internal supply for the device. Connect a 10-µF capacitor between the VCC pin and ground to keep VCC charged for phase dimming applications. For analog dimming or non-dimming applications a 4.7-µF capacitor is sufficient.

7.3.9 Error Amplifier (COMP)

The COMP pin functions as the output of the internal g_M error amplifier. To ensure stability over all conditions, connect a 4.7-µF capacitor between the COMP pin and ground. The bandwidth of the PFC can be calculated using the following equation:

$$BW = \frac{g_M}{2\pi \times C_{COMP}} \tag{10}$$

7.3.10 Linear MOSFET Gate Drive (GDL)

The GDL pin functions as the gate drive for the linear MOSFET that regulates current. Connect the GDL pin to the gate of the power MOSFET. To reduce EMI, connect a 10-Ω resistor in series with a 1-µF capacitor between the GDL pin and the CS pin with a diode connected between them that returns to the VCC pin as show in Figure 12. If phase dimming is not required, the diode can be omitted. Choose a linear MOSFET with a voltage rating of at least 250 V for a 120-VAC input application. Choose a linear MOSFET with a voltage rating of at least 400 V for a 230-VAC input application. The MOSFET voltage rating must take into account the MOV clamp voltage in protected applications as this may be higher than the MOSFET and damage may occur during a surge event. The Safe Operating Area (SOA) of the MOSFET must also be taken into account. During start-up the MOSFET experiences high voltages as the LED capacitors charge. This leads to high power dissipation during start-up that the MOSFET must withstand. Use with forward phase dimmers also causes a significant current spike in the MOSFET when the dimmer fires. The magnitude and duration of this current spike is dependent upon many factors and should be measured in any design to confirm the MOSFET is rated properly for long life operation. MOSFET parasitics should also be considered. A very large MOSFET with high parasitic capacitances can cause erroneous switching of the TPS92411 floating drivers.

Feature Description (continued)

7.3.11 EMI Filter

The input EMI filter requirements are specific to each design. A capacitor is needed for filtering and may also require an input resistor. For forward phase applications a snubber across the capacitor is likely to be required. The input resistor and snubber resistor need to have a pulse rating high enough for the particular application both during start-up and during forward phase dimming.

7.3.12 Thermal Shutdown

The TPS92410 device includes thermal shutdown protection. If the die temperature reaches approximately 175°C the device shuts down. When the die temperature cools to approximately 165°C, the device resumes normal operation.

7.4 Device Functional Modes

7.4.1 Multiplier Mode

When the MULT pin detects full rectified AC voltage, the CS voltage follows the rectified AC waveform around its regulation point. This behavior forces the current that is drawn from the line to follow the AC input voltage waveform. This action results in high power factor and low total harmonic distortion (THD). Line transients are rejected by the time constant that is initially set on the dimmer detect circuit to ensure dimmer detect mode is not engaged by random voltage spikes on the line.

7.4.2 Dimmer Detect Mode

When a forward phase dimmer is present there is a sharp edge presented to the MULT pin each cycle. This forces the dimmer detect circuit past its time constant and the device enters dimming mode. The CS voltage is then set at a DC level to prevent dimmer misfire

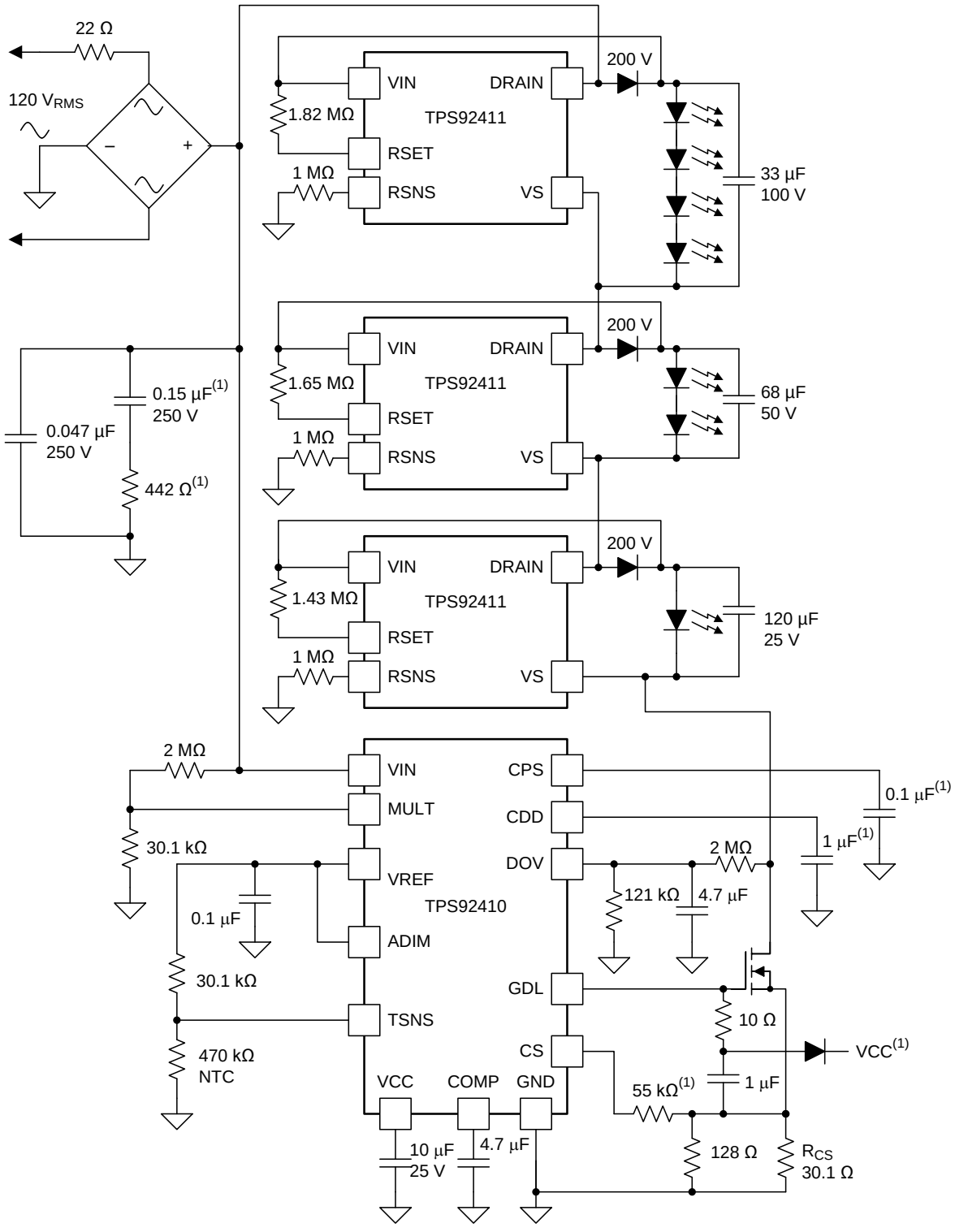
8 Application and Implementation

8.1 Application Information

The TPS92410 is a linear controller designed to be used in conjunction with the TPS92411 switch for high voltage off-line LED drive applications. Typical uses include 120 VAC and 230 VAC input LED drivers with either analog or phase dimming. However like any linear controller it may also be used with a DC input voltage up to 450 V. The following applications are for typical off-line LED drivers with 120 VAC and 230 VAC input voltages.

8.2 Typical Application

8.2.1 120-VAC Input, 6.6-W LED Driver



(1) Required only for forward phase dimmer capability.

Figure 12. 120-V Application Schematic

Typical Application (continued)

8.2.1.1 Design Requirements

This application requires a 6.6-W input power, high-efficiency, phase-dimmable LED lamp for use on 120-V systems.

8.2.1.2 Detailed Design Procedure

The TPS92411 components are chosen using the guidelines in the TPS92411 datasheet. Most of the values used for the TPS92410 are recommended values for any 120-V system. Connect the input voltage directly to the rectified AC while the MULT pin is connected to a 2-MΩ, 30.1-kΩ resistor divider from the rectified AC to ground. The VREF pin should have a 0.1-µF capacitor tied to ground for decoupling. The VCC pin should be decoupled using a 10-µF ceramic capacitor to ground and the COMP pin should have a 4.7-µF ceramic capacitor to ground. Connect a 0.1-µF ceramic capacitor from the CPS pin to ground. Connect a 1-µF ceramic capacitor from the CDD pin to ground to enable phase dimmable operation. This results in a 150 ms dimmer detect time constant. The over-voltage protection using the DOV pin can be set using Equation 3. In this case a MOSFET drain over-voltage level of approximately 27 V is chosen. A 4.7-µF capacitor should be placed in parallel with a 121-kΩ resistor from the DOV pin to ground to set a time constant and for filtering for all applications.

Choose R_{DRAIN} for the appropriate voltage, in this case 2 MΩ is chosen. Connect a 10-Ω resistor in series with a 1-µF ceramic capacitor from GDL to CS for stability and to help reduce EMI. Place a diode from the center point of these two components to the VCC pin to clamp the voltage on the GDL pin and the CS pin that can become high with some forward phase dimmers. A rating of at least 20 V and 100 mA is recommended with a peak-repetitive current rating of at least 2 A. A 55-kΩ resistor should be connected between the MOSFET source and the CS pin for additional protection. Connect a 30.1-kΩ resistor from the TSNS pin to the VREF pin. The NTC thermistor to ground should be selected so that the desired foldback temperature results in a thermistor value of 30.1 kΩ. R_{CS} is then calculated using Equation 1. R_{CS} = 25 Ω is very close, a 30.1 Ω in parallel with a 182 Ω resulting in about 25.83 Ω was chosen.

8.2.1.3 Application Curves

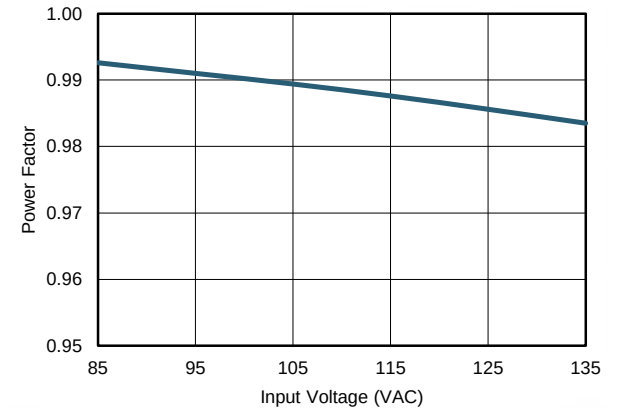


Figure 13. Power Factor vs Input Voltage

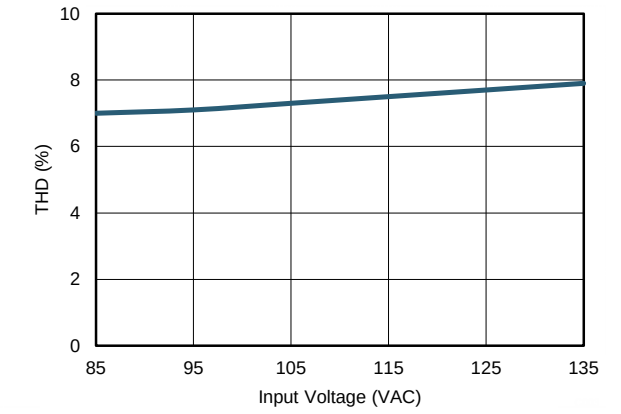
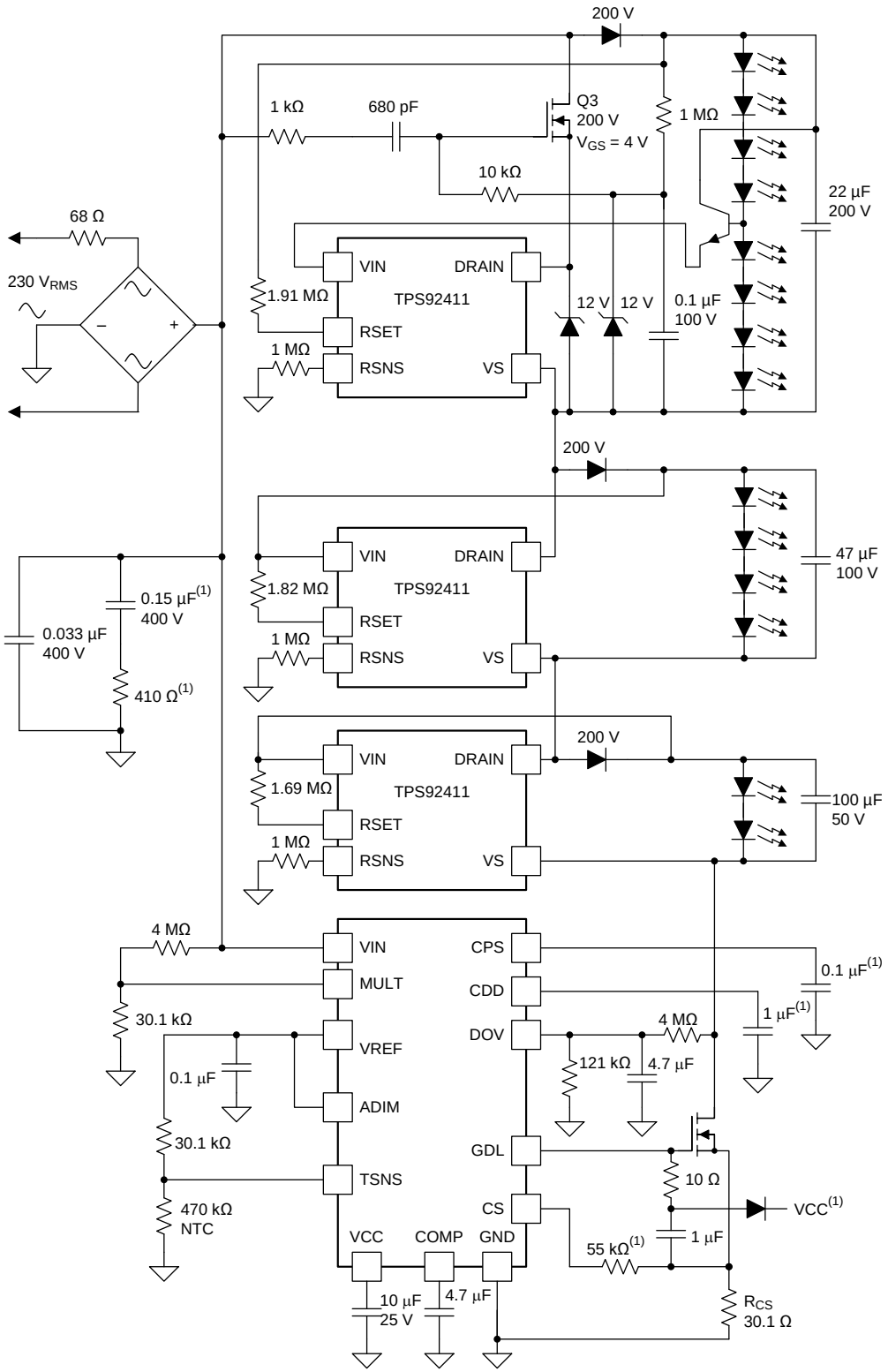


Figure 14. Total Harmonic Distortion vs Input Voltage

Typical Application (continued)

8.2.2 230-VAC Input, 11-W LED Driver



(1) Required only for forward phase dimmer capability.

Figure 15. 230-V Application Schematic

Typical Application (continued)

8.2.2.1 Design Requirements

This application requires a 11-W input power, high-efficiency, phase-dimmable LED lamp for use on 230-V systems.

8.2.2.2 Detailed Design Procedure

The TPS92411 components are chosen using the guidelines in the TPS92411 datasheet. Most of the values used for the TPS92410 are recommended values for any 230-V system. The input voltage should be connected directly to rectified AC while the MULT pin is connected to a 4-MΩ, 30.1-kΩ resistor divider between rectified AC and ground. The VREF pin should have a 0.1-µF capacitor connected to ground to provide decoupling. The VCC pin should be decoupled using a 10-µF ceramic capacitor to ground and the COMP pin should have a 4.7-µF ceramic capacitor to ground. Connect a 0.1-µF ceramic capacitor from the CPS pin to ground. Connect a 1-µF ceramic capacitor from CDD to ground to enable phase dimmable operation. This results in a 150 ms dimmer detect time constant. The over-voltage protection using the DOV pin can be set using Equation 3. This case includes a MOSFET drain over-voltage level of approximately 51 V. A 4.7-µF capacitor should be placed in parallel with a 121-kΩ resistor from the DOV pin to ground to set a time constant and for filtering for all applications.

Choose R_{DRAIN} for the appropriate voltage, this case uses a value of 4-MΩ. A 10-Ω resistor in series with a 1-µF ceramic capacitor from GDL to CS adds stability and helps reduce EMI. A diode should be placed from the center point of these two components to the VCC pin to clamp the voltage on the GDL pin and the CS pin that can become high with some forward phase dimmers. A rating of at least 20 V and 100 mA is recommended with a peak-repetitive current rating of at least 2 A. A 55-kΩ resistor should be connected between the MOSFET source and the CS pin for additional protection. Connect a 30.1-kΩ resistor from the TSNS pin to the VREF pin. The NTC thermistor to ground should be selected so that the desired foldback temperature results in a thermistor value of 30.1 kΩ. R_{CS} is then calculated using Equation 1. R_{CS} = 30.1 Ω is very close and was chosen for this design.

8.2.2.3 Application Curves

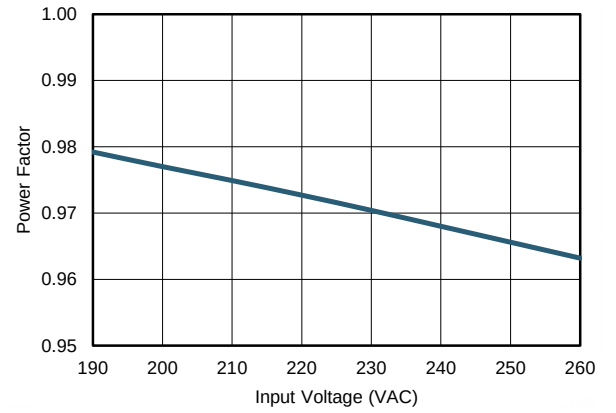


Figure 16. Power Factor vs Input Voltage

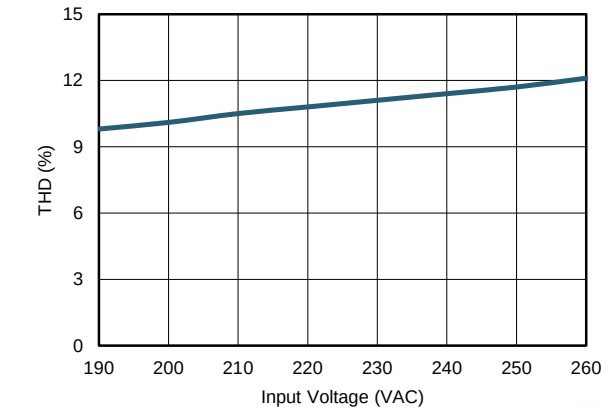


Figure 17. Total Harmonic Distortion vs Input Voltage

9 Power Supply Recommendations

For testing purposes any benchtop adjustable AC power supply with a power rating higher than what is required by the circuit is suitable. An example would be an Hewlett Packard 6811B or equivalent. An isolated supply is recommended for safety purposes.

10 Layout

Proper layout is important in any regulator design. The TPS92410 is a linear regulator which simplifies layout compared to a switching regulator, however some consideration should be taken.

10.1 Layout Guidelines

Components between CPS, CDD, DOV, COMP, VREF, MULT, and VCC to ground (GND) should be placed directly next to the device as shown in Figure 18. The linear MOSFET as well as the GDL and CS traces should be placed as close the TPS92410 as possible as well.

10.2 Layout Example

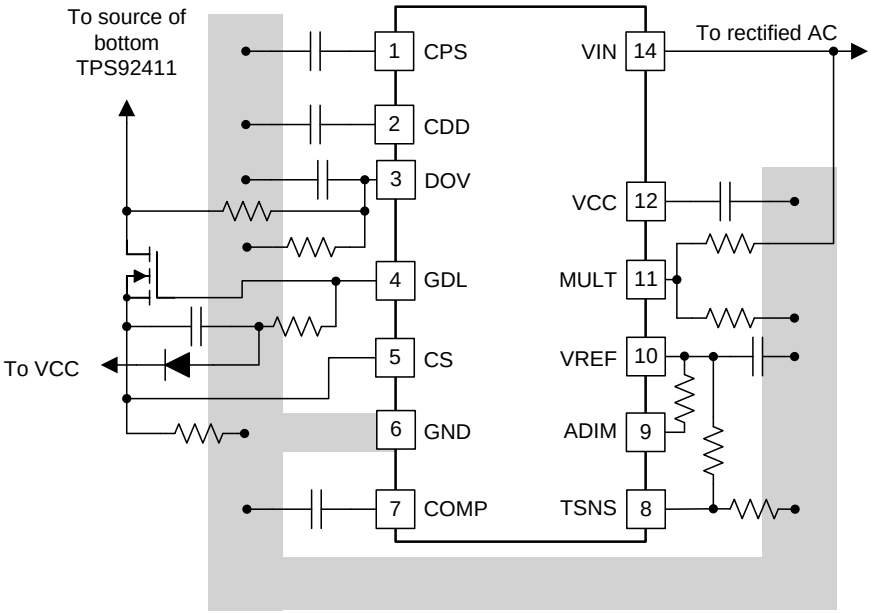


Figure 18. Recommended Component Placement

11 Device and Documentation Support

11.1 Trademarks

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92410D	ACTIVE	SOIC	D	13	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	TPS92410D	Samples
TPS92410DR	ACTIVE	SOIC	D	13	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	TPS92410D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

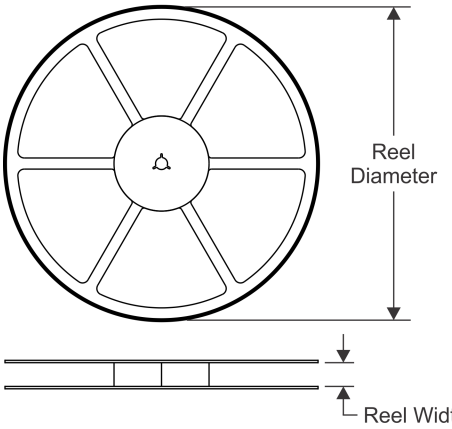
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

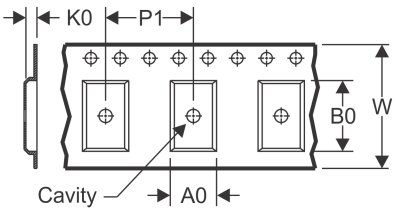
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

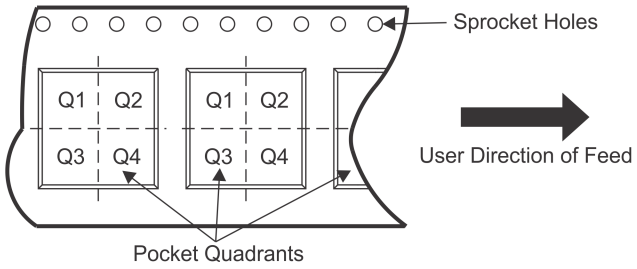


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

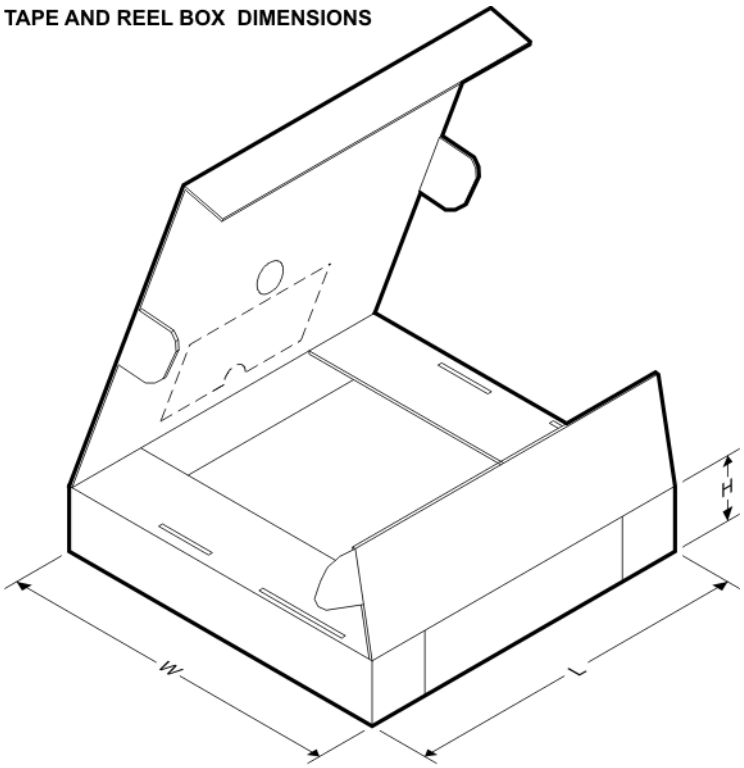
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92410DR	SOIC	D	13	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92410DR	SOIC	D	13	2500	367.0	367.0	38.0

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265