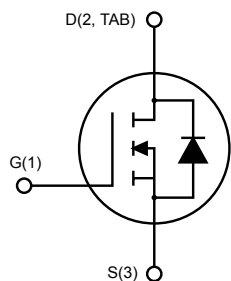
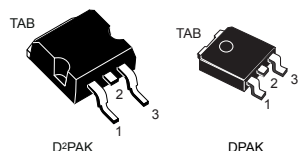


Automotive-grade N-channel 600 V, 0.8 Ω typ., 5 A MDmesh™ II Power MOSFETs in D²PAK and DPAK packages



AM01475v1_noZen

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	Package
STB7ANM60N	600 V	0.9 Ω	5 A	D ² PAK
STD7ANM60N				DPAK

- AEC-Q101 qualified
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high-efficiency converters.



Product status link

[STB7ANM60N](#)
[STD7ANM60N](#)

Product summary

Order code	STB7ANM60N
Marking	7ANM60N
Package	D ² PAK
Packing	Tape and reel
Order code	STD7ANM60N
Marking	7ANM60N
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	600	V
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	5	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	20	A
P_{TOT}	Total power dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	45	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
T_j	Operating junction temperature range	-55 to 150	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		

1. Pulse width limited by safe operating area.

2. $I_{SD} \leq 5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DSpeak} \leq V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	DPAK	
$R_{thj-case}$	Thermal resistance junction-case	2.78		$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	35	50	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_{jmax})	2	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AS}$, $V_{DD} = 50\text{ V}$)	119	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	600			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 600 V			1	μA
		V _{GS} = 0 V, V _{DS} = 600 V, T _C = 125 °C ⁽¹⁾			100	μA
I _{GSS}	Gate body leakage current	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 2.5 A		0.8	0.9	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 50 V, f = 1 MHz, V _{GS} = 0 V	-	363	-	pF
C _{oss}	Output capacitance			24.6		
C _{rss}	Reverse transfer capacitance			1.1		
C _{oss eq.} ⁽¹⁾	Equivalent capacitance time related	V _{DS} = 0 to 480 V, V _{GS} = 0 V	-	130	-	pF
R _G	Intrinsic gate resistance	f = 1 MHz open drain	-	5.4	-	Ω
Q _g	Total gate charge	V _{DD} = 480 V, I _D = 5 A, V _{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	14	-	nC
Q _{gs}	Gate-source charge			2.7		
Q _{gd}	Gate-drain charge			7.7		

1. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 300 V, I _D = 2.5 A, R _G = 4.7 Ω, V _{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	7	-	ns
t _r	Rise time			10		
t _{d(off)}	Turn-off delay time			26		
t _f	Fall time			12		

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{SD}	Source-drain current		-		5	A
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)				20	
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 5 A, V _{GS} = 0 V	-		1.3	V
t _{rr}	Reverse recovery time	I _{SD} = 5 A, di/dt = 100 A/μs	-	213		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)		1.5		μC
I _{RRM}	Reverse recovery current			14		A
t _{rr}	Reverse recovery time	I _{SD} = 5 A, di/dt = 100 A/μs	-	265		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 60 V, T _j = 150 °C(see Figure 16. Test circuit for inductive load switching and diode recovery times)		1.8		μC
I _{RRM}	Reverse recovery current			14		A

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

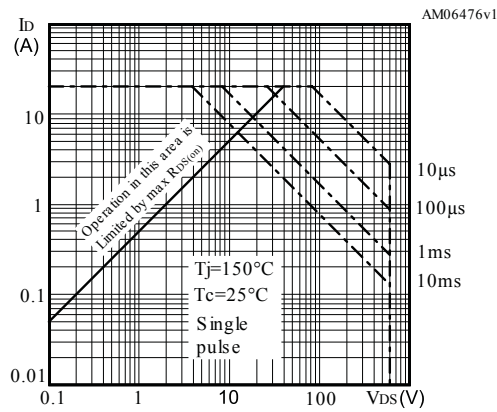
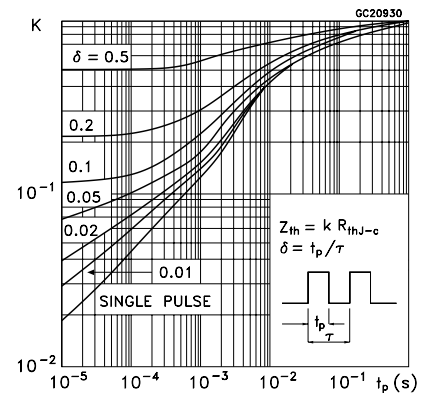
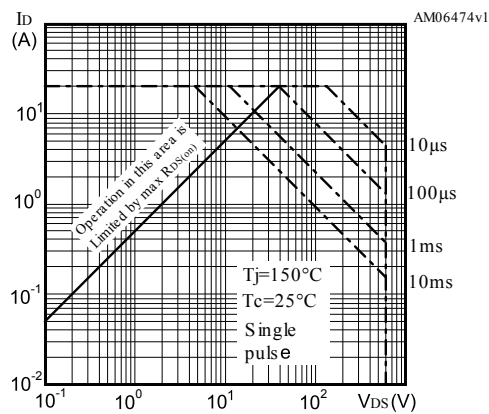
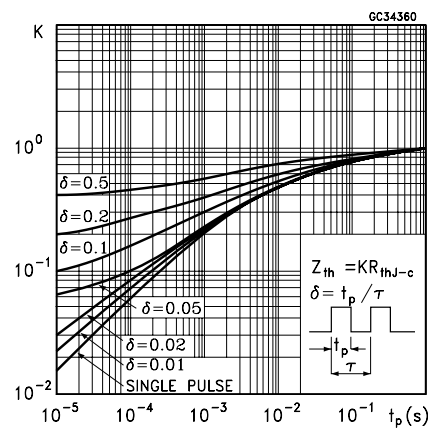
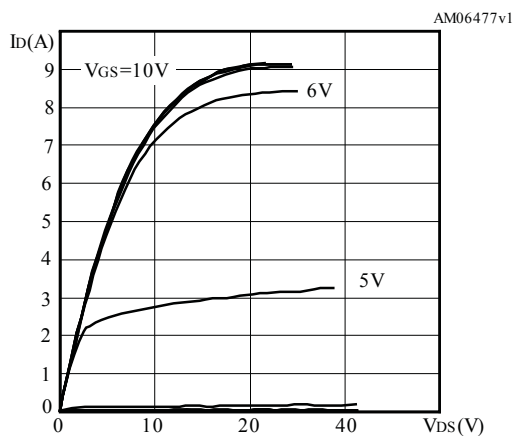
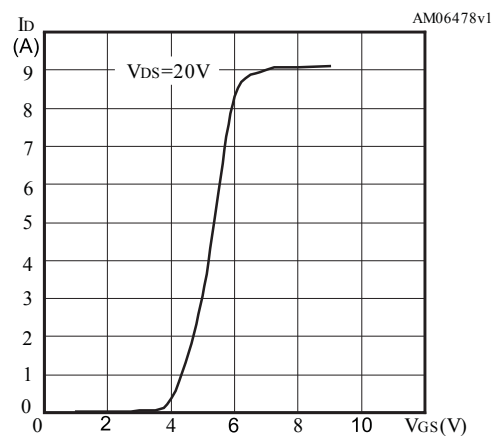
Figure 1. Safe operating area for D²PAK

Figure 2. Thermal impedance for D²PAK

Figure 3. Safe operating area for DPAK

Figure 4. Thermal impedance for DPAK

Figure 5. Output characteristics

Figure 6. Transfer characteristics


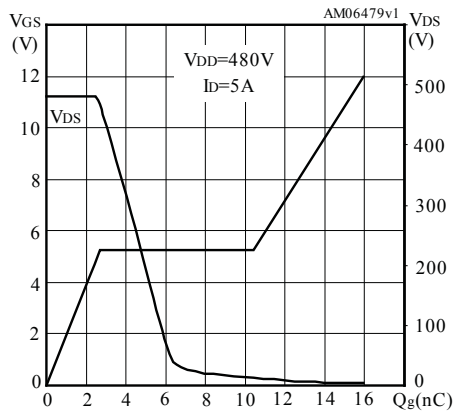
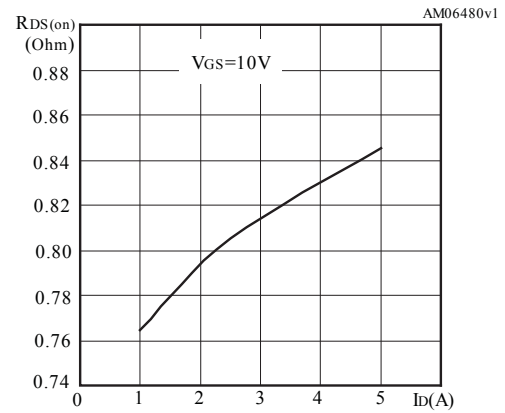
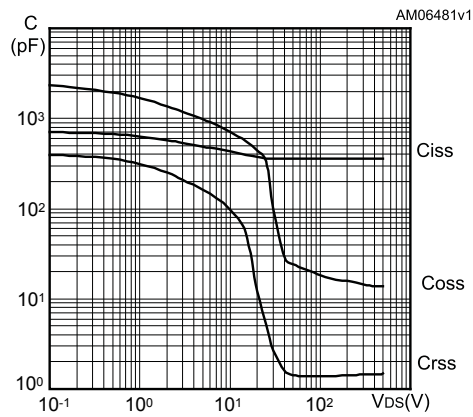
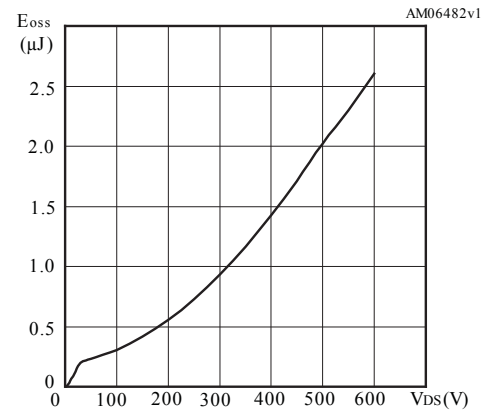
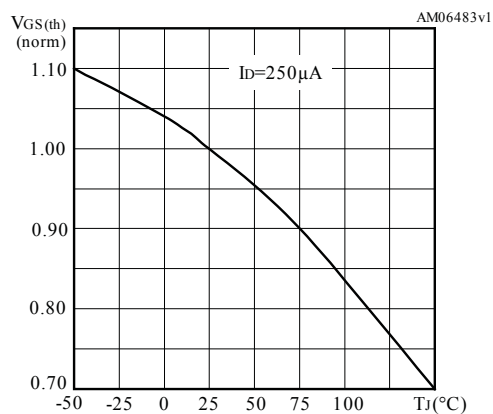
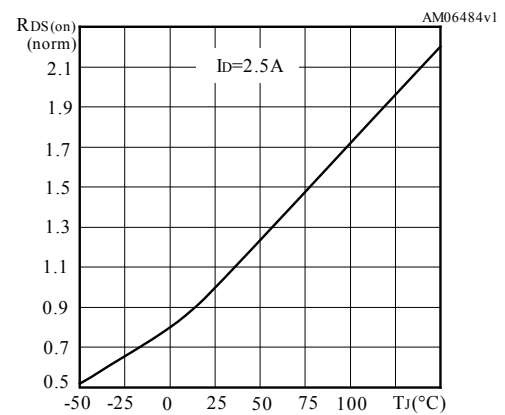
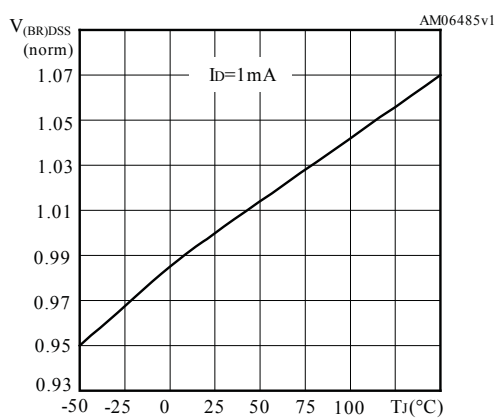
Figure 7. Gate charge vs gate-source voltage

Figure 8. Static drain-source on-resistance

Figure 9. Capacitance variations

Figure 10. Output capacitance stored energy

Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on-resistance vs temperature


Figure 13. Normalized $V_{(BR)DSS}$ vs temperature


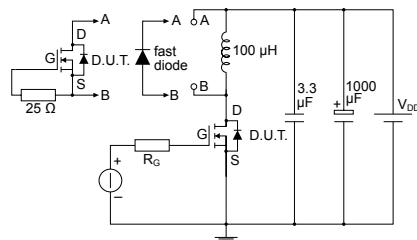
3 Test circuits

Figure 14. Test circuit for resistive load switching times

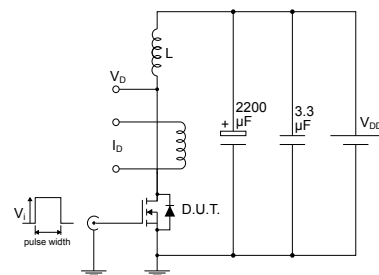

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Figure 15. Test circuit for gate charge behavior

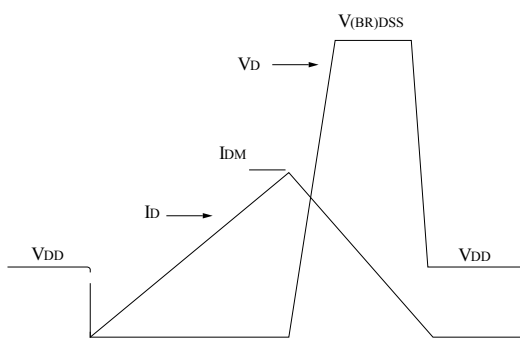

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Figure 16. Test circuit for inductive load switching and diode recovery times


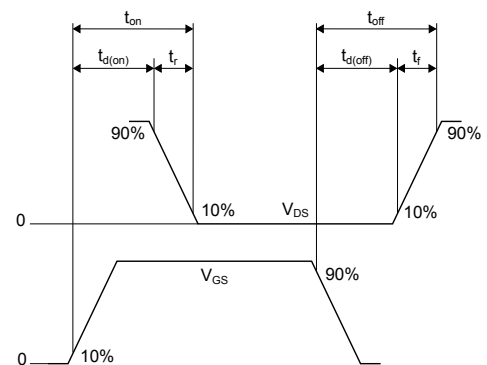
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Figure 17. Unclamped inductive load test circuit


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Figure 18. Unclamped inductive waveform


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Figure 19. Switching time waveform


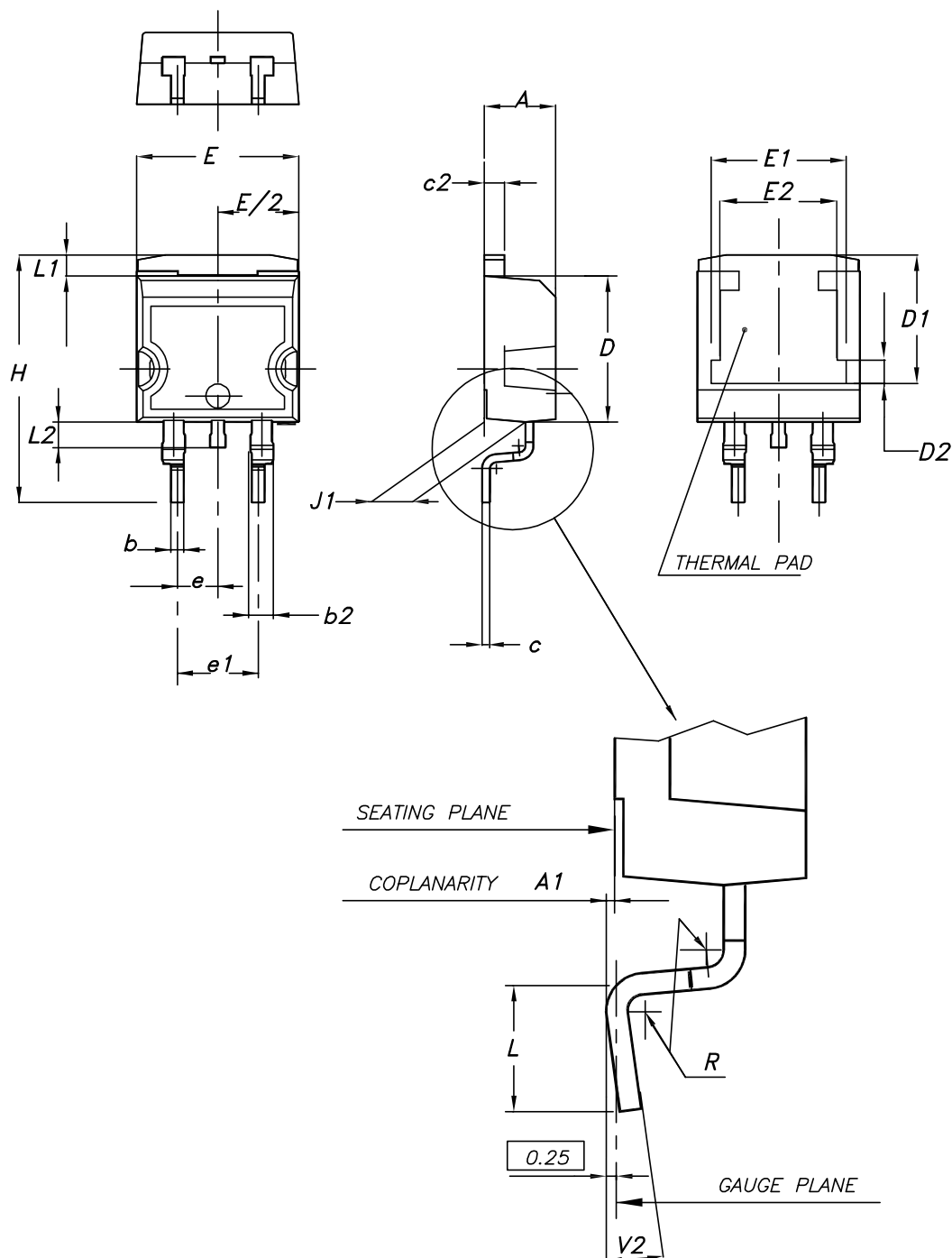
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK®** packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 20. D²PAK (TO-263) type A package outline



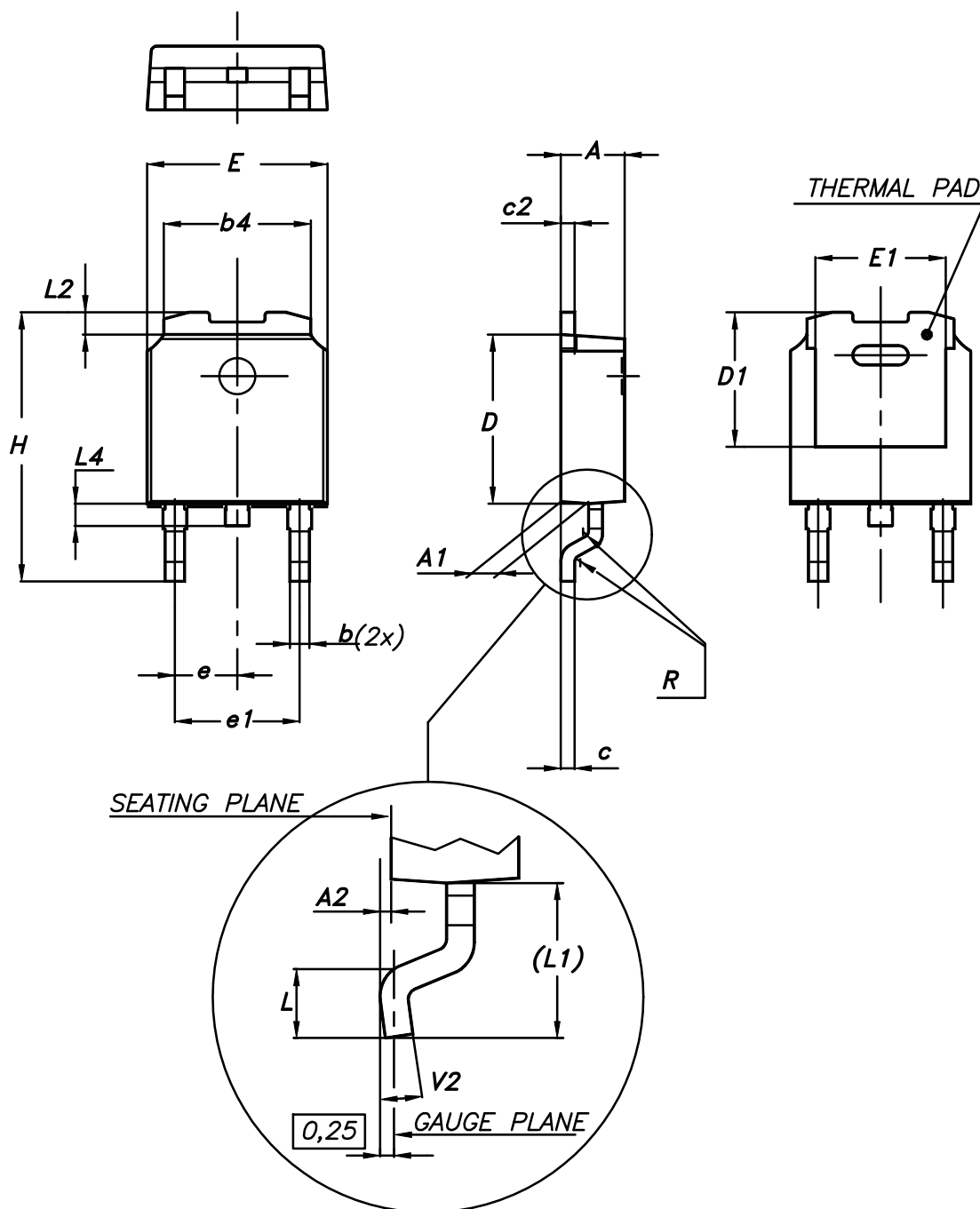
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Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

4.2 DPAK (TO-252) type A package information

Figure 21. DPAK (TO-252) type A package outline

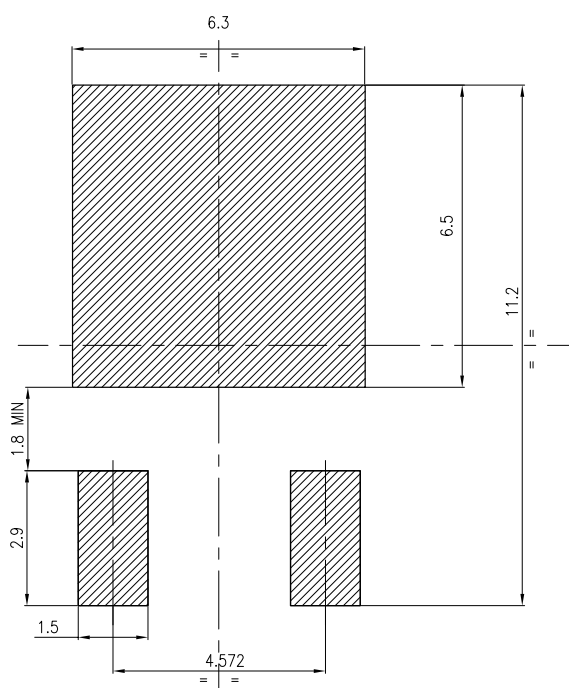


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Table 9. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

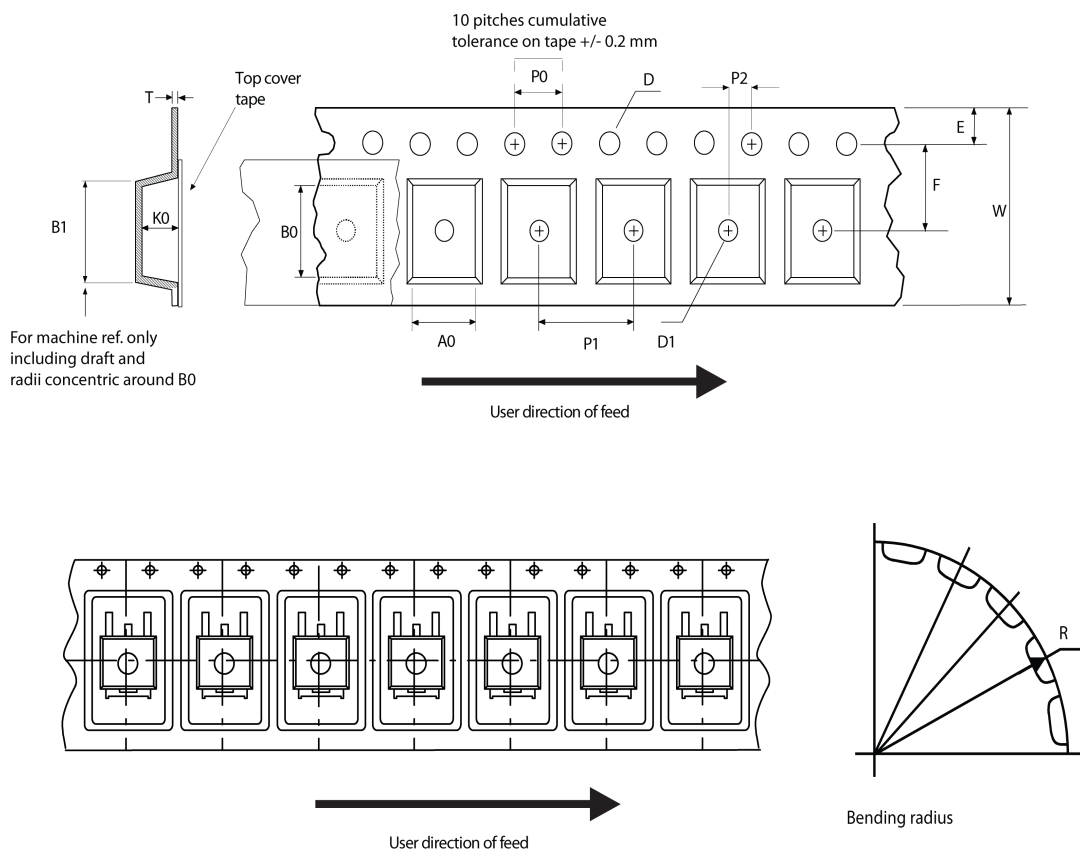
Figure 22. DPAK (TO-252) type A recommended footprint (dimensions are in mm)



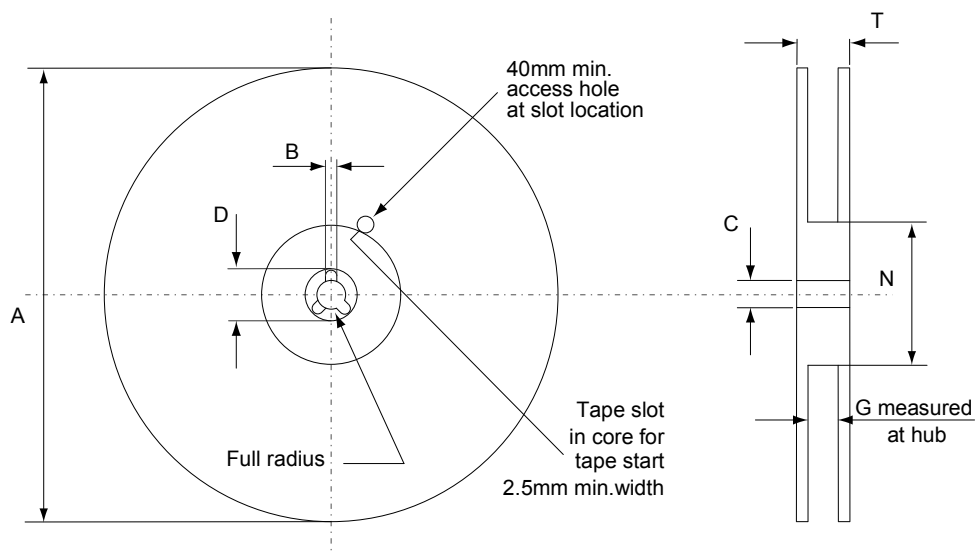
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4.3 D²PAK and DPAK packing information

Figure 23. Tape outline



AM08852v1

Figure 24. Reel outline


AM06038v1

Table 10. D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 11. DPAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 12. Document revision history

Date	Version	Changes
21-Jun-2012	1	First release.
12-Dec-2013	2	– Modified: title, Features and <i>Table 1</i> in cover page – Modified: <i>Figure 15</i>, <i>16</i>, <i>17</i> and <i>18</i> – Updated: <i>Table 10</i> and <i>Figure 23</i>, <i>24</i> – Minor text changes
07-Nov-2018	3	Removed maturity status indication from cover page. The document status is production data. Modified Table 4. On/off states. Updated Section 4 Package information. Minor text changes.

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	Revision history	18

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