MUN5231DW1, NSBC123EDXV6

Dual NPN Bias Resistor Transistors R1 = 2.2 kΩ, R2 = 2.2 kΩ

NPN Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

(T_A = 25°C, common for Q_1 and Q_2, unless otherwise noted)

Rating	Symbol	Max	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current – Continuous	I_C	100	mAdc
Input Forward Voltage	$V_{IN(fwd)}$	12	Vdc
Input Reverse Voltage	$V_{IN(rev)}$	10	Vdc

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ORDERING INFORMATION

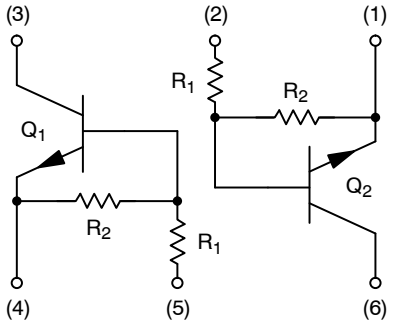
Device	Package	Shipping†
MUN5231DW1T1G	SOT−363	3,000/Tape & Reel
NSBC123EDXV6T1G	SOT−563	4,000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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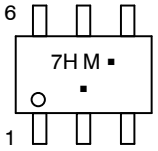
PIN CONNECTIONS



MARKING DIAGRAMS

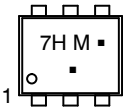


SOT−363
CASE 419B





SOT−563
CASE 463A



7H = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

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THERMAL CHARACTERISTICS

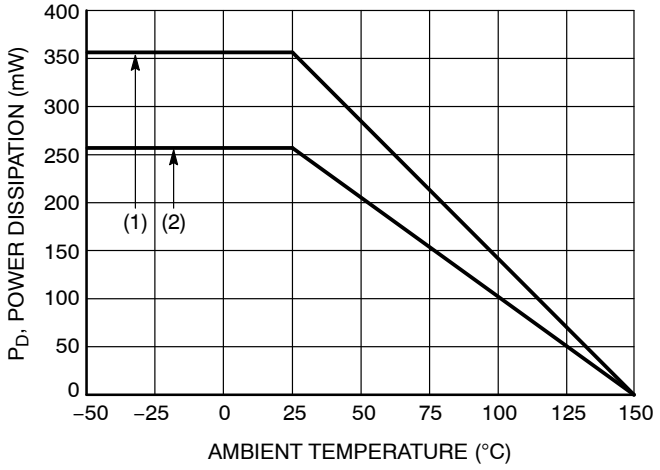
Characteristic		Symbol	Max	Unit
MUN5231DW1 (SOT−363) ONE JUNCTION HEATED				
Total Device Dissipation		P_D		
T_A = 25°C	(Note 1)		187	mW
	(Note 2)		256	
Derate above 25°C	(Note 1)		1.5	mW/°C
	(Note 2)		2.0	
Thermal Resistance, Junction to Ambient	(Note 1)	$R_{\theta JA}$	670	°C/W
	(Note 2)		490	
MUN5231DW1 (SOT−363) BOTH JUNCTION HEATED (Note 3)				
Total Device Dissipation		P_D		
T_A = 25°C	(Note 1)		250	mW
	(Note 2)		385	
Derate above 25°C	(Note 1)		2.0	mW/°C
	(Note 2)		3.0	
Thermal Resistance, Junction to Ambient		$R_{\theta JA}$		°C/W
	(Note 1)		493	
	(Note 2)		325	
Thermal Resistance, Junction to Lead		$R_{\theta JL}$		°C/W
	(Note 1)		188	
	(Note 2)		208	
Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150	°C
NSBC123EDXV6 (SOT−563) ONE JUNCTION HEATED				
Total Device Dissipation		P_D		
T_A = 25°C	(Note 1)		357	mW
Derate above 25°C	(Note 1)		2.9	mW/°C
Thermal Resistance, Junction to Ambient		$R_{\theta JA}$		°C/W
	(Note 1)		350	
NSBC123EDXV6 (SOT−563) BOTH JUNCTION HEATED (Note 3)				
Total Device Dissipation		P_D		
T_A = 25°C	(Note 1)		500	mW
Derate above 25°C	(Note 1)		4.0	mW/°C
Thermal Resistance, Junction to Ambient		$R_{\theta JA}$		°C/W
	(Note 1)		250	
Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ Minimum Pad.
2. FR−4 @ 1.0 × 1.0 Inch Pad.
3. Both junction heated values assume total power is sum of two equally powered channels.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, common for Q_1 and Q_2, unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Base Cutoff Current (V_{CB} = 50 V, I_E = 0)	I_{CBO}	–	–	100	nAdc
Collector-Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)	I_{CEO}	–	–	500	nAdc
Emitter-Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	I_{EBO}	–	–	2.3	mAdc
Collector-Base Breakdown Voltage (I_C = 10 μA, I_E = 0)	$V_{(BR)CBO}$	50	–	–	Vdc
Collector-Emitter Breakdown Voltage (Note 4) (I_C = 2.0 mA, I_B = 0)	$V_{(BR)CEO}$	50	–	–	Vdc
ON CHARACTERISTICS					
DC Current Gain (Note 4) (I_C = 5.0 mA, V_{CE} = 10 V)	h_{FE}	8.0	15	–	
Collector-Emitter Saturation Voltage (Note 4) (I_C = 10 mA, I_B = 5.0 mA)	$V_{CE(sat)}$	–	–	0.25	V
Input Voltage (Off) (V_{CE} = 5.0 V, I_C = 1.0 mA)	$V_{i(off)}$	–	1.3	–	Vdc
Input Voltage (On) (V_{CE} = 0.2 V, I_C = 20 mA)	$V_{i(on)}$	–	1.8	–	Vdc
Output Voltage (On) (V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	V_{OL}	–	–	0.2	Vdc
Output Voltage (Off) (V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	V_{OH}	4.9	–	–	Vdc
Input Resistor	R1	1.5	2.2	2.9	kΩ
Resistor Ratio	R_1/R_2	0.8	1.0	1.2	

4. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle ≤ 2%.



(1) SOT−363; 1.0 × 1.0 Inch Pad
(2) SOT−563; Minimum Pad

Figure 1. Derating Curve

TYPICAL CHARACTERISTICS
MUN5231DW1, NSBC123EDXV6

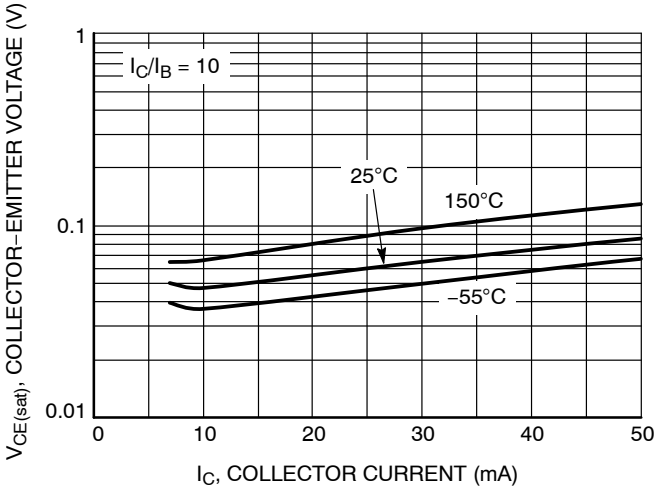


Figure 2. $V_{CE(sat)}$ vs. I_C

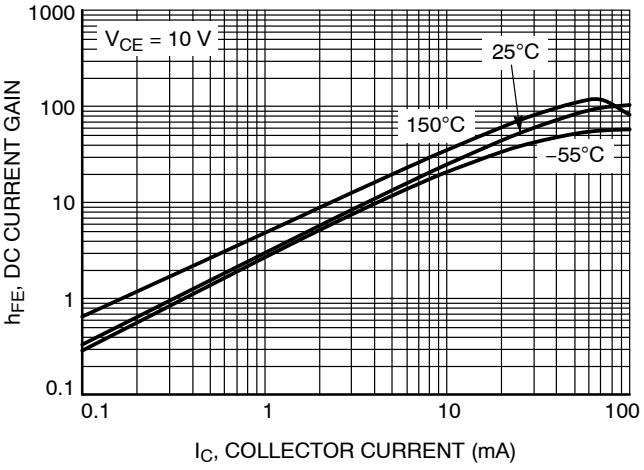


Figure 3. DC Current Gain

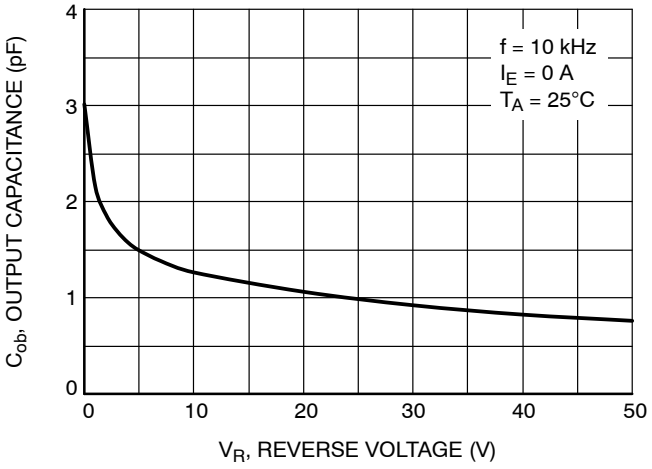


Figure 4. Output Capacitance

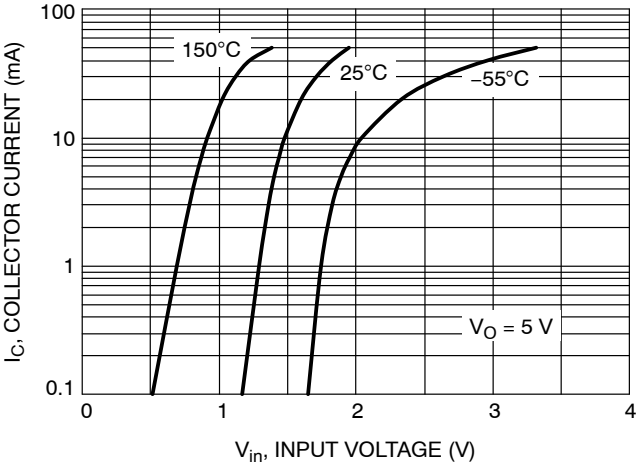


Figure 5. Output Current vs. Input Voltage

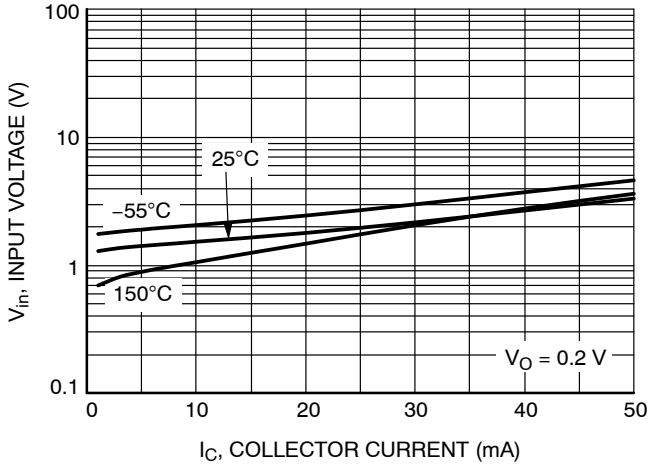
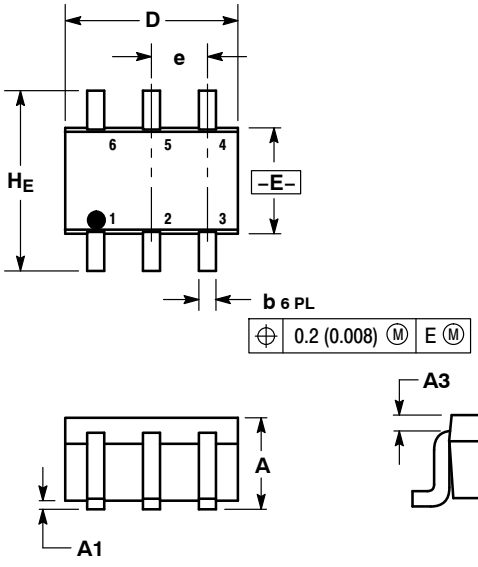


Figure 6. Input Voltage vs. Output Current

PACKAGE DIMENSIONS

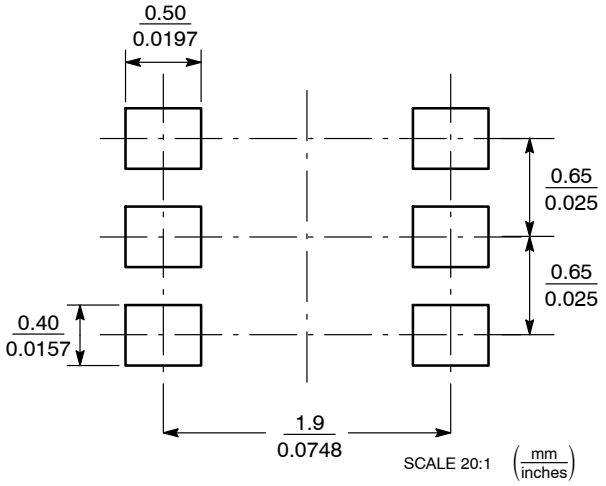
SC−88/SC70−6/SOT−363
CASE 419B−02
ISSUE W



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419B−01 OBSOLETE, NEW STANDARD 419B−02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.95	1.10	0.031	0.037	0.043
A1	0.00	0.05	0.10	0.000	0.002	0.004
A3	0.20 REF			0.008 REF		
b	0.10	0.21	0.30	0.004	0.008	0.012
C	0.10	0.14	0.25	0.004	0.005	0.010
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65 BSC			0.026 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	2.00	2.10	2.20	0.078	0.082	0.086

SOLDERING FOOTPRINT*

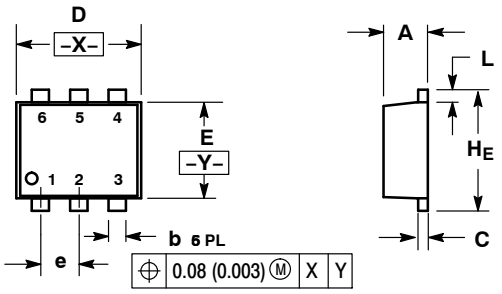


SC−88/SC70−6/SOT−363

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

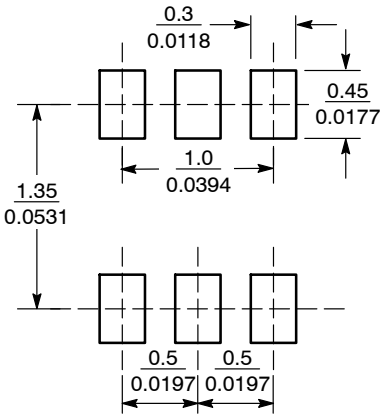
SOT−563, 6 LEAD
CASE 463A
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H_E	1.50	1.60	1.70	0.059	0.062	0.066

SOLDERING FOOTPRINT*



SCALE 20:1 (mm / inches)

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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