DESCRIPTION

Demonstration circuit 528 is a quick way to try the LTC®1740, and gives a clean, compact example of a PC board layout for the part. For a description of how the LTC1740 operates, please refer to the data sheet on the Linear Technology website.

Design files for this circuit board are available. Call the LTC factory.

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QUICK START PROCEDURE

Connecting the Analog Power Supplies

The part can run off a single supply or dual supplies:

Single Supply: VDD=+5V, VSS=0V, AGND=0V

Dual Supplies: VDD=+5V, VSS=–5V, AGND=0V

Connecting the Digital Output Power Supply

OVDD is the supply for the digital output drivers on the part. VCC is the supply for the 74ACT16373 transparent latch that buffers the outputs. For best results, set OVDD=VCC=+3V to +5V. Connect the ground of the digital output supply to OGND.

SENSE pin jumpers

JP1 configures the SENSE pin, which sets the voltage reference, VREF.

JP1 on right: SENSE=GND
VREF=4.50V

JP1 in middle: SENSE=VDD. VREF must be driven externally. Input impedance is about 1kΩ.

JP1 on left: SENSE=VREF
VREF=2.25V

Driving the Analog Input

Apply the analog input signal to the +AIN BNC connector. The negative analog input can be driven at the –AIN BNC connector. For convenience, the negative analog input can also be connected to VCM or AGND with JP2:

JP2 on left two pins: -AIN=AGND
Dual supply operation

JP2 on right two pins: -AIN=VCM (+2.5V)
Single supply operation

The analog input range, Vin = +AIN – -AIN is:

-VREF/2 < Vin < +VREF/2 for PGA gain=1x

Input RC filter

For optimal AC performance, the LTC1740 should have an NPO capacitor across its analog input (C6). This capacitor can be used along with R18 as an input filter to reduce noise in the input signal.

Driving the Clock Input

Apply the encode clock to the CLK BNC connector. For best performance, the clock should have low jitter and rise and fall times of less than 5ns. R17 is a 50 Ohm resistor that terminates the clock to ground. R17 should be removed if the clock signal source cannot drive a 50 Ohm load.

Digital Outputs

The digital outputs appear at the 40-pin connector on the right side of the board. The signals are the fourteen data bits, overflow, and a buffered version of the clock that can be used to latch the data. For best results all wires connected to the output bus should be as short as possible. The output coding format is selected with JP3:

JP3 on top two pins: 2's complement

JP3 on bottom two pins: straight binary

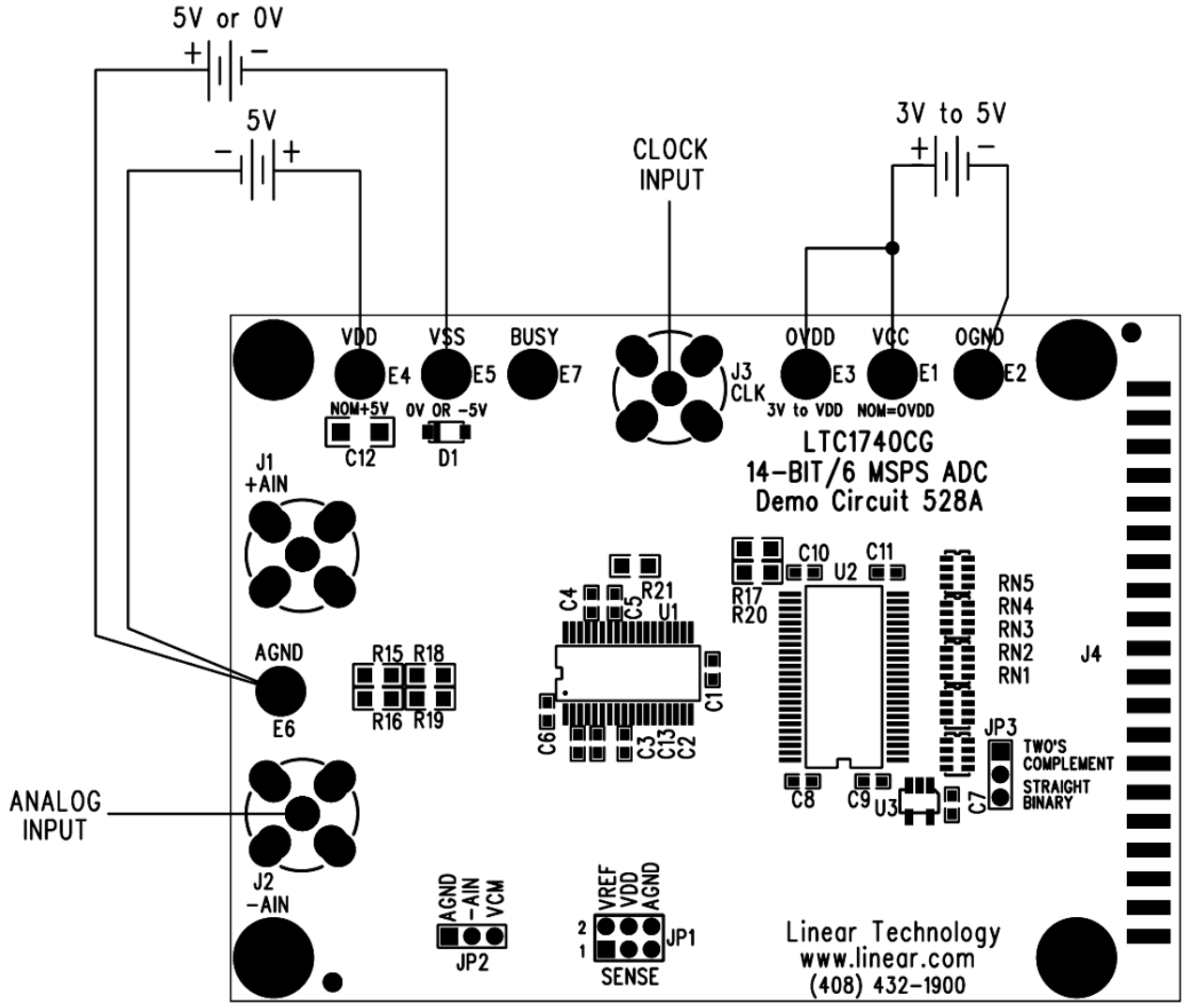
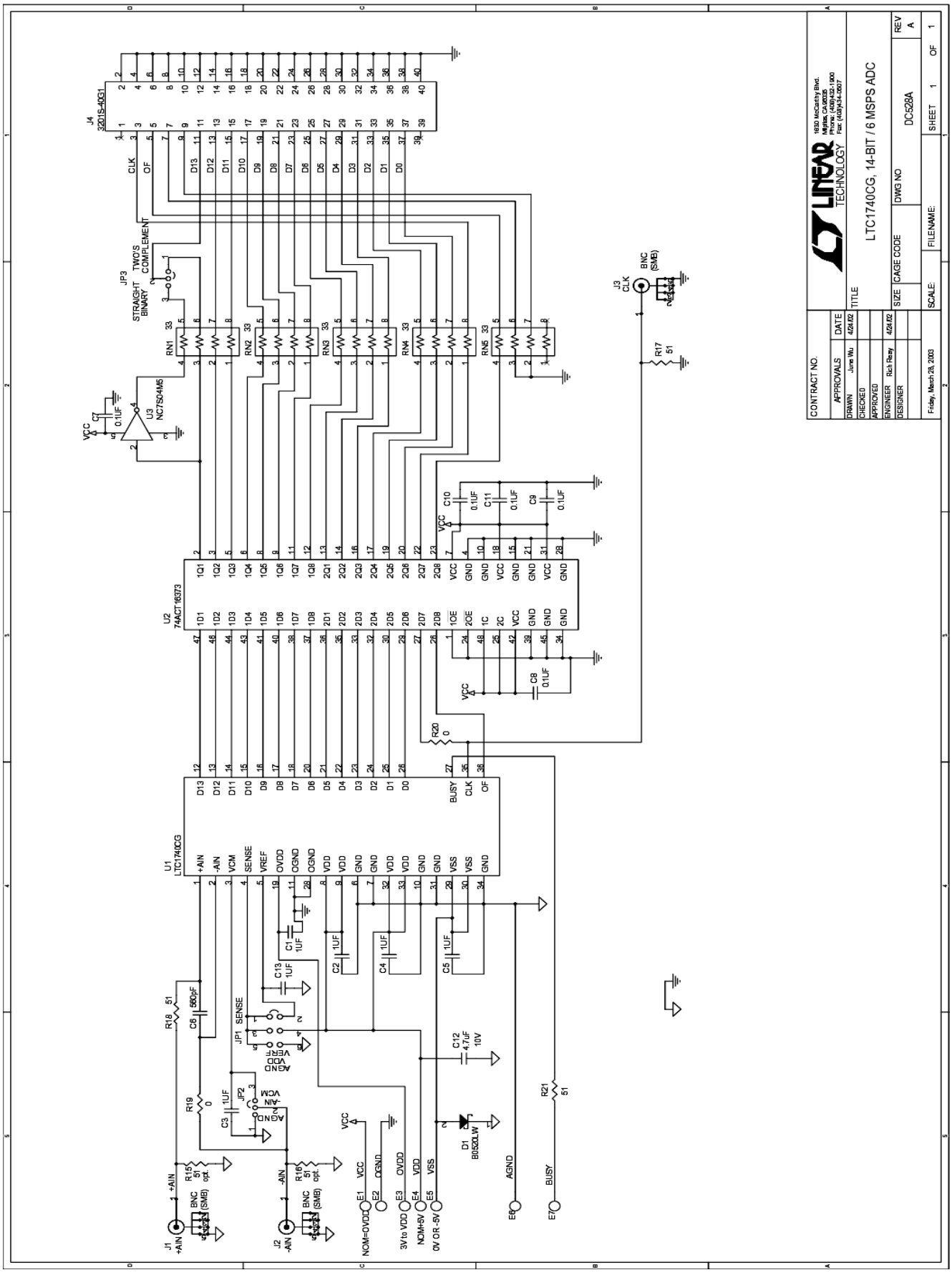


Figure 1. Proper Measurement Equipment Setup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SIZE
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SCALE:
FILENAME:
SHEET 1 OF 1
Friday, March 29, 2003
U1 LTC1740CG
U2 74ACT16373
U3 NC7SO4M5
J1 +AIN
J2 -AIN
J3 CLK
J4 3201S-40G1
JP1 SENSE
JP2 VCM
JP3 TWO'S COMPLEMENT
STRAIGHT BINARY
NOM=OVDD
3V to VDD
NOM+5V
0V OR -5V
BUSY
AGND
VCC