Multiformat SDTV Video Decoder

ADV7183B

FEATURES

- Multiformat video decoder supports NTSC-(J, M, 4.43), PAL-(B/D/G/H/I/M/N), SECAM
- Integrates three 54 MHz, 10-bit ADCs
- Clocked from a single 27 MHz crystal
- Line-locked clock-compatible (LLC)
- Adaptive Digital Line Length Tracking (ADLLT™), signal processing, and enhanced FIFO management give mini-TBC functionality
- 5-line adaptive comb filters
- Proprietary architecture for locking to weak, noisy, and unstable video sources such as VCRs and tuners
- Subcarrier frequency lock and status information output
- Integrated AGC with adaptive peak white mode
- Macrovision® copy protection detection
- Chroma transient improvement (CTI)
- Digital noise reduction (DNR)
- Multiple programmable analog input formats
  - Composite video (CVBS)
  - S-Video (Y/C)
  - YPrPb component (VESA, MII, SMPTE, and BetaCam)
- 12 analog video input channels
- Automatic NTSC/PAL/SECAM identification
- Digital output formats (8-bit or 16-bit)
  - ITU-R BT.656 YCrCb 4:2:2 output + HS, VS, and FIELD
- 0.5 V to 1.6 V analog signal input range
- Differential gain: 0.5% typ
- Differential phase: 0.5° typ
- Programmable video controls
  - Peak white/hue/brightness/saturation/contrast
- Integrated on-chip video timing generator
- Free-run mode (generates stable video output with no I/P)
- VBI decode support for close captioning, WSS, CGMS, EDTV, Gemstar® 1×/2×
- Power-down mode
- 2-wire serial MPU interface (I²C®-compatible)
- 3.3 V analog, 1.8 V digital core; 3.3 V IO supply
- 2 temperature grades: 0°C to +70°C and –40°C to +85°C
- 80-lead LQFP Pb-free package

APPLICATIONS

- DVD recorders
- Video projectors
- HDD-based PVRs/DVDRs
- LCD TVs
- Set-top boxes
- Security systems
- Digital televisions
- AVR receivers

GENERAL DESCRIPTION

The ADV7183B integrated video decoder automatically detects and converts a standard analog baseband television signal-compatible with worldwide standards NTSC, PAL, and SECAM into 4:2:2 component video data-compatible with 16-/8-bit CCIR601/CCIR656.

The advanced and highly flexible digital output interface enables performance video decoding and conversion in line-locked clock-based systems. This makes the device ideally suited for a broad range of applications with diverse analog video characteristics, including tape-based sources, broadcast sources, security/surveillance cameras, and professional systems.

The 10-bit accurate A/D conversion provides professional quality video performance and is unmatched. This allows true 8-bit resolution in the 8-bit output mode.

The 12 analog input channels accept standard composite, S-Video, YPrPb video signals in an extensive number of combinations. AGC and clamp restore circuitry allow an input video signal peak-to-peak range of 0.5 V up to 1.6 V. Alternatively, these can be bypassed for manual settings.

The fixed 54 MHz clocking of the ADCs and datapath for all modes allows very precise, accurate sampling and digital filtering. The line-locked clock output allows the output data rate, timing signals, and output clock signals to be synchronous, asynchronous, or line locked even with ±5% line length variation. The output control signals allow glueless interface connections in almost any application. The ADV7183B modes are set up over a 2-wire, serial, bidirectional port (I²C-compatible).

The ADV7183B is fabricated in a 3.3 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation.

The ADV7183B is packaged in a small 80-lead LQFP Pb-free package.

Rev. B

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **© 2005 Analog Devices, Inc. All rights reserved.**

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9/04—Revision 0: Initial Version

INTRODUCTION

The ADV7183B is a high quality, single chip, multiformat video decoder that automatically detects and converts PAL, NTSC, and SECAM standards in the form of composite, S-Video, and component video into a digital ITU-R BT.656 format.

The advanced and highly flexible digital output interface enables performance video decoding and conversion in line-locked, clock-based systems. This makes the device ideally suited for a broad range of applications with diverse analog video characteristics, including tape based sources, broadcast sources, security/surveillance cameras, and professional systems.

ANALOG FRONT END

The ADV7183B analog front end comprises three 10-bit ADCs that digitize the analog video signal before applying it to the standard definition processor. The analog front end uses differential channels to each ADC to ensure high performance in mixed-signal applications.

The front end also includes a 12-channel input mux that enables multiple video signals to be applied to the ADV7183B. Current and voltage clamps are positioned in front of each ADC to ensure the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping within the ADV7183B. The ADCs are configured to run in 4× oversampling mode.

STANDARD DEFINITION PROCESSOR (SDP)

The ADV7183B is capable of decoding a large selection of baseband video signals in composite, S-Video, and component formats. The video standards supported include PAL B/D/I/G/H, PAL60, PAL M, PAL N, PAL Nc, NTSC M/J, NTSC 4.43, and SECAM B/D/G/K/L. The ADV7183B can automatically detect the video standard and process it accordingly.

The ADV7183B has a 5-line, superadaptive, 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to video standard and signal quality with no user intervention required. Video user controls such as brightness, contrast, saturation, and hue are also available within the ADV7183B.

The ADV7183B implements a patented adaptive digital line-length tracking (ADLLT) algorithm to track varying video line lengths from sources. ADLLT enables the ADV7183B to track and decode poor quality video sources such as VCRs, noisy sources from tuner outputs, VCD players, and camcorders. The ADV7183B contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The ADV7183B can process a variety of VBI data services, such as closed captioning (CC), wide screen signaling (WSS), copy generation management system (CGMS), EDTV, Gemstar 1×/2×, and extended data service (XDS). The ADV7183B is fully Macrovision® certified; detection circuitry enables Type I, II, and III protection levels to be identified and reported to the user. The decoder is also fully robust to all Macrovision signal inputs.

FUNCTIONAL BLOCK DIAGRAM

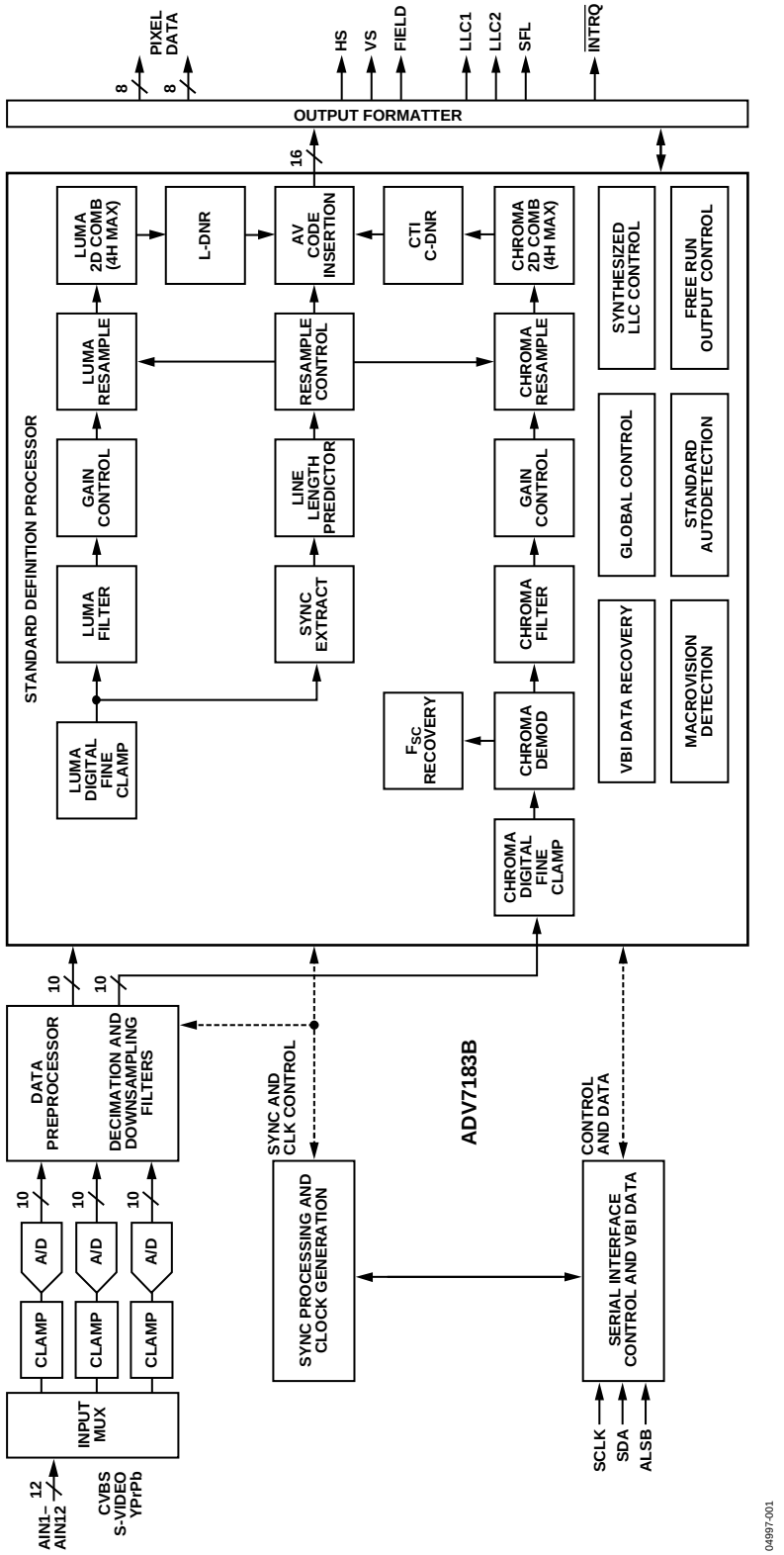


Figure 1.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

At A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, operating temperature range, unless otherwise specified.

Table 1.

Parameter[1, 2]	Symbol	Test Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution (each ADC)	N				10	Bits
Integral Nonlinearity	INL	BSL at 54 MHz		–0.475/+0.6	±3	LSB
Differential Nonlinearity	DNL	BSL at 54 MHz		–0.25/+0.5	–0.7/+2	LSB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	Pins listed in Note 3	–50		+50	µA
		All other pins	–10		+10	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.4 mA	2.4			V
Output Low Voltage	V_{OL}	I_{SINK} = 3.2 mA			0.4	V
High Impedance Leakage Current	I_{LEAK}	Pins listed in Note 4			50	µA
		All other pins			10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS[5]						
Digital Core Power Supply	D_{VDD}		1.65	1.8	2	V
Digital I/O Power Supply	D_{VDDIO}		3.0	3.3	3.6	V
PLL Power Supply	P_{VDD}		1.65	1.8	2.0	V
Analog Power Supply	A_{VDD}		3.15	3.3	3.45	V
Digital Core Supply Current	I_{DVDD}			82		mA
Digital I/O Supply Current	I_{DVDDIO}			2		mA
PLL Supply Current	I_{PVDD}			10.5		mA
Analog Supply Current	I_{AVDD}	CVBS input[6]		85		mA
		YPrPb input[7]		180		mA
Power-Down Current	I_{PWRDN}			1.5		mA
Power-Up Time	t_{PWRUP}			20		ms

[1]Temperature range: T_{MIN} to T_{MAX}, –40°C to +85°C (0°C to 70°C for ADV7183BKSTZ).
[2]The min/max specifications are guaranteed over this range.
[3] Pins 36 and 79.
[4] Pins 1, 2, 5, 6, 8, 12, 17, 18 to 24, 32 to 35, 74 to 76, 80.
[5] Guaranteed by characterization.
[6] ADC1 powered on.
[7] All three ADCs powered on.

VIDEO SPECIFICATIONS

At A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, operating temperature range, unless otherwise specified.

Table 2.

Parameter[1, 2]	Symbol	Test Conditions	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS I/P, modulate 5-step		0.5	0.7	Degrees
Differential Gain	DG	CVBS I/P, modulate 5-step		0.5	0.7	%
Luma Nonlinearity	LNL	CVBS I/P, 5-step		0.5	0.7	%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp	54	56		dB
		Luma flat field	58	60		dB
Analog Front End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			–5		+5	%
Vertical Lock Range			40		70	Hz
F_{SC} Subcarrier Lock Range				±1.3		Hz
Color Lock In Time				60		Lines
Sync Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed				100		Lines
CHROMA SPECIFICATIONS						
Hue Accuracy	HUE			1		Degrees
Color Saturation Accuracy	CL_AC			1		%
Color AGC Range			5		400	%
Chroma Amplitude Error				0.5		%
Chroma Phase Error				0.4		Degrees
Chroma Luma Intermodulation				0.2		%
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V I/P		1		%
Luma Contrast Accuracy		CVBS, 1 V I/P		1		%

[1] Temperature range: T_{MIN} to T_{MAX}, –40°C to +85°C (0°C to 70°C for ADV7183BKSTZ).
[2] The min/max specifications are guaranteed over this range.

TIMING SPECIFICATIONS

Guaranteed by characterization. At A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V, operating temperature range, unless otherwise specified.

Table 3.

Parameter[1, 2]	Symbol	Test Conditions	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Nominal Frequency				28.6363		MHz
Frequency Stability					±50	ppm
I²C PORT						
SCLK Frequency					400	kHz
SCLK Min Pulse Width High	t_1		0.6			µs
SCLK Min Pulse Width Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDA Setup Time	t_5		100			ns
SCLK and SDA Rise Time	t_6				300	ns
SCLK and SDA Fall Time	t_7				300	ns
Setup Time for Stop Condition	t_8			0.6		µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC1 Mark Space Ratio	t_9:t_{10}		45:55		55:45	% duty cycle
LLC1 Rising to LLC2 Rising	t_{11}			0.5		ns
LLC1 Rising to LLC2 Falling	t_{12}			0.5		ns
DATA AND CONTROL OUTPUTS						
Data Output Transitional Time	t_{13}	Negative clock edge to start of valid data; ($t_{ACCESS} = t_{10} - t_{13}$)			3.4	ns
Data Output Transitional Time	t_{14}	End of valid data to negative clock edge; ($t_{HOLD} = t_9 + t_{14}$)			2.4	ns
Propagation Delay to Hi-Z	t_{15}			6		ns
Max Output Enable Access Time	t_{16}			7		ns
Min Output Enable Access Time	t_{17}			4		ns

[1] Temperature range: T_{MIN} to T_{MAX}, –40°C to +85°C (0°C to 70°C for ADV7183BKSTZ).
[2] The min/max specifications are guaranteed over this range.

ANALOG SPECIFICATIONS

Guaranteed by characterization. A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V (operating temperature range, unless otherwise noted). Recommended analog input video signal range: 0.5 V to 1.6 V, typically 1 V p-p.

Table 4.

Parameter[1, 2]	Symbol	Test Conditions	Min	Typ	Max	Unit
CLAMP CIRCUITRY						
External Clamp Capacitor				0.1		µF
Input Impedance		Clamps switched off		10		MΩ
Large Clamp Source Current				0.75		mA
Large Clamp Sink Current				0.75		mA
Fine Clamp Source Current				60		µA
Fine Clamp Sink Current				60		µA

[1] Temperature range: T_{MIN} to T_{MAX}, –40°C to +85°C (0°C to 70°C for ADV7183BKSTZ).
[2] The min/max specifications are guaranteed over this range.

THERMAL SPECIFICATIONS

Table 5.

Parameter[1,2]	Symbol	Test Conditions	Min	Typ	Max	Unit
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane		7.6		°C/W
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	4-layer PCB with solid ground plane		38.1		°C/W

[1] Temperature range: T_{MIN} to T_{MAX}, –40°C to +85°C (0°C to 70°C for ADV7183BKSTZ).
[2] The min/max specifications are guaranteed over this range.

TIMING DIAGRAMS

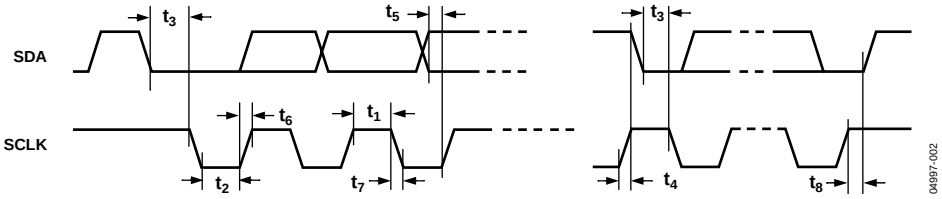


Figure 2. I²C Timing

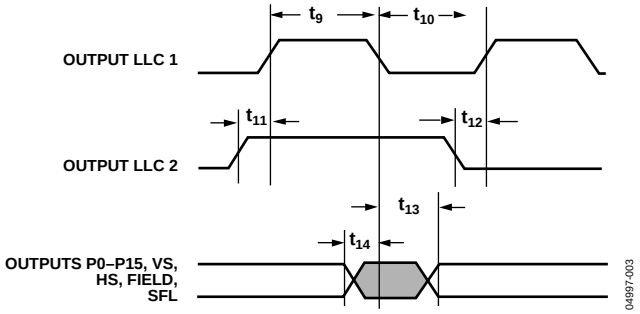


Figure 3. Pixel Port and Control Output Timing

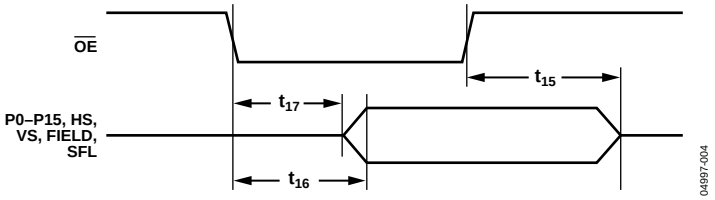


Figure 4. $\overline{OE}$ Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
A_{VDD} to GND	4 V
A_{VDD} to AGND	4 V
D_{VDD} to DGND	2.2 V
P_{VDD} to AGND	2.2 V
D_{VDDIO} to DGND	4 V
D_{VDDIO} to A_{VDD}	–0.3 V to +0.3 V
P_{VDD} to D_{VDD}	–0.3 V to +0.3 V
D_{VDDIO} – P_{VDD}	–0.3 V to +2 V
D_{VDDIO} – D_{VDD}	–0.3 V to +2 V
A_{VDD} – P_{VDD}	–0.3 V to +2 V
A_{VDD} – D_{VDD}	–0.3 V to +2 V
Digital Inputs Voltage to DGND	–0.3 V to D_{VDDIO} + 0.3 V
Digital Output Voltage to DGND	–0.3 V to D_{VDDIO} + 0.3 V
Analog Input to AGND	AGND – 0.3 V to A_{VDD} + 0.3 V
Maximum Junction Temperature (T_J max)	150°C
Storage Temperature Range	–65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

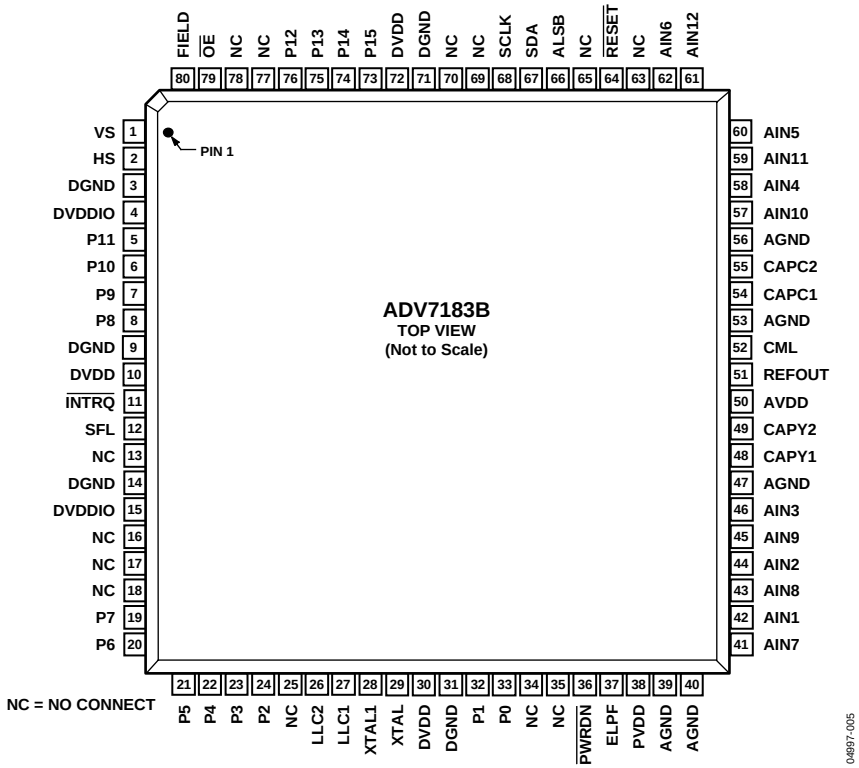


Figure 5. 80-Lead LQFP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
3, 9, 14, 31, 71	DGND	G	Digital Ground.
39, 40, 47, 53, 56	AGND	G	Analog Ground.
4, 15	DVDDIO	P	Digital I/O Supply Voltage (3.3 V).
10, 30, 72	DVDD	P	Digital Core Supply Voltage (1.8 V).
50	AVDD	P	Analog Supply Voltage (3.3 V).
38	PVDD	P	PLL Supply Voltage (1.8 V).
42, 44, 46, 58, 60, 62, 41, 43, 45, 57, 59, 61	AIN1 to AIN12	I	Analog Video Input Channels.
11	$\overline{\text{INTRQ}}$	O	Interrupt Request Output. Interrupt occurs when certain signals are detected on the input video. See the interrupt register map in Table 83.
13, 16 to 18, 25, 34, 35, 63, 65, 69, 70, 77, 78	NC		No Connect Pins.
33, 32, 24, 23, 22, 21, 20, 19, 8, 7, 6, 5, 76, 75, 74, 73	P0 to P15	O	Video Pixel Output Port.
2	HS	O	Horizontal Synchronization Output Signal.
1	VS	O	Vertical Synchronization Output Signal.
80	FIELD	O	Field Synchronization Output Signal.
67	SDA	I/O	I^2C Port Serial Data Input/Output Pin.
68	SCLK	I	I^2C Port Serial Clock Input. Maximum clock rate of 400 kHz.
66	ALSB	I	This pin selects the I^2C address for the ADV7183B. ALSB set to Logic 0 sets the address for a write as 0x40; for ALSB set to logic high, the address selected is 0x42.
64	$\overline{\text{RESET}}$	I	System Reset Input, Active Low. A minimum low reset pulse width of 5 ms is required to reset the ADV7183B circuitry.
27	LLC1	O	This is a line-locked output clock for the pixel data output by the ADV7183B. Nominally 27 MHz, but varies up or down according to video line length.
26	LLC2	O	This is a divide-by-2 version of the LLC1 output clock for the pixel data output by the ADV7183B. Nominally 13.5 MHz, but varies up or down according to video line length.
29	XTAL	I	This is the input pin for the 28.6363 MHz crystal, or can be overdriven by an external 3.3 V, 27 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
28	XTAL1	O	This pin should be connected to the 28.6363 MHz crystal or left as a no connect if an external 3.3 V, 27 MHz clock oscillator source is used to clock the ADV7183B. In crystal mode, the crystal must be a fundamental crystal.
36	$\overline{\text{PWRDN}}$	I	A logic low on this pin places the ADV7183B in a power-down mode. Refer to the IP2PC Register Maps section for more options on power-down modes for the ADV7183B.
79	$\overline{\text{OE}}$	I	When set to a logic low, $\overline{\text{OE}}$ enables the pixel output bus, P15 to P0 of the ADV7183B. A logic high on the $\overline{\text{OE}}$ pin places Pins P15 to P0, HS, VS, SFL into a high impedance state.
37	ELPF	I	The recommended external loop filter must be connected to this ELPF pin, as shown in Figure 46.
12	SFL	O	Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices, Inc. digital video encoder.
51	REFOUT	O	Internal Voltage Reference Output. Refer to Figure 46 for a recommended capacitor network for this pin.
52	CML	O	The CML pin is a common-mode level for the internal ADCs. Refer to Figure 46 for a recommended capacitor network for this pin.
48, 49	CAPY1, CAPY2	I	ADC's Capacitor Network. Refer to Figure 46 for a recommended capacitor network for this pin.
54, 55	CAPC1, CAPC2	I	ADC's Capacitor Network. Refer to Figure 46 for a recommended capacitor network for this pin.

ANALOG FRONT END

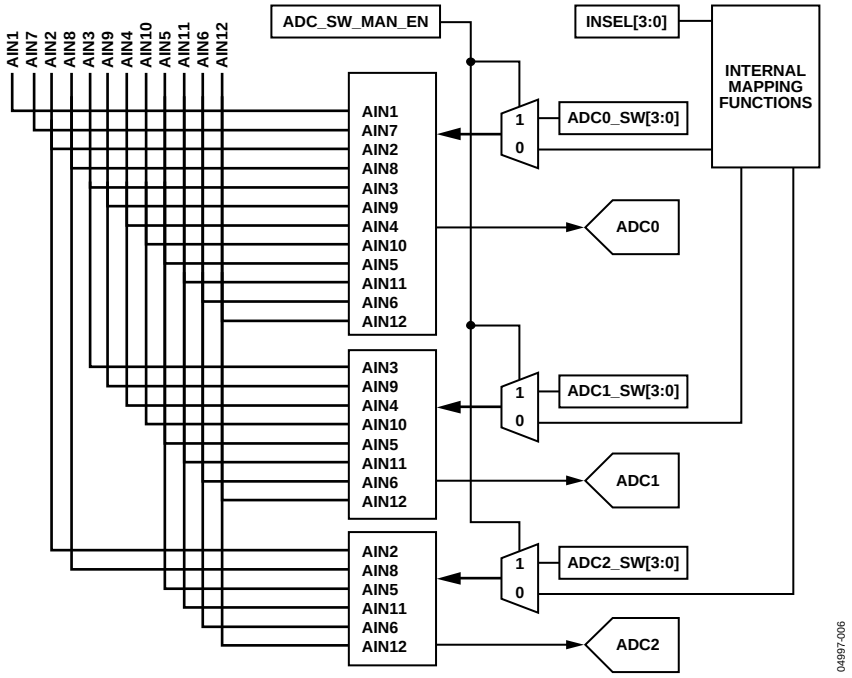


Figure 6. Internal Pin Connections

ANALOG INPUT MUXING

The ADV7183B has an integrated analog muxing section that allows more than one source of video signal to be connected to the decoder. Figure 6 outlines the overall structure of the input muxing provided in the ADV7183B.

As seen in Figure 6, the analog input muxes can be controlled by functional registers (INSEL) or manually. Using INSEL[3:0] simplifies the setup of the muxes and minimizes crosstalk between channels by pre-assigning the input channels. This is referred to as ADI recommended input muxing.

Control via an I²C manual override (ADC_sw_man_en, ADC0_sw, and ADC1_sw, ADC2_sw) is provided for applications with special requirements (for example, number/combinations of signals) that would not be served by the pre-assigned input connections. This is referred to as manual input muxing.

Refer to Figure 7 for an overview of the two methods of controlling the ADV7183B's input muxing.

ADI Recommended Input Muxing

A maximum of 12 CVBS inputs can be connected and decoded by the ADV7183B. As seen in Figure 5, this means the sources will have to be connected to adjacent pins on the IC. This calls for a careful design of the PCB layout, such as ground shielding between all signals routed through tracks that are physically close together.

INSEL[3:0] Input Selection, Address 0x00[3:0]

The INSEL bits allow the user to select an input channel as well as the input format. Depending on the PCB connections, only a subset of the INSEL modes is valid. The INSEL[3:0] not only switches the analog input muxing, it also configures the standard definition processor core to process CVBS (Comp), S-Video (Y/C), or component (YPbPr) format.

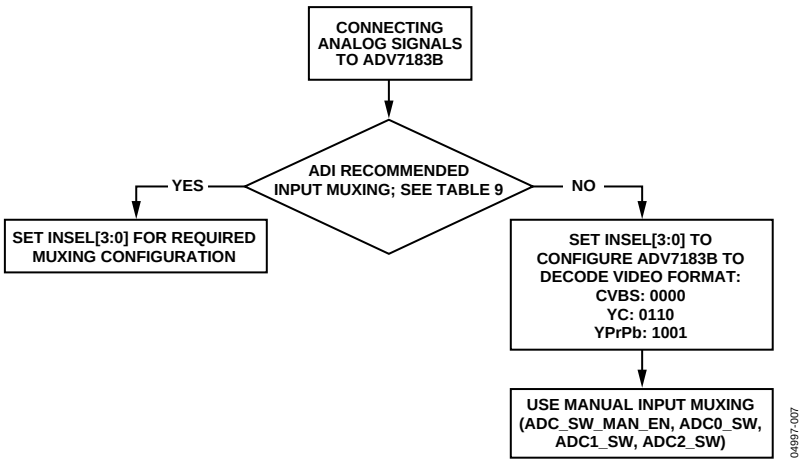


Figure 7. Input Muxing Overview

Table 8. Input Channel Switching Using INSEL[3:0]

	Description	
INSEL[3:0]	**Analog Input Pins**	**Video Format**
0000 (default)	CVBS1 = AIN1	Composite
0001	CVBS2 = AIN2	Composite
0010	CVBS3 = AIN3	Composite
0011	CVBS4 = AIN4	Composite
0100	CVBS5 = AIN5	Composite
0101	CVBS6 = AIN6	Composite
0110	Y1 = AIN1	Y/C
	C1 = AIN4	Y/C
0111	Y2 = AIN2	Y/C
	C2 = AIN5	Y/C
1000	Y3 = AIN3	Y/C
	C3 = AIN6	Y/C
1001	Y1 = AIN1	YPrPb
	PB1 = AIN4	YPrPb
	PR1 = AIN5	YPrPb
1010	Y2 = AIN2	YPrPb
	PB2 = AIN3	YPrPb
	PR2 = AIN6	YPrPb
1011	CVBS7 = AIN7	Composite
1100	CVBS8 = AIN8	Composite
1101	CVBS9 = AIN9	Composite
1110	CVBS10 = AIN10	Composite
1111	CVBS11 = AIN11	Composite

Table 9. Input Channel Assignments

Input Channel	Pin No.	ADI Recommended Input Muxing Control INSEL[3:0]		
AIN7	41	CVBS7		
AIN1	42	CVBS1	Y/C1-Y	YPrPb1-Y
AIN8	43	CVBS8		
AIN2	44	CVBS2	Y/C2-Y	YPrPb2-Y
AIN9	45	CVBS9		
AIN3	46	CVBS3	Y/C3-Y	YPrPb2-Pb
AIN10	57	CVBS10		
AIN4	58	CVBS4	Y/C1-C	YPrPb1-Pb
AIN11	59	CVBS11		
AIN5	60	CVBS5	Y/C2-C	YPrPb1-Pr
AIN12	61	Not available		
AIN6	62	CVBS6	Y/C3-C	YPrPb2-Pr

ADI recommended input muxing is designed to minimize crosstalk between signal channels and to obtain the highest level of signal integrity. Table 9 summarizes how the PCB layout should connect analog video signals to the ADV7183B.

It is strongly recommended to connect any unused analog input pins to AGND to act as a shield.

Inputs AIN7 to AIN11 should be connected to AGND when only six input channels are used. This improves the quality of the sampling due to better isolation between the channels.

AIN12 is not under the control of INSEL[3:0]. It can be routed to ADC0/ADC1/ADC2 only by manual muxing. See Table 10 for details.

MANUAL INPUT MUXING

By accessing a set of manual override muxing registers, the analog input muxes of the ADV7183B can be controlled directly. This is referred to as manual input muxing.

Manual input muxing overrides other input muxing control bits, such as INSEL.

The manual muxing is activated by setting the ADC_SW_MAN_EN bit. It affects only the analog switches in front of the ADCs. This means if the settings of INSEL and the manual input muxing registers (ADC0/ADC1/ADC2_sw) contradict each other, the ADC0/ADC1/ADC2_sw settings apply, and INSEL is ignored.

Manual input muxing controls only the analog input muxes. INSEL[3:0] still has to be set so the follow-on blocks process the video data in the correct format. This means INSEL must still be used to tell the ADV7183B whether the input signal is of component, Y/C, or CVBS format.

Restrictions in the channel routing are imposed by the analog signal routing inside the IC; every input pin cannot be routed to each ADC. Refer to Figure 6 for an overview on the routing capabilities inside the chip. The three mux sections can be controlled by the reserved control signal buses ADC0/ADC1/ADC2_sw[3:0]. Table 10 explains the control words used.

SETADC_sw_man_en, Manual Input Muxing Enable, Address 0xC4[7]

ADC0_sw[3:0], ADC0 mux configuration, Address 0xC3[3:0]
ADC1_sw[3:0], ADC1 mux configuration, Address 0xC3[7:4]
ADC2_sw[3:0], ADC2 mux configuration, Address 0xC4[3:0]

Table 10. Manual Mux Settings for All ADCs (SETADC_sw_man_en = 1)

ADC0_sw[3:0]	ADC0 Connected to	ADC1_sw[3:0]	ADC1 Connected to	ADC2_sw[3:0]	ADC2 Connected to
0000	No connection	0000	No connection	0000	No connection
0001	AIN1	0001	No connection	0001	No connection
0010	AIN2	0010	No connection	0010	AIN2
0011	AIN3	0011	AIN3	0011	No connection
0100	AIN4	0100	AIN4	0100	No connection
0101	AIN5	0101	AIN5	0101	AIN5
0110	AIN6	0110	AIN6	0110	AIN6
0111	No connection	0111	No connection	0111	No connection
1000	No connection	1000	No connection	1000	No connection
1001	AIN7	1001	No connection	1001	No connection
1010	AIN8	1010	No connection	1010	AIN8
1011	AIN9	1011	AIN9	1011	No connection
1100	AIN10	1100	AIN10	1100	No connection
1101	AIN11	1101	AIN11	1101	AIN11
1110	AIN12	1110	AIN12	1110	AIN12
1111	No connection	1111	No connection	1111	No connection

GLOBAL CONTROL REGISTERS

Register control bits listed in this section affect the whole chip.

POWER-SAVE MODES

Power-Down

PDBP, Address 0x0F[2]

The digital core of the ADV7183B can be shut down by using the $\overline{\text{PWRDN}}$ pin and the PWRDN bit (see below). The PDBP controls which of the two pins has the higher priority. The default is to give priority to the $\overline{\text{PWRDN}}$ pin. This allows the user to have the ADV7183B powered down by default.

When PDBD is 0 (default), the digital core power is controlled by the $\overline{\text{PWRDN}}$ pin (the bit is disregarded).

When PDBD is 1, the bit has priority (the pin is disregarded).

PWRDN, Address 0x0F[5]

Setting the PWRDN bit switches the ADV7183B into a chip-wide power-down mode. The power-down stops the clock from entering the digital section of the chip, thereby freezing its operation. No I^2C bits are lost during power-down. The PWRDN bit also affects the analog blocks and switches them into low current modes. The I^2C interface is unaffected and remains operational in power-down mode.

The ADV7183B leaves the power-down state if the PWRDN bit is set to 0 (via I^2C), or if the overall part is reset using the $\overline{\text{RESET}}$ pin.

PDBP must be set to 1 for the PWRDN bit to power down the ADV7183B.

When PWRDN is 0 (default), the chip is operational.

When PWRDN is 1, the ADV7183B is in chip-wide power-down.

ADC Power-Down Control

The ADV7183B contains three 10-bit ADCs (ADC 0, ADC 1, and ADC 2). If required, each ADC can be powered down individually.

The ADCs should be powered down when in:

- CVBS mode. ADC 1 and ADC 2 should be powered down to save on power consumption.
- S-Video mode. ADC 2 should be powered down to save on power consumption.

PWRDN_ADC_0, Address 0x3A[3]

When PWRDN_ADC_0 is 0 (default), the ADC is in normal operation.

When PWRDN_ADC_0 is 1, ADC 0 is powered down.

PWRDN_ADC_1, Address 0x3A[2]

When PWRDN_ADC_1 is 0 (default), the ADC is in normal operation.

When PWRDN_ADC_1 is 1, ADC 1 is powered down.

PWRDN_ADC_2, Address 0x3A[1]

When PWRDN_ADC_2 is 0 (default), the ADC is in normal operation.

When PWRDN_ADC_2 is 1, ADC 2 is powered down.

RESET CONTROL

Chip Reset (RES), Address 0x0F[7]

Setting this bit, equivalent to controlling the $\overline{\text{RESET}}$ pin on the ADV7183B, issues a full chip reset. All I^2C registers are reset to their default values. (Some register bits do not have a reset value specified. They keep their last written value. Those bits are marked as having a reset value of x in the register table.) After the reset sequence, the part immediately starts to acquire the incoming video signal.

After setting the RES bit (or initiating a reset via the pin), the part returns to the default mode of operation with respect to its primary mode of operation. All I^2C bits are loaded with their default values, making this bit self-clearing.

Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5 ms before any further I^2C writes are performed.

The I^2C master controller receives a no acknowledge condition on the ninth clock cycle when chip reset is implemented. See the MPU Port Description section.

When RES is 0 (default), operation is normal.

When RES is 1, the reset sequence starts.

GLOBAL PIN CONTROL

Three-State Output Drivers

TOD, Address 0x03[6]

This bit allows the user to three-state the output drivers of the ADV7183B.

Upon setting the TOD bit, the P15 to P0, HS, VS, FIELD, and SFL pins are three-stated.

The timing pins (HS/VS/FIELD) can be forced active via the TIM_OE bit. For more information on three-state control, refer to the Three-State LLC Driver and the Timing Signals Output Enable sections.

Individual drive strength controls are provided via the DR_STR_XX bits.

The ADV7183B supports three-stating via a dedicated pin. When set high, the $\overline{OE}$ pin three-states the output drivers for the P15 to P0, HS, VS, FIELD, and SFL pins. The output drivers are three-stated if the TOD bit or the $\overline{OE}$ pin is set high.

When TOD is 0 (default), the output drivers are enabled.

When TOD is 1, the output drivers are three-stated.

Three-State LLC Driver

TRI_LLC, Address 0x1D[7]

This bit allows the output drivers for the LLC1 and LLC2 pins of the ADV7183B to be three-stated. For more information on three-state control, refer to the Three-State Output Drivers and the Timing Signals Output Enable sections.

Individual drive strength controls are provided via the DR_STR_XX bits.

When TRI_LLC is 0 (default), the LLC pin drivers work according to the DR_STR_C[1:0] setting (pin enabled).

When TRI_LLC is 1, the LLC pin drivers are three-stated.

Timing Signals Output Enable

TIM_OE, Address 0x04[3]

The TIM_OE bit should be regarded as an addition to the TOD bit. Setting it high forces the output drivers for HS, VS, and FIELD pins into the active (driving) state even if the TOD bit is set. If set to low, the HS, VS, and FIELD pins are three-stated, dependent on the TOD bit. This functionality is useful if the decoder is used as a timing generator only. This can happen when only the timing signals are to be extracted from an incoming signal, or if the part is in free-run mode where a separate chip can output, for an example, a company logo.

For more information on three-state control, refer to the Three-State Output Drivers and the Three-State LLC Driver sections.

Individual drive strength controls are provided via the DR_STR_XX bits.

When TIM_OE is 0 (default), the HS, VS, and FIELD pins are three-stated according to the TOD bit.

When TIM_OE is 1, HS, VS, and FIELD are forced active all the time.

Drive Strength Selection (Data)

DR_STR[1:0] Address 0xF4[5:4]

For EMC and crosstalk reasons, it can be desirable to strengthen or weaken the drive strength of the output drivers. The DR_STR[1:0] bits affect the P[15:0] output drivers.

For more information on three-state control, refer to the Drive Strength Selection (Clock) and the Drive Strength Selection (Sync) sections.

Table 11. DR_STR Function

DR_STR[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Drive Strength Selection (Clock)

DR_STR_C[1:0] Address 0xF4[3:2]

The DR_STR_C[1:0] bits can be used to select the strength of the clock signal output driver (LLC pin). For more information, refer to the Drive Strength Selection (Sync) and the Drive Strength Selection (Data) sections.

Table 12. DR_STR_C Function

DR_STR_C[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Drive Strength Selection (Sync)

DR_STR_S[1:0] Address 0xF4[1:0]

The DR_STR_S[1:0] bits allow the user to select the strength of the synchronization signals with which HS, VS, and F are driven. For more information, refer to the Drive Strength Selection (Clock) and the Drive Strength Selection (Data) sections.

Table 13. DR_STR_S Function

DR_STR_S[1:0]	Description
00	Low drive strength (1×)
01 (default)	Medium low drive strength (2×)
10	Medium high drive strength (3×)
11	High drive strength (4×)

Enable Subcarrier Frequency Lock Pin

EN_SFL_PIN Address 0x04[1]

The EN_SFL_PIN bit enables the output of subcarrier lock information (also known as GenLock) from the ADV7183B to an encoder in a decoder-encoder back-to-back arrangement.

When EN_SFL_PIN is 0 (default), the subcarrier frequency lock output is disabled.

When EN_SFL_PIN is 1, the subcarrier frequency lock information is presented on the SFL pin.

Polarity LLC Pin

PCLK Address 0x37[0]

The polarity of the clock that leaves the ADV7183B via the LLC1 and LLC2 pins can be inverted using the PCLK bit.

Changing the polarity of the LLC clock output can be necessary to meet the setup-and-hold time expectations of follow-on chips.

This bit also inverts the polarity of the LLC2 clock.

When PCLK is 0, the LLC output polarity is inverted.

When PCLK is 1 (default), the LLC output polarity is normal (as per the timing diagrams).

GLOBAL STATUS REGISTERS

Four registers provide summary information about the video decoder. The IDENT register allows the user to identify the revision code of the ADV7183B. The three other registers contain status bits regarding IC operation.

IDENTIFICATION

IDENT[7:0] Address 0x11[7:0]

This register provides identification of the revision of the ADV7183B.

An identification value of 0x11 indicates the ADV7183, released silicon.

An identification value of 0x13 indicates the ADV7183B silicon.

STATUS 1

STATUS_1[7:0] Address 0x10[7:0]

This read-only register provides information about the internal status of the ADV7183B.

See VS_Coast[1:0] Address 0xF9[3:2], CIL[2:0] Count Into Lock, Address 0x51[2:0], and COL[2:0] Count Out-of-Lock, Address 0x51[5:3] for information on the timing.

Depending on the setting of the FSCLE bit, the Status[0] and Status[1] bits are based solely on horizontal timing information on the horizontal timing and lock status of the color subcarrier. See the FSCLE FSC Lock Enable, Address 0x51[7] section.

AUTODETECTION RESULT

AD_RESULT[2:0] Address 0x10[6:4]

The AD_RESULT[2:0] bits report back on the findings from the autodetection block. For more information on enabling the autodetection block, see the General Setup section. For information on configuring it, see the Autodetection of SD Modes section.

Table 14. AD_RESULT Function

AD_RESULT[2:0]	Description
000	NTSM-MJ
001	NTSC-443
010	PAL-M
011	PAL-60
100	PAL-BGHID
101	SECAM
110	PAL-Combination N
111	SECAM 525

Table 15. STATUS 1 Function

STATUS 1[7:0]	Bit Name	Description
0	IN_LOCK	In lock (right now)
1	LOST_LOCK	Lost lock (since last read of this register)
2	FSC_LOCK	F_{SC} locked (right now)
3	FOLLOW_PW	AGC follows peak white algorithm
4	AD_RESULT.0	Result of autodetection
5	AD_RESULT.1	Result of autodetection
6	AD_RESULT.2	Result of autodetection
7	COL_KILL	Color kill active

STATUS 2

STATUS_2[7:0], Address 0x12[7:0]

Table 16. STATUS 2 Function

STATUS 2[7:0]	Bit Name	Description
0	MVCS DET	Detected Macrovision color striping
1	MVCS T3	Macrovision color striping protection. Conforms to Type 3 if high and to Type 2 if low
2	MV_PS DET	Detected Macrovision pseudo sync pulses
3	MV_AGC DET	Detected Macrovision AGC pulses
4	LL_NSTD	Line length is nonstandard
5	FSC_NSTD	F_{SC} frequency is nonstandard
6	Reserved	
7	Reserved	

STATUS 3

STATUS_3[7:0], Address 0x13[7:0]

Table 17. STATUS 3 Function

STATUS 3[7:0]	Bit Name	Description
0	INST_HLOCK	Horizontal lock indicator (instantaneous).
1	GEMD	Gemstar detect.
2	SD_OP_50HZ	Flags whether 50 Hz or 60 Hz are present at output.
3		Reserved for future use.
4	FREE_RUN_ACT	Outputs a blue screen (see the DEF_VAL_AUTO_EN Default Value Automatic Enable, Address 0x0C[1] section).
5	STD_FLD_LEN	Field length is correct for currently selected video standard.
6	INTERLACED	Interlaced video detected (field sequence found).
7	PAL_SW_LOCK	Reliable sequence of swinging bursts detected.

STANDARD DEFINITION PROCESSOR (SDP)

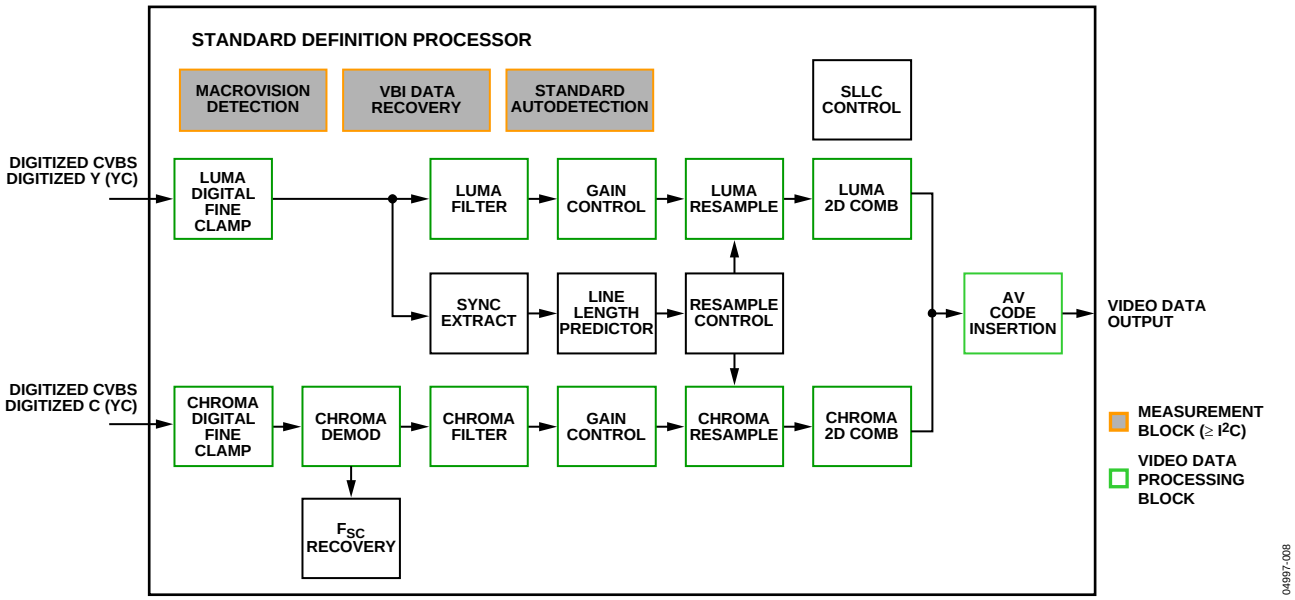


Figure 8. Block Diagram of the Standard Definition Processor

A block diagram of the ADV7183B's standard definition processor (SDP) is shown in Figure 8.

The SDP block can handle standard definition video in CVBS, Y/C, and YPrPb formats. It can be divided into a luminance and a chrominance path. If the input video is of a composite type (CVBS), both processing paths are fed with the CVBS input.

SD LUMA PATH

The input signal is processed by the following blocks:

- Digital Fine Clamp. This block uses a high precision algorithm to clamp the video signal.
- Luma Filter Block. This block contains a luma decimation filter (YAA) with a fixed response and some shaping filters (YSH) that have selectable responses.
- Luma Gain Control. The automatic gain control (AGC) can operate on a variety of different modes, including gain based on the depth of the horizontal sync pulse, peak white mode, and fixed manual gain.
- Luma Resample. To correct for line-length errors as well as dynamic line-length changes, the data is digitally resampled.
- Luma 2D Comb. The two-dimensional comb filter provides Y/C separation.
- AV Code Insertion. At this point, the decoded luma (Y) signal is merged with the retrieved chroma values. AV codes (as per ITU-R. BT-656) can be inserted.

SD CHROMA PATH

The input signal is processed by the following blocks:

- Digital Fine Clamp. This block uses a high precision algorithm to clamp the video signal.
- Chroma Demodulation. This block uses a color subcarrier (F_{SC}) recovery unit to regenerate the color subcarrier for any modulated chroma scheme. The demodulation block then performs an AM demodulation for PAL and NTSC, and an FM demodulation for SECAM.
- Chroma Filter Block. This block contains a chroma decimation filter (CAA) with a fixed response and some shaping filters (CSH) that have selectable responses.
- Gain Control. Automatic gain control (AGC) can operate on several different modes, including gain based on the color subcarrier's amplitude, gain based on the depth of the horizontal sync pulse on the luma channel, or fixed manual gain.
- Chroma Resample. The chroma data is digitally resampled to keep it perfectly aligned with the luma data. The resampling is done to correct for static and dynamic line-length errors of the incoming video signal.
- Chroma 2D Comb. The two-dimensional, 5-line, superadaptive comb filter provides high quality Y/C separation when the input signal is CVBS.
- AV Code Insertion. At this point, the demodulated chroma (Cr and Cb) signal is merged with the retrieved luma values. AV codes (as per ITU-R. BT-656) can be inserted.

SYNC PROCESSING

The ADV7183B extracts syncs embedded in the video data stream. There is currently no support for external HS/VS inputs. The sync extraction has been optimized to support imperfect video sources such as VCRs with head switches. The actual algorithm used employs a coarse detection based on a threshold crossing followed by a more detailed detection using an adaptive interpolation algorithm. The raw sync information is sent to a line-length measurement and prediction block. The output of this is then used to drive the digital resampling section to ensure the ADV7183B outputs 720 active pixels per line.

The sync processing on the ADV7183B also includes the following specialized postprocessing blocks that filter and condition the raw sync information retrieved from the digitized analog video.

- Vsync Processor. This block provides extra filtering of the detected Vsyncs to give improved vertical lock.
- Hsync Processor. The Hsync processor is designed to filter incoming Hsyncs that are corrupted by noise, providing much improved performance for video signals with stable time base but poor SNR.

VBI DATA RECOVERY

The ADV7183B can retrieve the following information from the input video:

- Wide-screen signaling (WSS)
- Copy generation management system (CGMS)
- Closed caption (CC)
- Macrovision protection presence
- EDTV data
- Gemstar-compatible data slicing

The ADV7183B is also capable of automatically detecting the incoming video standard with respect to

- Color subcarrier frequency
- Field rate
- Line rate

The SPD can configure itself to support PAL-B/G/H/I/D, PAL-M/N, PAL-combination N, NTSC-M, NTSC-J, SECAM 50 Hz/60 Hz, NTSC4.43, and PAL60.

GENERAL SETUP

Video Standard Selection

The VID_SEL[3:0] bits allows the user to force the digital core into a specific video standard. Under normal circumstances, this should not be necessary. The VID_SEL[3:0] bits default to an autodetection mode that supports PAL, NTSC, SECAM, and variants thereof. The following section describes the autodetection system.

Autodetection of SD Modes

To guide the autodetection system, individual enable bits are provided for each of the supported video standards. Setting the relevant bit to 0 inhibits the standard from being detected automatically. Instead, the system picks the closest of the remaining enabled standards. The results of the autodetection can be read back via the status registers. See the Global Status Registers section for more information.

VID_SEL[3:0] Address 0x00[7:4]

Table 18. VID_SEL Function

VID_SEL	Description
0000 (default)	Autodetect (PAL BGHID) <–> NTSC J (no pedestal), SECAM
0001	Autodetect (PAL BGHID) <–> NTSC M (pedestal), SECAM
0010	Autodetect (PAL N) (pedestal) <–> NTSC J (no pedestal), SECAM
0011	Autodetect (PAL N) (pedestal) <–> NTSC M (pedestal), SECAM
0100	NTSC-J (1)
0101	NTSC-M (1)
0110	PAL60
0111	NTSC-.43 (1)
1000	PAL-B/G/H/I/D
1001	PAL-N (= PAL BGHID (with pedestal))
1010	PAL-M (without pedestal)
1011	PAL-M
1100	PAL-Combination N
1101	PAL COMBINATION N (with pedestal)
1110	SECAM
1111	SECAM (with pedestal)

AD_SEC525_EN Enable Autodetection of SECAM 525 Line Video, Address 0x07[7]

Setting AD_SEC525_EN to 0 (default) disables the autodetection of a 525-line system with a SECAM style, FM-modulated color component.

Setting AD_SEC525_EN to 1 enables the detection.

AD_SECAM_EN Enable Autodetection of SECAM, Address 0x07[6]

Setting AD_SECAM_EN to 0 disables the autodetection of SECAM.

Setting AD_SECAM_EN to 1 (default) enables the detection.

AD_N443_EN Enable Autodetection of NTSC 443, Address 0x07[5]

Setting AD_N443_EN to 0 disables the autodetection of NTSC style systems with a 4.43 MHz color subcarrier.

Setting AD_N443_EN to 1 (default) enables the detection.

AD_P60_EN Enable Autodetection of PAL60, Address 0x07[4]

Setting AD_P60_EN to 0 disables the autodetection of PAL systems with a 60 Hz field rate.

Setting AD_P60_EN to 1 (default) enables the detection.

AD_PALN_EN Enable Autodetection of PAL N, Address 0x07[3]

Setting AD_PALN_EN to 0 disables the detection of the PAL N standard.

Setting AD_PALN_EN to 1 (default) enables the detection.

AD_PALM_EN Enable Autodetection of PAL M, Address 0x07[2]

Setting AD_PALM_EN to 0 disables the autodetection of PAL M.

Setting AD_PALM_EN to 1 (default) enables the detection.

AD_NTSC_EN Enable Autodetection of NTSC, Address 0x07[1]

Setting AD_NTSC_EN to 0 disables the detection of standard NTSC.

Setting AD_NTSC_EN to 1 (default) enables the detection.

AD_PAL_EN Enable Autodetection of PAL, Address 0x07[0]

Setting AD_PAL_EN to 0 disables the detection of standard PAL.

Setting AD_PAL_EN to 1 (default) enables the detection.

SFL_INV Subcarrier Frequency Lock Inversion

This bit controls the behavior of the PAL switch bit in the SFL (GenLock Telegram) data stream. It was implemented to solve some compatibility issues with video encoders. It solves two problems.

First, the PAL switch bit is only meaningful in PAL. Some encoders (including ADI encoders) also look at the state of this bit in NTSC.

Second, there was a design change in ADI encoders from ADV717x to ADV719x. The older versions used the SFL (Genlock Telegram) bit directly, while the later ones invert the bit prior to using it. The reason for this is that the inversion compensated for the 1-line delay of an SFL (GenLock Telegram) transmission.

As a result, ADV717x encoders need the PAL switch bit in the SFL (Genlock Telegram) to be 1 for NTSC to work, and ADV7190/ADV7191/ADV7194 encoders need the PAL switch bit in the SFL to be 0 to work in NTSC. If the state of the PAL switch bit is wrong, a 180° phase shift occurs.

In a decoder/encoder back-to-back system in which SFL is used, this bit must be set up properly for the specific encoder used.

SFL_INV Address 0x41[6]

Setting SFL_INV to 0 makes the part SFL-compatible with ADV7190/ADV7191/ADV7194 encoders.

Setting SFL_INV to 1 (default), makes the part SFL-compatible with ADV717x/ADV7173x encoders.

Lock-Related Controls

Lock information is presented to the user through Bits[1:0] of the Status 1 register. See the STATUS_1[7:0] Address 0x10[7:0] section. Figure 9 outlines the signal flow and the controls available to influence the way the lock status information is generated.

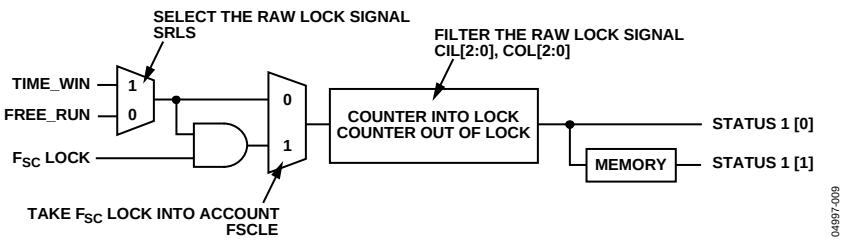


Figure 9. Lock-Related Signal Path

SRLS Select Raw Lock Signal, Address 0x51[6]

Using the SRLS bit, the user can choose between two sources for determining the lock status (per Bits[1:0] in the Status 1 register).

- The time_win signal is based on a line-to-line evaluation of the horizontal synchronization pulse of the incoming video. It reacts quite quickly.
- The free_run signal evaluates the properties of the incoming video over several fields and takes vertical synchronization information into account.

Setting SRLS to 0 (default) selects the free_run signal.

Setting SRLS to 1 selects the time_win signal.

FSCLE F_{SC} Lock Enable, Address 0x51[7]

The FSCLE bit allows the user to choose whether the status of the color subcarrier loop is taken into account when the overall lock status is determined and presented via Bits[1:0] in Status Register 1. This bit must be set to 0 when operating in YPrPb component mode to generate a reliable HLOCK status bit.

Setting FSCLE to 0 (default) makes the overall lock status dependent on only horizontal sync lock.

Setting FSCLE to 1 makes the overall lock status dependent on horizontal sync lock and F_{SC} lock.

VS_Coast[1:0] Address 0xF9[3:2]

These bits are used to set VS free-run (coast) frequency.

Table 19. VS_COAST[1:0] Function

VS_COAST[1:0]	Description
00 (default)	Auto coast mode—follows VS frequency from last video input
01	Forces 50 Hz coast mode
10	Forces 60 Hz coast mode
11	Reserved

CIL[2:0] Count Into Lock, Address 0x51[2:0]

CIL[2:0] determines the number of consecutive lines for which the lock condition must be true before the system switches into the locked state, and reports this via Status 0[1:0]. It counts the value in lines of video.

Table 20. CIL Function

CIL[2:0]	Description
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100000

COL[2:0] Count Out-of-Lock, Address 0x51[5:3]

COL[2:0] determines the number of consecutive lines for which the out-of-lock condition must be true before the system switches into unlocked state, and reports this via Status 0[1:0]. It counts the value in lines of video.

Table 21. COL Function

COL[2:0]	Description
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100000

COLOR CONTROLS

These registers allow the user to control the picture appearance, including control of the active data in the event of video being lost. These controls are independent of any other controls. For instance, brightness control is independent from picture clamping, although both controls affect the signal's dc level.

CON[7:0] Contrast Adjust, Address 0x08[7:0]

This allows the user to adjust the contrast of the picture.

Table 22. CON Function

CON[7:0]	Description
0x80 (default)	Gain on luma channel = 1
0x00	Gain on luma channel = 0
0xFF	Gain on luma channel = 2

SD_SAT_Cb[7:0] SD Saturation Cb Channel, Address 0xE3[7:0]

This register allows the user to control the gain of the Cb channel only. The user can adjust the saturation of the picture.

Table 23. SD_SAT_Cb Function

SD_SAT_Cb[7:0]	Description
0x80 (default)	Gain on Cb channel = 0 dB
0x00	Gain on Cb channel = −42 dB
0xFF	Gain on Cb channel = +6 dB

SD_SAT_Cr[7:0] SD Saturation Cr Channel, Address 0xE4[7:0]

This register allows the user to control the gain of the Cr channel only. The user can adjust the saturation of the picture.

Table 24. SD_SAT_Cr Function

SD_SAT_Cr[7:0]	Description
0x80 (default)	Gain on Cr channel = 0 dB
0x00	Gain on Cb channel = −42 dB
0xFF	Gain on Cb channel = +6 dB

SD_OFF_Cb[7:0] SD Offset Cb Channel, Address 0xE1[7:0]

This register allows the user to select an offset for data on the Cb channel only and adjust the hue of the picture. There is a functional overlap with the Hue[7:0] register.

Table 25.SD_OFF_Cb Function

SD_OFF_Cb[7:0]	Description
0x80 (default)	0 offset applied to the Cb channel
0x00	−312 mV offset applied to the Cb channel
0xFF	+312 mV offset applied to the Cb channel

SD_OFF_Cr[7:0] SD Offset Cr Channel, Address 0xE2[7:0]

This register allows the user to select an offset for data on the Cr channel only and adjust the hue of the picture. There is a functional overlap with the Hue[7:0] register.

Table 26. SD_OFF_Cr Function

SD_OFF_Cr[7:0]	Description
0x80 (default)	0 offset applied to the Cr channel
0x00	−312 mV offset applied to the Cr channel
0xFF	+312 mV offset applied to the Cr channel

BRI[7:0] Brightness Adjust, Address 0x0A[7:0]

This register controls the brightness of the video signal. It allows the user to adjust the brightness of the picture.

Table 27. BRI Function

BRI[7:0]	Description
0x00 (default)	Offset of the luma channel = 0IRE
0x7F	Offset of the luma channel = +100IRE
0xFF	Offset of the luma channel = −100IRE

HUE[7:0] Hue Adjust, Address 0x0B[7:0]

This register contains the value for the color hue adjustment. It allows the user to adjust the hue of the picture.

HUE[7:0] has a range of ±90°, with 0x00 equivalent to an adjustment of 0°. The resolution of HUE[7:0] is 1 bit = 0.7°.

The hue adjustment value is fed into the AM color demodulation block. Therefore, it applies only to video signals that contain chroma information in the form of an AM modulated carrier (CVBS or Y/C in PAL or NTSC). It does not affect SECAM and does not work on component video inputs (YPrPb).

Table 28. HUE Function

HUE[7:0]	Description
0x00 (default)	Phase of the chroma signal = 0°
0x7F	Phase of the chroma signal = −90°
0x80	Phase of the chroma signal = +90°

DEF_Y[5:0] Default Value Y, Address 0x0C[7:2]

If the ADV7183B loses lock on the incoming video signal or if there is no input signal, the DEF_Y[5:0] bits allow the user to specify a default luma value to be output. This value is used if

- The DEF_VAL_AUTO_EN bit is set to high and the ADV7183B lost lock to the input video signal. This is the intended mode of operation (automatic mode).
- The DEF_VAL_EN bit is set, regardless of the lock status of the video decoder. This is a forced mode that may be useful during configuration.

The DEF_Y[5:0] values define the 6 MSBs of the output video. The remaining LSBs are padded with 0s. For example, in 8-bit mode, the output is Y[7:0] = {DEF_Y[5:0], 0, 0}.

DEF_Y[5:0] is 0x0D (blue) is the default value for Y.

Register 0x0C has a default value of 0x36.

DEF_C[7:0] Default Value C, Address 0x0D[7:0]

The DEF_C[7:0] register complements the DEF_Y[5:0] value. It defines the 4 MSBs of Cr and Cb values to be output if

- The DEF_VAL_AUTO_EN bit is set to high and the ADV7183B cannot lock to the input video (automatic mode).
- The DEF_VAL_EN bit is set to high (forced output).

The data that is finally output from the ADV7183B for the chroma side is Cr[7:0] = {DEF_C[7:4], 0, 0, 0, 0}, Cb[7:0] = {DEF_C[3:0], 0, 0, 0, 0}.

DEF_C[7:0] is 0x7C (blue) is the default value for Cr and Cb.

DEF_VAL_EN Default Value Enable, Address 0x0C[0]

This bit forces the use of the default values for Y, Cr, and Cb. Refer to the descriptions for DEF_Y and DEF_C for additional information. In this mode, the decoder also outputs a stable 27 MHz clock, HS, and VS.

Setting DEF_VAL_EN to 0 (default) outputs a colored screen determined by user-programmable Y, Cr, and Cb values when the decoder free-runs. Free-run mode is turned on and off by the DEF_VAL_AUTO_EN bit.

Setting DEF_VAL_EN to 1 forces a colored screen output determined by user-programmable Y, Cr, and Cb values. This overrides picture data even if the decoder is locked.

DEF_VAL_AUTO_EN Default Value Automatic Enable, Address 0x0C[1]

This bit enables the automatic usage of the default values for Y, Cr, and Cb when the ADV7183B cannot lock to the video signal.

Setting DEF_VAL_AUTO_EN to 0 disables free-run mode. If the decoder is unlocked, it outputs noise.

Setting DEF_VAL_EN to 1 (default) enables free-run mode. A colored screen set by the user-programmable Y, Cr, and Cb values is displayed when the decoder loses lock.

CLAMP OPERATION

The input video is ac-coupled into the ADV7183B through a 0.1 µF capacitor. The recommended range of the input video signal is 0.5 V to 1.6 V (typically 1 V p-p). If the signal exceeds this range, it cannot be processed correctly in the decoder. Since the input signal is ac-coupled into the decoder, its dc value needs to be restored. This process is referred to as clamping the video. This section explains the general process of clamping on the ADV7183B and shows the different ways in which a user can configure its behavior.

The ADV7183B uses a combination of current sources and a digital processing block for clamping, as shown in Figure 10. The analog processing channel shown is replicated three times inside the IC. While only one single channel (and only one ADC) is needed for a CVBS signal, two independent channels are needed for Y/C (S-VHS) type signals, and three independent channels are needed to allow component signals (YPrPb) to be processed.

The clamping can be divided into two sections:

- Clamping before the ADC (analog domain): current sources
- Clamping after the ADC (digital domain): digital processing block

The ADCs can digitize an input signal only if it resides within the ADC's 1.6 V input voltage range. An input signal with a dc level that is too large or too small is clipped at the top or bottom of the ADC range.

The primary task of the analog clamping circuits is to ensure the video signal stays within the valid ADC input window so that the analog-to-digital conversion can take place. It is not necessary to clamp the input signal with a very high accuracy in the analog domain as long as the video signal fits the ADC range.

After digitization, the digital fine clamp block corrects for any remaining variations in dc level. Since the dc level of an input video signal refers directly to the brightness of the picture transmitted, it is important to perform a fine clamp with high accuracy; otherwise, brightness variations can occur. Furthermore, dynamic changes in the dc level almost certainly lead to visually objectionable artifacts and must therefore be prohibited.

The clamping scheme has to be able to acquire a newly connected video signal with a completely unknown dc level, and it must maintain the dc level during normal operation.

For quickly acquiring an unknown video signal, the large current clamps can be activated. (It is assumed that the amplitude of the video signal at this point is of a nominal value.) Control of the coarse and fine current clamp parameters is performed automatically by the decoder.

Standard definition video signals can have excessive noise on them. In particular, CVBS signals transmitted by terrestrial broadcast and demodulated using a tuner usually show very large levels of noise (>100 mV). A voltage clamp is unsuitable for this type of video signal. Instead, the ADV7183B uses a set of four current sources that can cause coarse (>0.5 mA) and fine (<0.1 mA) currents to flow into and away from the high impedance node that carries the video signal (see Figure 10).

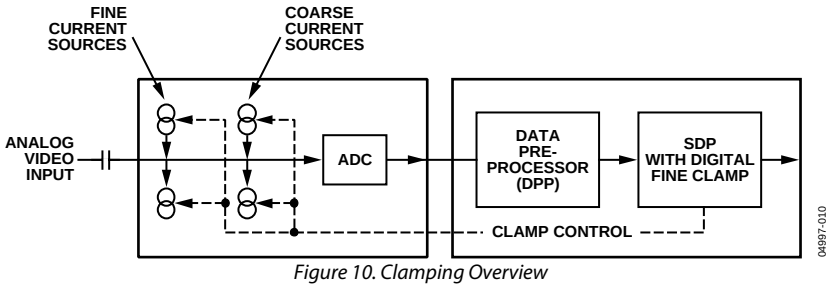


Figure 10. Clamping Overview

The following sections describe the I²C signals that can be used to influence the behavior of the clamps on the ADV7183B.

Previous revisions of the ADV7183B had controls (FACL/FICL, fast and fine clamp length) to allow configuration of the length for which the coarse (fast) and fine current sources are switched on. These controls were removed on the ADV7183B-FT and replaced by an adaptive scheme.

CCLEN Current Clamp Enable, Address 0x14[4]

The current clamp enable bit allows the user to switch off the current sources in the analog front end altogether. This can be useful if the incoming analog video signal is clamped externally.

When CCLEN is 0, the current sources are switched off.

When CCLEN is 1 (default), the current sources are enabled.

DCT[1:0] Digital Clamp Timing, Address 0x15[6:5]

The clamp timing register determines the time constant of the digital fine clamp circuitry. It is important to realize that the digital fine clamp reacts very quickly because it is supposed to immediately correct any residual dc level error for the active line. The time constant of the digital fine clamp must be much faster than the one from the analog blocks.

By default, the time constant of the digital fine clamp is adjusted dynamically to suit the currently connected input signal.

Table 29. DCT Function

DCT[1:0]	Description
00	Slow (TC = 1 sec)
01	Medium (TC = 0.5 sec)
10 (default)	Fast (TC = 0.1 sec)
11	Determined by the ADV7183B, depending on the I/P video parameters

DCFE Digital Clamp Freeze Enable, Address 0x15[4]

This register bit allows the user to freeze the digital clamp loop at any time. It is intended for users who would like to do their own clamping. Users should disable the current sources for analog clamping via the appropriate register bits, wait until the digital clamp loop settles, and then freeze it via the DCFE bit.

When DCFE is 0 (default), the digital clamp is operational.

When DCFE is 1, the digital clamp loop is frozen.

LUMA FILTER

Data from the digital fine clamp block is processed by three sets of filters. The data format at this point is CVBS for CVBS input or luma only for Y/C and YPrPb input formats.

- Luma Antialias Filter (YAA). The ADV7183B receives video at a rate of 27 MHz. (For 4× oversampled video, the ADCs sample at 54 MHz, and the first decimation is performed inside the DPP filters. Therefore, the data rate into the SDP core is always 27 MHz.) The ITU-R BT.601 recommends a sampling frequency of 13.5 MHz. The luma antialias filter decimates the oversampled video using a high quality, linear phase, low-pass filter that preserves the luma signal while at the same time attenuating out-of-band components. The luma antialias filter has a fixed response.

- Luma Shaping Filters (YSH). The shaping filter block is a programmable low-pass filter with a wide variety of responses. It can be used to selectively reduce the luma video signal bandwidth (needed prior to scaling, for example). For some video sources that contain high frequency noise, reducing the bandwidth of the luma signal improves visual picture quality. A follow-on video compression stage can work more efficiently if the video is low-pass filtered.

  The ADV7183B has two responses for the shaping filter: one that is used for good quality CVBS, component, and S-VHS type sources, and a second for nonstandard CVBS signals.

  The YSH filter responses also include a set of notches for PAL and NTSC. However, using the comb filters for Y/C separation is recommended.

- Digital Resampling Filter. This block is used to allow dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is selected by the system, and user intervention is not required.

Figure 12 through Figure 15 show the overall response of all filters together. Unless otherwise noted, the filters are set into a typical wideband mode.

Y-Shaping Filter

For input signals in CVBS format, the luma shaping filters play an essential role in removing the chroma component from a composite signal. Y/C separation must aim for best possible crosstalk reduction while still retaining as much bandwidth (especially on the luma component) as possible. High quality Y/C separation can be achieved by using the internal comb filters of the ADV7183B. Comb filtering, however, relies on the frequency relationship of the luma component (multiples of the video line rate) and the color subcarrier (F_{SC}). For good quality CVBS signals, this relationship is known; the comb filter algorithms can be used to separate out luma and chroma with high accuracy.

For nonstandard video signals, the frequency relationship may be disturbed, and the comb filters may not be able to optimally remove all crosstalk artifacts without the assistance of the shaping filter block.

An automatic mode is provided. The ADV7183B evaluates the quality of the incoming video signal and selects the filter responses in accordance with the signal quality and video standard. YFSM, WYSFMOVR, and WYSFM allow the user to manually override the automatic decisions in part or in full.

The luma shaping filter has three control registers:

- YSFM[4:0] allows the user to manually select a shaping filter mode (applied to all video signals) or to enable an automatic selection (dependent on video quality and video standard).
- WYSFMOVR allows the user to manually override the WYSFM decision.
- WYSFM[4:0] allows the user to select a different shaping filter mode for good quality CVBS, component (YPrPb), and S-VHS (Y/C) input signals.

In automatic mode, the system preserves the maximum possible bandwidth for good CVBS sources, since they can successfully be combed, as well as for luma components of YPrPb and Y/C sources, since they need not be combed. For poor quality signals, the system selects from a set of proprietary shaping filter responses that complements comb filter operation to reduce visual artifacts.

The decisions of the control logic are shown in Figure 11.

YSFM[4:0] Y-Shaping Filter Mode, Address 0x17[4:0]

The Y shaping filter mode bits allow the user to select from a wide range of low-pass and notch filters. When switched in automatic mode, the filter is selected based on other register selections (for example, detected video standard) as well as properties extracted from the incoming video itself (for example, quality, time-base stability). The automatic selection always selects the widest possible bandwidth for the video input encountered.

If the YSFM settings specify a filter (where YSFM is set to values other than 00000 or 00001), the chosen filter is applied to all video, regardless of its quality.

In automatic selection mode, the notch filters are used only for bad quality video signals. For all other video signals, wideband filters are used.

WYSFMOVR Wideband Y-Shaping Filter Override, Address 0x18[7]

Setting the WYSFMOVR bit enables the use of the WYSFM[4:0] settings for good quality video signals. For more information, refer to the general discussion of the luma shaping filters in the Y-Shaping Filter section and the flowchart shown in Figure 11.

When WYSFMOVR is 0, the shaping filter for good quality video signals is selected automatically.

Setting WYSFMOVR to 1 enables manual override via WYSFM[4:0] (default).

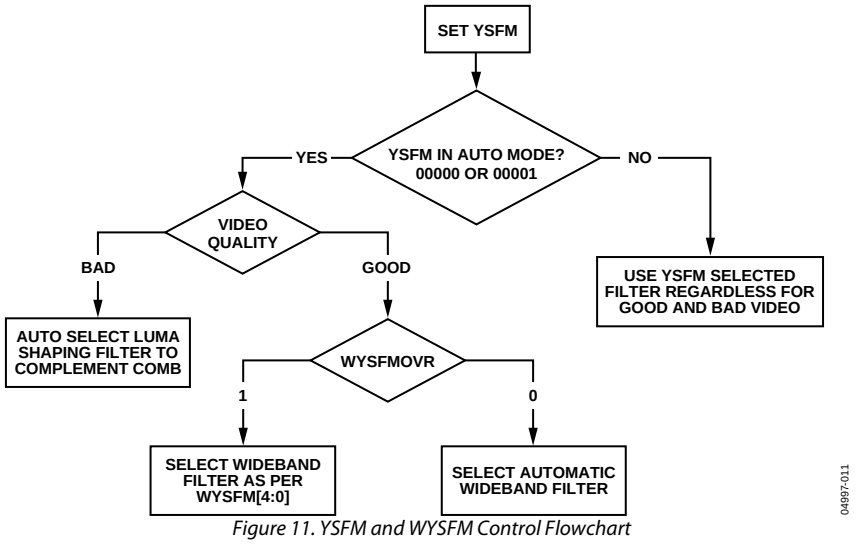


Figure 11. YSFM and WYSFM Control Flowchart

Table 30. YSFM Function

YSFM[4:0]	Description
0'0000	Automatic selection including a wide notch response (PAL/NTSC/SECAM)
0'0001 (default)	Automatic selection including a narrow notch response (PAL/NTSC/SECAM)
0'0010	SVHS 1
0'0011	SVHS 2
0'0100	SVHS 3
0'0101	SVHS 4
0'0110	SVHS 5
0'0111	SVHS 6
0'1000	SVHS 7
0'1001	SVHS 8
0'1010	SVHS 9
0'1011	SVHS 10
0'1100	SVHS 11
0'1101	SVHS 12
0'1110	SVHS 13
0'1111	SVHS 14
1'0000	SVHS 15
1'0001	SVHS 16
1'0010	SVHS 17
1'0011	SVHS 18 (CCIR 601)
1'0100	PAL NN 1
1'0101	PAL NN 2
1'0110	PAL NN 3
1'0111	PAL WN 1
1'1000	PAL WN 2
1'1001	NTSC NN 1
1'1010	NTSC NN 2
1'1011	NTSC NN 3
1'1100	NTSC WN 1
1'1101	NTSC WN 2
1'1110	NTSC WN 3
1'1111	Reserved

WYSFM[4:0] Wideband Y-Shaping Filter Mode, Address 0x18[4:0]

The WYSFM[4:0] bits allow the user to manually select a shaping filter for good quality video signals, for example, CVBS with time-base stability, luma component of YPrPb and luma component of Y/C. The WYSFM bits are active only if the WYSFMOVR bit is set to 1. See the general discussion of the shaping filter settings in the Y-Shaping Filter section.

Table 31. WYSFM Function

WYSFM[4:0]	Description
0'0000	Do not use
0'0001	Do not use
0'0010	SVHS 1
0'0011	SVHS 2
0'0100	SVHS 3
0'0101	SVHS 4
0'0110	SVHS 5
0'0111	SVHS 6
0'1000	SVHS 7
0'1001	SVHS 8
0'1010	SVHS 9
0'1011	SVHS 10
0'1100	SVHS 11
0'1101	SVHS 12
0'1110	SVHS 13
0'1111	SVHS 14
1'0000	SVHS 15
1'0001	SVHS 16
1'0010	SVHS 17
1'0011 (default)	SVHS 18 (CCIR 601)
1'0100 to 1'1111	Do not use

The filter plots in Figure 12 show the S-VHS 1 (narrowest) to S-VHS 18 (widest) shaping filter settings. Figure 14 shows the PAL notch filter responses. The NTSC-compatible notches are shown in Figure 15.

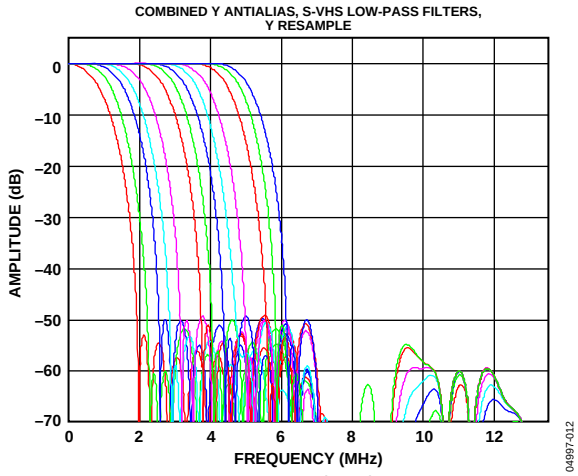


Figure 12. Y S-VHS Combined Responses

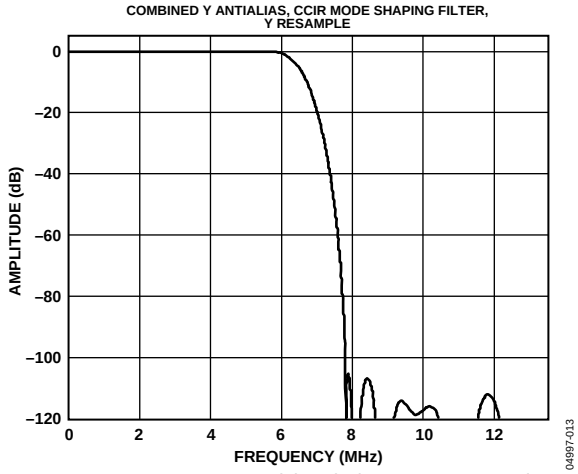


Figure 13. Y S-VHS 18 Extra Wideband Filter (CCIR 601 Compliant)

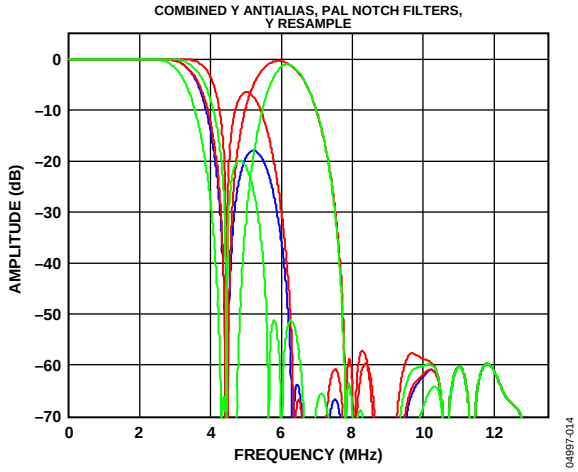


Figure 14. PAL Notch Filter Response

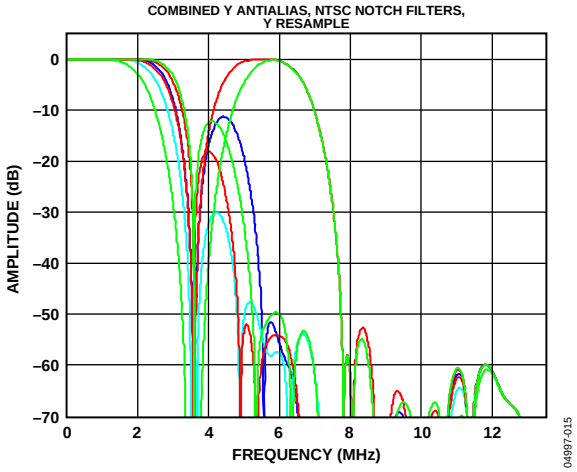


Figure 15. NTSC Notch Filter Response

CHROMA FILTER

Data from the digital fine clamp block is processed by three sets of filters. The data format at this point is CVBS for CVBS inputs, chroma only for Y/C, or U/V interleaved for YPrPb input formats.

- Chroma Antialias Filter (CAA). The ADV7183B oversamples the CVBS by a factor of 2 and the Chroma/PrPb by a factor of 4. A decimating filter (CAA) is used to preserve the active video band and to remove any out-of-band components. The CAA filter has a fixed response.
- Chroma Shaping Filters (CSH). The shaping filter block (CSH) can be programmed to perform a variety of low-pass responses. It can be used to selectively reduce the bandwidth of the chroma signal for scaling or compression.
- Digital Resampling Filter. This block is used to allow dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system without user intervention.

The plots in Figure 16 show the overall response of all filters together.

CSFM[2:0] C- Shaping Filter Mode, Address 0x17[7]

The C-shaping filter mode bits allow the user to select from a range of low-pass filters, SH1 to SH5 and wideband mode for the chrominance signal. The autoselection options automatically select from the filter options to give the specified response. (See settings 000 and 001 in Table 32).

Table 32. CSFM Function

CSFM[2:0]	Description
000 (default)	Autoselect 1.5 MHz bandwidth
001	Autoselect 2.17 MHz bandwidth
010	SH1
011	SH2
100	SH3
101	SH4
110	SH5
111	Wideband mode

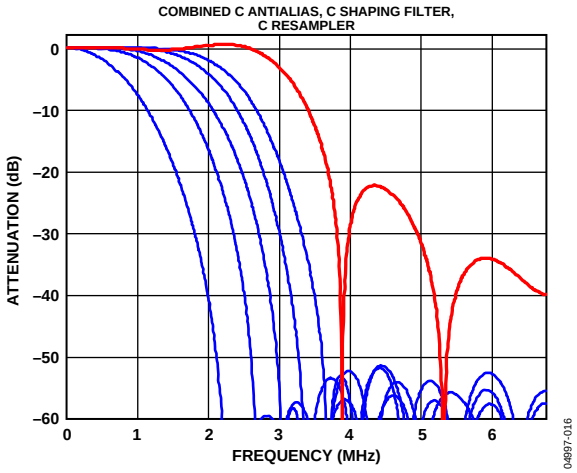


Figure 16. Chroma Shaping Filter Responses

Figure 16 shows the responses of SH1 (narrowest) to SH5 (widest) and the wide band mode (in red).

GAIN OPERATION

The gain control within the ADV7183B is performed strictly on a digital basis. The input ADCs support a 10-bit range, mapped into a 1.6 V analog voltage range. Gain correction occurs after the digitization in the form of a digital multiplier.

One advantage of this architecture over the commonly used programmable gain amplifier (PGA) before the ADCs is that the gain is now completely independent of supply, temperature, and process variations.

As shown in Figure 17, the ADV7183B can decode a video signal providing it fits into the ADC window. Two components to this are the amplitude of the input signal and the dc level on which it resides. The dc level is set by the clamping circuitry (see the Clamp Operation section).

If the amplitude of the analog video signal is too high, clipping can occur, resulting in visual artifacts. The analog input range of the ADC, together with the clamp level, determines the maximum supported amplitude of the video signal.

The minimum supported amplitude of the input video is determined by the ADV7183B's ability to retrieve horizontal and vertical timing and to lock to the color burst, if present.

There are two gain control units, one each for luma and chroma data. Both can operate independently of each other. The chroma unit, however, can also take its gain value from the luma path.

The possible AGC modes are summarized in Table 33.

It is possible to freeze the automatic gain control loops. This causes the loops to stop updating and the AGC determined gain, at the time of the freeze, to stay active. The ACG determined gain stays active until the automatic gain control loop is either unfrozen, or the gain mode of the operation is changed.

The currently active gain from any of the modes can be read back. Refer to the description of the dual function manual gain registers, LG[11:0] Luma Gain and CG[11:0] Chroma Gain, in the Luma Gain and Chroma Gain sections.

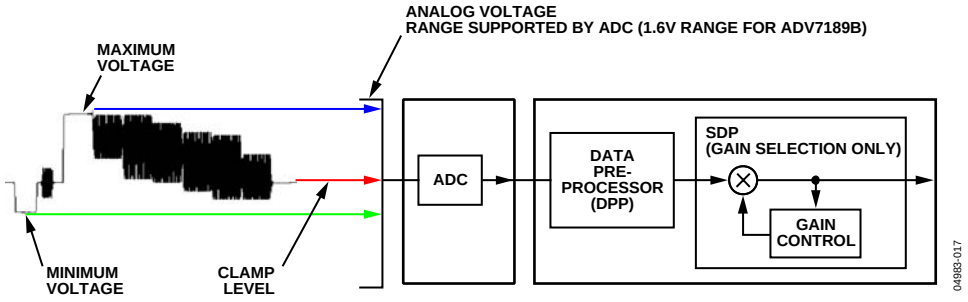


Figure 17. Gain Control Overview

Table 33. AGC Modes

Input Video Type	Luma Gain	Chroma Gain
Any	Manual gain luma	Manual gain chroma
CVBS	Dependent on horizontal sync depth	Dependent on color burst amplitude Taken from luma path
	Peak white	Dependent on color burst amplitude Taken from luma path
Y/C	Dependent on horizontal sync depth	Dependent on color burst amplitude Taken from luma path
	Peak white	Dependent on color burst amplitude Taken from luma path
YPrPb	Dependent on horizontal sync depth	Taken from luma path

Luma Gain

LAGC[2:0] Luma Automatic Gain Control, Address 0x2C[7:0]

The luma automatic gain control mode bits select the mode of operation for the gain control in the luma path.

ADI internal parameters are available to customize the peak white gain control. Contact ADI sales for more information.

Table 34. LAGC Function

LAGC[2:0]	Description
000	Manual fixed gain (use LMG[11:0])
001	AGC (blank level to sync tip); peak white algorithm off
010 (default)	AGC (blank level to sync tip); peak white algorithm on
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Freeze gain

LAGT[1:0] Luma Automatic Gain Timing, Address 0x2F[7:6]

The luma automatic gain timing register allows the user to influence the tracking speed of the luminance automatic gain control. Note that this register has an effect only if the LAGC[2:0] register is set to 001, 010, 011, or 100 (automatic gain control modes).

If peak white AGC is enabled and active (see the STATUS_1[7:0] Address 0x10[7:0] section), the actual gain update speed is dictated by the peak white AGC loop and, as a result, the LAGT settings have no effect. As soon as the part leaves peak white AGC, LAGT becomes relevant again.

The update speed for the peak white algorithm can be customized by the use of internal parameters. Contact ADI sales for more information.

Table 35. LAGT Function

LAGT[1:0]	Description
00	Slow (TC = 2 sec)
01	Medium (TC = 1 sec)
10	Fast (TC = 0.2 sec)
11 (default)	Adaptive

LG[11:0] Luma Gain, Address 0x2F[3:0]; Address 0x30[7:0]; LMG[11:0] Luma Manual Gain, Address 0x2F[3:0]; Address 0x30[7:0]

Luma gain[11:0] is a dual-function register. If written to, a desired manual luma gain can be programmed. This gain becomes active if the LAGC[2:0] mode is switched to manual fixed gain. Equation 1 shows how to calculate a desired gain.

If read back, this register returns the current gain value. Depending on the setting in the LAGC[2:0] bits, one of these gain values is returned

- Luma manual gain value (LAGC[2:0] set to luma manual gain mode)
- Luma automatic gain value (LAGC[2:0] set to any of the automatic modes)

Table 36. LG/LMG Function

LG[11:0]/LMG[11:0]	Read/Write	Description
LMG[11:0] = X	Write	Manual gain for luma path
LG[11:0]	Read	Actually used gain

$$Luma_Gain = \frac{(0 < LG \leq 4095)}{2048} = 0...2 \quad (1)$$

For example, program the ADV7183B into manual fixed gain mode with a desired gain of 0.89.

1. Use Equation 1 to convert the gain:
   0.89 × 2048 = 1822.72
2. Truncate to integer value:
   1822.72 = 1822
3. Convert to hexadecimal:
   1822d = 0x71E
4. Split into two registers and program:
   Luma Gain Control 1[3:0] = 0x7
   Luma Gain Control 2[7:0] = 0x1E
5. Enable manual fixed gain mode:
   Set LAGC[2:0] to 000

BETACAM Enable Betacam Levels, Address 0x01[5]

If YPrPb data is routed through the ADV7183B, the automatic gain control modes can target different video input levels, as outlined in Figure 40. The BETACAM bit is valid only if the input mode is YPrPb (component). The BETACAM bit sets the target value for AGC operation.

A review of the following sections is useful:

- INSEL[3:0] Input Selection, Address 0x00[3:0] to find how component video (YPrPb) can be routed through the ADV7183B.
- Video Standard Selection to select the various standards, such as those with and without pedestal.

The automatic gain control (AGC) algorithms adjust the levels based on the setting of the BETACAM bit (see Table 37).

Table 37. BETACAM Function

BETACAM	Description
0 (default)	Assuming YPrPb is selected as input format Selecting PAL with pedestal selects MII Selecting PAL without pedestal selects SMPTE Selecting NTSC with pedestal selects MII Selecting NTSC without pedestal selects SMPTE
1	Assuming YPrPb is selected as input format Selecting PAL with pedestal selects BETACAM Selecting PAL without pedestal selects BETACAM variant Selecting NTSC with pedestal selects BETACAM Selecting NTSC without pedestal selects BETACAM variant

PW_UPD Peak White Update, Address 0x2B[0]

The peak white and average video algorithms determine the gain based on measurements taken from the active video. The PW_UPD bit determines the rate of gain change. The LAGC[2:0] must be set to the appropriate mode to enable the peak white or average video mode in the first place. For more information, refer to the LAGC[2:0] Luma Automatic Gain Control,
Address 0x2C[7:0] section.

Setting PW_UPD to 0 updates the gain once per video line.

Setting PW_UPD to 1 (default) updates the gain once per field.

Chroma Gain

CAGC[1:0] Chroma Automatic Gain Control, Address 0x2C[1:0]

The two bits of the Color Automatic Gain Control mode select the basic mode of operation for automatic gain control in the chroma path.

Table 38. CAGC Function

CAGC[1:0]	Description
00	Manual fixed gain (use CMG[11:0])
01	Use luma gain for chroma
10 (default)	Automatic gain (based on color burst)
11	Freeze chroma gain

CAGT[1:0] Chroma Automatic Gain Timing, Address 0x2D[7:6]

The chroma automatic gain timing register allows the user to influence the tracking speed of the chroma automatic gain control. This register has an effect only if the CAGC[1:0] register is set to 10 (automatic gain).

Table 39. CAGT Function

CAGT[1:0]	Description
00	Slow (TC = 2 sec)
01	Medium (TC = 1 sec)
10	Fast (TC = 0.2 sec)
11 (default)	Adaptive

Table 40. Betacam Levels

Name	Betacam (mV)	Betacam Variant (mV)	SMPTE (mV)	MII (mV)
Y Range	0 to 714 (includes 7.5% pedestal)	0 to 714	0 to 700	0 to 700 (includes 7.5% pedestal)
Pb and Pr Range	–467 to +467	–505 to +505	–350 to +350	–324 to +324
Sync Depth	286	286	300	300

CG[11:0] Chroma Gain, Address 0x2D[3:0]; Address 0x2E[7:0] CMG[11:0] Chroma Manual Gain, Address 0x2D[3:0]; Address 0x2E[7:0]

Chroma Gain[11:0] is a dual-function register. If written to, a desired manual chroma gain can be programmed. This gain becomes active if the CAGC[1:0] mode is switched to manual fixed gain. Refer to Equation 2 for calculating a desired gain. If read back, this register returns the current gain value. Depending on the setting in the CAGC[1:0] bits, one of these gain values is returned

- Chroma manual gain value (CAGC[1:0] set to chroma manual gain mode)
- Chroma automatic gain value (CAGC[1:0] set to any of the automatic modes)

Table 41. CG/CMG Function

CG[11:0]/CMG[11:0]	Read/Write	Description
CMG[11:0]	Write	Manual gain for chroma path
CG[11:0]	Read	Currently active gain

$$Chroma_Gain = \frac{(0 < CG \le 4095)}{1024} = 0...4 \quad (2)$$

For example, freezing the automatic gain loop and reading back the CG[11:0] register results in a value of 0x47A.

1. Convert the readback value to decimal: 0x47A = 1146d
2. Apply Equation 2 to convert the readback value: 1146/1024 = 1.12

CKE Color Kill Enable, Address 0x2B[6]

The color kill enable bit allows the optional color kill function to be switched on or off.

For QAM-based video standards (PAL and NTSC) and FM-based systems (SECAM), the threshold for the color kill decision is selectable via the CKILLTHR[2:0] bits.

If color kill is enabled, and if the color carrier of the incoming video signal is less than the threshold for 128 consecutive video lines, color processing is switched off (black and white output). To switch the color processing back on, another 128 consecutive lines with a color burst greater than the threshold are required.

The color kill option works only for input signals with a modulated chroma part. For component input (YPrPb), there is no color kill.

Setting CKE to 0 disables color kill.

Setting CKE to 1 (default) enables color kill.

CKILLTHR[2:0] Color Kill Threshold, Address 0x3D[6:4]

The CKILLTHR[2:0] bits allow the user to select a threshold for the color kill function. The threshold applies only to QAM based (NTSC and PAL) or FM-modulated (SECAM) video standards.

To enable the color kill function, the CKE bit must be set. For settings 000, 001, 010, and 011, chroma demodulation inside the ADV7183B may not work satisfactorily for poor input video signals.

Table 42. CKILLTHR Function

	Description	
CKILLTHR[2:0]	SECAM	NTSC, PAL
000	No color kill	Kill at < 0.5%
001	Kill at < 5%	Kill at < 1.5%
010	Kill at < 7%	Kill at < 2.5%
011	Kill at < 8%	Kill at < 4.0%
100 (default)	Kill at < 9.5%	Kill at < 8.5%
101	Kill at < 15%	Kill at < 16.0%
110	Kill at < 32%	Kill at < 32.0%
111	Reserved for ADI internal use only; do not select	

CHROMA TRANSIENT IMPROVEMENT (CTI)

The signal bandwidth allocated for chroma is typically much smaller than that of luminance. In the past, this was a valid way to fit a color video signal into a given overall bandwidth because the human eye is less sensitive to chrominance than to luminance.

The uneven bandwidth, however, can lead to visual artifacts in sharp color transitions. At the border of two bars of color, both components (luma and chroma) change at the same time (see Figure 18). Due to the higher bandwidth, the signal transition of the luma component is usually much sharper than that of the chroma component. The color edge is not sharp but blurred, in the worst case, over several pixels.

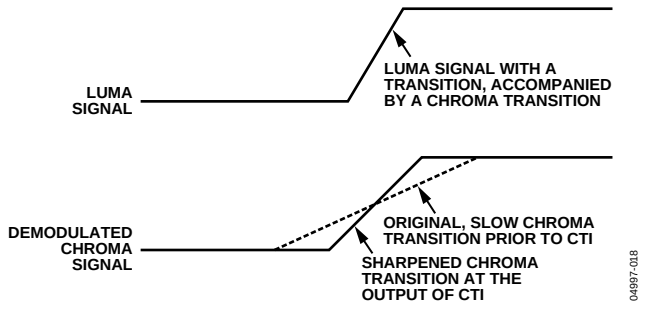


Figure 18. CTI Luma/Chroma Transition

The chroma transient improvement block examines the input video data. It detects transitions of chroma and can be programmed to steepen the chroma edges in an attempt to artificially restore lost color bandwidth. The CTI block, however, operates only on edges above a certain threshold to ensure that noise is not emphasized. Care has also been taken to ensure that edge ringing and undesirable saturation or hue distortion are avoided.

Chroma transient improvements are needed primarily for signals that experienced severe chroma bandwidth limitations. For those types of signals, it is strongly recommended to enable the CTI block via CTI_EN.

CTI_EN Chroma Transient Improvement Enable, Address 0x4D[0]

The CTI_EN bit enables the CTI function. If set to 0, the CTI block is inactive and the chroma transients are left untouched.

Setting CTI_EN to 0 disables the CTI block.

Setting CTI_EN to 1 (default) enables the CTI block.

CTI_AB_EN Chroma Transient Improvement Alpha Blend Enable, Address 0x4D[1]

The CTI_AB_EN bit enables an alpha-blend function within the CTI block. If set to 1, the alpha blender mixes the transient improved chroma with the original signal. The sharpness of the alpha blending can be configured via the CTI_AB[1:0] bits.

For the alpha blender to be active, the CTI block must be enabled via the CTI_EN bit.

Setting CTI_AB_EN to 0 disables the CTI alpha blender.

Setting CTI_AB_EN to 1 (default) enables the CTI alpha-blend mixing function.

CTI_AB[1:0] Chroma Transient Improvement Alpha Blend, Address 0x4D[3:2]

The CTI_AB[1:0] controls the behavior of alpha-blend circuitry that mixes the sharpened chroma signal with the original one. It thereby controls the visual impact of CTI on the output data.

For CTI_AB[1:0] to become active, the CTI block must be enabled via the CTI_EN bit, and the alpha blender must be switched on via CTI_AB_EN.

Sharp blending maximizes the effect of CTI on the picture, but can also increase the visual impact of small amplitude, high frequency chroma noise.

Table 43. CTI_AB Function

CTI_AB[1:0]	Description
00	Sharpest mixing between sharpened and original chroma signal
01	Sharp mixing
10	Smooth mixing
11 (default)	Smoothest alpha blend function

CTI_C_TH[7:0] CTI Chroma Threshold, Address 0x4E[7:0]

The CTI_C_TH[7:0] value is an unsigned, 8-bit number specifying how big the amplitude step in a chroma transition must be steepened by the CTI block. Programming a small value into this register causes even smaller edges to be steepened by the CTI block. Making CTI_C_TH[7:0] a large value causes the block to improve large transitions only.

The default value for CTI_C_TH[7:0] is 0x08, indicating the threshold for the chroma edges prior to CTI.

DIGITAL NOISE REDUCTION (DNR)

Digital noise reduction is based on the assumption that high frequency signals with low amplitude are probably noise and that their removal, therefore, improves picture quality.

DNR_EN Digital Noise Reduction Enable, Address 0x4D[5]

The DNR_EN bit enables or bypasses the DNR block.

Setting DNR_EN to 0 bypasses DNR (disables it).

Setting DNR_EN to 1 (default) enables digital noise reduction on the luma data.

DNR_TH[7:0] DNR Noise Threshold, Address 0x50[7:0]

The DNR_TH[7:0] value is an unsigned 8-bit number used to determine the maximum edge to be interpreted as noise and, therefore, blanked from the luma data. Programming a large value into DNR_TH[7:0] causes the DNR block to interpret even large transients as noise and remove them. The effect on the video data is, therefore, more visible.

Programming a small value causes only small transients to be seen as noise and to be removed.

The recommended DNR_TH[7:0] setting for A/V inputs is 0x04, and the recommended DNR_TH[7:0] setting for tuner inputs is 0x0A.

The default value for DNR_TH[7:0] is 0x08, indicating the threshold for maximum luma edges to be interpreted as noise.

COMB FILTERS

The comb filters of the ADV7183B have been greatly improved to automatically handle video of all types, standards, and levels of quality. The NTSC and PAL configuration registers allow the user to customize comb filter operation, depending on which video standard is detected (by autodetection) or selected (by manual programming). In addition to the bits listed in this section, there are some other ADI internal controls; contact ADI for more information.

NTSC Comb Filter Settings

Used for NTSC-M/J CVBS inputs.

NSFSEL[1:0] Split Filter Selection NTSC, Address 0x19[3:2]

The NSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A narrow split filter selection gives better performance on diagonal lines, but leaves more dot crawl in the final output image; the opposite is true for selecting a wide bandwidth split filter.

Table 44. NSFSEL Function

NSFSEL[1:0]	Description
00 (default)	Narrow
01	Medium
10	Medium
11	Wide

CTAPSN[1:0] Chroma Comb Taps NTSC, Address x38[7:6]

Table 45. CTAPSN Function

CTAPSN[1:0]	Description
00	Do not use
01	NTSC chroma comb adapts 3 lines (3 taps) to 2 lines (2 taps)
10 (default)	NTSC chroma comb adapts 5 lines (5 taps) to 3 lines (3 taps)
11	NTSC chroma comb adapts 5 lines (5 taps) to 4 lines (4 taps)

CCMN[2:0] Chroma Comb Mode NTSC, Address 0x38[5:3]

Table 46. CCMN Function

CCMN[2:0]	Description	
0xx (default)	Adaptive comb mode	Adaptive 3-line chroma comb for CTAPSN = 01
		Adaptive 4-line chroma comb for CTAPSN = 10
		Adaptive 5-line chroma comb for CTAPSN = 11
100	Disable chroma comb	
101	Fixed chroma comb (top lines of line memory)	Fixed 2-line chroma comb for CTAPSN = 01
		Fixed 3-line chroma comb for CTAPSN = 10
		Fixed 4-line chroma comb for CTAPSN = 11
110	Fixed chroma comb (all lines of line memory)	Fixed 3-line chroma comb for CTAPSN = 01
		Fixed 4-line chroma comb for CTAPSN = 10
		Fixed 5-line chroma comb for CTAPSN = 11
111	Fixed chroma comb (bottom lines of line memory)	Fixed 2-line chroma comb for CTAPSN = 01
		Fixed 3-line chroma comb for CTAPSN = 10
		Fixed 4-line chroma comb for CTAPSN = 11

YCMN[2:0] Luma Comb Mode NTSC, Address 0x38[2:0]

Table 47.YCMN Function

YCMN[2:0]	Description	
0xx (default)	Adaptive comb mode	Adaptive 3-line (3 taps) luma comb
100	Disable luma comb	Use low-pass/notch filter; see the Y-Shaping Filter section
101	Fixed luma comb (top lines of line memory)	Fixed 2-line (2 taps) luma comb
110	Fixed luma comb (all lines of line memory)	Fixed 3-line (3 taps) luma comb
111	Fixed luma comb (bottom lines of line memory)	Fixed 2-line (2 taps) luma comb

PAL Comb Filter Settings

Used for PAL-B/G/H/I/D, PAL-M, PAL-Combination N, PAL60 and NTSC443 CVBS inputs.

PSFSEL[1:0] Split Filter Selection PAL, Address 0x19[1:0]

The PSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A wide split filter selection eliminates dot crawl, but shows imperfections on diagonal lines; the opposite is true for selecting a narrow bandwidth split filter.

Table 48. PSFSEL Function

PSFSEL[1:0]	Description
00	Narrow
01 (default)	Medium
10	Wide
11	Widest

CTAPSP[1:0] Chroma Comb Taps PAL, Address 0x39[7:6]

Table 49. CTAPSP Function

CTAPSP[1:0]	Description
00	Do not use.
01	PAL chroma comb adapts 5 lines (3 taps) to 3 lines (2 taps); cancels cross luma only
10	PAL chroma comb adapts 5 lines (5 taps) to 3 lines (3 taps); cancels cross luma and hue error less well
11 (default)	PAL chroma comb adapts 5 lines (5 taps) to 4 lines (4 taps); cancels cross luma and hue error well

CCMP[2:0] Chroma Comb Mode PAL, Address 0x39[5:3]

Table 50. CCMP Function

CCMP[2:0]	Description	Configuration
0xx (default)	Adaptive comb mode	Adaptive 3-line chroma comb for CTAPSP = 01 Adaptive 4-line chroma comb for CTAPSP = 10 Adaptive 5-line chroma comb for CTAPSP = 11
100	Disable chroma comb	
101	Fixed chroma comb (top lines of line memory)	Fixed 2-line chroma comb for CTAPSP = 01 Fixed 3-line chroma comb for CTAPSP = 10 Fixed 4-line chroma comb for CTAPSP = 11
110	Fixed chroma comb (all lines of line memory)	Fixed 3-line chroma comb for CTAPSP = 01 Fixed 4-line chroma comb for CTAPSP = 10 Fixed 5-line chroma comb for CTAPSP = 11
111	Fixed chroma comb (bottom lines of line memory)	Fixed 2-line chroma comb for CTAPSP = 01 Fixed 3-line chroma comb for CTAPSP = 10 Fixed 4-line chroma comb for CTAPSP = 11

YCMP[2:0] Luma Comb Mode PAL, Address 0x39[2:0]

Table 51. YCMP Function

YCMP[2:0]	Description	Configuration
0xx (default)	Adaptive comb mode	Adaptive 5 lines (3 taps) luma comb
100	Disable luma comb	Use low-pass/notch filter; see the Y-Shaping Filter section
101	Fixed luma comb (top lines of line memory)	Fixed 3 lines (2 taps) luma comb
110	Fixed luma comb (all lines of line memory)	Fixed 5 lines (3 taps) luma comb
111	Fixed luma comb (bottom lines of line memory)	Fixed 3 lines (2 taps) luma comb

AV CODE INSERTION AND CONTROLS

This section describes the I²C based controls that affect:

- Insertion of AV codes into the data stream
- Data blanking during the vertical blank interval (VBI)
- The range of data values permitted in the output data stream
- The relative delay of luma vs. chroma signals

Some of the decoded VBI data is inserted during the horizontal blanking interval. See the Gemstar Data Recovery section for more information.

BT656-4 ITU Standard BT-R.656-4 Enable, Address 0x04[7]

The ITU has changed the position for toggling of the V bit within the SAV EAV codes for NTSC between revisions 3 and 4. The BT656-4 standard bit allows the user to select an output mode that is compliant with either the previous or the new standard. For more information, review the standard at www.itu.int.

Note that the standard change affects NTSC only and has no bearing on PAL.

When BT656-4 is 0 (default), the BT656-3 specification is used. The V bit goes low at EAV of Line 10 and Line 273.

When BT656-4 is 1, the BT656-4 specification is used. The V bit goes low at EAV of Line 20 and Line 283.

SD_DUP_AV Duplicate AV Codes, Address 0x03[0]

Depending on the output interface width, it can be necessary to duplicate the AV codes from the luma path into the chroma path.

In an 8-bit-wide output interface (Cb/Y/Cr/Y interleaved data), the AV codes are defined as FF/00/00/AV, with AV as the transmitted word that contains information about H/V/F.

In this output interface mode, the following assignment takes place: Cb = FF, Y = 00, Cr = 00, and Y = AV.

In a 16-bit output interface where Y and Cr/Cb are delivered via separate data buses, the AV code is over the whole 16 bits. The SD_DUP_AV bit allows the user to replicate the AV codes on both busses, so the full AV sequence can be found on the Y bus and on the Cr/Cb bus. See Figure 19.

When SD_DUP_AV is 0 (default), the AV codes are in single fashion (for 8-bit interleaved data output).

When SD_DUP_AV is 1, the AV codes are duplicated (for 16-bit interfaces).

VBI_EN Vertical Blanking Interval Data Enable, Address 0x03[7]

The VBI enable bit allows data such as intercast and closed caption data to be passed through the luma channel of the decoder with a minimal amount of filtering. All data for Line 1 to Line 21 is passed through and available at the output port. The ADV7183B does not blank the luma data, and automatically switches all filters along the luma data path into their widest bandwidth. For active video, the filter settings for YSH and YPK are restored.

Refer to the BL_C_VBI Blank Chroma During VBI, Address 0x04[2] section for information on the chroma path.

When VBI_EN is 0 (default), all video lines are filtered/scaled.

When VBI_EN is 1, only the active video region is filtered/scaled.

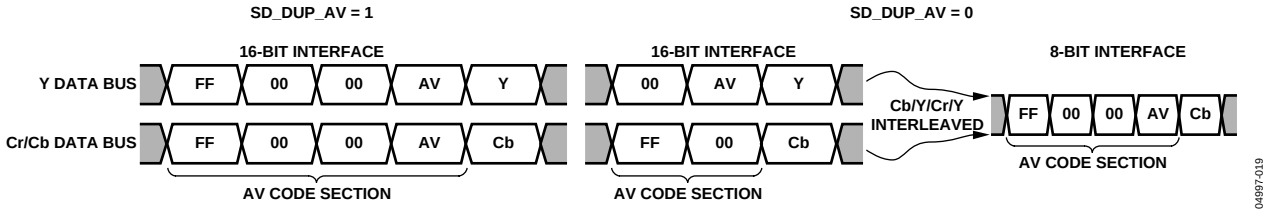


Figure 19. AV Code Duplication Control

BL_C_VBI Blank Chroma During VBI, Address 0x04[2]

Setting BL_C_VBI high, the Cr and Cb values of all VBI lines are blanked. This is done so any data that arrives during VBI is not decoded as color and output through Cr and Cb. As a result, it should be possible to send VBI lines into the decoder, then output them through an encoder again, undistorted. Without this blanking, any wrongly decoded color is encoded by the video encoder; therefore, the VBI lines are distorted.

Setting BL_C_VBI to 0 decodes and outputs color during VBI.

Setting BL_C_VBI to 1 (default) blanks Cr and Cb values during VBI.

RANGE Range Selection, Address 0x04[0]

AV codes (as per ITU-R BT-656, formerly known as CCIR-656) consist of a fixed header made up of 0xFF and 0x00 values. These two values are reserved and therefore cannot be used for active video. Additionally, the ITU specifies that the nominal range for video should be restricted to values between 16 and 235 for luma and 16 to 240 for chroma.

The RANGE bit allows the user to limit the range of values output by the ADV7183B to the recommended value range. In any case, it ensures that the reserved values of 255d (0xFF) and 00d (0x00) are not presented on the output pins unless they are part of an AV code header.

Table 52. RANGE Function

RANGE	Description	
0	16 ≤ Y ≤ 235	16 ≤ C/P ≤ 240
1 (default)	1 ≤ Y ≤ 254	1 ≤ C/P ≤ 254

AUTO_PDC_EN Automatic Programmed Delay Control, Address 0x27[6]

Enabling the AUTO_PDC_EN function activates a function within the ADV7183B that automatically programs the LTA[1:0] and CTA[2:0] to have the chroma and luma data match delays for all modes of operation. If set, manual registers LTA[1:0] and CTA[2:0] are not used. If the automatic mode is disabled (via setting the AUTO_PDC_EN bit to 0), the values programmed into LTA[1:0] and CTA[2:0] registers become active.

When AUTO_PDC_EN is 0, the ADV7183 uses the LTA[1:0] and CTA[2:0] values for delaying luma and chroma samples. Refer to the LTA[1:0] Luma Timing Adjust, Address 0x27[1:0] and the CTA[2:0] Chroma Timing Adjust, Address 0x27[5:3] sections.

When AUTO_PDC_EN is 1 (default), the ADV7183B automatically determines the LTA and CTA values to have luma and chroma aligned at the output.

LTA[1:0] Luma Timing Adjust, Address 0x27[1:0]

The Luma Timing Adjust register allows the user to specify a timing difference between chroma and luma samples.

There is a certain functionality overlap with the CTA[2:0] register. For manual programming, use the following defaults:

- CVBS input LTA[1:0] = 00
- Y/C input LTA[1:0] = 01
- YPrPb input LTA[1:0] = 01

Table 53. LTA Function

LTA[1:0]	Description
00 (default)	No delay
01	Luma 1 clk (37 ns) delayed
10	Luma 2 clk (74 ns) early
11	Luma 1 clk (37 ns) early

CTA[2:0] Chroma Timing Adjust, Address 0x27[5:3]

The Chroma Timing Adjust register allows the user to specify a timing difference between chroma and luma samples. This can be used to compensate for external filter group delay differences in the luma vs. chroma path, and to allow a different number of pipeline delays while processing the video downstream. Review this functionality together with the LTA[1:0] register.

The chroma can only be delayed/advanced in chroma pixel steps. One chroma pixel step is equal to two luma pixels. The programmable delay occurs after demodulation, where one can no longer delay by luma pixel steps.

For manual programming, use the following defaults:

- CVBS input CTA[2:0] = 011
- Y/C input CTA[2:0] = 101
- YPrPb input CTA[2:0] =110

Table 54. CTA Function

CTA[2:0]	Description
000	Not used
001	Chroma + 2 chroma pixel (early)
010	Chroma + 1 chroma pixel (early)
011 (default)	No delay
100	Chroma – 1 chroma pixel (late)
101	Chroma – 2 chroma pixel (late)
110	Chroma – 3 chroma pixel (late)
111	Not used

SYNCHRONIZATION OUTPUT SIGNALS

HS Configuration

The following controls allow the user to configure the behavior of the HS output pin only:

- Beginning of HS signal via HSB[10:0]
- End of HS signal via HSE[10:0]
- Polarity of HS using PHS

The HS begin and HS end registers allow the user to freely position the HS output (pin) within the video line. The values in HSB[10:0] and HSE[10:0] are measured in pixel units from the falling edge of HS. Using both values, the user can program both the position and length of the HS output signal.

HSB[10:0] HS Begin, Address 0x34[6:4], Address 0x35[7:0]

The position of this edge is controlled by placing a binary number into HSB[10:0]. The number applied offsets the edge with respect to an internal counter that is reset to 0 immediately after EAV Code FF, 00, 00, XY (see Figure 20). HSB is set to 00000000010b, which is 2 LLC1 clock cycles from Count[0].

The default value of HSB[10:0] is 0x002, indicating the HS pulse starts two pixels after the falling edge of HS.

HSE[10:0] HS End, Address 0x34[2:0], Address 0x36[7:0]

The position of this edge is controlled by placing a binary number into HSE[10:0]. The number applied offsets the edge with respect to an internal counter that is reset to 0 immediately after EAV Code FF, 00, 00, XY (see Figure 20). HSE is set to 00000000000b, which is 0 LLC1 clock cycles from Count[0].

The default value of HSE[9:0] is 000, indicating that the HS pulse ends zero pixels after falling edge of HS.

For example:

1. To shift the HS toward active video by 20 LLC1s, add 20 LLC1s to both HSB and HSE, that is, HSB[10:0] = [00000010110], HSE[10:0] = 00000010100].
2. To shift the HS away from active video by 20 LLC1s, add 1696 LLC1s to both HSB and HSE (for NTSC), that is, HSB[10:0] = [11010100010], HSE[10:0] = [11010100000]. 1696 is derived from the NTSC total number of pixels = 1716.

To move 20 LLC1s away from active video is equal to subtracting 20 from 1716 and adding the result in binary to both HSB[10:0] and HSE[10:0].

PHS Polarity HS, Address 0x37[7]

The polarity of the HS pin can be inverted using the PHS bit.

When PHS is 0 (default), HS is active high.

When PHS is 1, HS is active low.

Table 55. HS Timing Parameters (see Figure 20)

	Characteristic				
Standard	**HS Begin Adjust (HSB[10:0]) (Default)**	**HS End Adjust (HSE[10:0]) (Default)**	**HS to Active Video (LLC1 Clock Cycles) (C in Figure 20) (Default)**	**Active Video Samples/Line (D in Figure 20)**	**Total LLC1 Clock Cycles (E in Figure 20)**
NTSC	00000000010b	00000000000b	272	720Y + 720C = 1440	1716
NTSC Square Pixel	00000000010b	00000000000b	276	640Y + 640C = 1280	1560
PAL	00000000010b	00000000000b	284	720Y + 720C = 1440	1728

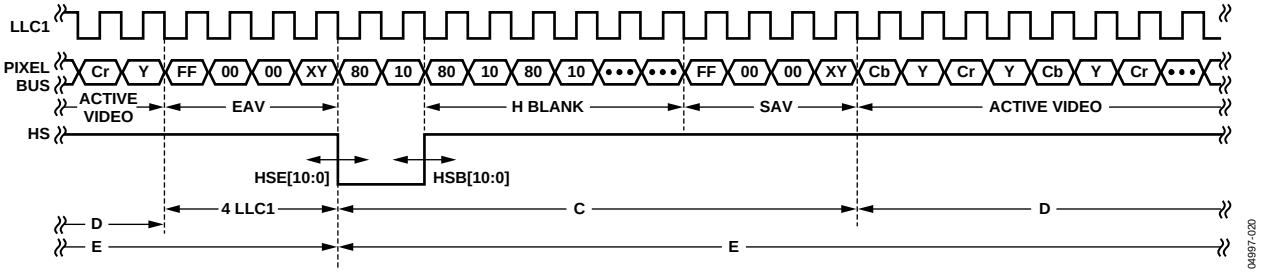


Figure 20. HS Timing

VS and FIELD Configuration

The following controls allow the user to configure the behavior of the VS and FIELD output pins and to generate embedded AV codes:

- ADV encoder-compatible signals via NEWAVMODE
- PVS, PF
- HVSTIM
- VSBHO, VSBHE
- VSEHO, VSEHE
- For NTSC control:
    - NVBEGDELO, NVBEGDELE, NVBEGSIGN, NVBEG[4:0]
    - NVENDDELO, NVENDDELE, NVENDSIGN, NVEND[4:0]
    - NFTOGDELO, NFTOGDELE, NFTOGSIGN, NFTOG[4:0]
- For PAL control:
    - PVBEGDELO, PVBEGDELE, PVBEGSIGN, PVBEG[4:0]
    - PVENDDELO, PVENDDELE, PVENDSIGN, PVEND[4:0]
    - PFTOGDELO, PFTOGDELE, PFTOGSIGN, PFTOG[4:0]

NEWAVMODE New AV Mode, Address 0x31[4]

When NEWAVMODE is 0, EAV/SAV codes are generated to suit ADI encoders. No adjustments are possible.

Setting NEWAVMODE to 1 (default) enables the manual posi-tion of the Vsync, Field, and AV codes using Register 0x34 to Register 0x37 and Register 0xE5 to Register 0xEA. Default register settings are CCIR656-compliant; see Figure 21 for NTSC and Figure 26 for PAL. For recommended manual user settings, see Table 56 and Figure 22 for NTSC; see Table 57 and Figure 27 for PAL.

HVSTIM Horizontal VS Timing, Address 0x31[3]

The HVSTIM bit allows the user to select where the VS signal is being asserted within a line of video. Some interface circuitry can require VS to go low while HS is low.

When HVSTIM is 0 (default), the start of the line is relative to HSE.

When HVSTIM is 1, the start of the line is relative to HSB.

VSBHO VS Begin Horizontal Position Odd, Address 0x32[7]

The VSBHO and VSBHE bits select the position within a line at which the VS pin (not the bit in the AV code) becomes active. Some follow-on chips require the VS pin to change state only when HS is high/low.

When VSBHO is 0 (default), the VS pin goes high at the middle of a line of video (odd field).

When VSBHO is 1, the VS pin changes state at the start of a line (odd field).

VSBHE VS Begin Horizontal Position Even, Address 0x32[6]

The VSBHO and VSBHE bits select the position within a line at which the VS pin (not the bit in the AV code) becomes active. Some follow-on chips require the VS pin to change state when only HS is high/low.

When VSBHE is 0, the VS pin goes high at the middle of a line of video (even field).

When VSBHE is 1 (default), the VS pin changes state at the start of a line (even field).

VSEHO VS End Horizontal Position Odd, Address 0x33[7]

The VSEHO and VSEHE bits select the position within a line at which the VS pin (not the bit in the AV code) becomes active. Some follow-on chips require the VS pin to change state only when HS is high/low.

When VSEHO is 0 (default), the VS pin goes low (inactive) at the middle of a line of video (odd field).

When VSEHO is 1, the VS pin changes state at the start of a line (odd field).

VSEHE VS End Horizontal Position Even, Address 0x33[6]

The VSEHO and VSEHE bits select the position within a line at which the VS pin (not the bit in the AV code) becomes active. Some follow-on chips require the VS pin to change state only when HS is high/low.

When VSEHE is 0 (default), the VS pin goes low (inactive) at the middle of a line of video (even field).

When VSEHE is 1, the VS pin changes state at the start of a line (even field).

PVS Polarity VS, Address 0x37[5]

The polarity of the VS pin can be inverted using the PVS bit.

When PVS is 0 (default), VS is active high.

When PVS is 1, VS is active low. PF Polarity FIELD, Address 0x37[3]

The polarity of the FIELD pin can be inverted using the PF bit.

When PF is 0 (default), FIELD is active high.
When PF is 1, FIELD is active low.

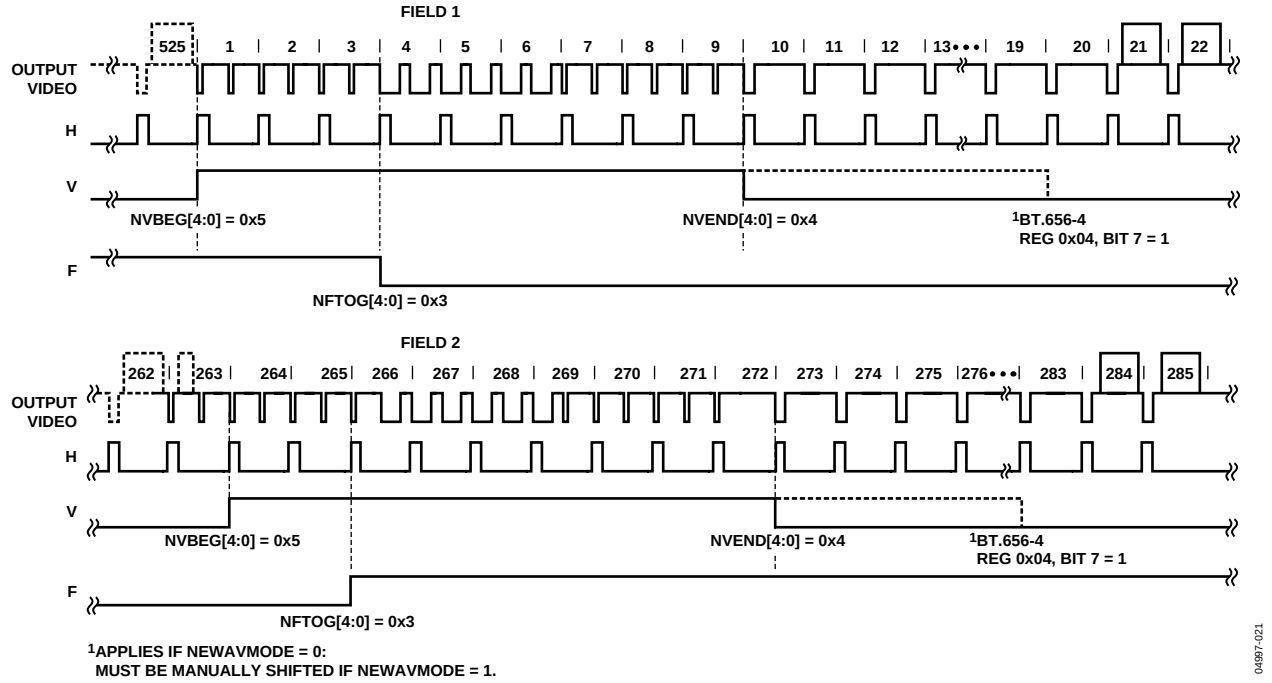


Figure 21. NTSC Default (BT.656). The Polarity of H, V, and F is Embedded in the Data.

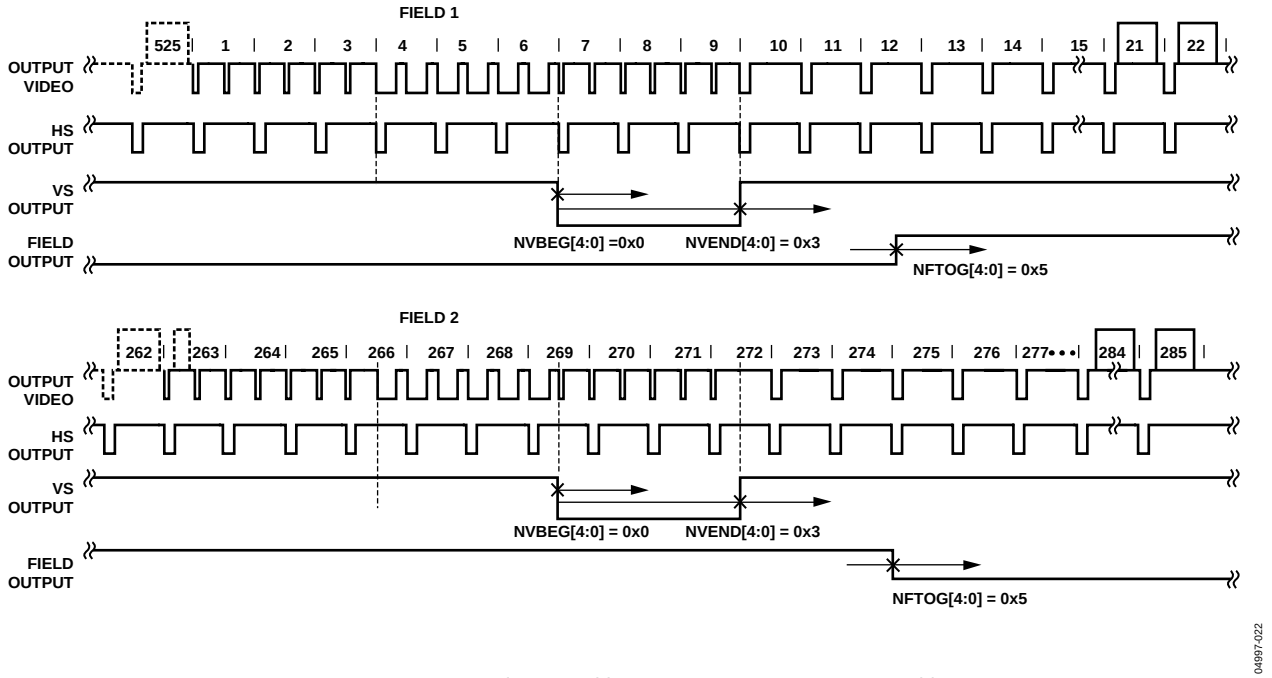


Figure 22. NTSC Typical Vsync/Field Positions Using Register Writes in Table 56

Table 56. Recommended User Settings for NTSC (See Figure 22)

Register	Register Name	Write
0x31	Vsync Field Control 1	0x1A
0x32	Vsync Field Control 2	0x81
0x33	Vsync Field Control 3	0x84
0x34	Hsync Pos. Control 1	0x00
0x35	Hsync Pos. Control 2	0x00
0x36	Hsync Pos. Control 3	0x7D
0x37	Polarity	0xA1
0xE5	NTSV_V_Bit_Beg	0x41
0xE6	NTSC_V_Bit_End	0x84
0xE7	NTSC_F_Bit_Tog	0x06

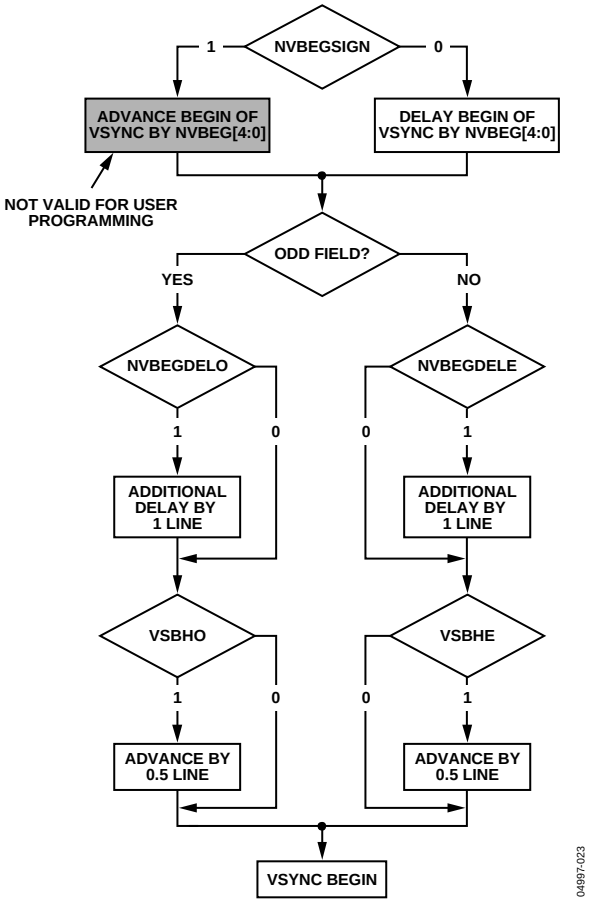


Figure 23. NTSC Vsync Begin

NVBEGDELO NTSC Vsync Begin Delay on Odd Field, Address 0xE5[7]

When NVBEGDELO is 0 (default), there is no delay.

Setting NVBEGDELO to 1, delay Vsync going high on an odd field by a line relative to NVBEG.

NVBEGDELE NTSC Vsync Begin Delay on Even Field, Address 0xE5[6]

When NVBEGDELE is 0 (default), there is no delay.

Setting NVBEGDELE to 1 delays Vsync going high on an even field by a line relative to NVBEG.

NVBEGSIGN NTSC Vsync Begin Sign, Address 0xE5[5]

Setting NVBEGSIGN to 0 delays the start of Vsync. Set for user manual programming.

Setting NVBEGSIGN to 1 (default), advances the start of Vsync. Not recommended for user programming.

NVBEG[4:0] NTSC Vsync Begin, Address 0xE5[4:0]

The default value of NVBEG is 00101, indicating the NTSC Vsync begin position.

For all NTSC/PAL Vsync timing controls, both the V bit in the AV code and the Vsync on the VS pin are modified.

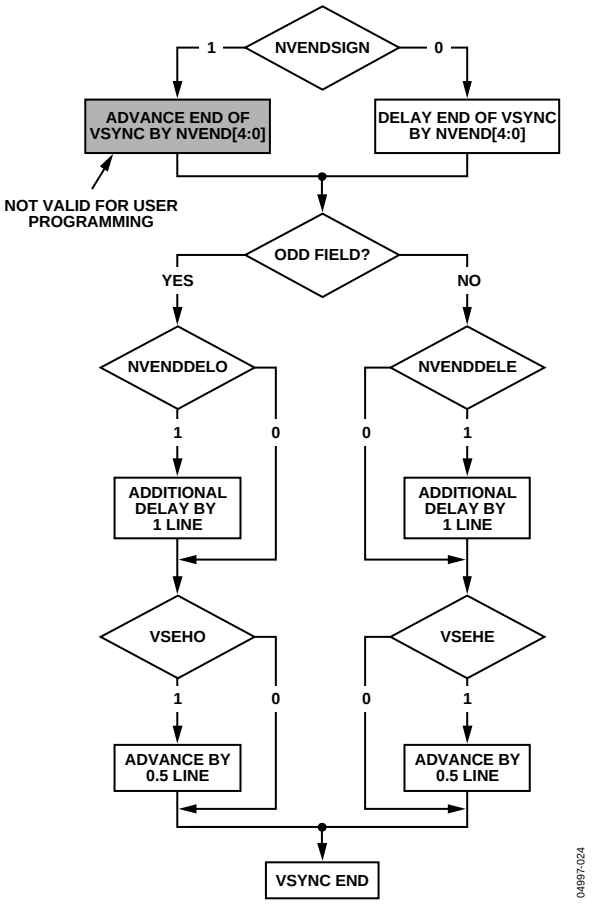


Figure 24. NTSC Vsync End

NVENDDELO NTSC Vsync End Delay on Odd Field, Address 0xE6[7]

When NVENDDELO is 0 (default), there is no delay.

Setting NVENDDELO to 1 delays Vsync from going low on an odd field by a line relative to NVEND.

NVENDDELE NTSC Vsync End Delay on Even Field, Address 0xE6[6]

When NVENDDELE is set to 0 (default), there is no delay.

Setting NVENDDELE to 1 delays Vsync from going low on an even field by a line relative to NVEND.

NVENDSIGN NTSC Vsync End Sign, Address 0xE6[5]

Setting NVENDSIGN to 0 (default) delays the end of Vsync (default). Set for user manual programming.

Setting NVENDSIGN to 1 advances the end of Vsync. Not recommended for user programming.

NVEND NTSC[4:0] Vsync End, Address 0xE6[4:0]

The default value of NVEND is 00100, indicating the NTSC Vsync end position.

For all NTSC/PAL Vsync timing controls, both the V bit in the AV code and the Vsync on the VS pin are modified.

NFTOGDELO NTSC Field Toggle Delay on Odd Field, Address 0xE7[7]

When NFTOGDELO is 0 (default), there is no delay.

Setting NFTOGDELO to 1 delays the field toggle/transition on an odd field by a line relative to NFTOG.

NFTOGDELE NTSC Field Toggle Delay on Even Field, Address 0xE7[6]

When NFTOGDELE is 0, there is no delay.

Setting NFTOGDELE to 1 (default) delays the field toggle/transition on an even field by a line relative to NFTOG.

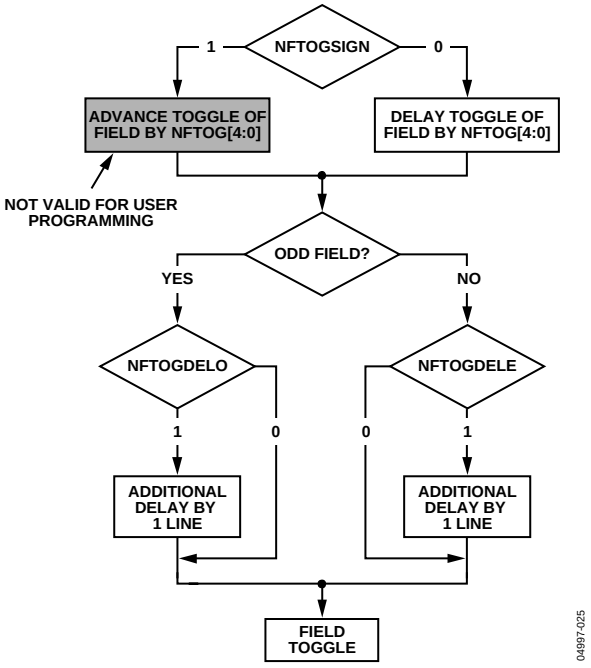


Figure 25. NTSC FIELD Toggle

NFTOGSIGN NTSC Field Toggle Sign, Address 0xE7[5]

Setting NFTOGSIGN to 0 delays the field transition. Set for user manual programming.

Setting NFTOGSIGN to 1 (default) advances the field transition. Not recommended for user programming.

NFTOG[4:0] NTSC Field Toggle, Address 0xE7[4:0]

The default value of NFTOG is 00011, indicating the NTSC Field toggle position.

For all NTSC/PAL Field timing controls, both the F bit in the AV code and the Field signal on the FIELD pin are modified.

Table 57. Recommended User Settings for PAL (see Figure 27)

Register	Register Name	Write
0x31	Vsync Field Control 1	0x1A
0x32	Vsync Field Control 2	0x81
0x33	Vsync Field Control 3	0x84
0x34	Hsync Pos. Control 1	0x00
0x35	Hsync Pos. Control 2	0x00
0x36	Hsync Pos. Control 3	0x7D
0x37	Polarity	0x29
0xE8	PAL_V_Bit_Beg	0x41
0xE9	PAL_V_Bit_End	0x84
0xEA	PAL_F_Bit_Tog	0x06

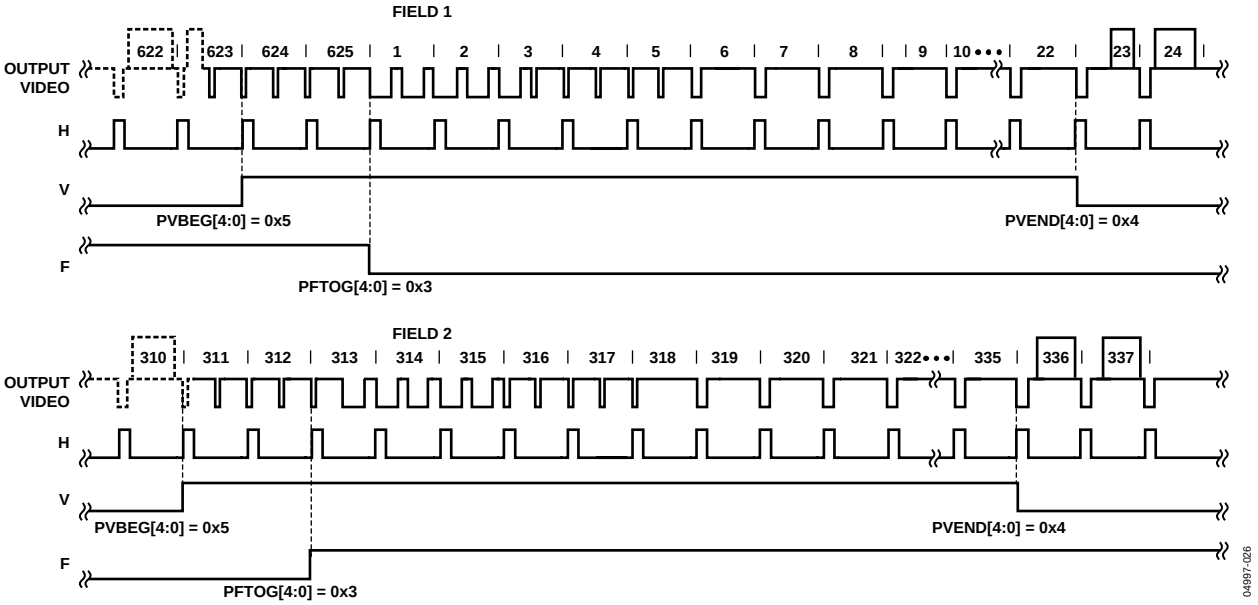


Figure 26. PAL Default (BT.656). The Polarity of H, V, and F is Embedded in the Data.

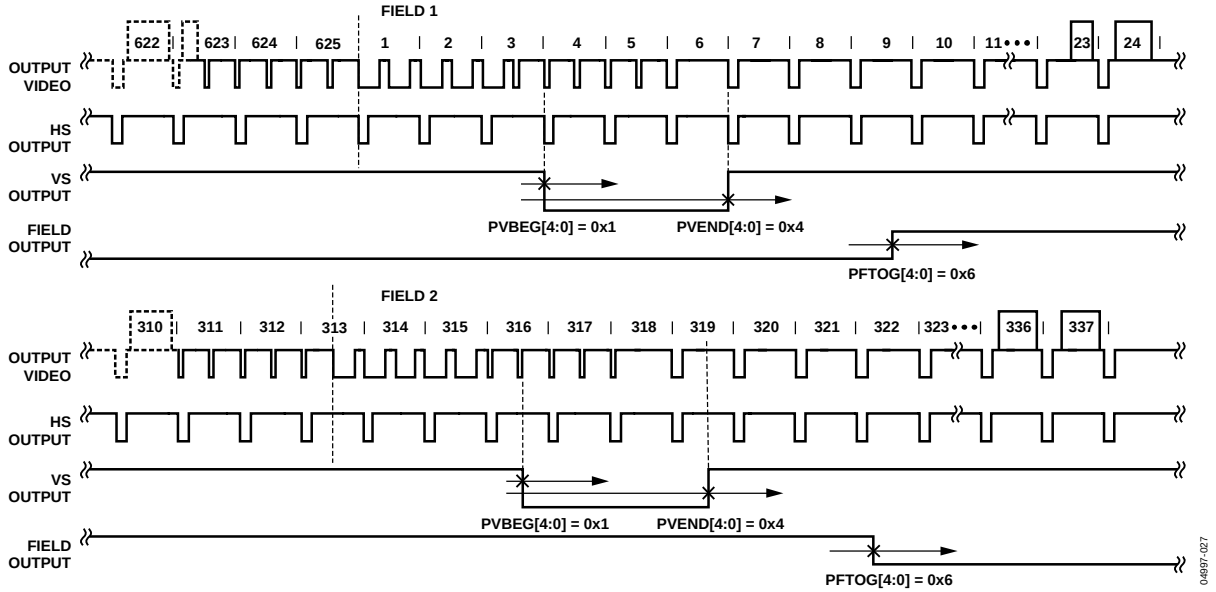


Figure 27. PAL Typical Vsync/Field Positions Using Register Writes in Table 57

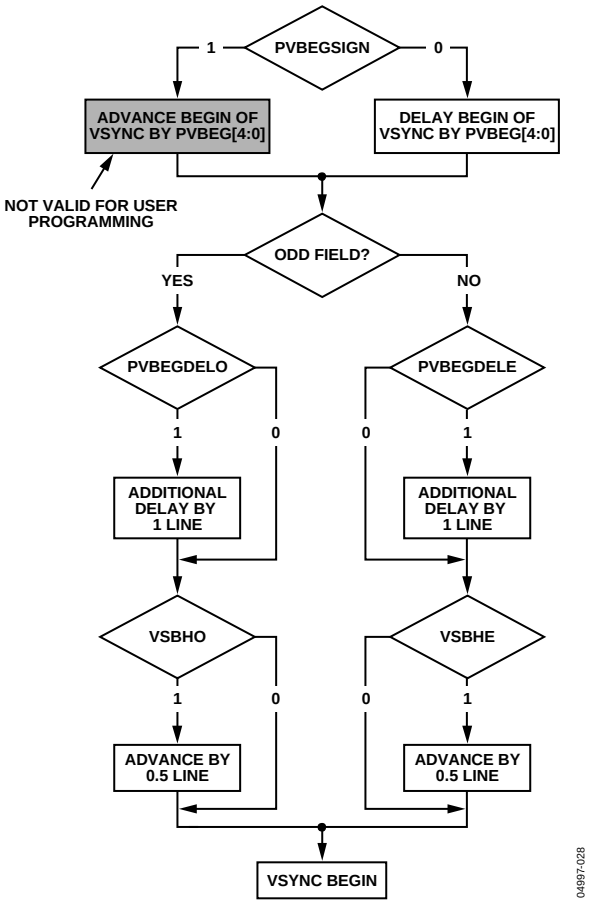


Figure 28. PAL Vsync Begin

PVBEGDELO PAL Vsync Begin Delay on Odd Field, Address 0xE8[7]

When PVBEGDELO is 0 (default), there is no delay.

Setting PVBEGDELO to 1 delays Vsync going high on an odd field by a line relative to PVBEG.

PVBEGDELE PAL Vsync Begin Delay on Even Field, Address 0xE8[6]

When PVBEGDELE is 0, there is no delay.

Setting PVBEGDELE to 1 (default) delays Vsync going high on an even field by a line relative to PVBEG.

PVBEGSIGN PAL Vsync Begin Sign, Address 0xE8[5]

Setting PVBEGSIGN to 0 delays the beginning of Vsync. Set for user manual programming.

Setting PVBEGSIGN to 1 (default) advances the beginning of Vsync. Not recommended for user programming.

PVBEG[4:0] PAL Vsync Begin, Address 0xE8[4:0]

The default value of PVBEG is 00101, indicating the PAL Vsync begin position.

For all NTSC/PAL Vsync timing controls, both the V bit in the AV code and the Vsync on the VS pin are modified.

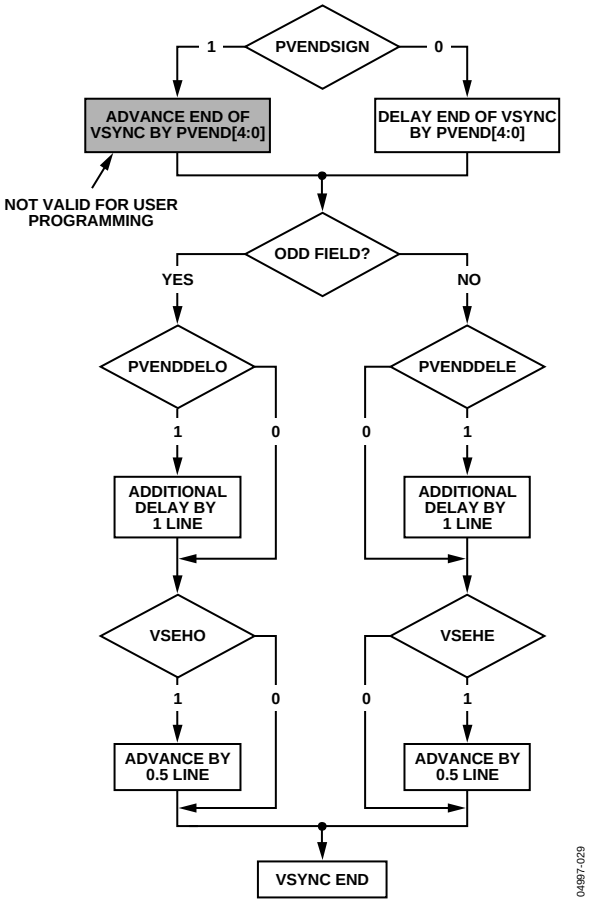


Figure 29. PAL Vsync End

PVENDDELO PAL Vsync End Delay on Odd Field, Address 0xE9[7]

When PVENDDELO is 0 (default), there is no delay.

Setting PVENDDELO to 1 delays Vsync going low on an odd field by a line relative to PVEND.

PVENDDELE PAL Vsync End Delay on Even Field, Address 0xE9[6]

When PVENDDELE is 0 (default), there is no delay.

Setting PVENDDELE to 1 delays Vsync going low on an even field by a line relative to PVEND.

PVENDSIGN PAL Vsync End Sign, Address 0xE9[5]

Setting PVENDSIGN to 0 (default) delays the end of Vsync. Set for user manual programming.

Setting PVENDSIGN to 1 advances the end of Vsync. Not recommended for user programming.

PVEND[4:0] PAL Vsync End, Address 0xE9[4:0]

The default value of PVEND is 10100, indicating the PAL Vsync end position.

For all NTSC/PAL Vsync timing controls, both the V bit in the AV code and the Vsync on the VS pin are modified.

PFTOGDELO PAL Field Toggle Delay on Odd Field, Address 0xEA[7]

When PFTOGDELO is 0 (default), there is no delay.

Setting PFTOGDELO to 1 delays the F toggle/transition on an odd field by a line relative to PFTOG.

PFTOGDELE PAL Field Toggle Delay on Even Field, Address 0xEA[6]

When PFTOGDELE is 0, there is no delay.

Setting PFTOGDELE to 1 (default) delays the F toggle/transition on an even field by a line relative to PFTOG.

PFTOGSIGN PAL Field Toggle Sign, Address 0xEA[5]

Setting PFTOGSIGN to 0 delays the field transition. Set for user manual programming.

Setting PFTOGSIGN to 1 (default) advances the field transition. Not recommended for user programming.

PFTOG PAL Field Toggle, Address 0xEA[4:0]

The default value of PFTOG is 00011, indicating the PAL field toggle position.

For all NTSC/PAL Field timing controls, the F bit in the AV code and the field signal on the FIELD/DE pin are modified.

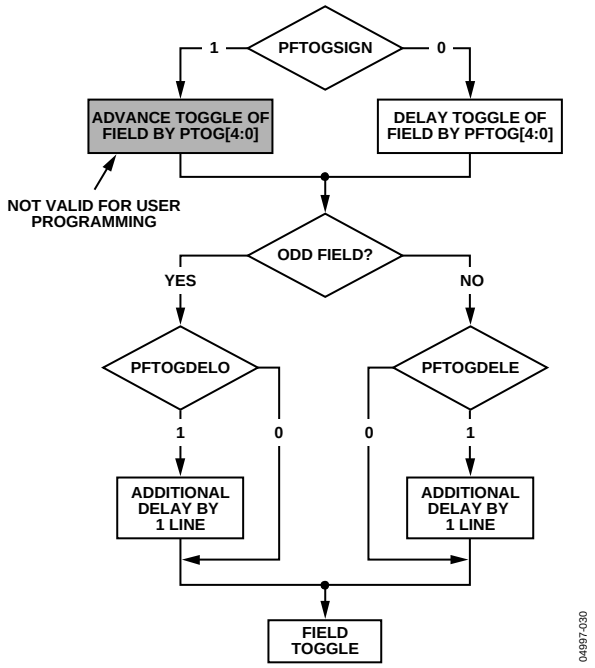


Figure 30. PAL F Toggle

SYNC PROCESSING

The ADV7183B has two additional sync processing blocks that postprocess the raw synchronization information extracted from the digitized input video. If desired, the blocks can be disabled via the following two I²C bits.

ENHSPLL Enable Hsync Processor, Address 0x01[6]

The Hsync processor is designed to filter incoming Hsyncs that have been corrupted by noise, providing improved performance for video signals with stable time bases but poor SNR.

Setting ENHSPLL to 0 disables the Hsync processor.

Setting ENHSPLL to 1 (default) enables the Hsync processor.

ENVSPROC Enable Vsync Processor, Address 0x01[3]

This block provides extra filtering of the detected Vsyncs to give improved vertical lock.

Setting ENVSPROC to 0 disables the Vsync processor.

Setting ENVSPROC to 1 (default) enables the Vsync processor.

VBI DATA DECODE

The following low data rate VBI signals can be decoded by the ADV7183B:

- Wide screen signaling (WSS)
- Copy generation management systems (CGMS)
- Closed captioning (CCAP)
- EDTV
- Gemstar 1×- and 2×-compatible data recovery

The presence of any of the above signals is detected and, if applicable, a parity check is performed. The result of this testing is contained in a confidence bit in the VBI Info[7:0] register. Users are encouraged to first examine the VBI Info register before reading the corresponding data registers. All VBI data decode bits are read only.

All VBI data registers are double-buffered with the field signals. This means that data is extracted from the video lines and appears in the appropriate I²C registers with the next field transition. They are then static until the next field.

The user should start an I²C read sequence with VS by first examining the VBI Info register. Then, depending on what data was detected, the appropriate data registers should be read.

Note that the data registers are filled with decoded VBI data even if their corresponding detection bits are low; it is likely that bits within the decoded data stream are wrong.

The closed captioning data (CCAP) is available in the I²C registers and is also inserted into the output video data stream during horizontal blanking.

The Gemstar-compatible data is not available in the I²C registers and is inserted into the data stream only during horizontal blanking.

WSSD Wide Screen Signaling Detected, Address 0x90[0]

Logic 1 for this bit indicates the data in the WSS1 and WSS2 registers is valid.

The WSSD bit goes high if the rising edge of the start bit is detected within a time window and if the polarity of the parity bit matches the data transmitted.

When WSSD is 0, no WSS is detected and confidence in the decoded data is low.

When WSSD is 1, WSS is detected and confidence in the decoded data is high.

CCAPD Closed Caption Detected, Address 0x90[1]

A Logic 1 for this bit indicates that the data in the CCAP1 and CCAP2 registers is valid.

The CCAPD bit goes high if the rising edge of the start bit is detected within a time window and if the polarity of the parity bit matches the data transmitted.

When CCAPD is 0, no CCAP sequences are detected and confidence in the decoded data is low.

When CCAPD is 1, the CCAP sequence is detected and confidence in the decoded data is high.

EDTVD EDTV Sequence Detected, Address 0x90[2]

A Logic 1 for this bit indicates the data in the EDTV1, 2, 3 registers is valid.

The EDTVD bit goes high if the rising edge of the start bit is detected within a time window and if the polarity of the parity bit matches the data transmitted.

When EDTVD is 0, no EDTV sequence is detected and confidence in the decoded data is low.

When EDTVD is 1, an EDTV sequence is detected and confidence in the decoded data is high.

CGMSD CGMS-A Sequence Detected, Address 0x90[3]

Logic 1 for this bit indicates that the data in the CGMS1, 2, 3 registers is valid. The CGMSD bit goes high if a valid CRC checksum has been calculated from a received CGMS packet.

When CGMSD is 0, no CGMS transmission is detected and confidence in the decoded data is low.

When CGMSD is 1, the CGMS sequence is decoded and confidence in the decoded data is high.

CRC_ENABLE CRC, Address 0xB2[2]

For certain video sources, the CRC data bits can have an invalid format. In these circumstances, the CRC checksum validation procedure can be disabled. The CGMSD bit goes high if the rising edge of the start bit is detected within a time window.

When CRC_ENABLE is 0, no CRC check is performed. The CGMSD bit goes high if the rising edge of the start bit is detected within a time window.

When CRC_ENABLE is 1 (default), CRC checksum is used to validate the CGMS sequence. The CGMSD bit goes high for a valid checksum. The default is ADI's recommended setting.

Wide Screen Signaling Data

WSS1[7:0], Address 0x91[7:0],
WSS2[7:0], Address 0x92[7:0]

Figure 31 shows the bit correspondence between the analog video waveform and the WSS1/WSS2 registers. WSS2[7:6] are undetermined and should be masked out by software.

EDTV Data Registers

EDTV1[7:0], Address 0x93[7:0],
EDTV2[7:0], Address 0x94[7:0],
EDTV3[7:0], Address 0x95[7:0]

Figure 32 shows the bit correspondence between the analog video waveform and the EDTV1/EDTV2/EDTV3 registers.

EDTV3[7:6] are undetermined and should be masked out by software. EDTV3[5] is reserved for future use and, for now, contains 0. The 3 LSBs of the EDTV waveform are currently not supported.

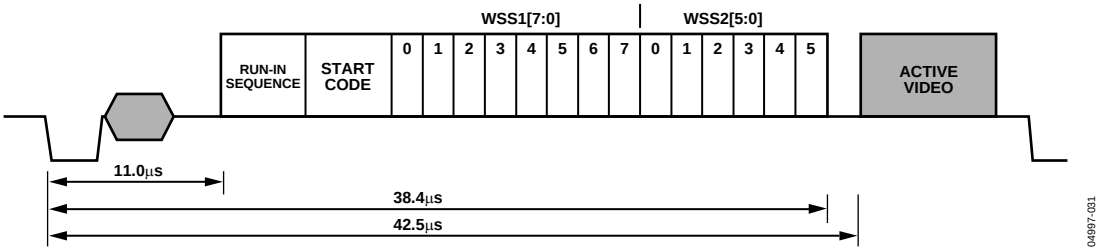


Figure 31. WSS Data Extraction

Table 58. WSS Access Information

Signal Name	Register Location	Address		Register Default Value
WSS1[7:0]	WSS 1[7:0]	145d	0x91	Readback Only
WSS2[5:0]	WSS 2[5:0]	146d	0x92	Readback Only

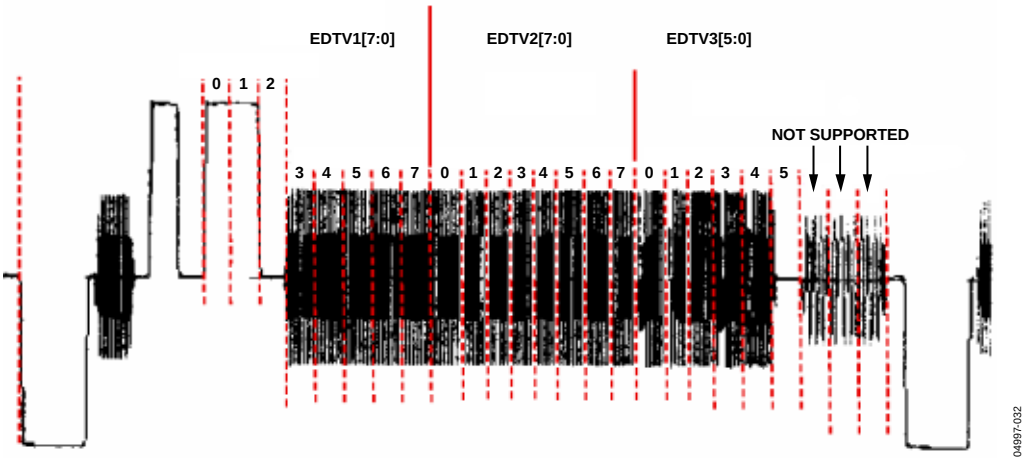


Figure 32. EDTV Data Extraction

Table 59. EDTV Access Information

Signal Name	Register Location	Address		Register Default Value
EDTV1[7:0]	EDTV 1[7:0]	147d	0x93	Readback only
EDTV2[7:0]	EDTV 2[7:0]	148d	0x94	Readback only
EDTV3[7:0]	EDTV 3[7:0]	149d	0x95	Readback only

CGMS Data Registers

CGMS1[7:0], Address 0x96[7:0],
CGMS2[7:0], Address 0x97[7:0],
CGMS3[7:0], Address 0x98[7:0]

Figure 33 shows the bit correspondence between the analog video waveform and the CGMS1/CGMS2/CGMS3 registers. CGMS3[7:4] are undetermined and should be masked out by software.

Closed Caption Data Registers

CCAP1[7:0], Address 0x99[7:0],
CCAP2[7:0], Address 0x9A[7:0]

Figure 34 shows the bit correspondence between the analog video waveform and the CCAP1/CCAP2 registers.

CCAP1[7] contains the parity bit from the first word. CCAP2[7] contains the parity bit from the second word.

Refer to the GDECAD Gemstar Decode Ancillary Data Format, Address 0x4C[0] section.

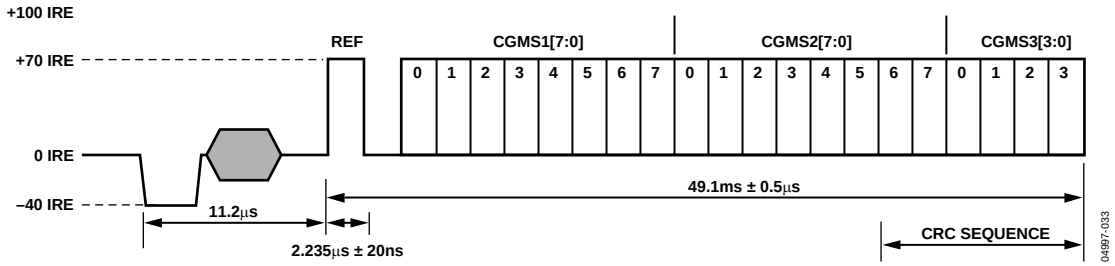


Figure 33. CGMS Data Extraction

Table 60. CGMS Access Information

Signal Name	Register Location	Address		Register Default Value
CGMS1[7:0]	CGMS 1[7:0]	150d	0x96	Readback only
CGMS2[7:0]	CGMS 2[7:0]	151d	0x97	Readback only
CGMS3[3:0]	CGMS 3[3:0]	152d	0x98	Readback only

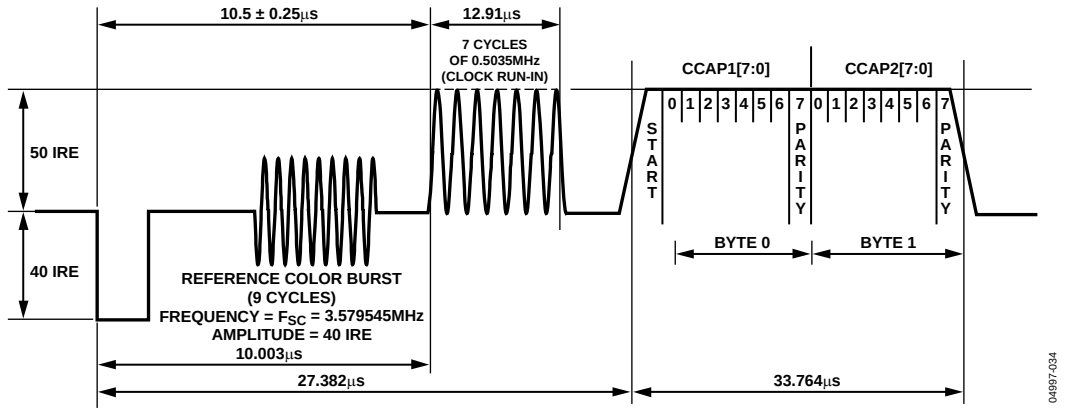


Figure 34. Closed Caption Data Extraction

Table 61. CCAP Access Information

Signal Name	Register Location	Address		Register Default Value
CCAP1[7:0]	CCAP1[7:0]	153d	0x99	Readback only
CCAP2[7:0]	CCAP2[7:0]	154d	0x9A	Readback only

Letterbox Detection

Incoming video signals may conform to different aspect ratios (16:9 wide screen of 4:3 standard). For certain transmissions in the wide screen format, a digital sequence (WSS) is transmitted with the video signal. If a WSS sequence is provided, the aspect ratio of the video can be derived from the digitally decoded bits WSS contains.

In the absence of a WSS sequence, letterbox detection may be used to find wide screen signals. The detection algorithm examines the active video content of lines at the start and end of a field. If black lines are detected, this indicates that the picture currently displayed is in wide screen format.

The active video content (luminance magnitude) over a line of video is summed together. At the end of a line, this accumulated value is compared with a threshold, and a decision is made as to whether or not a particular line is black. The threshold value needed depends on the type of input signal; some control is provided via LB_TH[4:0].

Detection at the Start of a Field

The ADV7183B expects a section of at least six consecutive black lines of video at the top of a field. Once those lines are detected, Register LB_LCT[7:0] reports back the number of black lines actually found. By default, the ADV7183B starts looking for those black lines in sync with the beginning of active video, for example, straight after the last VBI video line. LB_SL[3:0] allows the user to set the start of letterbox detection from the beginning of a frame on a line-by-line basis. The detection window closes in the middle of the field.

Detection at the End of a Field

The ADV7183B expects at least six continuous lines of black video at the bottom of a field before reporting back the number of lines actually found via the LB_LCB[7:0] value. The activity window for letterbox detection (end of field) starts in the middle of an active field. Its end is programmable via LB_EL[3:0].

Detection at the Midrange

Some transmissions of wide screen video include subtitles within the lower black box. If the ADV7183B finds at least two black lines followed by some more nonblack video, for example, the subtitle, and is then followed by the remainder of the bottom black block, it reports back a midcount via LB_LCM[7:0]. If no subtitles are found, LB_LCM[7:0] reports the same number as LB_LCB[7:0].

There is a 2-field delay in the reporting of any line count parameters.

There is no letterbox detected bit. The user is asked to read the LB_LCT[7:0] and LB_LCB[7:0] register values and to conclude whether or not the letterbox-type video is present in software.

LB_LCT[7:0] Letterbox Line Count Top, Address 0x9B[7:0], LB_LCM[7:0] Letterbox Line Count Mid, Address 0x9C[7:0], LB_LCB[7:0] Letterbox Line Count Bottom, Address 0x9D[7:0]

Table 62. LB_LCx Access Information

Signal Name	Address	Register Default Value
LB_LCT[7:0]	0x9B	Readback only
LB_LCM[7:0]	0x9C	Readback only
LB_LCB[7:0]	0x9D	Readback only

LB_TH[4:0] Letterbox Threshold Control, Address 0xDC[4:0]

Table 63. LB_TH Function

LB_TH[4:0]	Description
01100 (default)	Default threshold for detection of black lines
01101 to 10000	Increase threshold (need larger active video content before identifying nonblack lines)
00000 to 01011	Decrease threshold (even small noise levels can cause the detection of nonblack lines)

LB_SL[3:0] Letterbox Start Line, Address 0xDD[7:4]

The LB_SL[3:0] bits are set at 0100b by default. This means the letterbox detection window starts after the EDTV VBI data line. For an NTSC signal, this window is from Line 23 to Line 286.

Changing the bits to 0101, the detection window starts on Line 24 and ends on Line 287.

LB_EL[3:0] Letterbox End Line, Address 0xDD[3:0]

The LB_EL[3:0] bits are set at 1101b by default. This means the letterbox detection window ends with the last active video line. For an NTSC signal, this window is from Line 262 to Line 525.

Changing the bits to 1100, the detection window starts on Line 261 and ends on Line 254.

Gemstar Data Recovery

The Gemstar-compatible data recovery block (GSCD) supports 1× and 2× data transmissions. It can also serve as a closed caption decoder. Gemstar-compatible data transmissions can occur only in NTSC. Closed caption data can be decoded in both PAL and NTSC.

The block is configured via I^2C in the following ways:

- GDECEL[15:0] allow data recovery on selected video lines on even fields to be enabled and disabled.
- GDECOL[15:0] enable the data recovery on selected lines for odd fields.
- GDECAD configures the way in which data is embedded in the video data stream.

The recovered data is not available through I²C, but is inserted into the horizontal blanking period of an ITU-R BT656-compatible data stream. The data format is intended to comply with the recommendation by the International Telecommunications Union, ITU-R BT.1364. For more information, see the ITU website at www.itu.ch. See Figure 35.

The format of the data packet depends on the following criteria:

- Transmission is 1× or 2×.
- Data is output in 8-bit or 4-bit format (see the description of the GDECAD Gemstar Decode Ancillary Data Format, Address 0x4C[0] bit).
- Data is closed caption (CCAP) or Gemstar-compatible.

Data packets are output if the corresponding enable bit is set (see the GDECEL and GDECOL descriptions) and if the decoder detects the presence of data. This means that for video lines where no data has been decoded, no data packet is output even if the corresponding line enable bit is set.

Each data packet starts immediately after the EAV code of the preceding line. See Figure 35 and Table 64, which show the overall structure of the data packet.

Entries within the packet are as follows:

- Fixed preamble sequence of 0x00, 0xFF, 0xFF.
- Data identification word (DID). The value for the DID marking a Gemstar or CCAP data packet is 0x140 (10-bit value).
- Secondary data identification word (SDID) contains information about the video line from which data was retrieved, whether the Gemstar transmission was of 1× or 2× format, and whether it was retrieved from an even or odd field.
- Data count byte, giving the number of user data-words that follow.
- User data section.
- Optional padding to ensure the length of the user data-word section of a packet is a multiple of four bytes (requirement as set in ITU-R BT.1364).
- Checksum byte.

Table 64 lists the values within a generic data packet that is output by the ADV7183B in 8-bit format.

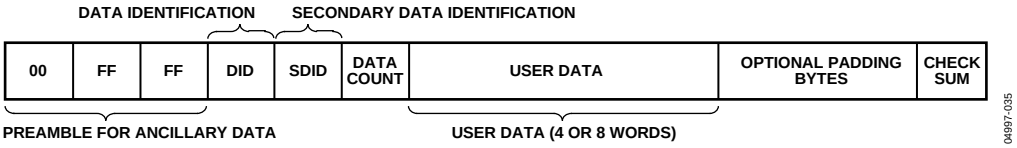


Figure 35. Gemstar and CCAP Embedded Data Packet (Generic)

Table 64. Generic Data Output Packet

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	!EP	EP	EF	2X	Line[3:0]				0	0	SDID
5	!EP	EP	0	0	0	0	DC[1]	DC[0]	0	0	Data count (DC)
6	!EP	EP	0	0	Word1[7:4]				0	0	User data-words
7	!EP	EP	0	0	Word1[3:0]				0	0	User data-words
8	!EP	EP	0	0	Word2[7:4]				0	0	User data-words
9	!EP	EP	0	0	Word2[3:0]				0	0	User data-words
10	!EP	EP	0	0	Word3[7:4]				0	0	User data-words
11	!EP	EP	0	0	Word3[3:0]				0	0	User data-words
12	!EP	EP	0	0	Word4[7:4]				0	0	User data-words
13	!EP	EP	0	0	Word4[3:0]				0	0	User data-words
14	!CS[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	0	0	Checksum

Table 65. Data Byte Allocation

2×	Raw Information Bytes Retrieved from the Video Line	GDECAD	User Data-Words (Including Padding)	Padding Bytes	DC[1:0]
1	4	0	8	0	10
1	4	1	4	0	01
0	2	0	4	0	01
0	2	1	4	2	01

Gemstar Bit Names

- DID. The data identification value is 0x140 (10-bit value). Care has been taken that in 8-bit systems, the two LSBs do not carry vital information.
- EP and !EP. The EP bit is set to ensure even parity on the data-word D[8:0]. Even parity means there will always be an even number of 1s within the D[8:0] bit arrangement. This includes the EP bit. !EP describes the logic inverse of EP and is output on D[9]. The !EP is output to ensure that the reserved codes of 00 and FF cannot happen.
- EF. Even field identifier. EF = 1 indicates that the data was recovered from a video line on an even field.
- 2X. This bit indicates whether the data sliced was in Gemstar 1× or 2× format. A high indicates 2× format.
- Line[3:0]. This entry provides a code that is unique for each of the possible 16 source lines of video from which Gemstar data can be retrieved. Refer to Table 74 and Table 75.
- DC[1:0]. Data count value. The number of user data-words in the packet divided by 4. The number of user data-words (UDW) in any packet must be an integral number of 4. Padding is required at the end, if necessary, as set in ITU-R BT.1364. See Table 65.
- The 2X bit determines whether the raw information retrieved from the video line was 2 or 4 bytes. The state of the GDECAD bit affects whether the bytes are transmitted straight (that is, two bytes transmitted as two bytes) or whether they are split into nibbles (that is, two bytes transmitted as four half bytes). Padding bytes are then added where necessary.
- CS[8:2]. The checksum is provided to determine the integrity of the ancillary data packet. It is calculated by summing up D[8:2] of DID, SDID, the Data Count byte, and all UDWs, and ignoring any overflow during the summation. Since all data bytes that are used to calculate the checksum have their two LSBs set to 0, the CS[1:0] bits are also always 0.

  !CS[8] describes the logic inversion of CS[8]. The value !CS[8] is included in the checksum entry of the data packet to ensure the reserved values of 0x00 and 0xFF do not occur.

Table 66 to Table 71 outline the possible data packages.

Gemstar 2× Format, Half-Byte Output Mode

Half-byte output mode is selected by setting CDECAD = 0; full-byte output mode is selected by setting CDECAD = 1. See the GDECAD Gemstar Decode Ancillary Data Format, Address 0x4C[0] section.

Gemstar 1× Format

Half-byte output mode is selected by setting CDECAD = 0; full-byte output mode is selected by setting CDECAD = 1. See the GDECAD Gemstar Decode Ancillary Data Format, Address 0x4C[0] section.

Table 66. Gemstar 2× Data, Half-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	!EP	EP	EF	**1**	Line[3:0]				0	0	SDID
5	!EP	EP	0	0	0	0	**1**	**0**	0	0	Data count
6	!EP	EP	0	0	Gemstar Word1[7:4]				0	0	User data-words
7	!EP	EP	0	0	Gemstar Word1[3:0]				0	0	User data-words
8	!EP	EP	0	0	Gemstar Word2[7:4]				0	0	User data-words
9	!EP	EP	0	0	Gemstar Word2[3:0]				0	0	User data-words
10	!EP	EP	0	0	Gemstar Word3[7:4]				0	0	User data-words
11	!EP	EP	0	0	Gemstar Word3[3:0]				0	0	User data-words
12	!EP	EP	0	0	Gemstar Word4[7:4]				0	0	User data-words
13	!EP	EP	0	0	Gemstar Word4[3:0]				0	0	User data-words
14	!CS[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 67. Gemstar 2× Data, Full-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	!EP	EP	EF	**1**	Line[3:0]				0	0	SDID
5	!EP	EP	0	0	0	0	**0**	**1**	0	0	Data count
6	Gemstar Word1[7:0]								0	0	User data-words
7	Gemstar Word2[7:0]								0	0	User data-words
8	Gemstar Word3[7:0]								0	0	User data-words
9	Gemstar Word4[7:0]								0	0	User data-words
10	!CS[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 68. Gemstar 1× Data, Half-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	!EP	EP	EF	**0**	Line[3:0]				0	0	SDID
5	!EP	EP	0	0	0	0	**0**	**1**	0	0	Data count
6	!EP	EP	0	0	Gemstar Word1[7:4]				0	0	User data-words
7	!EP	EP	0	0	Gemstar Word1[3:0]				0	0	User data-words
8	!EP	EP	0	0	Gemstar Word2[7:4]				0	0	User data-words
9	!EP	EP	0	0	Gemstar Word2[3:0]				0	0	User data-words
10	!CS[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 69. Gemstar 1× Data, Full-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	!EP	EP	EF	**0**	Line[3:0]				0	0	SDID
5	!EP	EP	0	0	0	0	**0**	**1**	0	0	Data count
6	Gemstar Word1[7:0]								0	0	User data-words
7	Gemstar Word2[7:0]								0	0	User data-words
8	1	0	0	0	0	0	0	0	0	0	UDW padding 0x200
9	1	0	0	0	0	0	0	0	0	0	UDW padding 0x200
10	!CS[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 70. NTSC CCAP Data, Half-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	!EP	EP	EF	**0**	**1**	**0**	**1**	**1**	0	0	SDID
5	!EP	EP	0	0	0	0	**0**	**1**	0	0	Data count
6	!EP	EP	0	0	CCAP Word1[7:4]				0	0	User data-words
7	!EP	EP	0	0	CCAP Word1[3:0]				0	0	User data-words
8	!EP	EP	0	0	CCAP Word2[7:4]				0	0	User data-words
9	!EP	EP	0	0	CCAP Word2[3:0]				0	0	User data-words
10	!CS[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 71. NTSC CCAP Data, Full-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	!EP	EP	EF	**0**	**1**	**0**	**1**	**1**	0	0	SDID
5	!EP	EP	0	0	0	0	**0**	**1**	0	0	Data count
6	CCAP Word1[7:0]								0	0	User data-words
7	CCAP Word2[7:0]								0	0	User data-words
8	1	0	0	0	0	0	0	0	0	0	UDW padding 0x200
9	1	0	0	0	0	0	0	0	0	0	UDW padding 0x200
10	!CS[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

NTSC CCAP Data

Half-byte output mode is selected by setting CDECAD = 0; the full-byte mode is enabled by CDECAD = 1. See the GDECAD Gemstar Decode Ancillary Data Format, Address 0x4C[0] section. The data packet formats are shown in Table 72 and Table 73.

Only closed caption data can be embedded in the output data stream.

NTSC closed caption data is sliced on Line 21d on even and odd fields. The corresponding enable bit has to be set high. See the and the GDECOL[15:0] Gemstar Decoding Odd Lines, Address 0x4A[7:0]; Address 0x4B[7:0] sections.

PAL CCAP Data

Half-byte output mode is selected by setting CDECAD = 0; full-byte output mode is selected by setting CDECAD = 1. See the GDECAD Gemstar Decode Ancillary Data Format, Address 0x4C[0] section.

Table 72 and Table 73 list the bytes of the data packet.

Only closed caption data can be embedded in the output data stream. PAL closed caption data is sliced from Line 22 and Line 335. The corresponding enable bits have to be set.

See the GDECAD Gemstar Decode Ancillary Data Format, Address 0x4C[0] and GDECOL[15:0] Gemstar Decoding Odd Lines, Address 0x4A[7:0]; Address 0x4B[7:0] sections.

Table 72. PAL CCAP Data, Half-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	!EP	EP	EF	**0**	**1**	**0**	**1**	**0**	0	0	SDID
5	!EP	EP	0	0	0	0	**0**	**1**	0	0	Data count
6	!EP	EP	0	0	CCAP Word1[7:4]				0	0	User data-words
7	!EP	EP	0	0	CCAP Word1[3:0]				0	0	User data-words
8	!EP	EP	0	0	CCAP Word2[7:4]				0	0	User data-words
9	!EP	EP	0	0	CCAP Word2[3:0]				0	0	User data-words
10	!CS[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

Table 73. PAL CCAP Data, Full-Byte Mode

Byte	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]	Description
0	0	0	0	0	0	0	0	0	0	0	Fixed preamble
1	1	1	1	1	1	1	1	1	1	1	Fixed preamble
2	1	1	1	1	1	1	1	1	1	1	Fixed preamble
3	0	1	0	1	0	0	0	0	0	0	DID
4	!EP	EP	EF	**0**	**1**	**0**	**1**	**0**	0	0	SDID
5	!EP	EP	0	0	0	0	**0**	**1**	0	0	Data count
6	CCAP Word1[7:0]								0	0	User data-words
7	CCAP Word2[7:0]								0	0	User data-words
8	1	0	0	0	0	0	0	0	0	0	UDW padding 0x200
9	1	0	0	0	0	0	0	0	0	0	UDW padding 0x200
10	!CS[8]	CS[8]	CS[7]	CS[6]	CS[5]	CS[4]	CS[3]	CS[2]	CS[1]	CS[0]	Checksum

GDECEL[15:0] Gemstar Decoding Even Lines, Address 0x48[7:0]; Address 0x49[7:0]

The 16 bits of the GDECEL[15:0] are interpreted as a collection of 16 individual line decode enable signals. Each bit refers to a line of video in an even field. Setting the bit enables the decoder block trying to find Gemstar or closed caption-compatible data on that particular line. Setting the bit to 0 prevents the decoder from trying to retrieve data. See Table 74 and Table 75.

To retrieve closed caption data services on NTSC (Line 284), GDECEL[11] must be set.

To retrieve closed caption data services on PAL (Line 335), GDECEL[14] must be set.

The default value of GDECEL[15:0] is 0x0000. This setting instructs the decoder not to attempt to decode Gemstar or CCAP data from any line in the even field.

GDECOL[15:0] Gemstar Decoding Odd Lines, Address 0x4A[7:0]; Address 0x4B[7:0]

The 16 bits of the GDECOL[15:0] form a collection of 16 individual line decode enable signals. See Table 74 and Table 75.

To retrieve closed caption data services on NTSC (Line 21), GDECOL[11] must be set.

To retrieve closed caption data services on PAL (Line 22), GDECOL[14] must be set.

The default value of GDECOL[15:0] is 0x0000. This setting instructs the decoder not to attempt to decode Gemstar or CCAP data from any line in the odd field.

GDECAD Gemstar Decode Ancillary Data Format, Address 0x4C[0]

The decoded data from Gemstar-compatible transmissions or closed caption is inserted into the horizontal blanking period of the respective line of video. There is a potential problem if the retrieved data bytes have the value 0x00 or 0xFF. In an ITU-R BT.656-compatible data stream, those values are reserved and used only to form a fixed preamble.

The GDECAD bit allows the data to be inserted into the horizontal blanking period in two ways:

- Insert all data straight into the data stream, even the reserved values of 0x00 and 0xFF, if they occur. This can violate the output data format specification ITU-R BT.1364.
- Split all data into nibbles and insert the half-bytes over double the number of cycles in a 4-bit format.

When GDECAD is 0, the data is split into half-bytes and inserted (default).

When GDECAD is 1, the data is output straight in 8-bit format.

Table 74. NTSC Line Enable Bits and Corresponding Line Numbering

Line[3:0]	Line Number (ITU-R BT.470)	Enable Bit	Comment
0	10	GDECOL[0]	Gemstar
1	11	GDECOL[1]	Gemstar
2	12	GDECOL[2]	Gemstar
3	13	GDECOL[3]	Gemstar
4	14	GDECOL[4]	Gemstar
5	15	GDECOL[5]	Gemstar
6	16	GDECOL[6]	Gemstar
7	17	GDECOL[7]	Gemstar
8	18	GDECOL[8]	Gemstar
9	19	GDECOL[9]	Gemstar
10	20	GDECOL[10]	Gemstar
11	21	GDECOL[11]	Gemstar or closed caption
12	22	GDECOL[12]	Gemstar
13	23	GDECOL[13]	Gemstar
14	24	GDECOL[14]	Gemstar
15	25	GDECOL[15]	Gemstar
0	273 (10)	GDECEL[0]	Gemstar
1	274 (11)	GDECEL[1]	Gemstar
2	275 (12)	GDECEL[2]	Gemstar
3	276 (13)	GDECEL[3]	Gemstar
4	277 (14)	GDECEL[4]	Gemstar
5	278 (15)	GDECEL[5]	Gemstar
6	279 (16)	GDECEL[6]	Gemstar
7	280 (17)	GDECEL[7]	Gemstar
8	281 (18)	GDECEL[8]	Gemstar
9	282 (19)	GDECEL[9]	Gemstar
10	283 (20)	GDECEL[10]	Gemstar
11	284 (21)	GDECEL[11]	Gemstar or closed caption
12	285 (22)	GDECEL[12]	Gemstar
13	286 (23)	GDECEL[13]	Gemstar
14	287 (24)	GDECEL[14]	Gemstar
15	288 (25)	GDECEL[15]	Gemstar

Table 75. PAL Line Enable Bits and Corresponding Line Numbering

Line[3:0]	Line Number (ITU-R BT.470)	Enable Bit	Comment
12	8	GDECOL[0]	Not valid
13	9	GDECOL[1]	Not valid
14	10	GDECOL[2]	Not valid
15	11	GDECOL[3]	Not valid
0	12	GDECOL[4]	Not valid
1	13	GDECOL[5]	Not valid
2	14	GDECOL[6]	Not valid
3	15	GDECOL[7]	Not valid
4	16	GDECOL[8]	Not valid
5	17	GDECOL[9]	Not valid
6	18	GDECOL[10]	Not valid
7	19	GDECOL[11]	Not valid
8	20	GDECOL[12]	Not valid
9	21	GDECOL[13]	Not valid
10	**22**	**GDECOL[14]**	**Closed caption**
11	23	GDECOL[15]	Not valid
12	321 (8)	GDECEL[0]	Not valid
13	322 (9)	GDECEL[1]	Not valid
14	323 (10)	GDECEL[2]	Not valid
15	324 (11)	GDECEL[3]	Not valid
0	325 (12)	GDECEL[4]	Not valid
1	326 (13)	GDECEL[5]	Not valid
2	327 (14)	GDECEL[6]	Not valid
3	328 (15)	GDECEL[7]	Not valid
4	329 (16)	GDECEL[8]	Not valid
5	330 (17)	GDECEL[9]	Not valid
6	331 (18)	GDECEL[10]	Not valid
7	332 (19)	GDECEL[11]	Not valid
8	333 (20)	GDECEL[12]	Not valid
9	334 (21)	GDECEL[13]	Not valid
10	**335 (22)**	**GDECEL[14]**	**Closed caption**
11	336 (23)	GDECEL[15]	Not valid

IF Compensation Filter

IF FILTSEL[2:0] IF Filter Select Address 0xF8[2:0]

The IF FILTSEL[2:0] register allows the user to compensate for SAW filter characteristics on a composite input as observed on tuner outputs. Figure 36 and Figure 37 show IF filter compensation for NTSC and PAL.

The options for this feature are as follows:

- Bypass mode (default)
- NTSC—consists of three filter characteristics
- PAL—consists of three filter characteristics

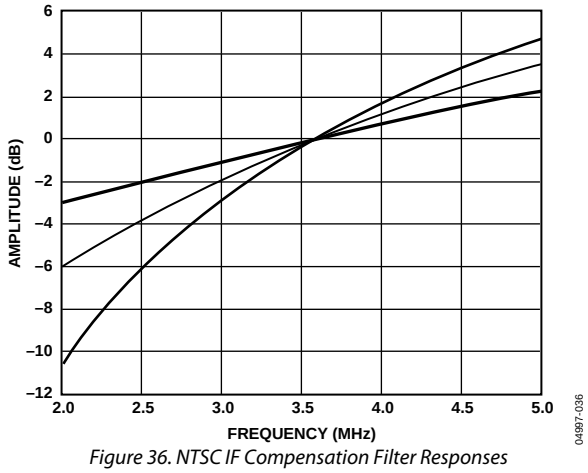


Figure 36. NTSC IF Compensation Filter Responses

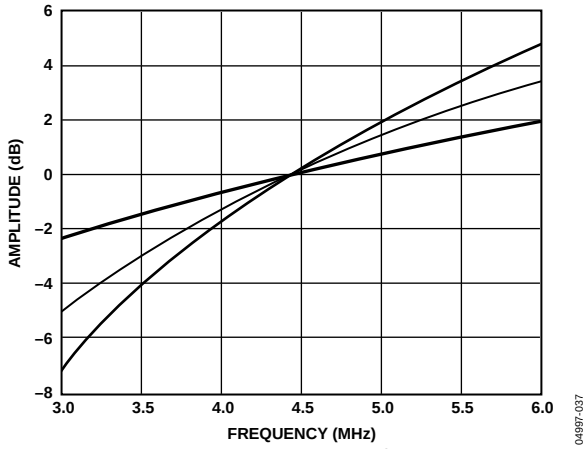


Figure 37. PAL IF Compensation Filter Responses

See Table 86 for programming details.

I²C Interrupt System

The ADV7183B has a comprehensive interrupt register set. This map is located in Register Access Page 2. See Table 84 for details of the interrupt register map.

How to access this map is described in Figure 38.

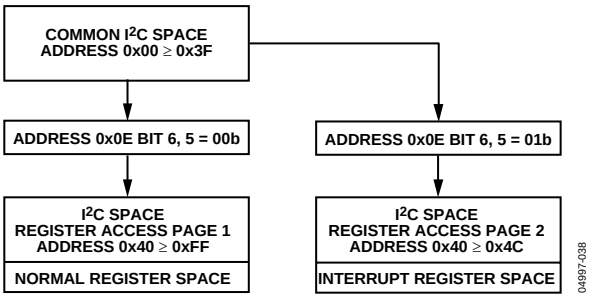


Figure 38. Register Access —Page 1 and Page 2

Interrupt Request Output Operation

When an interrupt event occurs, the interrupt pin $\overline{\text{INTRQ}}$ goes low with a programmable duration given by INTRQ_DUR_SEL[1:0]

INTRQ_DURSEL[1:0], Interrupt Duration Select Address 0x40 (Interrupt Space)[7:6]
Table 76. INTRQ_DUR_SEL

INTRQ_DURSEL[1:0]	Description
00 (default)	3 Xtal periods
01	15 Xtal periods
10	63 Xtal periods
11	Active until cleared

When the active until cleared interrupt duration is selected and the event that caused the interrupt is no longer in force, the interrupt persists until it is masked or cleared.

For example, if the ADV7183B loses lock, an interrupt is generated and $\overline{\text{INTRQ}}$ pin goes low. If the ADV7183B returns to the locked state, $\overline{\text{INTRQ}}$ continues to drive low until the SD_LOCK bit is either masked or cleared.

Interrupt Drive Level

The ADV7183B resets with open drain enabled and all interrupts masked off. Therefore, $\overline{\text{INTRQ}}$ is in a high impedance state after reset. 01 or 10 has to be written to INTRQ_OP_SEL[1:0] for a logic level to be driven out from the $\overline{\text{INTRQ}}$ pin.

It is also possible to write to a register in the ADV7183B that manually asserts the $\overline{\text{INTRQ}}$ pin. This bit is MPU_STIM_INTRQ.

INTRQ_OP_SEL[1:0], Interrupt Duration Select Address 0x40 (Interrupt Space)[1:0]
Table 77. INTRQ_OP_SEL

INTRQ_OP_SEL[1:0]	Description
00 (default)	Open drain
01	Drive low when active
10	Drive high when active
11	Reserved

Multiple Interrupt Events

If Interrupt Event 1 occurs and then Interrupt Event 2 occurs before the system controller has cleared or masked Interrupt Event 1, the ADV7183B will not generate a second interrupt signal. The system controller should check all unmasked interrupt status bits, as more than one can be active.

Macrovision Interrupt Selection Bits

The user can select between pseudo sync pulse and color stripe detection as shown in this section.

MV_INTRQ_SEL[1:0], Macrovision Interrupt Selection Bits Address 0x40 (Interrupt Space)[5:4]
Table 78. MV_INTRQ_SEL

MV_INTRQ_SEL[1:0]	Description
00	Reserved
01 (default)	Pseudo sync only
10	Color stripe only
11	Either pseudo sync or color stripe

Additional information relating to the interrupt system is detailed in Table 84.

PIXEL PORT CONFIGURATION

The ADV7183B has a very flexible pixel port that can be configured in a variety of formats to accommodate downstream ICs. Table 79 and Table 80 summarize the various functions that the ADV7183B's pins can have in different modes of operation.

The ordering of components (for example, Cr versus Cb, CHA/B/C) can be changed. Refer to the section. Table 79 indicates the default positions for the Cr/Cb components.

OF_SEL[3:0] Output Format Selection, Address 0x03[5:2]

The modes in which the ADV7183B pixel port can be onfigured are under the control of OF_SEL[3:0]. See Table 80 for details.

The default LLC frequency output on the LLC1 pin is approximately 27 MHz. For modes that operate with a nominal data rate of 13.5 MHz (0001, 0010), the clock frequency on the LLC1 pin stays at the higher rate of 27 MHz. For information on outputting the nominal 13.5 MHz clock on the LLC1 pin, see the PAD_SEL[2:0], Address 0x8F[6:4] section.

SWPC Swap Pixel Cr/Cb, Address 0x27[7]

This bit allows Cr and Cb samples to be swapped.

When SWPC is 0 (default), no swapping is allowed.

When SWPC is 1, the Cr and Cb values can be swapped.

PAD_SEL[2:0], Address 0x8F[6:4]

This I^2C write allows the user to select between the LLC1 (nominally at 27 MHz) and LLC2 (nominally at 13.5 MHz).

The LLC2 signal is useful for LLC2-compatible wide bus (16-bit) output modes. See the OF_SEL[3:0] Output Format Selection, Address 0x03[5:2] section for additional information. The LLC2 signal and data on the data bus are synchronized. By default, the rising edge of LLC1/LLC2 is aligned with the Y data; the falling edge occurs when the data bus holds C data. The polarity of the clock, and therefore the Y/C assignments to the clock edges, can be altered by using the Polarity LLC pin.

When LLC_PAD_SEL[2:0] is 000 (default), the output is nominally 27 MHz LLC on the LLC1 pin.

When LLC_PAD_SEL[2:0] is 101, the output is nominally 13.5 MHz LLC on the LLC1 pin.

Table 79. P15 to P0 Output/Input Pin Mapping

	Data Port Pins P[15:0]															
Format, and Mode	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Video Out, 8-Bit, 4:2:2	YCrCb[7:0] OUT															
Video Out, 16-Bit, 4:2:2	Y[7:0] OUT								CrCb[7:0] OUT							

Table 80. Standard Definition Pixel Port Modes

		P[15: 0]	
OF_SEL[3:0]	**Format**	**P[15:8]**	**P[7: 0]**
0010	16-bit @ LLC2 4:2:2	Y[7:0]	CrCb[7:0]
0011 (default)	8-bit @ LLC1 4:2:2 (default)	YCrCb[7:0] (default)	Three-state
0110-1111	Reserved	Reserved. Do not use.	

MPU PORT DESCRIPTION

The ADV7183B supports a 2-wire (I^2C-compatible) serial interface. Two inputs, serial data (SDA) and serial clock (SCLK), carry information between the ADV7183B and the system I^2C master controller. Each slave device is recognized by a unique address. The ADV7183B's I^2C port allows the user to set up and configure the decoder and to read back captured VBI data. The ADV7183B has two possible slave addresses for both read and write operations, depending on the logic level on the ALSB pin. These four unique addresses are shown in Table 81. The ADV7183B's ALSB pin controls Bit 1 of the slave address. By altering the ALSB, it is possible to control two ADV7183Bs in an application without having a conflict with the same slave address. The LSB (Bit 0) sets either a read or write operation. Logic 1 corresponds to a read operation; Logic 0 corresponds to a write operation.

Table 81. I^2C Address for the ADV7183B

ALSB	R/W	Slave Address
0	0	0x40
0	1	0x41
1	0	0x42
1	1	0x43

To control the device on the bus, a specific protocol must be followed. First, the master initiates a data transfer by establishing a start condition, which is defined by a high-to-low transition on SDA while SCLK remains high. This indicates that an address/data stream will follow. All peripherals respond to the start condition and shift the next eight bits (7-bit address + R/W bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse; this is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDA and SCLK lines, waiting for the start condition and the correct transmitted address. The R/W bit determines the direction of the data. Logic 0 on the LSB of the first byte means the master writes information to the peripheral. Logic 1 on the LSB of the first byte means the master reads information from the peripheral.

The ADV7183B acts as a standard slave device on the bus. The data on the SDA pin is eight bits long, supporting the 7-bit addresses and the R/W bit. The ADV7183B has 249 subaddresses to enable access to the internal registers. It therefore interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, which allows data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCLK high period, the user should only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued by the user, the ADV7183B does not issue an acknowledge and returns to the idle condition.

If the user exceeds the highest subaddress in auto-increment mode, the following occurs:

- In read mode, the highest subaddress register contents continue to be output until the master device issues a no-acknowledge. This indicates the end of a read. A no acknowledge condition is where the SDA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the ADV7183B, and the part returns to the idle condition.

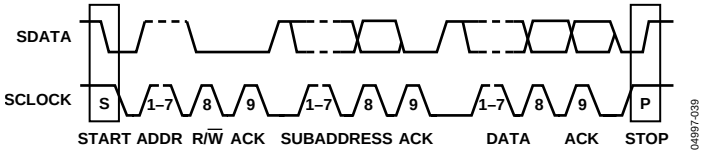


Figure 39. Bus Data Transfer

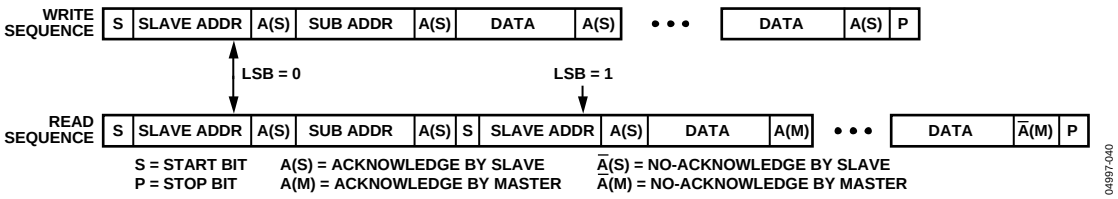


Figure 40. Read and Write Sequence

REGISTER ACCESSES

The MPU can write to or read from most of the ADV7183B's registers, except the registers that are read only or write only. The subaddress register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the subaddress register. Next, a read/write operation is performed from/to the target address, which then increments to the next address until a stop command on the bus is performed.

REGISTER PROGRAMMING

This section describes the configuration of each register. The communications register is an 8-bit, write only register. After the part has been accessed over the bus and a read/write operation is selected, the subaddress is set up. The subaddress register determines to/from which register the operation takes place. Table 82 lists the various operations under the control of the subaddress register for the control port.

Register Select (SR7 to SR0)

These bits are set up to point to the required starting address.

I²C SEQUENCER

An I²C sequencer is used when a parameter exceeds eight bits and is, therefore, distributed over two or more I²C registers, such as HSB[11:0].

When such a parameter is changed using two or more I²C write operations, the parameter can hold an invalid value for the time between the first I²C completion and the last I²C completion. This means, the top bits of the parameter can already hold the new value while the remaining bits of the parameter still hold the previous value.

To avoid this problem, the I²C sequencer holds the already updated bits of the parameter in local memory; all bits of the parameter are updated together once the last register write operation has completed.

The correct operation of the I²C sequencer relies on the following:

- All I²C registers for the target parameter must be written to in order of ascending addresses. For example, for HSB[10:0], write to Address 0x34 first, followed by 0x35.
- No other I²C can take place between the two (or more) I²C writes for the sequence. For example, for HSB[10:0], write to Address 0x34 first, immediately followed by 0x35.

IP2PC REGISTER MAPS

Table 82. Common and Normal (Page 1) Register Map Details

Register Name	Reset Value	rw	Subaddress	
			Dec	Hex
Input Control	0000 0000	rw	0	0x00
Video Selection	1100 1000	rw	1	0x01
Reserved	0000 0100	rw	2	0x02
Output Control	0000 1100	rw	3	0x03
Extended Output Control	01xx 0101	rw	4	0x04
Reserved	0000 0000	rw	5	0x05
Reserved	0000 0010	rw	6	0x06
Autodetect Enable	0111 1111	rw	7	0x07
Contrast	1000 0000	rw	8	0x08
Reserved	1000 0000	rw	9	0x09
Brightness	0000 0000	rw	10	0x0A
Hue	0000 0000	rw	11	0x0B
Default Value Y	0011 0110	rw	12	0x0C
Default Value C	0111 1100	rw	13	0x0D
ADI Control	0000 0000	rw	14	0x0E
Power Management	0000 0000	rw	15	0x0F
Status 1	xxxx xxxx	r	16	0x10
Ident	xxxx xxxx	r	17	0x11
Status 2	xxxx xxxx	r	18	0x12
Status 3	xxxx xxxx	r	19	0x13
Analog Clamp Control	0001 0010	rw	20	0x14
Digital Clamp Control 1	0100 xxxx	rw	21	0x15
Reserved	xxxx xxxx	rw	22	0x16
Shaping Filter Control	0000 0001	rw	23	0x17
Shaping Filter Control 2	1001 0011	rw	24	0x18
Comb Filter Control	1111 0001	rw	25	0x19
Reserved	xxxx xxxx	rw	26 to 28	0x1A to 0x1C
ADI Control 2	0000 0xxx	rw	29	0x1D
Reserved	xxxx xxxx	rw	30 to 38	0x1E to 0x26
Pixel Delay Control	0101 1000	rw	39	0x27
Reserved	xxxx xxxx	rw	40 to 42	0x28 to 0x2A
Misc Gain Control	1110 0001	rw	43	0x2B
AGC Mode Control	1010 1110	rw	44	0x2C
Chroma Gain Control 1	1111 0100	rw	45	0x2D
Chroma Gain Control 2	0000 0000	rw	46	0x2E
Luma Gain Control 1	1111 xxxx	rw	47	0x2F
Luma Gain Control 2	xxxx xxxx	rw	48	0x30
Vsync Field Control 1	0001 0010	rw	49	0x31
Vsync Field Control 2	0100 0001	rw	50	0x32
Vsync Field Control 3	1000 0100	rw	51	0x33
Hsync Position Control 1	0000 0000	rw	52	0x34
Hsync Position Control 2	0000 0010	rw	53	0x35
Hsync Position Control 3	0000 0000	rw	54	0x36
Polarity	0000 0001	rw	55	0x37
NTSC Comb Control	1000 0000	rw	56	0x38
PAL Comb Control	1100 0000	rw	57	0x39
ADC Control	0001 0000	rw	58	0x3A
Reserved	xxxx xxxx	rw	59 to 60	0x3B to 0x3C
Manual Window Control	0100 0011	rw	61	0x3D

Register Name	Reset Value	rw	Subaddress	
			Dec	Hex
Reserved	xxxx xxxx	rw	62 to 64	0x3E to 0x40
Resample Control	0100 0001	rw	65	0x41
Reserved	xxxx xxxx	rw	66 to 71	0x42 to 0x47
Gemstar Ctrl 1	00000000	rw	72	0x48
Gemstar Ctrl 2	0000 0000	rw	73	0x49
Gemstar Ctrl 3	0000 0000	rw	74	0x4A
Gemstar Ctrl 4	0000 0000	rw	75	0x4B
GemStar Ctrl 5	xxxx xxx0	rw	76	0x4C
CTI DNR Ctrl 1	1110 1111	rw	77	0x4D
CTI DNR Ctrl 2	0000 1000	rw	78	0x4E
Reserved	xxxx xxxx	rw	79	0x4F
CTI DNR Ctrl 4	0000 1000	rw	80	0x50
Lock Count	0010 0100	rw	81	0x51
Reserved	xxxx xxxx	rw	82 to 142	0x52 to 0x8E
Free-Run Line Length 1	0000 0000	w	143	0x8F
Reserved	0000 0000	w	144	0x90
VBI Info	xxxx xxxx	r	144	0x90
WSS 1	xxxx xxxx	r	145	0x91
WSS 2	xxxx xxxx	r	146	0x92
EDTV 1	xxxx xxxx	r	147	0x93
EDTV 2	xxxx xxxx	r	148	0x94
EDTV 3	xxxx xxxx	r	149	0x95
CGMS 1	xxxx xxxx	r	150	0x96
CGMS 2	xxxx xxxx	r	151	0x97
CGMS 3	xxxx xxxx	r	152	0x98
CCAP1	xxxx xxxx	r	153	0x99
CCAP2	xxxx xxxx	r	154	0x9A
Letterbox 1	xxxx xxxx	r	155	0x9B
Letterbox 2	xxxx xxxx	r	156	0x9C
Letterbox 3	xxxx xxxx	r	157	0x9D
Reserved	xxxx xxxx	rw	158 to 177	0x9E to 0xB1
CRC Enable	0001 1100	w	178	0xB2
Reserved	xxxx xxxx	rw	179 to 194	0xB2 to 0xC2
ADC Switch 1	xxxx xxxx	rw	195	0xC3
ADC Switch 2	0xxx xxxx	rw	196	0xC4
Reserved	xxxx xxxx	rw	197 to 219	0xC5 to 0xDB
Letterbox Control 1	1010 1100	rw	220	0xDC
Letterbox Control 2	0100 1100	rw	221	0xDD
Reserved	0000 0000	rw	222	0xDE
Reserved	0000 0000	rw	223	0xDF
Reserved	0001 0100	rw	224	0xE0
SD Offset Cb	1000 0000	rw	225	0xE1
SD Offset Cr	1000 0000	rw	226	0xE2
SD Saturation Cb	1000 0000	rw	227	0xE3
SD Saturation Cr	1000 0000	rw	228	0xE4
NTSC V Bit Begin	0010 0101	rw	229	0xE5
NTSC V Bit End	0000 0100	rw	230	0xE6
NTSC F Bit Toggle	0110 0011	rw	231	0xE7
PAL V Bit Begin	0110 0101	rw	232	0xE8
PAL V Bit End	0001 0100	rw	233	0xE9
PAL F Bit Toggle	0110 0011	rw	234	0xEA
Reserved	xxxx xxxx	rw	235 to 243	0xEB to 0xF3

Register Name	Reset Value	rw	Subaddress	
			Dec	Hex
Drive Strength	xx01 0101	rw	244	0xF4
Reserved	xxxx xxxx	rw	245 to 247	0xF5 to 0xF7
IF Comp Control	0000 0000	rw	248	0xF8
VS Mode Control	0000 0000	rw	249	0xF9

Table 83. Common and Normal (Page 1) Register Map Bit Names

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Input Control	VID_SEL.3	VID_SEL.2	VID_SEL.1	VID_SEL.0	INSEL.3	INSEL.2	INSEL.1	INSEL.0
Video Selection		ENHSPLL	BETACAM		ENVSPROC			
Reserved								
Output Control	VBI_EN	TOD	OF_SEL.3	OF_SEL.2	OF_SEL.1	OF_SEL.0		SD_DUP_AV
Extended Output Control	BT656-4				TIM_OE	BL_C_VBI	EN_SFL_PI	RANGE
Reserved								
Reserved								
Autodetect Enable	AD_SEC525_EN	AD_SECAM_EN	AD_N443_EN	AD_P60_EN	AD_PALN_EN	AD_PALM_EN	AD_NTSC_EN	AD_PAL_EN
Contrast	CON.7	CON.6	CON.5	CON.4	CON.3	CON.2	CON.1	CON.0
Reserved								
Brightness	BRI.7	BRI.6	BRI.5	BRI.4	BRI.3	BRI.2	BRI.1	BRI.0
Hue	HUE.7	HUE.6	HUE.5	HUE.4	HUE.3	HUE.2	HUE.1	HUE.0
Default Value Y	DEF_Y.5	DEF_Y.4	DEF_Y.3	DEF_Y.2	DEF_Y.1	DEF_Y.0	DEF_VAL_ AUTO_EN	DEF_VAL_EN
Default Value C	DEF_C.7	DEF_C.6	DEF_C.5	DEF_C.4	DEF_C.3	DEF_C.2	DEF_C.1	DEF_C.0
ADI Control				SUB_USR_EN.0				
Power Management	RES		PWRDN			PDBP		
Status 1	COL_KILL	AD_RESULT.2	AD_RESULT.1	AD_RESULT.0	FOLLOW_PW	FSC_LOCK	LOST_LOCK	IN_LOCK
Ident	IDENT.7	IDENT.6	IDENT.5	IDENT.4	IDENT.3	IDENT.2	IDENT.1	IDENT.0
Status 2			FSC NSTD	LL NSTD	MV AGC DET	MV PS DET	MVCS T3	MVCS DET
Status 3	PAL SW LOCK	INTERLACE	STD FLD LEN	FREE_RUN_ACT		SD_OP_50HZ	GEMD	INST_HLOCK
Analog Clamp Control				CCLEN				
Digital Clamp Control 1		DCT.1	DCT.0					
Reserved								
Shaping Filter Control	CSFM.2	CSFM.1	CSFM.0	YSFM.4	YSFM.3	YSFM.2	YSFM.1	YSFM.0
Shaping Filter Control 2	WYSFMOVR			WYSFM.4	WYSFM.3	WYSFM.2	WYSFM.1	WYSFM.0
Comb Filter Control					NSFSEL.1	NSFSEL.0	PSFSEL.1	PSFSEL.0
Reserved								
ADI Control 2	TRI_LLC	EN28XTAL	VS_JIT_ COMP_EN					
Reserved								
Pixel Delay Control	SWPC	AUTO_PDC_EN	CTA.2	CTA.1	CTA.0		LTA.1	LTA.0
Reserved								
Misc Gain Control		CKE						PW_UPD
AGC Mode Control		LAGC.2	LAGC.1	LAGC.0			CAGC.1	CAGC.0
Chroma Gain Control 1	CAGT.1	CAGT.0			CMG.11	CMG.10	CMG.9	CMG.8
Chroma Gain Control 2	CMG.7	CMG.6	CMG.5	CMG.4	CMG.3	CMG.2	CMG.1	CMG.0
Luma Gain Control 1	LAGT.1	LGAT.0			LMG.11	LMG.10	LMG.9	LMG.8
Luma Gain Control 2	LMG.7	LMG.6	LMG.5	LMG.4	LMG.3	LMG.2	LMG.1	LMG.0
Vsync Field Control 1				NEWAVMODE	HVSTIM			
Vsync Field Control 2	VSBHO	VSBHE						
Vsync Field Control 3	VSEHO	VSEHE						
Hsync Position Control 1		HSB.10	HSB.9	HSB.8		HSE.10	HSE.9	HSE.8
Hsync Position Control 2	HSB.7	HSB.6	HSB.5	HSB.4	HSB.3	HSB.2	HSB.1	HSB.0
Hsync Position Control 3	HSE.7	HSE.6	HSE.5	HSE.4	HSE.3	HSE.2	HSE.1	HSE.0
Polarity	PHS		PVS		PF			PCLK
NTSC Comb Control	CTAPSN.1	CTAPSN.0	CCMN.2	CCMN.1	CCMN.0	YCMN.2	YCMN.1	YCMN.0
PAL Comb Control	CTAPSP.1	CTAPSP.0	CCMP.2	CCMP.1	CCMP.0	YCMP.2	YCMP.1	YCMP.0
ADC Control					PWRDN_AD C_0	PWRDN_AD C_ 1	PWRDN_ADC_2	
Reserved								
Manual Window Control		CKILLTHR.2	CKILLTHR.1	CKILLTHR.0				

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved								
Resample Control		SFL_INV						
Reserved								
Gemstar Ctrl 1	GDECEL.15	GDECEL.14	GDECEL.13	GDECEL.12	GDECEL.11	GDECEL.10	GDECEL.9	GDECEL.8
Gemstar Ctrl 2	GDECEL.7	GDECEL.6	GDECEL.5	GDECEL.4	GDECEL.3	GDECEL.2	GDECEL.1	GDECEL.0
Gemstar Ctrl 3	GDECOL.15	GDECOL.14	GDECOL.13	GDECOL.12	GDECOL.11	GDECOL.10	GDECOL.9	GDECOL.8
Gemstar Ctrl 4	GDECOL.7	GDECOL.6	GDECOL.5	GDECOL.4	GDECOL.3	GDECOL.2	GDECOL.1	GDECOL.0
Gemstar Ctrl 5								GDECAD
CTI DNR Ctrl 1			DNR_EN		CTI_AB.1	CTI_AB.0	CTI_AB_EN	CTI_EN
CTI DNR Ctrl 2	CTI_C_TH.7	CTI_C_TH.6	CTI_C_TH.5	CTI_C_TH.4	CTI_C_TH.3	CTI_C_TH.2	CTI_C_TH.1	CTI_C_TH.0
Reserved								
CTI DNR Ctrl 4	DNR_TH.7	DNR_TH.6	DNR_TH.5	DNR_TH.4	DNR_TH.3	DNR_TH.2	DNR_TH.1	DNR_TH.0
Lock Count	FSCLE	SRLS	COL.2	COL.1	COL.0	CIL.2	CIL.1	CIL.0
Reserved								
Free-run Line Length 1		LLC_PAD_SEL.2	LLC_PAD_SEL.1	LLC_PAD_SEL.0				
Reserved								
VBI Info					CGMSD	EDTVD	CCAPD	WSSD
WSS 1	WSS1.7	WSS1.6	WSS1.5	WSS1.4	WSS1.3	WSS1.2	WSS1.1	WSS1.0
WSS 2	WSS2.7	WSS2.6	WSS2.5	WSS2.4	WSS2.3	WSS2.2	WSS2.1	WSS2.0
EDTV 1	EDTV1.7	EDTV1.6	EDTV1.5	EDTV1.4	EDTV1.3	EDTV1.2	EDTV1.1	EDTV1.0
EDTV 2	EDTV2.7	EDTV2.6	EDTV2.5	EDTV2.4	EDTV2.3	EDTV2.2	EDTV2.1	EDTV2.0
EDTV 3	EDTV3.7	EDTV3.6	EDTV3.5	EDTV3.4	EDTV3.3	EDTV3.2	EDTV3.1	EDTV3.0
CGMS 1	CGMS1.7	CGMS1.6	CGMS1.5	CGMS1.4	CGMS1.3	CGMS1.2	CGMS1.1	CGMS1.0
CGMS 2	CGMS2.7	CGMS2.6	CGMS2.5	CGMS2.4	CGMS2.3	CGMS2.2	CGMS2.1	CGMS2.0
CGMS 3	CGMS3.7	CGMS3.6	CGMS3.5	CGMS3.4	CGMS3.3	CGMS3.2	CGMS3.1	CGMS3.0
CCAP1	CCAP1.7	CCAP1.6	CCAP1.5	CCAP1.4	CCAP1.3	CCAP1.2	CCAP1.1	CCAP1.0
CCAP2	CCAP2.7	CCAP2.6	CCAP2.5	CCAP2.4	CCAP2.3	CCAP2.2	CCAP2.1	CCAP2.0
Letterbox 1	LB_LCT.7	LB_LCT.6	LB_LCT.5	LB_LCT.4	LB_LCT.3	LB_LCT.2	LB_LCT.1	LB_LCT.0
Letterbox 2	LB_LCM.7	LB_LCM.6	LB_LCM.5	LB_LCM.4	LB_LCM.3	LB_LCM.2	LB_LCM.1	LB_LCM.0
Letterbox 3	LB_LCB.7	LB_LCB.6	LB_LCB.5	LB_LCB.4	LB_LCB.3	LB_LCB.2	LB_LCB.1	LB_LCB.0
Reserved								
CRC Enable						CRC_ENABLE		
Reserved								
ADC Switch 1	ADC1_SW.3	ADC1_SW.2	ADC1_SW.1	ADC1_SW.0	ADC0_SW.3	ADC0_SW.2	ADC0_SW.1	ADC0_SW.0
ADC Switch 2	ADC_SW_MAN				ADC2_SW.3	ADC2_SW.2	ADC2_SW.1	ADC2_SW.0
Reserved								
Letterbox Control 1				LB_TH.4	LB_TH.3	LB_TH.2	LB_TH.1	LB_TH.0
Letterbox Control 2	LB_SL.3	LB_SL.2	LB_SL.1	LB_SL.0	LB_EL.3	LB_EL.2	LB_EL.1	LB_EL.0
Reserved								
Reserved								
Reserved								
SD Offset Cb	SD_OFF_CB.7	SD_OFF_CB.6	SD_OFF_CB.5	SD_OFF_CB.4	SD_OFF_CB.3	SD_OFF_CB.2	SD_OFF_CB.1	SD_OFF_CB.0
SD Offset Cr	SD_OFF_CR.7	SD_OFF_CR.6	SD_OFF_CR.5	SD_OFF_CR.4	SD_OFF_CR.3	SD_OFF_CR.2	SD_OFF_CR .1	SD_OFF_CR.0
SD Saturation Cb	SD_SAT_CB.7	SD_SAT_CB.6	SD_SAT_CB.5	SD_SAT_CB.4	SD_SAT_CB.3	SD_SAT_CB.2	SD_SAT_CB.1	SD_SAT_CB.0
SD Saturation Cr	SD_SAT_CR.7	SD_SAT_CR.6	SD_SAT_CR.5	SD_SAT_CR.4	SD_SAT_CR.3	SD_SAT_CR.2	SD_SAT_CR.1	SD_SAT_CR.0
NTSC V Bit Begin	NVBEGDEL O	NVBEGDEL E	NVBEGSIGN	NVBEG.4	NVBEG.3	NVBEG.2	NVBEG.1	NVBEG.0
NTSC V Bit End	NVENDDEL O	NVENDDEL E	NVENDSIGN	NVEND.4	NVEND.3	NVEND.2	NVEND.1	NVEND.0
NTSC F Bit Toggle	NFTOGDEL O	NFTOGDEL E	NFTOGSIGN	NFTOG.4	NFTOG.3	NFTOG.2	NFTOG.1	NFTOG.0
PAL V Bit Begin	PVBEGDEL O	PVBEGDEL E	PVBEGSIGN	PVBEG.4	PVBEG.3	PVBEG.2	PVBEG.1	PVBEG.0
PAL V Bit End	PVENDDEL O	PVENDDEL E	PVENDSIGN	PVEND.4	PVEND.3	PVEND.2	PVEND.1	PVEND.0
PAL F Bit Toggle	PFTOGDEL O	PFTOGDEL E	PFTOGSIGN	PFTOG.4	PFTOG.3	PFTOG.2	PFTOG.1	PFTOG.0
Reserved								
Drive Strength			DR_STR.1	DR_STR.0	DR_STR_C.1	DR_STR_C.0	DR_STR_S.1	DR_STR_S.0
Reserved								
IF Comp Control						IFFILTSEL.2	IFFILTSEL.1	IFFILTSEL.0
VS Mode Control					VS_COAST_MODE.1	VS_COAST_MODE.0	EXTEND_VS_MIN_FREQ	EXTEND_VS_MAX_FREQ

I²C REGISTER MAP DETAILS

The following registers are located in the Common I²C Map and Register Access Page 2.

Table 84. Interrupt (Page 2) Register Map Bit Names [1]

Register Name	Reset Value	rw	Subaddress		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
			Dec	Hex								
Interrupt Config 0	0001 x000	rw	64	0x40	INTRQ_DUR _SEL.1	INTRQ_DUR _SEL.0	MV_INTRQ_ SEL.1	MV_INTRQ_ SEL.0		MPU_STIM_ INTRQ	INTRQ_OP_ SEL.1	INTRQ_OP_ SEL.0
Reserved			65	0x41								
Interrupt Status 1		r	66	0x42		MV_PS_CS_ Q	SD_FR_CHN G_Q				SD_UNLOCK _Q	SD_LOCK_Q
Interrupt Clear 1	x000 0000	w	67	0x43		MV_PS_CS_ CLR	SD_FR_CHN G_CLR				SD_UNLOCK _CLR	SD_LOCK_ CLR
Interrupt Maskb 1	x000 0000	rw	68	0x44		MV_PS_CS_ MSKB	SD_FR_CHN G_MSKB				SD_UNLOCK _MSKB	SD_LOCK_ MSKB
Reserved			69	0x45								
Interrupt Status 2		r	70	0x46	MPU_STIM_ INTRQ_Q				WSS_ CHNGD_Q	CGMS_ CHNGD_Q	GEMD_Q	CCAPD_Q
Interrupt Clear 2	0xxx 0000	w	71	0x47	MPU_STIM_ INTRQ_CLR				WSS_ CHNGD_CLR	CGMS_CHN GD_CLR	GEMD_CLR	CCAPD_CLR
Interrupt Maskb 2	0xxx 0000	rw	72	0x48	MPU_STIM_ INTRQ_ MSKB				WSS_ CHNGD_ MSKB	CGMS_ CHNGD_ MSKB	GEMD_ MSKB	CCAPD_ MSKB
Raw Status 3		r	73	0x49				SCM_LOCK		SD_H_LOCK	SD_V_LOCK	SD_OP_ 50HZ
Interrupt Status 3		r	74	0x4A			PAL_SW_LK _CHNG_Q	SCM_LOCK_ CHNG_Q	SD_AD_ CHNG_Q	SD_H_LOCK _CHNG_Q	SD_V_LOCK _CHNG_Q	SD_OP_ CHNG_Q
Interrupt Clear 3	xx00 0000	w	75	0x4B			PAL_SW_LK _CHNG_CLR	SCM_LOCK_ CHNG_CLR	SD_AD_CH NG_CLR	SD_H_LOCK _CHNG_CLR	SD_V_LOCK _CHNG_CLR	SD_OP_ CHNG_CLR
Interrupt Maskb 3	xx00 0000	rw	76	0x4C			PAL_SW_LK _CHNG_ MSKB	SCM_LOCK_ CHNG_ MSKB	SD_AD_ CHNG_ MSKB	SD_H_LOCK _CHNG_ MSKB	SD_V_LOCK _CHNG_ MSKB	SD_OP_ CHNG_ MSKB

[1] To access the Interrupt Register Map, the Register Access page[1:0] in Register Address 0x0E must be programmed to 01b.

Table 85. Interrupt Register Map Details

Subaddress	Register	Bit Description	Bit 7	6	5	4	3	2	1	0	Comments	Notes
0x40	Interrupt Config 1 Register Access Page 2	INTRQ_OP_SEL[1:0]. Interrupt Drive Level Select							0	0	Open drain.	
									0	1	Drive low when active.	
									1	0	Drive high when active.	
									1	1	Reserved.	
		MPU_STIM_INTRQ[1:0]. Manual Interrupt Set Mode						0			Manual interrupt mode disabled.	
								1			Manual interrupt mode enabled.	
		Reserved					x				Not used.	
		MV_INTRQ_SEL[1:0]. Macrovision Interrupt Select			0	0					Reserved.	
					0	1					Pseudo sync only.	
					1	0					Color stripe only.	
					1	1					Pseudo sync or color stripe.	
		INTRQ_DUR_SEL[1:0]. Interrupt Duration Select	0	0							3 Xtal periods.	
			0	1							15 Xtal periods.	
			1	0							63 Xtal periods.	
			1	1							Active until cleared.	
0x41	Reserved		x	x	x	x	x	x	x	x		
0x42	Interrupt Status 1 Read Only Register Access Page 2	SD_LOCK_Q								0	No change.	These bits can be cleared or masked in Registers 0x43 and 0x44, respectively.
										1	SD input has caused the decoder to go from an un-locked state to a locked state.	
		SD_UNLOCK_Q							0		No change.	
									1		SD input has caused the decoder to go from a locked state to an unlocked state.	
		Reserved						x				
		Reserved					x					
		Reserved				x						
		SD_FR_CHNG_Q			0						No change.	
					1						Denotes a change in the free-run status.	
		MV_PS_CS_Q		0							No change.	
				1							Pseudo sync/color striping detected. See MV_INTRQ_SEL[1:0], Macrovision Interrupt Selection Bits Address 0x40 (Interrupt Space)[5:4] for selection.	
		Reserved	x									
0x43	Interrupt Clear 1 Write Only Register Access Page 2	SD_LOCK_CLR								0	Do not clear.	
										1	Clears SD_LOCK_Q bit.	
		SD_UNLOCK_CLR							0		Do not clear.	
									1		Clears SD_UNLOCK_Q bit.	
		Reserved						0			Not used.	
		Reserved					0				Not used.	
		Reserved				0					Not used.	
		SD_FR_CHNG_CLR			0						Do not clear.	
					1						Clears SD_FR_CHNG_Q bit.	
		MV_PS_CS_CLR		0							Do not clear.	
				1							Clears MV_PS_CS_Q bit.	
		Reserved	x								Not used.	

Subaddress	Register	Bit Description	Bit 7	6	5	4	3	2	1	0	Comments	Notes
0x44	Interrupt Mask 1 Read/Write Register Register Access Page 2	SD_LOCK_MSKB								0	Masks SD_LOCK_Q bit.	
										1	Unmasks SD_LOCK_Q bit.	
		SD_UNLOCK_MSKB							0		Masks SD_UNLOCK_Q bit.	
									1		Unmasks SD_UNLOCK_Q bit	
		Reserved						0			Not used.	
		Reserved					0				Not used.	
		Reserved				0					Not used.	
		SD_FR_CHNG_MSKB			0						Masks SD_FR_CHNG_Q bit.	
					1						Unmasks SD_FR_CHNG_Q bit.	
		MV_PS_CS_MSKB		0							Masks MV_PS_CS_Q bit.	
				1							Unmasks MV_PS_CS_Q bit.	
		Reserved	x								Not used.	
0x45	Reserved		x	x	x	x	x	x	x	x		
0x46	Interrupt Status 2 Read Only Register Register Access Page 2	CCAPD_Q								0	Closed captioning not detected in the input video signal	These bits can be cleared or masked by Registers 0x47 and 0x48, respectively.
										1	Closed captioning data detected in the video input signal.	
		GEMD_Q							0		Gemstar data not detected in the input video signal.	
									1		Gemstar data detected in the input video signal.	
		CGMS_CHNGD_Q						0			No change detected in CGMS data in the input video signal.	
								1			A change is detected in the CGMS data in the input video signal.	
		WSS_CHNGD_Q					0				No change detected in WSS data in the input video signal.	
							1				A change is detected in the WSS data in the input video signal.	
		Reserved				x					Not used.	
		Reserved			x						Not used.	
		Reserved		x							Not used.	
		MPU_STIM_INTRQ_Q	0								Manual interrupt not set.	
			1								Manual interrupt set.	
0x47	Interrupt Clear 2 Write Only Register Access Page 2	CCAPD_CLR								0	Do not clear.	
										1	Clears CCAPD_Q bit.	
		GEMD_CLR							0		Do not clear.	
									1		Clears GEMD_Q bit.	
		CGMS_CHNGD_CLR						0			Do not clear.	
								1			Clears CGMS_CHNGD_Q bit.	
		WSS_CHNGD_CLR					0				Do not clear.	
							1				Clears WSS_CHNGD_Q bit.	
		Reserved				x					Not used.	
		Reserved			x						Not used.	
		Reserved		x							Not used.	
		MPU_STIM_INTRQ_CLR	0								Do not clear.	
			1								Clears MPU_STIM_INTRQ_Q bit.	

Subaddress	Register	Bit Description	Bit 7	6	5	4	3	2	1	0	Comments	Notes
0x48	Interrupt Mask 2 Read/Write Register Access Page 2	CCAPD_MSKB								0	Masks CCAPD_Q bit.	
										1	Unmasks CCAPD_Q bit.	
		GEMD_MSKB							0		Masks GEMD_Q bit.	
									1		Unmasks GEMD_Q bit.	
		CGMS_CHNGD_MSKB						0			Masks CGMS_CHNGD_Q bit.	
								1			Unmasks CGMS_CHNGD_Q bit.	
		WSS_CHNGD_MSKB					0				Masks WSS_CHNGD_Q bit..	
							1				Unmasks WSS_CHNGD_Q bit.	
		Reserved				0					Not used.	
		Reserved			0						Not used.	
		Reserved		0							Not used.	
		MPU_STIM_INTRQ_MSKB	0								Masks MPU_STIM_INTRQ_Q bit.	
			1								Unmasks MPU_STIM_INTRQ_Q bit.	
0x49	Raw Status 3 Read Only Register Register Access Page 2	SD_OP_50Hz SD 60/50Hz frame rate at output								0	SD 60 Hz signal output.	These bits **cannot** be cleared or masked. Register 0x4A is used for this purpose.
										1	SD 50 Hz signal output.	
		SD_V_LOCK							0		SD vertical sync lock not established.	
									1		SD vertical sync lock established.	
		SD_H_LOCK						0			SD horizontal sync lock not established.	
								1			SD horizontal sync lock established.	
		Reserved					x				Not used.	
		SCM_LOCK SECAM Lock				0					SECAM lock not established.	
						1					SECAM lock established.	
		Reserved			x						Not used.	
		Reserved		x							Not used.	
		Reserved	x								Not used.	
0x4A	Interrupt Status 3 Read Only Register Register Access Page 2	SD_OP_CHNG_Q SD 60/50 Hz frame rate at input								0	No change in SD signal standard detected at the input.	These bits can be cleared and masked by Registers 0x4B and 0x4C, respectively.
										1	A change in SD signal standard is detected at the input.	
		SD_V_LOCK_CHNG_Q							0		No change in SD vertical sync lock status.	
									1		SD vertical sync lock status has changed.	
		SD_H_LOCK_CHNG_Q						0			No change in SD horizontal sync lock status.	
								1			SD horizontal sync lock status has changed.	
		SD_AD_CHNG_Q SD autodetect changed					x				No change in AD_RESULT[2:0] bits in Status Register 1.	
											AD_RESULT[2:0] bits in Status Register 1 have changed.	
		SCM_LOCK_CHNG_Q SECAM Lock				0					No change in SECAM lock status.	
						1					SECAM lock status has changed.	
		PAL_SW_LK_CHNG_Q			x						No change in PAL swinging burst lock status.	
											PAL swinging burst lock status has changed.	
		Reserved		x							Not used.	
		Reserved	x								Not used.	

Subaddress	Register	Bit Description	Bit 7	6	5	4	3	2	1	0	Comments	Notes
0x4B	Interrupt Clear 3 Write Only Register Register Access Page 2	SD_OP_CHNG_CLR								0	Do not clear.	
										1	Clears SD_OP_CHNG_Q bit.	
		SD_V_LOCK_CHNG_CLR							0		Do not clear.	
									1		Clears SD_V_LOCK_CHNG_Q bit.	
		SD_H_LOCK_CHNG_CLR						0			Do not clear.	
								1			Clears SD_H_LOCK_CHNG_Q bit.	
		SD_AD_CHNG_CLR					0				Do not clear.	
							1				Clears SD_AD_CHNG_Q bit.	
		SCM_LOCK_CHNG_CLR				0					Do not clear.	
						1					Clears SCM_LOCK_CHNG_Q bit.	
		PAL_SW_LK_CHNG_CLR			0						Do not clear.	
					1						Clears PAL_SW_LK_CHNG_Q bit.	
		Reserved		x							Not used.	
		Reserved	x								Not used.	
0x4C	Interrupt Mask 2 Read/Write Register Register Access Page 2	SD_OP_CHNG_MSKB								0	Masks SD_OP_CHNG_Q bit.	
										1	Unmasks SD_OP_CHNG_Q bit.	
		SD_V_LOCK_CHNG_ MSKB							0		Masks SD_V_LOCK_CHNG_Q bit.	
									1		Unmasks SD_V_LOCK_CHNG_Q bit.	
		SD_H_LOCK_CHNG_ MSKB						0			Masks SD_H_LOCK_CHNG_Q bit.	
								1			Unmasks SD_H_LOCK_CHNG_Q bit.	
		SD_AD_CHNG_ MSKB					0				Masks SD_AD_CHNG_Q bit.	
							1				Unmasks SD_AD_CHNG_Q bit.	
		SCM_LOCK_CHNG_ MSKB				0					Masks SCM_LOCK_CHNG_Q bit	
						1					Unmasks SCM_LOCK_CHNG_Q bit.	
		PAL_SW_LK_CHNG_ MSKB			0						Masks PAL_SW_LK_CHNG_Q bit.	
					1						Unmasks PAL_SW_LK_CHNG_Q bit.	
		Reserved		x							Not used.	
		Reserved	x								Not used.	

The following registers are located in the Common I²C Map and Register Access Page 1.

Table 86. Interrupt Register Map Details

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x00	Input Control	INSEL[3:0]. The INSEL bits allow the user to select an input channel as well as the input format.					0	0	0	0	CVBS in on AIN1.	Composite.
							0	0	0	1	CVBS in on AIN2.	
							0	0	1	0	CVBS in on AIN3.	
							0	0	1	1	CVBS in on AIN4.	
							0	1	0	0	CVBS in on AIN5.	
							0	1	0	1	CVBS in on AIN6.	
							0	1	1	0	Y on AIN1, C on AIN4.	S-Video
							0	1	1	1	Y on AIN2, C on AIN5.	
							1	0	0	0	Y on AIN3, C on AIN6.	
							1	0	0	1	Y on AIN1, Pr on AIN4, Pb on AIN5.	YPbPr
							1	0	1	0	Y on AIN2, Pr on AIN3, Pb on AIN6.	
							1	0	1	1	CVBS in on AIN7.	Composite
							1	1	0	0	CVBS in on AIN8.	
							1	1	0	1	CVBS in on AIN9.	
							1	1	1	0	CVBS in on AIN10.	
							1	1	1	1	CVBS in on AIN11.	
		VID_SEL[3:0]. The VID_SEL bits allow the user to select the input video standard.	0	0	0	0					Auto-detect PAL (B/G/H/I/D), NTSC (without pedestal), SECAM.	
			0	0	0	1					Auto-detect PAL (B/G/H/I/D), NTSC-M (with pedestal), SECAM.	
			0	0	1	0					Auto-detect PAL-N, NTSC-M (without pedestal), SECAM.	
			0	0	1	1					Auto-detect PAL-N, NTSC-M (with pedestal), SECAM.	
			0	1	0	0					NTSC-J.	
			0	1	0	1					NTSC-M.	
			0	1	1	0					PAL60.	
			0	1	1	1					NTSC-4.43.	
			1	0	0	0					PAL-B/G/H/I/D.	
			1	0	0	1					PAL-N (B/G/H/I/D without pedestal).	
			1	0	1	0					PAL-M (without pedestal).	
			1	0	1	1					PAL-M.	
			1	1	0	0					PAL Combination N.	
			1	1	0	1					PAL Combination N.	
			1	1	1	0					SECAM (with pedestal).	
			1	1	1	1					SECAM (with pedestal).	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x01	Video Selection	Reserved						0	0	0	Set to default.	
		ENVSPROC					0				Disable Vsync processor.	
							1				Enable Vsync processor.	
		Reserved				0					Set to default.	
		BETACAM			0						Standard video input.	
					1						Betacam input enable.	
		ENHSPLL		0							Disable Hsync processor.	
				1							Enable Hsync processor.	
		Reserved	1								Set to default.	
0x03	Output Control	SD_DUP_AV. Duplicates the AV codes from the luma into the chroma path.								0	AV codes to suit 8-bit interleaved data output.	
										1	AV codes duplicated (for 16-bit interfaces).	
		Reserved							0		Set as default.	
		OF_SEL[3:0]. Allows the user to choose from a set of output formats.			0	0	0	0			Reserved.	
					0	0	0	1			Reserved.	
					0	0	1	0			16-bit @ LLC1 4:2:2.	
					0	0	1	1			8-bit @ LLC1 4:2:2 ITU-R BT.656.	
					0	1	0	0			Not used.	
					0	1	0	1			Not used.	
					0	1	1	0			Not used.	
					0	1	1	1			Not used.	
					1	0	0	0			Not used.	
					1	0	0	1			Not used.	
					1	0	1	0			Not used.	
					1	0	1	1			Not used.	
					1	1	0	0			Not used.	
					1	1	0	1			Not used.	
					1	1	1	0			Not used.	
					1	1	1	1			Not used.	
		TOD. Three-State Output Drivers. This bit allows the user to three-state the output drivers: P[19:0], HS, VS, FIELD, and SFL.		0							Output pins enabled.	See TIM_OE, Address 0x04[3] and Introduction.
				1							Drivers three-stated.	
		VBI_EN. Allows VBI data (Lines 1 to 21) to be passed through with only a minimum amount of filtering performed.	0								All lines filtered and scaled.	
			1								Only active video region filtered.	
0x04	Extended Output Control	RANGE. Allows the user to select the range of output values. Can be BT656 compliant, or can fill the whole accessible number range.								0	16 < Y < 235, 16 < C < 240.	ITU-R BT.656.
										1	1 < Y < 254, 1 < C < 254.	Extended range.
		EN_SFL_PIN							0		SFL output is disabled.	SFL output enables encoder and decoder to be connected directly.
									1		SFL information output on the SFL pin.	
		BL_C_VBI. Blank Chroma during VBI. If set, enables data in the VBI region to be passed through the decoder undistorted.						0			Decode and output color.	During VBI.
								1			Blank Cr and Cb.	
		TIM_OE. Timing signals output enable.					0				HS, VS, F three-stated.	Controlled by TOD.
							1				HS, VS, F forced active.	
		Reserved			x	x						
		Reserved		1								
		BT656-4. Allows the user to select an output mode-compatible with ITU- R BT656-3/4.	0								BT656-3-compatible.	
			1								BT656-4-compatible.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x07	Autodetect Enable	AD_PAL_EN. PAL B/G/I/H autodetect enable.								0	Disable.	
										1	Enable.	
		AD_NTSC_EN. NTSC autodetect enable.							0		Disable.	
									1		Enable.	
		AD_PALM_EN. PAL M autodetect enable.						0			Disable.	
								1			Enable.	
		AD_PALN_EN. PAL N autodetect enable.					0				Disable.	
							1				Enable.	
		AD_P60_EN. PAL60 autodetect enable.				0					Disable.	
						1					Enable.	
		AD_N443_EN. NTSC443 autodetect enable.			0						Disable.	
					1						Enable.	
		AD_SECAM_EN. SECAM autodetect enable.		0							Disable.	
				1							Enable	
		AD_SEC525_EN. SECAM 525 autodetect enable.	0								Disable.	
			1								Enable.	
0x08	Contrast Register	CON[7:0]. Contrast adjust. This is the user control for contrast adjustment.	1	0	0	0	0	0	0	0	Luma gain = 1.	0x00 Gain = 0; 0x80 Gain = 1; 0xFF Gain = 2.
0x09	Reserved	Reserved	1	0	0	0	0	0	0	0		
0x0A	Brightness Register	BRI[7:0]. This register controls the brightness of the video signal.	0	0	0	0	0	0	0	0		0x00 = 0IRE; 0x7F = +100IRE; 0x80 = –100IRE.
0x0B	Hue Register	HUE[7:0]. This register contains the value for the color hue adjustment.	0	0	0	0	0	0	0	0		Hue range = –90° to +90°.
0x0C	Default Value Y	DEF_VAL_EN. Default value enable.								0	Free-run mode dependent on DEF_VAL_AUTO_EN.	
										1	Force free-run mode on and output blue screen.	
		DEF_VAL_AUTO_EN. Default value.							0		Disable free-run mode.	When lock is lost, free-run mode can be enabled to output stable timing, clock, and a set color.
									1		Enable automatic free-run mode (blue screen).	
		DEF_Y[5:0]. Default value Y. This register holds the Y default value.	0	0	1	1	0	1			Y[7:0] = {DEF_Y[5:0], 0, 0}.	Default Y value output in free-run mode.
0x0D	Default Value C	DEF_C[7:0]. Default value C. The Cr and Cb default values are defined in this register.	0	1	1	1	1	1	0	0	Cr[7:0] = DEF_C[7:4], 0, 0, 0, 0}; Cb[7:0] = DEF_C[3:0], 0, 0, 0, 0}.	Default Cb/Cr value output in free-run mode. Default values give blue screen output.
0x0E	ADI Control	Reserved.				0	0	0	0	0	Set as default.	
		SUB_USR_EN. Enables the user to access the interrupt map.			0						Access user reg map.	See Figure 38.
					1						Access interrupt reg map.	
		Reserved.	0	0							Set as default.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x0F	Power Management	Reserved							0	0	Set to default.	
		PDBP. Power-down bit priority selects between PWRDN bit or PIN.						0			Chip power-down controlled by pin.	
								1			Bit has priority (pin disregarded).	
		Reserved				0	0				Set to default.	
		PWRDN. Power-down places the decoder in a full power-down mode.			0						System functional.	
					1						Powered down.	See PDBP, 0x0F Bit 2.
		Reserved		0							Set to default.	
		RES. Chip reset loads all I^2C bits with default values.	0								Normal operation.	
			1								Start reset sequence.	Executing reset takes approximately 2 ms. This bit is self-clearing.
0x10	Status Register 1, Read Only	IN_LOCK								x	In lock (right now) = 1.	Provides information about the internal status of the decoder.
		LOST_LOCK							x		Lost lock (since last read) = 1.	
		FSC_LOCK						x			F_{SC} lock (right now) = 1.	
		FOLLOW_PW					x				Peak white AGC mode active = 1.	
		AD_RESULT[2:0]. Autodetection result reports the standard of the input video.		0	0	0					NTSM-MJ.	Detected standard.
				0	0	1					NTSC-443.	
				0	1	0					PAL-M.	
				0	1	1					PAL60.	
				1	0	0					PAL-B/G/H/I/D.	
				1	0	1					SECAM.	
				1	1	0					PAL-combination N.	
				1	1	1					SECAM 525.	
		COL_KILL	x								Color kill is active = 1.	Color kill.
0x11	IDENT Read Only	IDENT[7:0]. Provides identification on the revision of the part.	x	x	x	x	x	x	x	x		ADV7183B = 0x13.
0x12	Status Register 2, Read Only.	MVCS DET								x	MV color striping detected.	1 = detected.
		MVCS T3							x		MV color striping type.	0 = Type 2, 1 = Type 3.
		MV PS DET						x			MV pseudo sync detected.	1 = detected.
		MV AGC DET					x				MV AGC pulses detected.	1 = detected.
		LL NSTD				x					Nonstandard line length.	1 = detected.
		FSC NSTD			x						F_{SC} frequency nonstandard.	1 = detected.
		Reserved	x	x								
0x13	Status Register 3, Read Only.	INST_HLOCK								x	1 = horizontal lock achieved.	Unfiltered.
		GEMD							x		1 = Gemstar data detected.	
		SD_OP_50HZ						x			SD 60 Hz detected.	SD Field rate detect.
		Reserved					x				SD 50 Hz detected.	
		FREE_RUN_ACT				x					1 = free-run mode active.	Blue screen output.
		STD FLD_LEN			x						1 = field length standard.	Correct field length found.
		INTERLACED		x							1 = interlaced video detected.	Field sequence found.
		PAL_SW_LOCK	x								1 = swinging burst detected.	Reliable swinging burst sequence.
0x14	Analog Clamp Control	Reserved					0	0	1	0	Set to default.	
		CCLEN. Current clamp enable allows the user to switch off the current sources in the analog front.				0					Current sources switched off.	
						1					Current sources enabled.	
		Reserved	0	0	0						Set to default.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x15	Digital Clamp Control 1	Reserved				0	x	x	x	x	Set to default.	
		DCT[1:0]. Digital clamp timing determines the time constant of the digital fine clamp circuitry.		0	0						Slow (TC = 1 sec).	
				0	1						Medium (TC = 0.5 sec).	
				1	0						Fast (TC = 0.1 sec).	
				1	1						TC dependent on video.	
		Reserved	0								Set to default.	
0x17	Shaping Filter Control	YSFM[4:0]. Selects Y-Shaping Filter mode when in CVBS only mode. Allows the user to select a wide range of low-pass and notch filters. If either auto mode is selected, the decoder selects the optimum Y filter depending on the CVBS video source quality (good vs. bad).				0	0	0	0	0	Auto wide notch for poor quality sources or wide-band filter with comb for good quality input.	Decoder selects optimum Y-shaping filter depending on CVBS quality.
						0	0	0	0	1	Auto narrow notch for poor quality sources or wideband filter with comb for good quality input.	
						0	0	0	1	0	SVHS 1.	If one of these modes is selected, the decoder does not change filter modes. Depending on video quality, a fixed filter response (the one selected) is used for good and bad quality video.
						0	0	0	1	1	SVHS 2.	
						0	0	1	0	0	SVHS 3.	
						0	0	1	0	1	SVHS 4.	
						0	0	1	1	0	SVHS 5.	
						0	0	1	1	1	SVHS 6.	
						0	1	0	0	0	SVHS 7.	
						0	1	0	0	1	SVHS 8.	
						0	1	0	1	0	SVHS 9.	
						0	1	0	1	1	SVHS 10.	
						0	1	1	0	0	SVHS 11.	
						0	1	1	0	1	SVHS 12.	
						0	1	1	1	0	SVHS 13.	
						0	1	1	1	1	SVHS 14.	
						1	0	0	0	0	SVHS 15.	
						1	0	0	0	1	SVHS 16.	
						1	0	0	1	0	SVHS 17.	
						1	0	0	1	1	SVHS 18 (CCIR601).	
						1	0	1	0	0	PAL NN1.	
						1	0	1	0	1	PAL NN2.	
						1	0	1	1	0	PAL NN3.	
						1	0	1	1	1	PAL WN 1.	
						1	1	0	0	0	PAL WN 2.	
						1	1	0	0	1	NTSC NN1.	
						1	1	0	1	0	NTSC NN2.	
						1	1	0	1	1	NTSC NN3.	
						1	1	1	0	0	NTSC WN1.	
						1	1	1	0	1	NTSC WN2.	
						1	1	1	1	0	NTSC WN3.	
						1	1	1	1	1	Reserved.	
		CSFM[2:0]. C-Shaping Filter mode allows the selection from a range of low-pass chrominance filters, SH1 to SH5 and wideband mode.	0	0	0						Auto selection 1.5 MHz.	Automatically selects a C filter for the specified bandwidth.
			0	0	1						Auto selection 2.17 MHz.	
			0	1	0						SH1.	
			0	1	1						SH2.	
			1	0	0						SH3.	
			1	0	1						SH4.	
			1	1	0						SH5.	
			1	1	1						Wideband mode.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x18	Shaping Filter Control 2	WYSFM[4:0]. Wideband Y shaping filter mode allows the user to select which Y shaping filter is used for the Y component of Y/C, YPbPr, B/W input signals; it is also used when a good quality input CVBS signal is detected. For all other inputs, the Y shaping filter chosen is controlled by YSFM[4:0].				0	0	0	0	0	Reserved. Do not use.	
						0	0	0	0	1	Reserved. Do not use.	
						0	0	0	1	0	SVHS 1.	
						0	0	0	1	1	SVHS 2.	
						0	0	1	0	0	SVHS 3.	
						0	0	1	0	1	SVHS 4.	
						0	0	1	1	0	SVHS 5.	
						0	0	1	1	1	SVHS 6.	
						0	1	0	0	0	SVHS 7.	
						0	1	0	0	1	SVHS 8.	
						0	1	0	1	0	SVHS 9.	
						0	1	0	1	1	SVHS 10.	
						0	1	1	0	0	SVHS 11.	
						0	1	1	0	1	SVHS 12.	
						0	1	1	1	0	SVHS 13.	
						0	1	1	1	1	SVHS 14.	
						1	0	0	0	0	SVHS 15.	
						1	0	0	0	1	SVHS 16.	
						1	0	0	1	0	SVHS 17.	
						1	0	0	1	1	SVHS 18 (CCIR 601).	
						1	0	1	0	0	Reserved. Do not use.	
						~	~	~	~	~	Reserved. Do not use.	
						1	1	1	1	1	Reserved. Do not use.	
		Reserved		0	0						Set to default.	
		WYSFMOVR. Enables the use of automatic WYSFN filter.	0								Auto selection of best filter.	
			1								Manual select filter using WYSFM[4:0].	
0x19	Comb Filter Control	PSFSEL[1:0]. Controls the signal bandwidth that is fed to the comb filters (PAL).							0	0	Narrow.	
									0	1	Medium.	
									1	0	Wide.	
									1	1	Widest.	
		NSFSEL[1:0]. Controls the signal bandwidth that is fed to the comb filters (NTSC).					0	0			Narrow.	
							0	1			Medium.	
							1	0			Medium.	
							1	1			Wide.	
		Reserved	1	1	1	1					Set as default.	
0x1D	ADI Control 2	Reserved				0	0	x	x	x	Set as default.	
		VS_JIT_COMP_EN			0						Enabled.	
					1						Disabled.	
		EN28XTAL		0							Use 27 MHz crystal.	
				1							Use 28 MHz crystal.	
		TRI_LLC	0								LLC pin active.	
			1								LLC pin three-stated.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x27	Pixel Delay Control	LTA[1:0]. Luma timing adjust allows the user to specify a timing difference between chroma and luma samples.							0	0	No delay.	CVBS mode LTA[1:0] = 00b; S-Video mode LTA[1:0]= 01b, YPrPb mode LTA[1:0] = 01b.
									1	0	Luma 1 clk (37 ns) delayed.	
									1	0	Luma 2 clk (74 ns) early.	
									1	1	Luma 1 clk (37 ns) early.	
		Reserved						0			Set to zero.	
		CTA[2:0]. Chroma timing adjust allows a specified timing difference between the luma and chroma samples.			0	0	0				Not valid setting.	CVBS mode CTA[2:0] = 011b. S-Video mode CTA[2:0] = 101b. YPrPb mode CTA[2:0] = 110b.
					0	0	1				Chroma + 2 pixels (early).	
					0	1	0				Chroma + 1 pixel (early).	
					0	1	1				No delay.	
					1	0	0				Chroma – 1 pixel (late).	
					1	0	1				Chroma – 2 pixels (late).	
					1	1	0				Chroma – 3 pixels (late).	
					1	1	1				Not valid setting.	
		AUTO_PDC_EN. Automatically programs the LTA/CTA values so that luma and chroma are aligned at the output for all modes of operation.		0							Use values in LTA[1:0] and CTA[2:0] for delaying luma/chroma.	
				1							LTA and CTA values determined automatically.	
		SWPC. Allows the Cr and Cb samples to be swapped.	0								No swapping.	
			1								Swap the Cr and Cb O/P samples.	
0x2B	Misc Gain Control	PW_UPD. Peak white update determines the rate of gain.								0	Update once per video line.	Peak white must be enabled. See LAGC[2:0] Luma Automatic Gain Control, Address 0x2C[7:0]
										1	Update once per field.	
		Reserved			1	0	0	0	0		Set to default.	
		CKE. Color kill enable allows the color kill function to be switched on and off.		0							Color kill disabled.	For SECAM color kill, threshold is set at 8%. See CKILLTHR[2:0].
				1							Color kill enabled.	
		Reserved	1								Set to default.	
0x2C	AGC Mode Control	CAGC[1:0]. Chroma automatic gain control selects the basic mode of operation for the AGC in the chroma path.							0	0	Manual fixed gain.	Use CMG[11:0].
									0	1	Use luma gain for chroma.	
									1	0	Automatic gain.	Based on color burst.
									1	1	Freeze chroma gain.	
		Reserved					1	1			Set to 1.	
		LAGC[2:0]. Luma automatic gain control selects the mode of operation for the gain control in the luma path.		0	0	0					Manual fixed gain.	Use LMG[11:0].
				0	0	1					AGC Peak white algorithm off.	Blank level to sync tip.
				0	1	0					AGC Peak white algorithm on.	Blank level to sync tip.
				0	1	1					Reserved	
				1	0	0					Reserved.	
				1	0	1					Reserved	
				1	1	0					Reserved.	
				1	1	1					Freeze gain.	
		Reserved	1								Set to 1.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x2D	Chroma Gain Control 1	CMG[11:8]. Chroma manual gain can be used to program a desired manual chroma gain. Reading back from this register in AGC mode gives the current gain.					0	1	0	0		CAGC[1:0] settings decide in which mode CMG[11:0] operates.
		Reserved			1	1					Set to 1.	
		CAGT[1:0]. Chroma automatic gain timing allows adjustment of the chroma AGC tracking speed.	0	0							Slow (TC = 2 sec).	Has an effect only if CAGC[1:0] is set to auto gain (10).
			0	1							Medium (TC = 1 sec).	
			1	0							Fast (TC = 0.2 sec).	
			1	1							Adaptive.	
0x2E	Chroma Gain Control 2	CMG[7:0]. Chroma manual gain lower 8 bits. See CMG[11:8] for description.	0	0	0	0	0	0	0	0	CMG[11:0] = 750d; gain is 1 in NTSC; CMG[11:0] = 741d; gain is 1 in PAL.	Min value is 0d (G = –60 dB) Max value is 3750 (G = 5).
0x2F	Luma Gain Control 1	LMG[11:8]. Luma manual gain can be used to program a desired manual chroma gain or to read back the actual gain value used.					x	x	x	x	LAGC[1:0] settings decide in which mode LMG[11:0] operates.	
		Reserved			1	1					Set to 1.	
		LAGT[1:0]. Luma automatic gain timing allows adjustment of the luma AGC tracking speed.	0	0							Slow (TC = 2 sec).	Has an effect only if LAGC[1:0] is set to auto gain (001, 010, 011,or 100).
			0	1							Medium (TC = 1 sec).	
			1	0							Fast (TC = 0.2 sec).	
			1	1							Adaptive.	
0x30	Luma Gain Control 2	LMG[7:0]. Luma manual gain can be used to program a desired manual chroma gain or read back the actual used gain value.	x	x	x	x	x	x	x	x	LMG[11:0] = 1234 dec; gain is 1 in NTSC. LMG[11:0] = 1266d; gain is 1 in PAL.	Min value: NTSC 1024 (G = 0.85), PAL (G = 0.81). Max value: NTSC 2468 (G = 2), PAL = 2532 (G = 2).
0x31	VS and FIELD Control 1	Reserved						0	1	0	Set to default.	
		HVSTIM. Selects where within a line of video the VS signal is asserted.					0				Start of line relative to HSE.	HSE = Hsync end.
							1				Start of line relative to HSB.	HSB = Hsync begin.
		NEWAVMODE. Sets the EAV/SAV mode.				0					EAV/SAV codes generated to suit ADI encoders.	
						1					Manual VS/field position controlled by Registers 0x32, 0x33, and 0xE5 to 0xEA.	
		Reserved	0	0	0						Set to default.	
0x32	Vsync Field Control 2	Reserved										NEWAVMODE bit must be set high.
					0	0	0	0	0	1	Set to default.	
		VSBHE		0							VS goes high in the middle of the line (even field).	
				1							VS changes state at the start of the line (even field).	
		VSBHO	0								VS goes high in the middle of the line (odd field).	
			1								VS changes state at the start of the line (odd field).	
0x33	Vsync Field Control 3	Reserved			0	0	0	1	0	0	Set to default.	
		VSEHE		0							VS goes low in the middle of the line (even field).	NEWAVMODE bit must be set high.
				1							VS changes state at the start of the line (even field).	
		VSEHO	0								VS goes low in the middle of the line (odd field).	
			1								VS changes state at the start of the line odd field.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x34	HS Position Control 1	HSE[10:8]. HS end allows the positioning of the HS output within the video line.						0	0	0	HS output ends HSE[10:0] pixels after the falling edge of Hsync.	Using HSB and HSE the user can program the position and length of the output Hsync.
		Reserved					0				Set to 0.	
		HSB[10:8]. HS begin allows the positioning of the HS output within the video line.		0	0	0					HS output starts HSB[10:0] pixels after the falling edge of Hsync.	
		Reserved	0								Set to 0.	
0x35	HS Position Control 2	HSB[7:0] Using HSB[10:0] and HSE[10:0], the user can program the position and length of HS output signal.	0	0	0	0	0	0	1	0		
0x36	HS Position Control 3	HSE[7:0] See above.	0	0	0	0	0	0	0	0		
0x37	Polarity	PCLK. Sets the polarity of LLC1.								0	Invert polarity.	
										1	Normal polarity as per the timing diagrams.	
		Reserved.						0	0		Set to 0.	
		PF. Sets the FIELD polarity.					0				Active high.	
							1				Active low.	
		Reserved.				0					Set to 0.	
		PVS. Sets the VS polarity.			0						Active high.	
					1						Active low.	
		Reserved		0							Set to 0.	
		PHS. Sets HS polarity.	0								Active high.	
			1								Active low.	
0x38	NTSC Comb Control	YCMN[2:0]. Luma comb mode, NTSC.						0	0	0	Adaptive 3-line, 3-tap luma .	
								1	0	0	Use low-pass notch.	
								1	0	1	Fixed luma comb (2-line).	Top lines of memory.
								1	1	0	Fixed luma comb (3-Line).	All lines of memory.
								1	1	1	Fixed luma comb (2-line).	Bottom lines of memory.
		CCMN[2:0]. Chroma comb mode, NTSC.			0	0	0				3-line adaptive for CTAPSN = 01; 4-line adaptive for CTAPSN = 10; 5-line adaptive for CTAPSN = 11.	
					1	0	0				Disable chroma comb.	
					1	0	1				Fixed 2-line for CTAPSN = 01; Fixed 3-line for CTAPSN = 10; Fixed 4-line for CTAPSN = 11.	Top lines of memory.
					1	1	0				Fixed 3-line for CTAPSN = 01; Fixed 4-line for CTAPSN = 10; Fixed 5-line for CTAPSN = 11.	All lines of memory.
					1	1	1				Fixed 2-line for CTAPSN = 01; Fixed 3-line for CTAPSN = 10; Fixed 4-line for CTAPSN = 11.	Bottom lines of memory.
		CTAPSN[1:0]. Chroma comb taps, NTSC.	0	0							Adapts 3 lines – 2 lines.	
			0	1							Not used.	
			1	0							Adapts 5 lines – 3 lines.	
			1	1							Adapts 5 lines – 4 lines.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x39	PAL Comb Control	YCMP[2:0]. Luma Comb mode, PAL.						0	0	0	Adaptive 5-line, 3-tap luma comb.	
								1	0	0	Use low-pass notch.	
								1	1	0	Fixed luma comb.	Top lines of memory.
								1	1	0	Fixed luma comb (5-line).	All lines of memory.
								1	1	1	Fixed luma comb (3-line).	Bottom lines of memory.
		CCMP[2:0]. Chroma Comb mode, PAL.			0	0	0				3-line adaptive for CTAPSN = 01; 4-line adaptive for CTAPSN = 10; 5-line adaptive for CTAPSN = 11.	
					1	0	0				Disable chroma comb	
					1	0	1				Fixed 2-line for CTAPSN = 01.	Top lines of memory.
											Fixed 3-line for CTAPSN = 10.	
											Fixed 4-line for CTAPSN = 11.	
					1	1	0				Fixed 3-line for CTAPSN = 01.	All lines of memory.
											Fixed 4-line for CTAPSN = 10.	
											Fixed 5-line for CTAPSN = 11.	
					1	1	1				Fixed 2-line for CTAPSN = 01.	Bottom lines of memory.
											Fixed 3-line for CTAPSN = 10.	
											Fixed 4-line for CTAPSN = 11.	
		CTAPSP[1:0]. Chroma comb taps, PAL.	0	0							Not used.	
			0	1							Adapts 5 lines – 3 lines (2 taps).	
			1	0							Adapts 5 lines – 3 lines (3 taps).	
			1	1							Adapts 5 lines – 4 lines (4 taps).	
0x3A		Reserved								0	Set as default.	
		PWRDN_ADC_2. Enables power-down of ADC2.							0		ADC2 normal operation.	
									1		Power down ADC2.	
		PWRDN_ADC_1. Enables power-down of ADC1.						0			ADC1 normal operation.	
								1			Power down ADC1.	
		PWRDN_ADC_0. Enables power-down of ADC0.					0				ADC0 normal operation.	
							1				Power down ADC0.	
		Reserved	0	0	0	1					Set as default.	
0x3D	Manual Window Control	Reserved					0	0	1	1	Set to default.	
		CKILLTHR[2:0].		0	0	0					Kill at 0.5%.	CKE = 1 enables the color kill function and must be enabled for CKILLTHR[2:0] to take effect.
				0	0	1					Kill at 1.5%.	
				0	1	0					Kill at 2.5%.	
				0	1	1					Kill at 4%.	
				1	0	0					Kill at 8.5%.	
				1	0	1					Kill at 16%.	
				1	1	0					Kill at 32%.	
				1	1	1					Reserved.	
		Reserved	0								Set to default.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x41	Resample Control	Reserved			0	1	0	0	0	0	Set to default.	
		SFL_INV. Controls the behavior of the PAL switch bit.		0							SFL compatible with ADV7190/ADV7191/ ADV7194 encoders.	
				1							SFL compatible with ADV717x/ADV7173x encoders.	
		Reserved	0								Set to default.	
0x48	Gemstar Control 1	GDECEL[15:8]. See the Comments column.	0	0	0	0	0	0	0	0	GDECEL[15:0]. 16 individual enable bits that select the lines of video (even field Lines 10 to 25) that the decoder checks for Gemstar-compatible data.	LSB = Line 10; MSB = Line 25. Default = Do not check for Gemstar-compatible data on any lines[10 to 25] in even fields.
0x49	Gemstar Control 2	GDECEL[7:0]. See Comments column.	0	0	0	0	0	0	0	0		
0x4A	Gemstar Control 3	GDECOL[15:8]. See the Comments column.	0	0	0	0	0	0	0	0	GDECOL[15:0]. 16 individual enable bits that select the lines of video (odd field lines 10 to 25) that the decoder checks for Gemstar-compatible data.	LSB = Line 10; MSB = Line 25. Default = Do not check for Gemstar-compatible data on any lines[10 to 25] in odd fields.
0x4B	Gemstar Control 4	GDECOL[7:0]. See Comments column.	0	0	0	0	0	0	0	0		
0x4C	Gemstar Control 5	GDECAD. Controls the manner in which decoded Gemstar data is inserted into the horizontal blanking period.								0	Split data into half byte.	To avoid 00/FF code.
										1	Output in straight 8-bit format.	
		Reserved	x	x	x	x	x	x	x		Undefined.	
0x4D	CTI DNR Control 1	CTI_EN. CTI enable.								0	Disable CTI.	
										1	Enable CTI.	
		CTI_AB_EN. Enables the mixing of the transient improved chroma with the original signal.							0		Disable CTI alpha blender.	
									1		Enable CTI alpha blender.	
		CTI_AB[1:0]. Controls the behavior of the alpha-blend circuitry.					0	0			Sharpest mixing.	
							0	1			Sharp mixing.	
							1	0			Smooth.	
							1	1			Smoothest.	
		Reserved				0					Set to default.	
		DNR_EN. Enable or bypass the DNR block.			0						Bypass the DNR block.	
					1						Enable the DNR block.	
		Reserved	1	1							Set to default.	
0x4E	CTI DNR Control 2	CTI_CTH[7:0]. Specifies how big the amplitude step must be to be steepened by the CTI block.	0	0	0	0	1	0	0	0	Set to 0x04 for A/V input; set to 0x0A for tuner input.	
0x50	CTI DNR Control 4	DNR_TH[7:0]. Specifies the maximum edge that is interpreted as noise and is therefore blanked.	0	0	0	0	1	0	0	0		

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x51	Lock Count	CIL[2:0]. Count-into-lock determines the number of lines the system must remain in lock before showing a locked status.						0	0	0	1 line of video.	
								0	0	1	2 lines of video.	
								0	1	0	5 lines of video.	
								0	1	1	10 lines of video.	
								1	0	0	100 lines of video.	
								1	0	1	500 lines of video.	
								1	1	0	1000 lines of video.	
								1	1	1	100000 lines of video.	
		COL[2:0]. Count-out-of-lock determines the number of lines the system must remain out-of-lock before showing a lost-locked status.			0	0	0				1 line of video.	
					0	0	1				2 lines of video.	
					0	1	0				5 lines of video.	
					0	1	1				10 lines of video.	
					1	0	0				100 lines of video.	
					1	0	1				500 lines of video.	
					1	1	0				1000 lines of video.	
					1	1	1				100000 lines of video.	
		SRLS. Select raw lock signal. Selects the determination of the lock status.		0							Over field with vertical info.	
				1							Line-to-line evaluation.	
		FSCLE. Fsc lock enable.	0								Lock status set only by horizontal lock.	
			1								Lock status set by horizontal lock and subcarrier lock.	
0x8F	Free Run Line Length 1	Reserved					0	0	0	0	Set to default.	
		LLC_PAD_SEL[2:0]. Enables manual selection of clock for LLC1 pin.		0	0	0					LLC1 (nominal 27 MHz) selected out on LLC1 pin.	
				1	0	1					LLC2 (nominally 13.5 MHz) selected out on LLC1 pin.	For 16-bit 4:2:2 out, OF_SEL[3:0] = 0010.
		Reserved	0								Set to default.	
0x90	VBI Info (Read Only)	WSSD. Screen signaling detected.								0	No WSS detected.	Read only status bits.
										1	WSS detected.	
		CCAPD. Closed caption data.							0		No CCAP signals detected.	
									1		CCAP sequence detected.	
		EDTVD. EDTV sequence.						0			No EDTV sequence detected.	
								1			EDTV sequence detected.	
		CGMSD. CGMS sequence.					0				No CGMS transition detected.	
							1				CGMS sequence decoded.	
		Reserved.	x	x	x	x						
0x91	WSS1 (Read Only)	WSS1[7:0] Wide screen signaling data.	x	x	x	x	x	x	x	x		
0x92	WSS2 (Read Only)	WSS2[7:0] Wide screen signaling data.	x	x	x	x	x	x	x	x	WSS2[7:6] are undetermined.	
0x93	WSS2 (Read Only)	WSS2[7:0] Wide screen signaling data.	x	x	x	x	x	x	x	x		
0x94	EDTV2 (Read Only)	EDTV2[7:0] EDTV data register.	x	x	x	x	x	x	x	x		
0x95	EDTV3 (Read Only)	EDTV3[7:0] EDTV data register.	x	x	x	x	x	x	x	x	EDTV3[7:6] are undetermined.	EDTV3[5] is reserved for future use.
0x96	CGMS1 (Read Only)	CGMS1[7:0] CGMS data register.	x	x	x	x	x	x	x	x		

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0x97	CGMS2 (Read Only)	CGMS2[7:0] CGMS data register.	x	x	x	x	x	x	x	x		
0x98	CGMS3 (Read Only)	CGMS3[7:0] CGMS data register.	x	x	x	x	x	x	x	x	CGMS3[7:4] are undetermined.	
0x99	CCAP1 (Read Only)	CCAP1[7:0] Closed caption data register.	x	x	x	x	x	x	x	x	CCAP1[7] contains parity bit for byte 0.	
0x9A	CCAP2 (Read Only)	CCAP2[7:0] Closed caption data register.	x	x	x	x	x	x	x	x	CCAP2[7] contains parity bit for byte 0.	
0x9B	Letterbox 1 (Read Only)	LB_LCT[7:0] Letterbox data register.	x	x	x	x	x	x	x	x	Reports the number of black lines detected at the top of active video.	This feature examines the active video at the start and at the end of each field. It enables format detection even if the video is not accompanied by a CGMS or WSS sequence.
0x9C	Letterbox 2 (Read Only)	LB_LCM[7:0] Letterbox data register.	x	x	x	x	x	x	x	x	Reports the number of black lines detected in the bottom half of active video if subtitles are detected.	
0x9D	Letterbox 3 (Read Only)	LB_LCB[7:0] Letterbox data register.	x	x	x	x	x	x	x	x	Reports the number of black lines detected at the bottom of active video.	
0xB2	CRC Enable Write Register	Reserved.							0	0	Set as default.	
		CRC_ENABLE. Enable CRC checksum decoded from CGMS packet to validate CGMSD.						0			Turn off CRC check.	
								1			CGMSD goes high with valid checksum.	
		Reserved	0	0	0	1	1				Set as default.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0xC3	ADC SWITCH 1	ADC0_SW[3:0]. Manual muxing control for ADC0.					0	0	0	0	No connection.	SETADC_sw_man_en = 1.
							0	0	0	1	AIN1.	
							0	0	1	0	AIN2.	
							0	0	1	1	AIN3.	
							0	1	0	0	AIN4.	
							0	1	0	1	AIN5.	
							0	1	1	0	AIN6.	
							0	1	1	1	No connection.	
							1	0	0	0	No connection.	
							1	0	0	1	AIN7.	
							1	0	1	0	AIN8.	
							1	0	1	1	AIN9.	
							1	1	0	0	AIN10.	
							1	1	0	1	AIN11.	
							1	1	1	0	AIN12.	
							1	1	1	1	No connection.	
		ADC1_SW[3:0]. Manual muxing control for ADC1.	0	0	0	0					No connection.	SETADC_sw_man_en = 1.
			0	0	0	1					No connection.	
			0	0	1	0					No connection.	
			0	0	1	1					AIN3.	
			0	1	0	0					AIN4.	
			0	1	0	1					AIN5.	
			0	1	1	0					AIN6.	
			0	1	1	1					No connection.	
			1	0	0	0					No connection.	
			1	0	0	1					No connection.	
			1	0	1	0					No connection.	
			1	0	1	1					AIN9.	
			1	1	0	0					AIN10.	
			1	1	0	1					AIN11.	
			1	1	1	0					AIN12.	
			1	1	1	1					No connection.	
0xC4	ADC SWITCH 2	ADC2_SW[3:0]. Manual muxing control for ADC2.					0	0	0	0	No connection.	SETADC_sw_man_en = 1.
							0	0	0	1	No connection.	
							0	0	1	0	AIN2.	
							0	0	1	1	No connection.	
							0	1	0	0	No connection.	
							0	1	0	1	AIN5.	
							0	1	1	0	AIN6.	
							0	1	1	1	No connection.	
							1	0	0	0	No connection.	
							1	0	0	1	No connection.	
							1	0	1	0	AIN8.	
							1	0	1	1	No connection.	
							1	1	0	0	No connection.	
							1	1	0	1	AIN11.	
							1	1	1	0	AIN12.	
							1	1	1	1	No connection.	
		Reserved		x	x	x						
		ADC_SW_MAN_EN. Enable manual setting of the input signal muxing.	0								Disable.	
			1								Enable.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0xDC	Letterbox Control 1	LB_TH[4:0]. Sets the threshold value that determines if a line is black.				0	1	1	0	0	Default threshold for the detection of black lines.	
		Reserved	1	0	1						Set as default.	
0xDD	Letterbox Control 2	LB_EL[3:0]. Programs the end line of the activity window for LB detection (end of field).					1	1	0	0	LB detection ends with the last line of active video on a field, 1100b: 262/525.	
		LB_SL[3:0]. Program the start line of the activity window for LB detection (start of field).	0	1	0	0					Letterbox detection aligned with the start of active video, 0100b: 23/286 NTSC.	
0xDE		Reserved	0	0	0	0	0	0	0	0		
0xDF		Reserved	0	0	0	0	0	0	0	0		
0xE0		Reserved	0	0	0	1	0	1	0	0		
0xE1	SD Offset Cb	SD_OFF_CB[7:0]. Adjusts the hue by selecting the offset for the Cb channel.	1	0	0	0	0	0	0	0		
0xE2	SD Offset Cr	SD_OFF_CR[7:0]. Adjusts the hue by selecting the offset for the Cr channel.	1	0	0	0	0	0	0	0		
0xE3	SD Saturation Cb	SD_SAT_CB[7:0]. Adjusts the saturation of the picture by affecting gain on the Cb channel.	1	0	0	0	0	0	0	0	Chroma gain = 0 dB.	
0xE4	SD Saturation Cr	SD_SAT_CR[7:0]. Adjusts the saturation of the picture by affecting gain on the Cr channel.	1	0	0	0	0	0	0	0	Chroma gain = 0 dB.	
0xE5	NTSC V Bit Begin	NVBEG[4:0]. Number of lines after I_{COUNT} rollover to set V high.				0	0	1	0	1	NTSC default (BT.656).	
		NVBEGSIGN			0						Set to low when manual programming.	
					1						Not suitable for user programming.	
		NVBEGDELE. Delay V bit going high by one line relative to NVBEG (even field).		0							No delay.	
				1							Additional delay by 1 line.	
		NVBEGDELO. Delay V bit going high by one line relative to NVBEG (odd field).	0								No delay.	
			1								Additional delay by 1 line.	
0xE6	NTSC V Bit End	NVEND[4:0]. Number of lines after I_{COUNT} rollover to set V low.				0	0	1	0	0	NTSC default (BT.656).	
		NVENDSIGN			0						Set to low when manual programming.	
					1						Not suitable for user programming.	
		NVENDDELE. Delay V bit going low by one line relative to NVEND (even field).		0							No delay.	
				1							Additional delay by 1 line.	
		NVENDDELO. Delay V bit going low by one line relative to NVEND (odd field).	0								No delay.	
			1								Additional delay by 1 line.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments	Notes
0xE7	NTSC F Bit Toggle	NFTOG[4:0]. Number of lines after I_{COUNT} rollover to toggle F signal.				0	0	0	1	1	NTSC default.	
		NFTOGSIGN			0						Set to low when manual programming.	
					1						Not suitable for user programming.	
		NFTOGDELE. Delay F transition by one line relative to NFTOG (even field).		0							No delay.	
				1							Additional delay by 1 line.	
		NFTOGDELO. Delay F transition by one line relative to NFTOG (odd field).	0								No delay.	
			1								Additional delay by 1 line.	
0xE8	PAL V Bit Begin	PVBEG[4:0]. Number of lines after I_{COUNT} rollover to set V high.				0	0	1	0	1	PAL default (BT.656).	
		PVBEGSIGN			0						Set to low when manual programming.	
					1						Not suitable for user programming.	
		PVBEGDELE. Delay V bit going high by one line relative to PVBEG (even field).		0							No delay.	
				1							Additional delay by 1 line.	
		PVBEGDELO. Delay V bit going high by one line relative to PVBEG (odd field).	0								No delay.	
			1								Additional delay by 1 line.	
0xE9	PAL V Bit End	PVEND[4:0]. Number of lines after I_{COUNT} rollover to set V low.				1	0	1	0	0	PAL default (BT.656).	
		PVENDSIGN			0						Set to low when manual programming.	
					1						Not suitable for user programming.	
		PVENDDELE. Delay V bit going low by one line relative to PVEND (even field).		0							No delay.	
				1							Additional delay by 1 line.	
		PVENDDELO. Delay V bit going low by one line relative to PVEND (odd field).	0								No delay.	
			1								Additional delay by 1 line.	
0xEA	PAL F Bit Toggle	PFTOG[4:0]. Number of lines after I_{COUNT} rollover to toggle F signal.				0	0	0	1	1	PAL default (BT.656).	
		PFTOGSIGN			0						Set to low when manual programming.	
					1						Not suitable for user programming.	
		PFTOGDELE. Delay F transition by one line relative to PFTOG (even field).		0							No delay.	
				1							Additional delay by 1 line.	
		PFTOGDELO. Delay F transition by one line relative to PFTOG (odd field).	0								No delay.	
			1								Additional delay by 1 line.	

Subaddress	Register	Bit Description	Bits 7	6	5	4	3	2	1	0	Comments		Notes
0xF4	Drive Strength	DR_STR_S[1:0]. Select the drive strength for the sync output signals.							0	0	Low drive strength (1×).		
									0	1	Medium-low drive strength (2×).		
									1	0	Medium-high drive strength (3×).		
									1	1	High drive strength (4×).		
		DR_STR_C[1:0]. Select the drive strength for the clock output signal.					0	0			Low drive strength (1×).		
							0	1			Medium-low drive strength (2×).		
							1	0			Medium-high drive strength (3×).		
							1	1			High drive strength (4×).		
		DR_STR[1:0]. Select the drive strength for the data output signals. Can be increased or decreased for EMC or crosstalk reasons.			0	0					Low drive strength (1×).		
					0	1					Medium-low drive strength (2×).		
					1	0					Medium-high drive strength (3×).		
					1	1					High drive strength (4×).		
		Reserved	x	x							No delay.		
0xF8	IF Comp Control	IFFILTSEL[2:0] IF filter selection for PAL and NTSC						0	0	0	Bypass mode.		0 dB.
											2 MHz	**5 MHz**	NTSC filters.
								0	0	1	−3 dB	−2 dB	
								0	1	0	−6 dB	+3.5 dB	
								0	1	1	−10 dB	+5 dB	
								1	0	0	Reserved.		
											3 MHz	**6 MHz**	PAL filters.
								1	0	1	−2 dB	+2 dB	
								1	1	0	−5 dB	+3 dB	
								1	1	1	−7 dB	+5 dB	
		Reserved	0	0	0	0	0						
0xF9	VS Mode Control	EXTEND_VS_MAX_FREQ								0	Limit maximum Vsync frequency to 66.25 Hz (475 lines/frame).		
										1	Limit maximum Vsync frequency to 70.09 Hz (449 lines/frame).		
		EXTEND_VS_MIN_FREQ							0		Limit minimum Vsync frequency to 42.75 Hz (731 lines/frame).		
									1		Limit minimum Vsync frequency to 39.51 Hz (791 lines/frame).		
		VS_COAST_MODE[1:0]					0	0			Auto coast mode.		This value sets up the output coast frequency.
							0	1			50 Hz coast mode.		
							1	0			60 Hz coast mode.		
							1	1			Reserved.		
		Reserved	0	0	0	0							

I²C PROGRAMMING EXAMPLES

EXAMPLES IN THIS SECTION USE A 28 MHz CLOCK.

Mode 1 CVBS Input (Composite Video on AIN5)

All standards are supported through autodetect, 8-bit, 4:2:2, ITU-R BT.656 output on P15 to P8.

Table 87. Mode 1 CVBS Input

Register Address	Register Value	Notes
0x00	0x04	CVBS input on AIN5.
0x15	0x00	Slow down digital clamps.
0x17	0x41	Set CSFM to SH1.
0x1D	0x40	Enable 28 MHz crystal.
0x0F	0x40	TRAQ.
0x3A	0x16	Power down ADC 1 and ADC 2.
0x3D	0xC3	MWE enable manual window.
0x3F	0xE4	BGB to 36.
0x50	0x04	Set DNR threshold to 4 for flat response.
0x0E	0x80	ADI recommended programming sequence. This sequence must be followed exactly when setting up the decoder.
0x50	0x20	Recommended setting.
0x52	0x18	Recommended setting.
0x58	0xED	Recommended setting.
0x77	0xC5	Recommended setting.
0x7C	0x93	Recommended setting.
0x7D	0x00	Recommended setting.
0x90	0xC9	Recommended setting.
0x91	0x40	Recommended setting.
0x92	0x3C	Recommended setting.
0x93	0xCA	Recommended setting.
0x94	0xdD	Recommended setting.
0xCF	0x50	Recommended setting.
0xD0	0x4E	Recommended setting.
0xD6	0xDD	Recommended setting.
0xE5	0x51	Recommended setting.
0xD5	0xA0	Recommended setting.
0xD7	0xEA	Recommended setting.
0xE4	0x3E	Recommended setting.
0xE9	0x3E	Recommended setting.
0xEA	0x0F	Recommended setting.
0x0E	0x00	Recommended setting.

Mode 2 S-Video Input (Y on AIN1 and C on AIN4)

All standards are supported through autodetect, 8-bit, ITU-R BT.656 output on P15 to P8.

Table 88. Mode 2 S-Video Input

Register Address	Register Value	Notes
0x00	0x06	Y1 = AIN1, C1 = AIN4.
0x15	0x00	Slow down digital clamps.
0x3A	0x12	Power down ADC 2.
0x1D	0x40	Enable 28 MHz crystal.
0x0F	0x40	TRAQ.
0x3D	0xC3	MWE enable manual window.
0x3F	0xE4	BGB to 36.
0x50	0x04	Set DNR threshold to 4 for flat response.
0x0E	0x80	ADI recommended programming sequence. This sequence must be followed exactly when setting up the decoder.
0x50	0x20	Recommended setting.
0x52	0x18	Recommended setting.
0x58	0xED	Recommended setting.
0x77	0xC5	Recommended setting.
0x7C	0x93	Recommended setting.
0x7D	0x00	Recommended setting.
0x90	0xC9	Recommended setting.
0x91	0x40	Recommended setting.
0x92	0x3C	Recommended setting.
0x93	0xCA	Recommended setting.
0x 94	0xdD	Recommended setting.
0xCF	0x50	Recommended setting.
0xD0	0x4E	Recommended setting.
0xD6	0xDD	Recommended setting.
0xE5	0x51	Recommended setting.
0xD5	0xA0	Recommended setting.
0xD7	0xEA	Recommended setting.
0xE4	0x3E	Recommended setting.
0xE9	0x3E	Recommended setting.
0xEA	0x0F	Recommended setting.
0x0E	0x00	Recommended setting.

Mode 3 525i/625i YPrPb Input (Y on AIN2, PB on AIN3, and PR on AIN6)

All standards are supported through autodetect, 8-bit, ITU-R BT.656 output on P15 to P8.

Table 89. Mode 3 YPrPb Input 525i/625i

Register Address	Register Value	Notes
0x00	0x0A	Y2 = AIN2, PB2 = AIN3, PR2 = AIN6.
0x1D	0x40	Enable 28 MHz crystal.
0x0F	0x40	TRAQ.
0x3D	0xC3	MWE enable manual window.
0x3F	0xE4	BGB to 36.
0x50	0x04	Set DNR threshold to 4 for flat response.
0x0E	0x80	ADI recommended programming sequence. This sequence must be followed exactly when setting up the decoder.
0x52	0x18	Recommended setting.
0x58	0xED	Recommended setting.
0x77	0xC5	Recommended setting.
0x7C	0x93	Recommended setting.
0x90	0xC9	Recommended setting.
0x91	0x40	Recommended setting.
0x92	0x3C	Recommended setting.
0x93	0xCA	Recommended setting.
0x94	0xdD	Recommended setting.
0xCF	0x50	Recommended setting.
0xD0	0x4E	Recommended setting.
0xD6	0xDD	Recommended setting.
0xE5	0x51	Recommended setting.
0xE9	0x3E	Recommended setting.
0x0E	0x00	Recommended setting.

Mode 4 CVBS Tuner Input PAL Only on AIN4

8-bit, ITU-R BT.656 output on P15 to P8.

Table 90. Mode 4 Tuner Input CVBS PAL Only

Register Address	Register Value	Notes
0x00	0x83	CVBS AIN4 Force PAL only mode.
0x07	0x01	Enable PAL autodetection only.
0x15	0x00	Slow down digital clamps.
0x17	0x41	Set CSFM to SH1.
0x1D	0x40	Enable 28 MHz crystal
0x0F	0x40	TRAQ
0x3D	0xC3	MWE enable manual window
0x3F	0xE4	BGB to 36
0x19	0xFA	Stronger dot crawl reduction.
0x3A	0x16	Power down ADC 1 and ADC 2.
0x50	0x0A	Set higher DNR threshold.
0x0E	0x80	ADI recommended programming sequence. This sequence must be followed exactly when setting up the decoder.
0x50	0x20	Recommended setting.
0x52	0x18	Recommended setting.
0x58	0xED	Recommended setting.
0x77	0xC5	Recommended setting.
0x7C	0x93	Recommended setting.
0x7D	0x00	Recommended setting.
0x90	0xC9	Recommended setting.
0x91	0x40	Recommended setting.
0x92	0x3C	Recommended setting.
0x93	0xCA	Recommended setting.
0x94	0xdD	Recommended setting.
0xCF	0x50	Recommended setting.
0xD0	0x4E	Recommended setting.
0xD6	0xDD	Recommended setting.
0xE5	0x51	Recommended setting.
0xD5	0xA0	Recommended setting.
0xD7	0xEA	Recommended setting.
0xE4	0x3E	Recommended setting.
0xE9	0x3E	Recommended setting.
0xEA	0x0F	Recommended setting.
0x0E	0x00	Recommended setting.

EXAMPLES USING 27 MHz CLOCK

Mode 1 CVBS Input (Composite Video on AIN5)

All standards are supported through autodetect, 8-bit, 4:2:2, ITU-R BT.656 output on P15 to P8.

Table 91. Mode 1 CVBS Input

Register Address	Register Value	Notes
0x00	0x04	CVBS input on AIN5.
0x15	0x00	Slow down digital clamps.
0x17	0x41	Set CSFM to SH1.
0x3A	0x16	Power down ADC 1 and ADC 2.
0x50	0x04	Set DNR threshold to 4 for flat response.
0x0E	0x80	ADI recommended programming sequence. This sequence must be followed exactly when setting up the decoder.
0x50	0x20	Recommended setting.
0x52	0x18	Recommended setting.
0x58	0xED	Recommended setting.
0x77	0xC5	Recommended setting.
0x7C	0x93	Recommended setting.
0x7D	0x00	Recommended setting.
0xD0	0x48	Recommended setting.
0xD5	0xA0	Recommended setting.
0xD7	0xEA	Recommended setting.
0xE4	0x3E	Recommended setting.
0xE9	0x3E	Recommended setting
0xEA	0x0F	Recommended setting.
0x0E	0x00	Recommended setting.

Mode 2 S-Video Input (Y on AIN1 and C on AIN4)

All standards are supported through autodetect, 8-bit, ITU-R BT.656 output on P15 to P8.

Table 92. Mode 2 S-Video Input

Register Address	Register Value	Notes
0x00	0x06	Y1 = AIN1, C1 = AIN4.
0x15	0x00	Slow down digital clamps.
0x3A	0x12	Power down ADC 2.
0x50	0x04	Set DNR threshold to 4 for flat response.
0x0E	0x80	ADI recommended programming sequence. This sequence must be followed exactly when setting up the decoder.
0x50	0x20	Recommended setting.
0x52	0x18	Recommended setting.
0x58	0xED	Recommended setting.
0x77	0xC5	Recommended setting.
0x7C	0x93	Recommended setting.
0x7D	0x00	Recommended setting.
0xD0	0x48	Recommended setting.
0xD5	0xA0	Recommended setting.
0xD7	0xEA	Recommended setting.
0xE4	0x3E	Recommended setting.
0xE9	0x3E	Recommended setting
0xEA	0x0F	Recommended setting.
0x0E	0x00	Recommended setting.

Mode 3 525i/625i YPrPb Input (Y on AIN2, PB on AIN3, and PR on AIN6)

All standards are supported through autodetect, 8-bit, ITU-R BT.656 output on P15 to P8.

Table 93. Mode 3 YPrPb Input 525i/625i

Register Address	Register Value	Notes
0x00	0x0A	Y2 = AIN2, PB2 = AIN3, PR2 = AIN6.
0x50	0x04	Set DNR threshold to 4 for flat response.
0x0E	0x80	ADI recommended programming sequence. This sequence must be followed exactly when setting up the decoder.
0x52	0x18	Recommended setting.
0x58	0xED	Recommended setting.
0x77	0xC5	Recommended setting.
0x7C	0x93	Recommended setting.
0x7D	0x00	Recommended setting.
0xD0	0x48	Recommended setting.
0xD5	0xA0	Recommended setting.
0xE4	0x3E	Recommended setting.
0xE9	0x3E	Recommended setting
0x0E	0x00	Recommended setting.

Mode 4 CVBS Tuner Input PAL Only on AIN4

8-bit, ITU-R BT.656 output on P15 to P8.

Table 94. Mode 4 Tuner Input CVBS PAL Only

Register Address	Register Value	Notes
0x00	0x83	CVBS AIN4 Force PAL only mode.
0x07	0x01	Enable PAL autodetection only.
0x15	0x00	Slow down digital clamps.
0x17	0x41	Set CSFM to SH1.
0x19	0xFA	Stronger dot crawl reduction.
0x3A	0x16	Power down ADC 1 and ADC 2.
0x50	0x0A	Set higher DNR threshold.
0x0E	0x80	ADI recommended programming sequence. This sequence must be followed exactly when setting up the decoder.
0x50	0x20	Recommended setting.
0x52	0x18	Recommended setting.
0x58	0xED	Recommended setting.
0x77	0xC5	Recommended setting.
0x7C	0x93	Recommended setting.
0x7D	0x00	Recommended setting.
0xD0	0x48	Recommended setting.
0xD5	0xA0	Recommended setting.
0xD7	0xEA	Recommended setting.
0xE4	0x3E	Recommended setting.
0xE9	0x3E	Recommended setting
0xEA	0x0F	Recommended setting.
0x0E	0x00	Recommended setting.

PCB LAYOUT RECOMMENDATIONS

The ADV7183B is a high precision, high speed, mixed-signal device. To achieve the maximum performance from the part, it is important to have a PCB board with a good layout. This section provides guidelines for designing a board using the ADV7183B.

ANALOG INTERFACE INPUTS

Care should be taken when routing the inputs on the PCB. Track lengths should be kept to a minimum, and 75 Ω trace impedances should be used when possible. Trace impedances other than 75 Ω also increase the chance of reflections.

POWER SUPPLY DECOUPLING

It is recommended to decouple each power supply pin with 0.1 µF and 10 nF capacitors. The fundamental idea is to have a decoupling capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the ADV7183B, as doing so interposes resistive vias in the path. The decoupling capacitors should be located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the 100 nF capacitor pads, down to the power plane, is generally the best approach (see Figure 41).

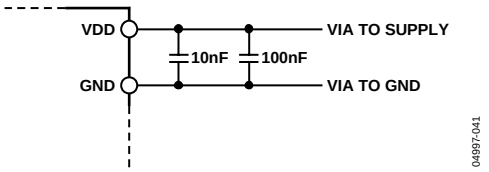


Figure 41. Recommended Power Supply Decoupling

It is very important to maintain low noise and good stability of PVDD. Careful attention must be paid to regulation, filtering, and decoupling. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (AVDD, DVDD, DVDDIO, and PVDD).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can, in turn, produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PVDD, from a different, cleaner power source, such as a 12 V supply.

It is also recommended to use a single ground plane for the entire board. This ground plane should have a space between the analog and digital sections of the PCB (see Figure 42).

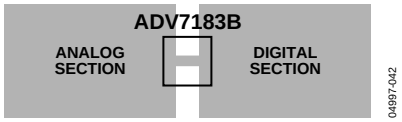


Figure 42. PCB Ground Layout

Experience shows that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases, it is recommended to place a single ground plane under the ADV7183B. The location of the split should be under the ADV7183B. For this case, it is even more important to place components wisely because the current loops will be much longer (current takes the path of least resistance). An example of a current loop: power plane to ADV7183B to digital output trace to digital data receiver to digital ground plane to analog ground plane.

PLL

Place the PLL loop filter components as close as possible to the ELPF pin. Do not place any digital or other high frequency traces near these components. Use the values suggested in Figure 46 with tolerances of 10% or less.

DIGITAL OUTPUTS (BOTH DATA AND CLOCKS)

Try to minimize the trace length the digital outputs have to drive. Longer traces have higher capacitance, which requires more current, which causes more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a 30 Ω to 50 Ω series resistor can suppress reflections, reduce EMI, and reduce the current spikes inside the ADV7183B. If series resistors are used, place them as close as possible to the ADV7183B pins. However, try not to add vias or extra length to the output trace to make the resistors closer.

If possible, limit the capacitance that each of the digital outputs drive to less than 15 pF. This can easily be accomplished by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the ADV7183B, creating more digital noise on its power supplies.

DIGITAL INPUTS

The digital inputs on the ADV7183B are designed to work with 3.3 V signals, and are not tolerant of 5 V signals. Extra components are needed if 5 V logic signals are required to be applied to the decoder.

ANTIALIASING FILTERS

For inputs from some video sources that are not bandwidth limited, signals outside the video band can alias back into the video band during A/D conversion and appear as noise on the output video. The ADV7183B oversamples the analog inputs by a factor of 4. This 54 MHz sampling frequency reduces the requirement for an input filter; for optimal performance, it is recommended that an antialiasing filter be used. The recommended low cost circuit for implementing this buffer and filter circuit for all analog input signals is shown in Figure 45.

The buffer is a simple emitter-follower using a single npn transistor. The antialiasing filter is implemented using passive components. The passive filter is a third-order Butterworth filter with a −3 dB point of 9 MHz. The frequency response of the passive filter is shown in Figure 43. The flat pass band up to 6 MHz is essential. The attenuation of the signal at the output of the filter due to the voltage divider of R24 and R63 is compensated for in the ADV7183B part by using the automatic gain control. The ac-coupling capacitor at the input to the buffer creates a high-pass filter with the biasing resistors for the transistor. This filter has a cutoff of

$$\{2 \times \pi \times (R39||R89) \times C93\}^{-1} = 0.62 \text{ Hz}$$

It is essential that the cutoff of this filter be less than 1 Hz to ensure correct operation of the internal clamps within the part. These clamps ensure the video stays within the 5 V range of the op amp used.

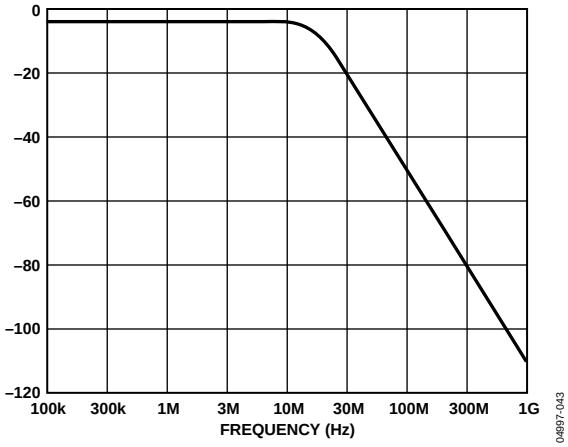


Figure 43. Third-Order Butterworth Filter Response

CRYSTAL LOAD CAPACITOR VALUE SELECTION

Figure 44 shows an example of a reference clock circuit for the ADV7183B. Special care must be taken when using a crystal circuit to generate the reference clock for the ADV7183B. Small variations in reference clock frequency can cause autodetection issues and impair the ADV7183B performance.

Load capacitor values are dependant on crystal attributes.

The load capacitance given in a crystal data sheet specifies the parallel resonance frequency within the tolerance at 25°C. Therefore, it is important to design a circuit that matches the load capacitance to achieve the frequency stipulated by the manufacturer. For accurate crystal circuit design and optimization, an applications note on crystal design considerations is available for more information.

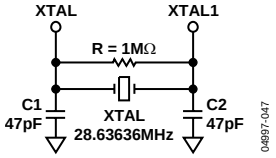


Figure 44. Crystal Circuit

Follow these guidelines to ensure correct operation:

- Use the correct frequency crystal, which is 28.63636 MHz. Tolerance is 50 ppm or higher.
- Use a parallel-resonant crystal.
- Place a 1 MΩ shunt resistor across pins XTAL and XTAL1, as is shown in Figure 44.
- Know the C_{LOAD} for the crystal part number selected. The value of Capacitor C1 and Capacitor C2 must match C_{LOAD} for the specific crystal part number in the user's system.
- Use the following guideline to find C_{LOAD}:

  $C1 = C2 = C$

  $C = 2(C_{LOAD} - C_S) - C_{pg}$

  where:

  C_{pg} is the pin-to-ground capacitance, approximately 4 pF to 10 pF.

  C_S is the PCB stray capacitance, approximately 2 pF to 3 pF.

  For Example,

  C_{LOAD} = 30 pF

  C = 2(30 − 3) − 4

  = 50 pF

  Therefore, two 47 pF capacitors may be selected for C1 and C2.

TYPICAL CIRCUIT CONNECTION

Figure 45 and Figure 46 show examples of how to connect the ADV7183B video decoder. For a detailed schematic diagram for the ADV7183B, refer to the ADV7183B evaluation note.

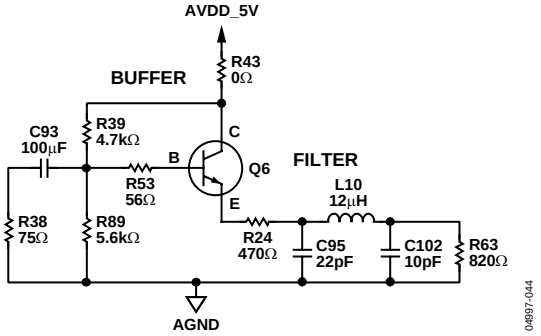


Figure 45. ADI Recommended Antialiasing Circuit for All Input Channels

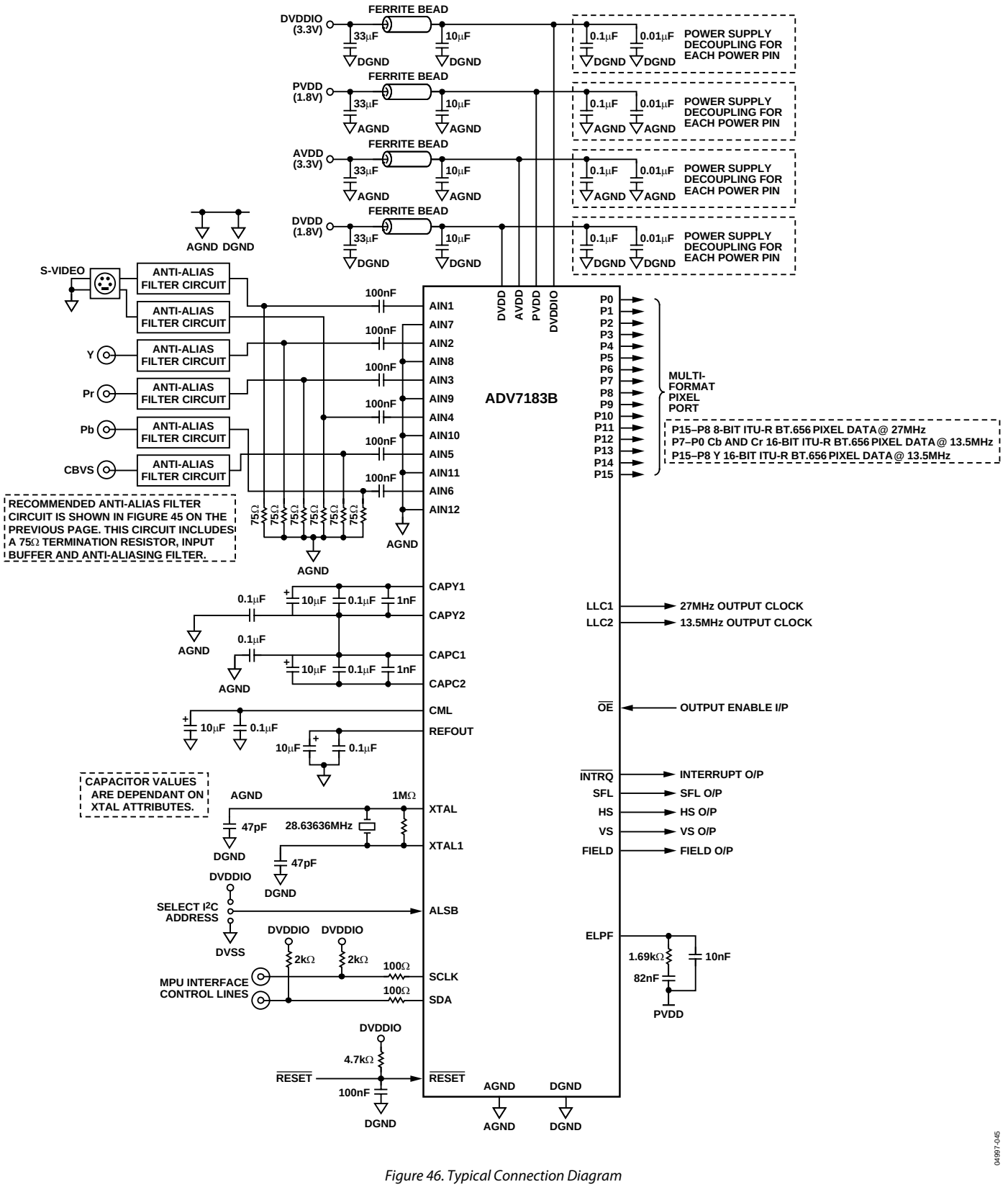
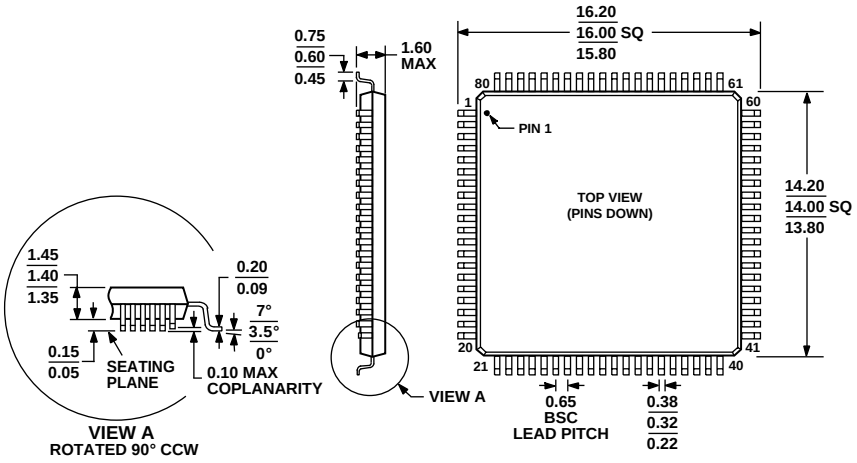


Figure 46. Typical Connection Diagram

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BEC

Figure 47. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADV7183BKSTZ[2]	0°C to +70°C	80-lead Low Profile Quad Flat Package (LQFP)	ST-80-2
ADV7183BBSTZ[2]	–40°C to +85°C	80-lead Low Profile Quad Flat Package (LQFP)	ST-80-2
EVAL-ADV7183BEB		Evaluation Board	

[1] The ADV7183B is a Pb-free, environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications and can withstand surface-mount soldering at up to 255°C (±5°C). In addition, the ADV71893B is backward-compatible with conventional SnPb soldering processes. This means the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.
[2] Z = Pb-free part.

NOTES

NOTES

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