

SN55138, SN75138 QUADRUPLE BUS TRANSCEIVERS

SLLS079B – SEPTEMBER 1973 – REVISED MAY 1995

- Single 5-V Supply
- High-Input-Impedance, High-Threshold Receivers
- Common Driver Strobe
- TTL-Compatible Driver and Strobe Inputs With Clamp Diodes
- High-Speed Operation
- 100-mA Open-Collector Driver Outputs
- Four Independent Channels
- TTL-Compatible Receiver Output

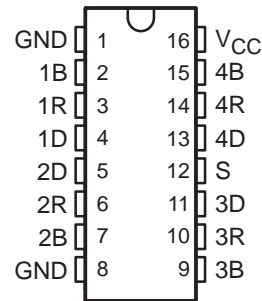
description

The SN55138 and SN75138 quadruple bus transceivers are designed for two-way data communication over single-ended transmission lines. Each of the four identical channels consists of a driver with TTL inputs and a receiver with a TTL output. The driver open-collector output is designed to handle loads up to 100-mA open collector. The receiver input is internally connected to the driver output, and has a high impedance to minimize loading of the transmission line. Because of the high driver-output current and the high receiver-input impedance, a very large number (typically hundreds) of transceivers may be connected to a single data bus.

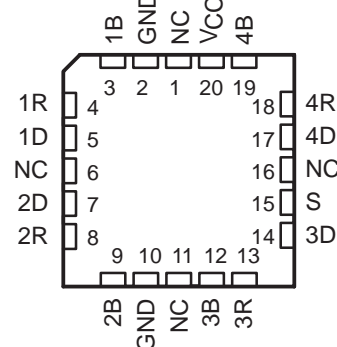
The receiver design also features a threshold of 2.3 V (typical), providing a wider noise margin than would be possible with a receiver having the usual TTL threshold. A strobe turns off all drivers (high impedance) but does not affect receiver operation. These circuits are designed for operation from a single 5-V supply and include a provision to minimize loading of the data bus when the power-supply voltage is zero.

The SN55138 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN75138 is characterized for operation from 0°C to 70°C .

SN55138 . . . J OR W PACKAGE
SN75138 . . . D OR N PACKAGE
(TOP VIEW)



SN55138 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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Function Tables

TRANSMITTING

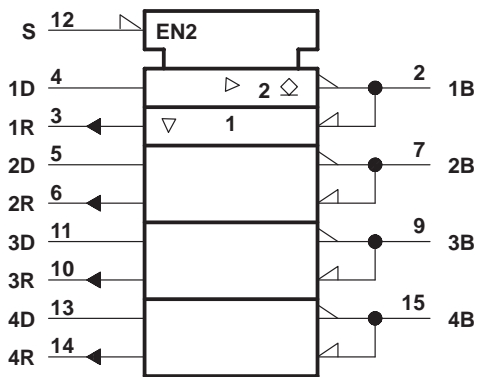
INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

RECEIVING

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

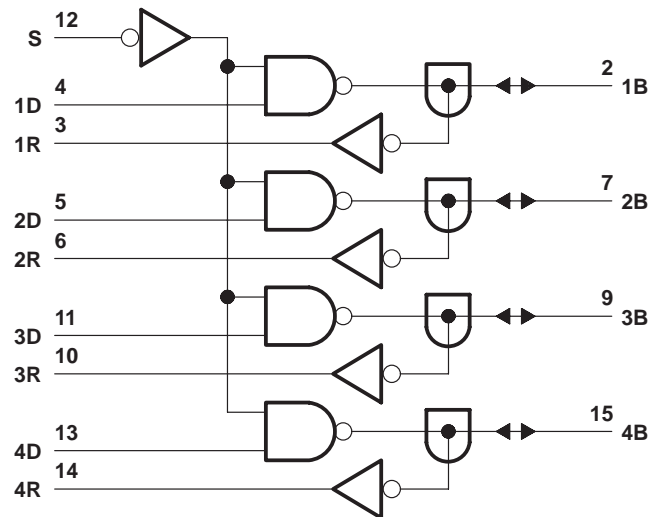
H = high level, L = low level, X = irrelevant

logic symbol†

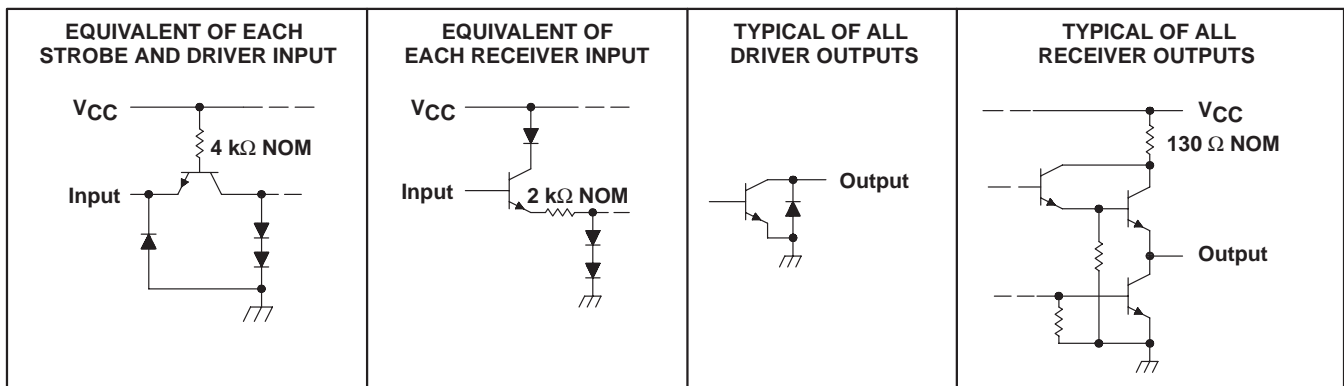


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)



schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	5.5 V
Driver off-state output voltage	7 V
Low-level output current into the driver output	150 mA
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A : SN55138	–55°C to 125°C
SN75138	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or W package	260°C
Case temperature for 60 seconds, T_C : FK package	260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J package	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to both ground terminals connected together.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$	DERATING FACTOR	$T_A = 70^\circ\text{C}$	$T_A = 125^\circ\text{C}$
	POWER RATING	ABOVE $T_A = 25^\circ\text{C}$	POWER RATING	POWER RATING
D	950 mW	7.6 mW/°C	608 mW	—
FK‡	1375 mW	11.0 mW/°C	880 mW	275 mW
J‡	1375 mW	11.0 mW/°C	880 mW	275 mW
N	1150 mW	9.2 mW/°C	736 mW	—
W	1000 mW	8.0 mW/°C	640 mW	200 mW

‡ In the FK and J packages, the SN55138 chip is alloy mounted.

recommended operating conditions

		SN55138			SN75138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5		5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	Driver or strobe	2			2			V
	Receiver	3.2			2.9			
Low-level input voltage, V_{IL}	Driver or strobe			0.8			0.8	V
	Receiver			1.5			1.8	
High-level output current, I_{OH}	Receiver output			–400			–400	μA
Low-level output current, I_{OL}	Driver output			100			100	mA
	Receiver output			16			16	
Operating free-air temperature, T_A		–55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55138			SN75138			UNIT	
					MIN	TYP‡	MAX	MIN	TYP‡	MAX		
V _{IK}	Input clamp voltage	Driver or strobe	V _{CC} = MIN,	I _I = -12 mA			-1.5			-1.5	V	
V _{OH}	High-level output voltage	Receiver	V _{CC} = MIN, V _{IL(R)} = V _{IL} max,	V _{IH(S)} = 2 V, I _{OH} = -400 μA	2.4	3.5		2.4	3.5		V	
V _{OL}	Low-level output voltage	Driver	V _{CC} = MIN, V _{IL(S)} = 0.8 V,	V _{IH(D)} = 2 V, I _{OL} = 100 mA			0.45			0.45	V	
		Receiver	V _{CC} = MIN, V _{IH(S)} = 2 V,	V _{IH(R)} = V _{IH} min, I _{OL} = 16 mA			0.4			0.4		
I _{I(max)}	Input current at maximum input voltage	Driver or strobe	V _{CC} = MAX,	V _I = V _{CC}			1			1	mA	
I _{IH}	High-level input current	Driver or strobe	V _{CC} = MAX,	V _I = 2.4 V			40			40	μA	
		Receiver	V _{CC} = 5 V, V _{I(S)} = 2 V	V _{I(R)} = 4.5 V,			25	300		25		300
I _{IL}	Low-level input current	Driver or strobe	V _{CC} = MAX,	V _I = 0.4 V			-1	-1.6		-1	-1.6	mA
		Receiver	V _{CC} = MAX, V _{I(S)} = 2 V	V _{I(R)} = 0.45 V,					-50			μA
I _{I(off)}	Input current with power off	Receiver	V _{CC} = 0,	V _I = 4.5 V			1.1	1.5		1.1	1.5	mA
I _{OS}	Short-circuit output current§	Receiver	V _{CC} = MAX				-20	-55		-18	-55	mA
I _{CC}	Supply current	All driver outputs low	V _{CC} = MAX, V _{I(S)} = 0.8 V	V _{I(D)} = 2 V,			50	65		50	65	mA
		All driver outputs high	V _{CC} = MAX, V _{I(S)} = 2 V, Receiver outputs open	V _{I(R)} = 3.5 V,			42	55		42	55	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. Parenthetical letters D, R, and S used with V_I refer to the driver input, receiver input, and strobe input, respectively.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

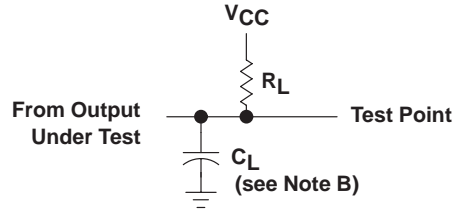
PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS			MIN	TYP	MAX	UNIT
t _{PLH}	Driver	Driver	C _L = 50 pF, R _L = 50 Ω,	See Figure 1		15	24	ns	
t _{PHL}						14	24		
t _{PLH}	Strobe	Driver					18	28	ns
t _{PHL}						22	32		
t _{PLH}	Receiver	Receiver	C _L = 15 pF, R _L = 400 Ω,	See Figure 2		7	15	ns	
t _{PHL}						8	15		

† t_{PLH} = propagation delay time, low- to high-level output

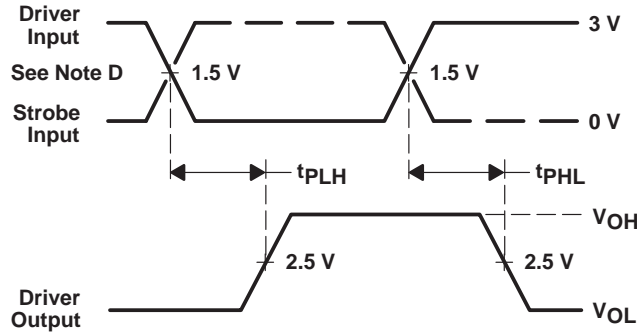
t_{PHL} = propagation delay time, high- to low-level output



PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

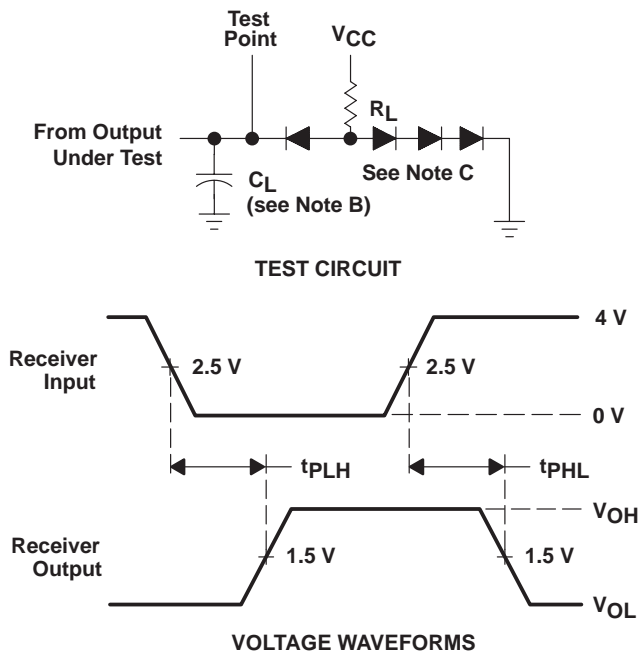
- NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_w = 100$ ns, $PRR \leq 1$ MHz, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O \approx 50 \Omega$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N916 or 1N3064.
 D. When testing driver input (solid line) strobe must be low; when testing strobe input (dashed line) driver input must be high.

Figure 1. Propagation Delay Times From Data and Strobe Inputs

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input pulses are supplied by generators having the following characteristics: $t_W = 100$ ns, $PRR \leq 1$ MHz, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_O \approx 50 \Omega$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N916 or 1N3064.
- D. When testing driver input (solid line) strobe must be low; when testing strobe input (dashed line) driver input must be high.

Figure 2. Propagation Delay Times From Receiver Input

TYPICAL CHARACTERISTICS†

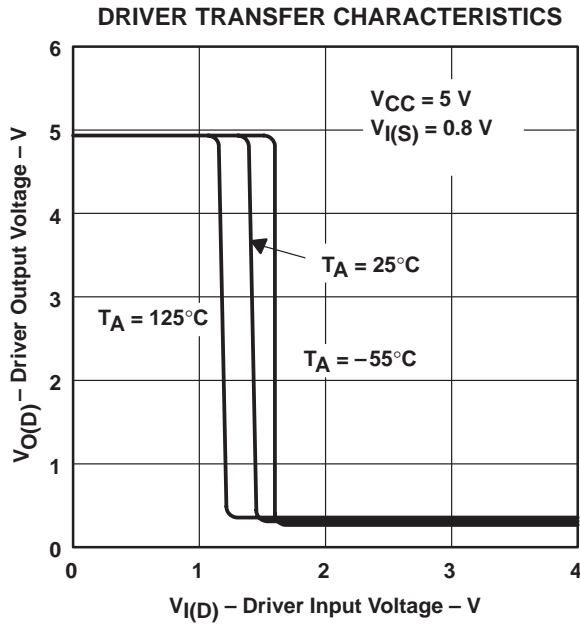


Figure 3

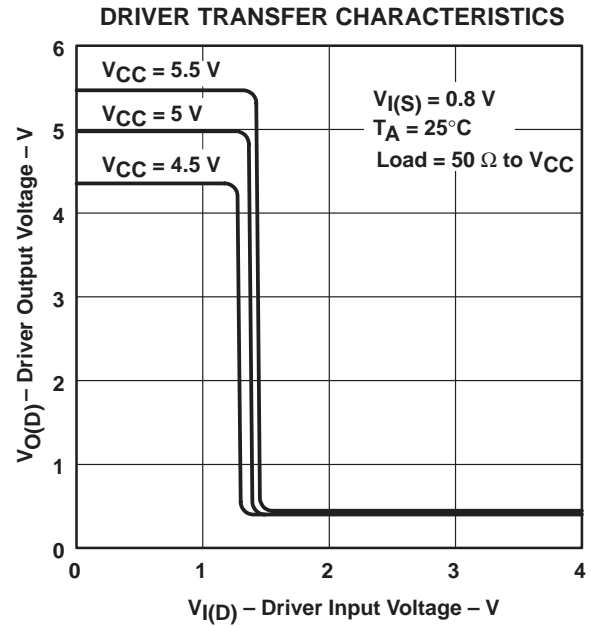


Figure 4

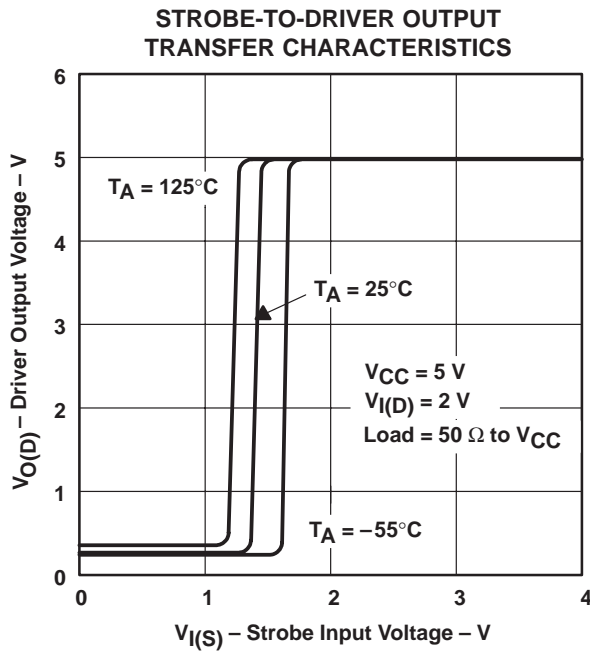


Figure 5

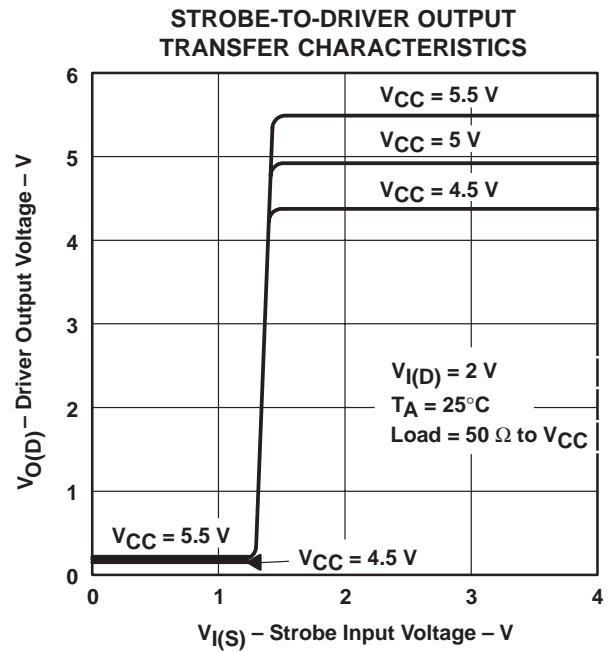


Figure 6

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

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TYPICAL CHARACTERISTICS†

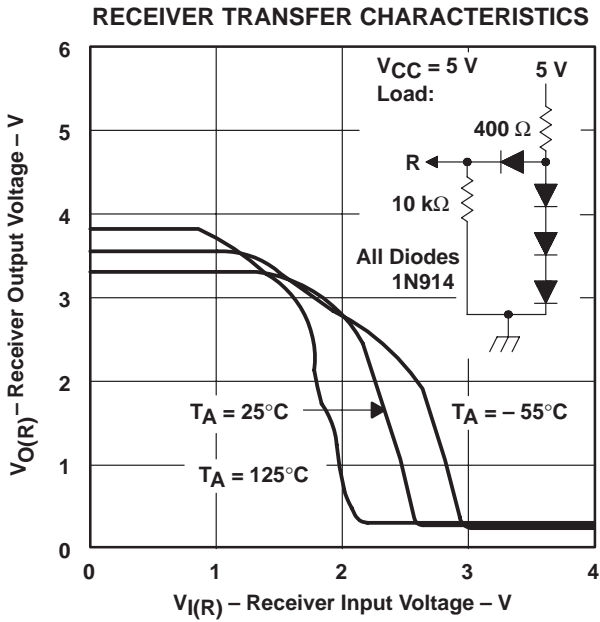


Figure 7

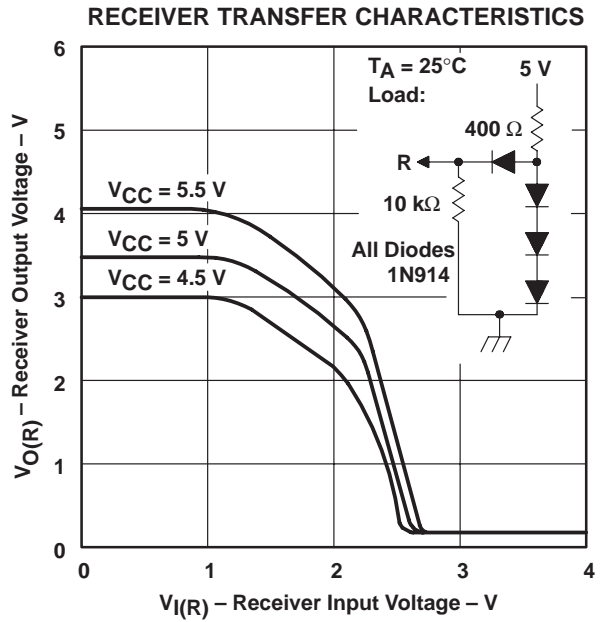


Figure 8

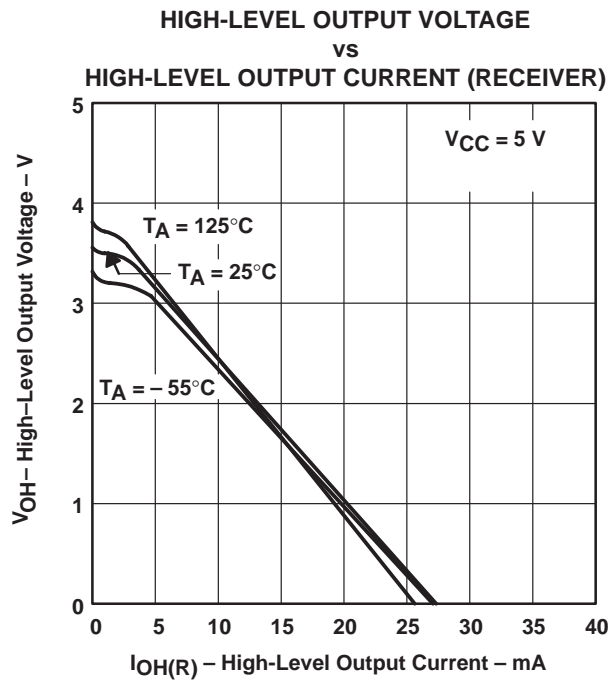


Figure 9

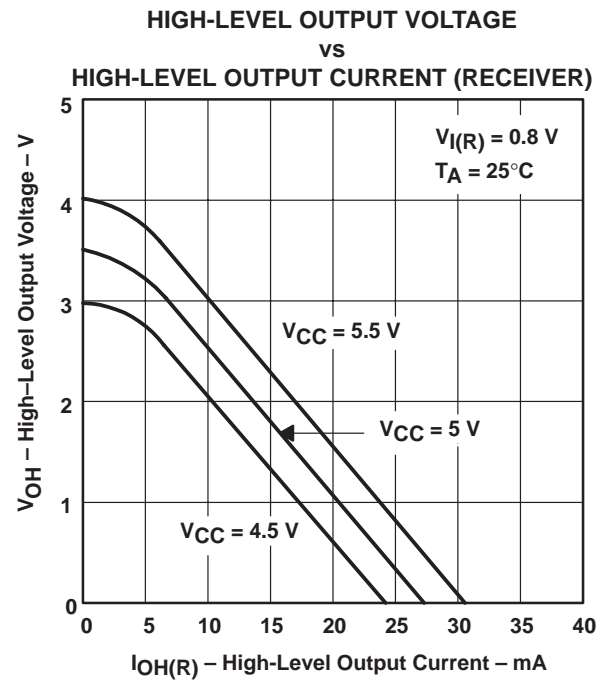


Figure 10

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

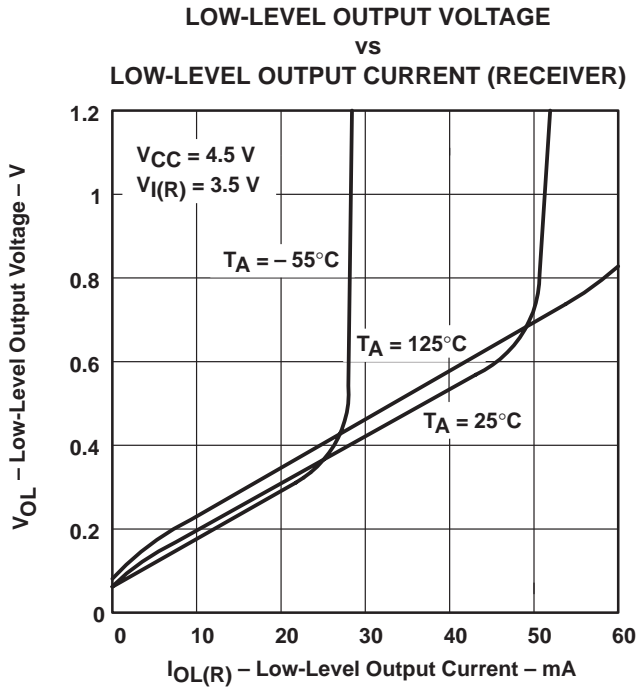


Figure 11

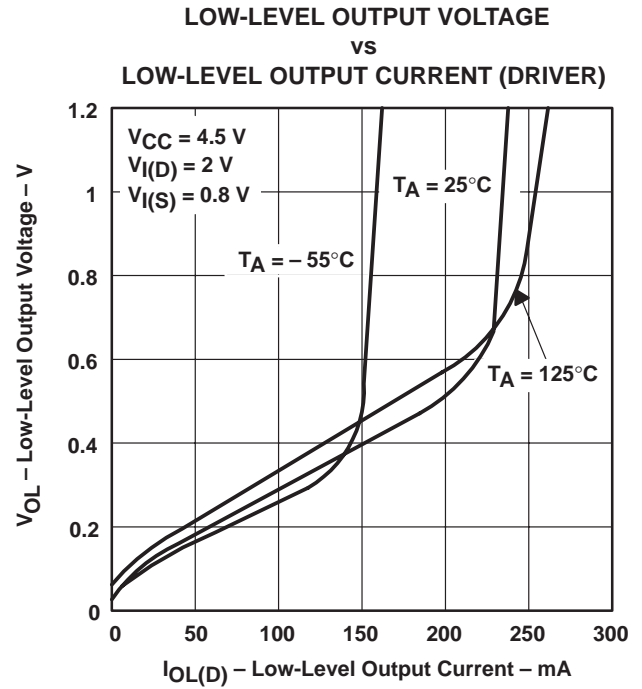


Figure 12

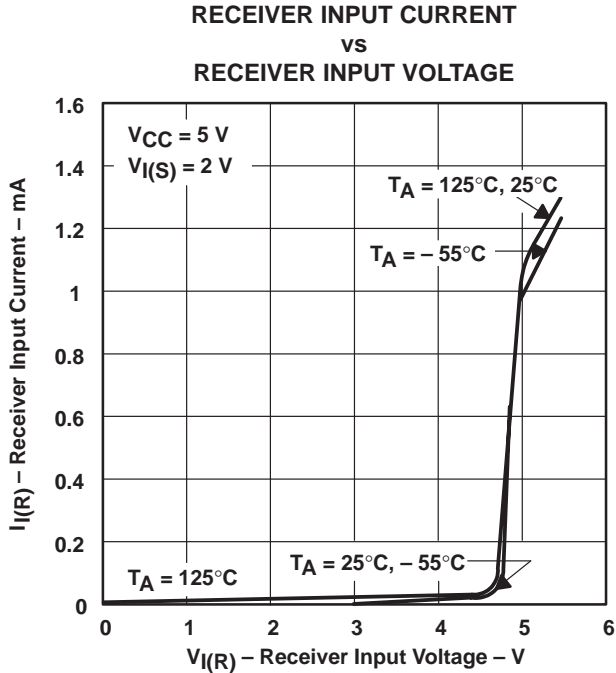


Figure 13

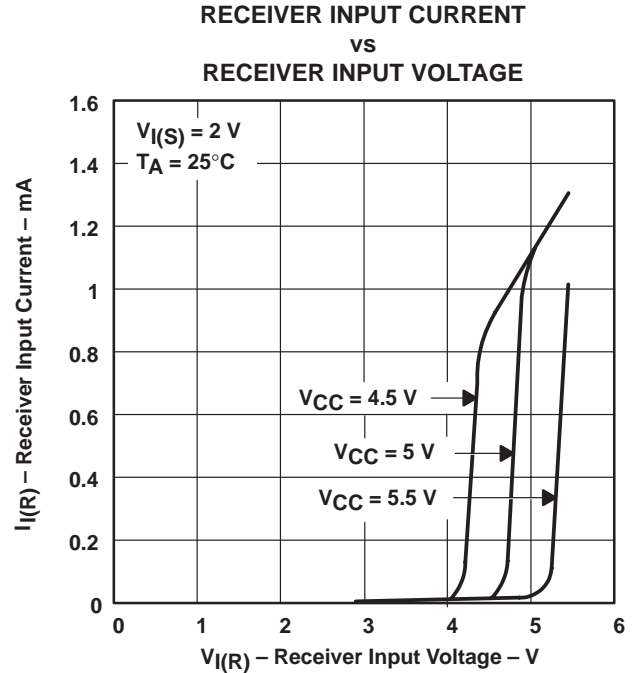


Figure 14

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

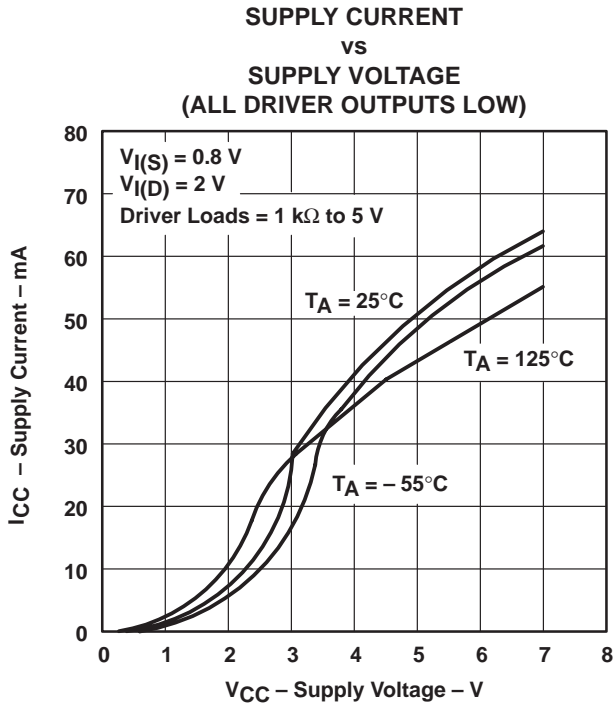


Figure 15

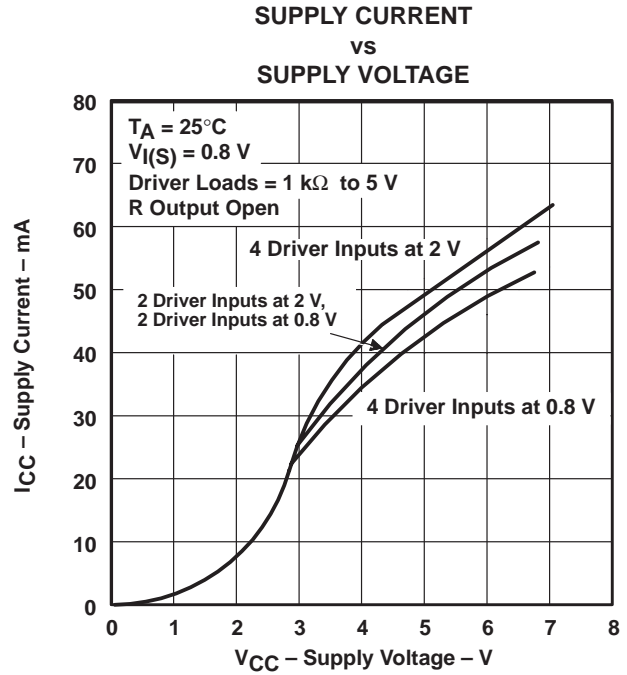


Figure 16

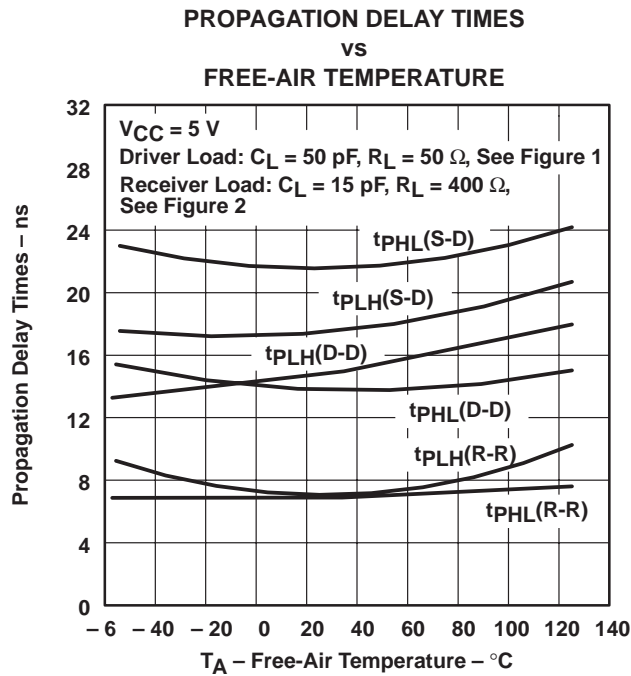


Figure 17

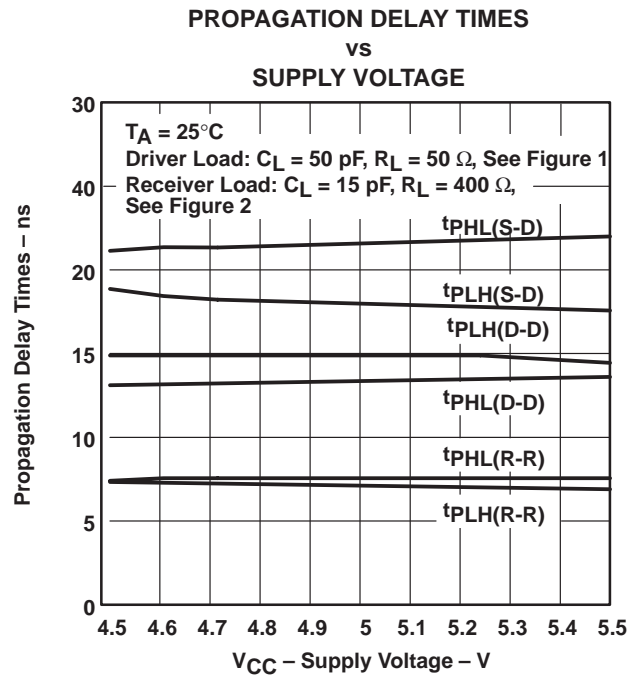
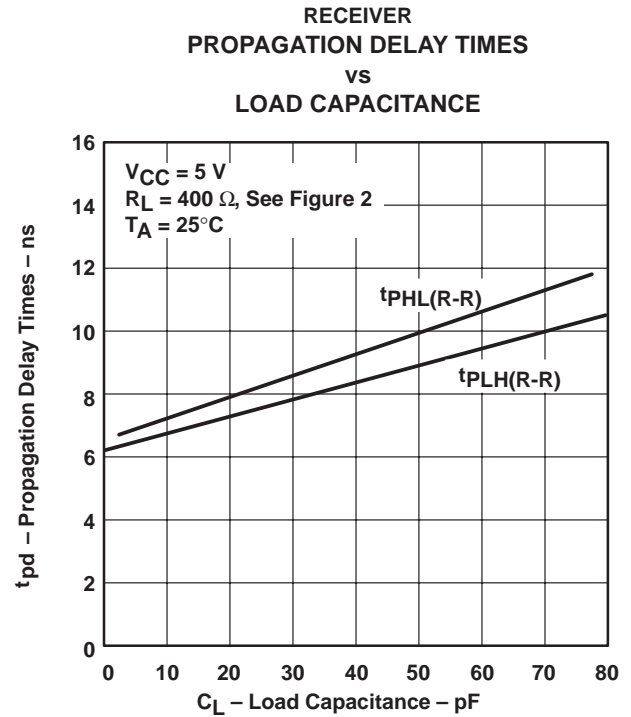
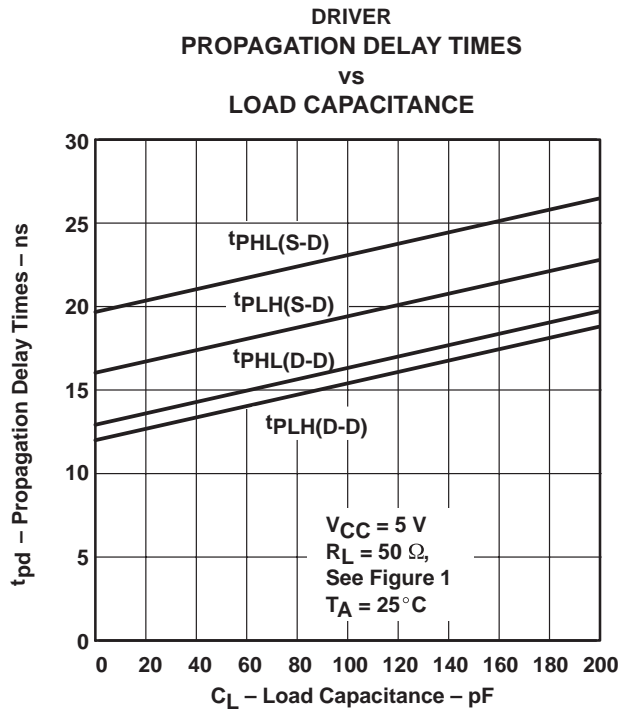


Figure 18

† Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS



APPLICATION INFORMATION

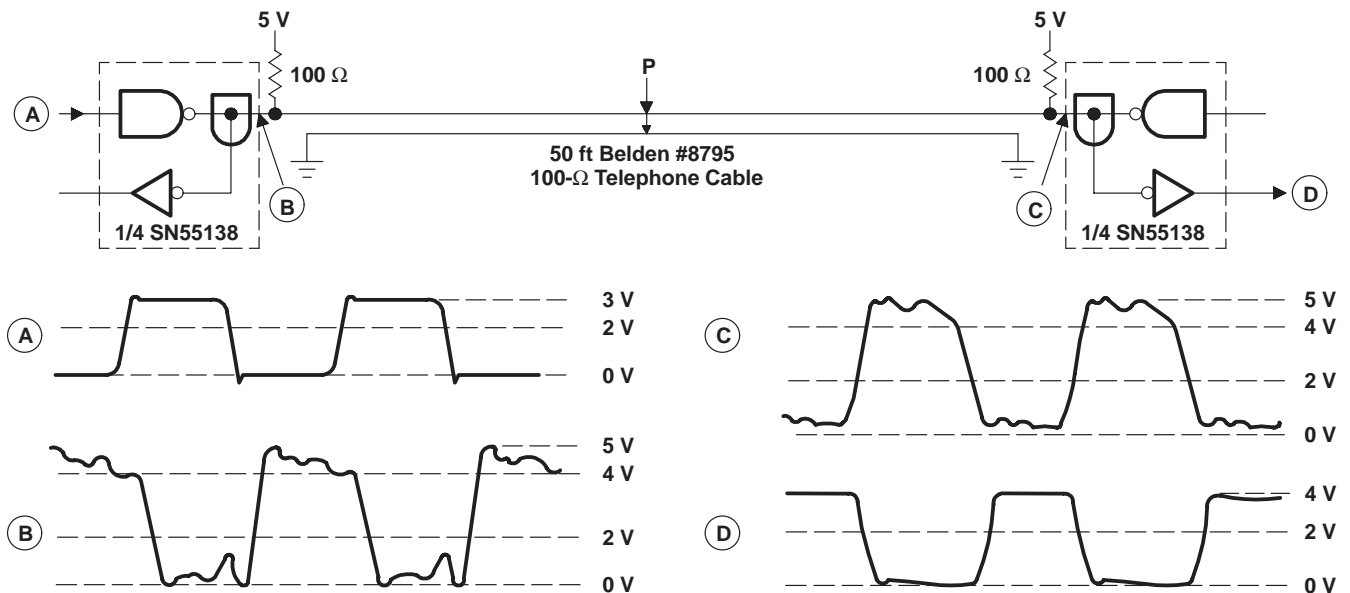
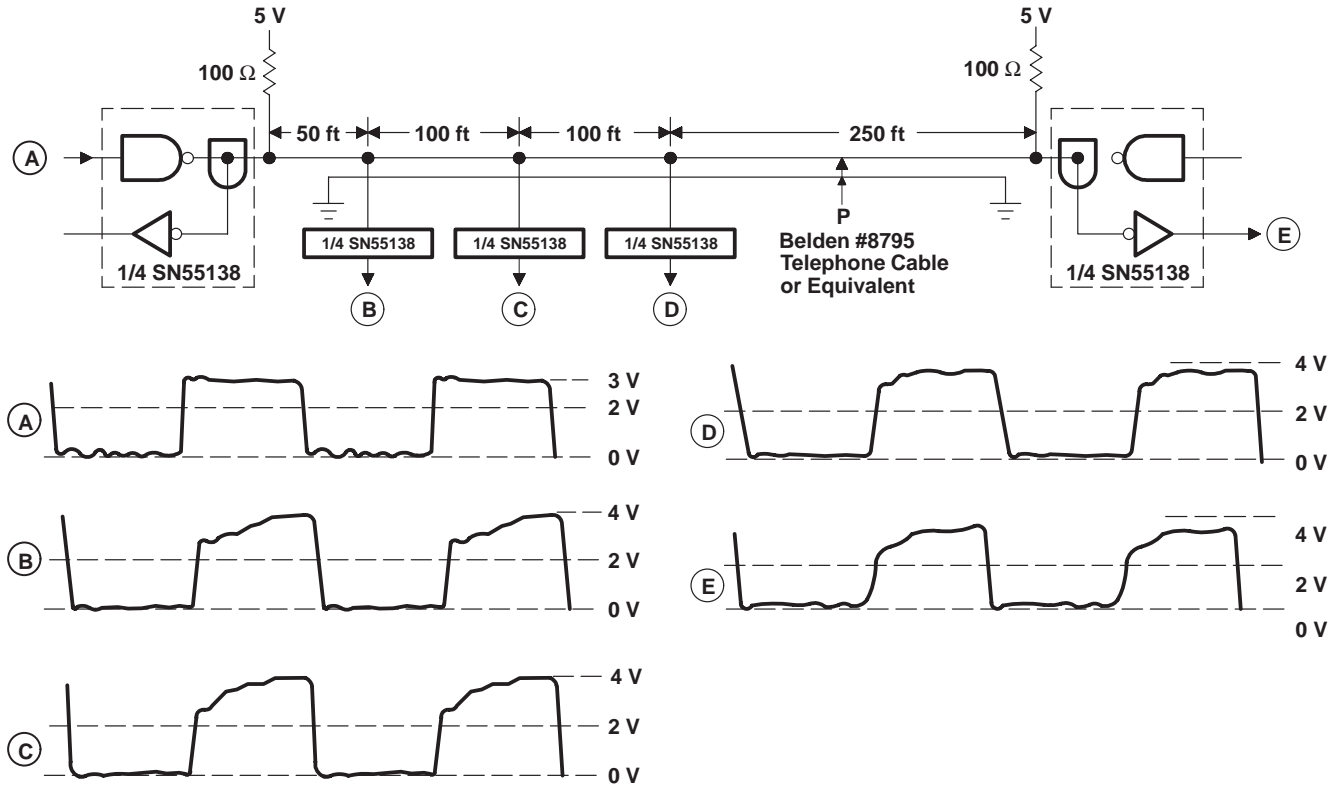


Figure 21. Point-to-Point Communication Over 50 Feet of Twisted Pair at 5 MHz

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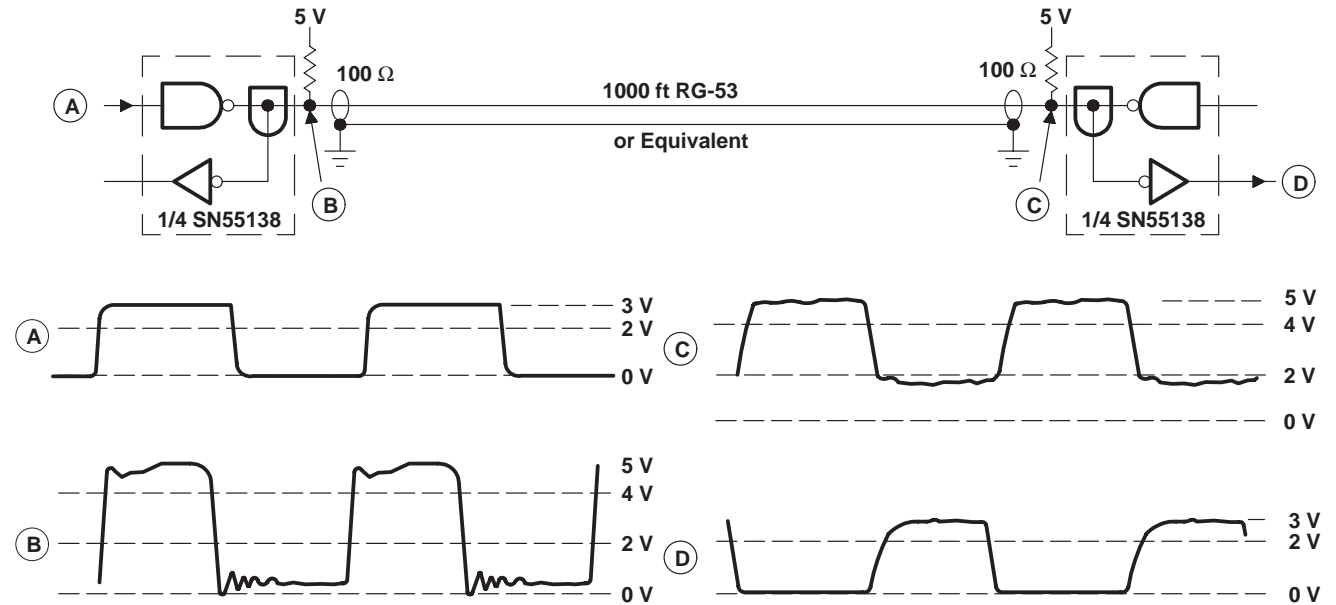
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APPLICATION INFORMATION



TYPICAL VOLTAGE WAVEFORMS

Figure 22. Party-Line Communication on 500 Feet of Twisted Pair at 1 MHz



TYPICAL VOLTAGE WAVEFORMS

Figure 23. Point-to-Point Communication Over 1000 Feet of Coaxial Cable at 1 MHz

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75138D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75138	Samples
SN75138DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75138	Samples
SN75138N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN75138N	Samples
SN75138NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75138	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

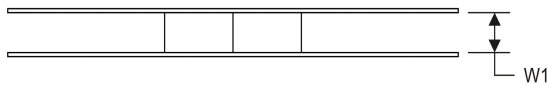
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TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75138DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75138NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

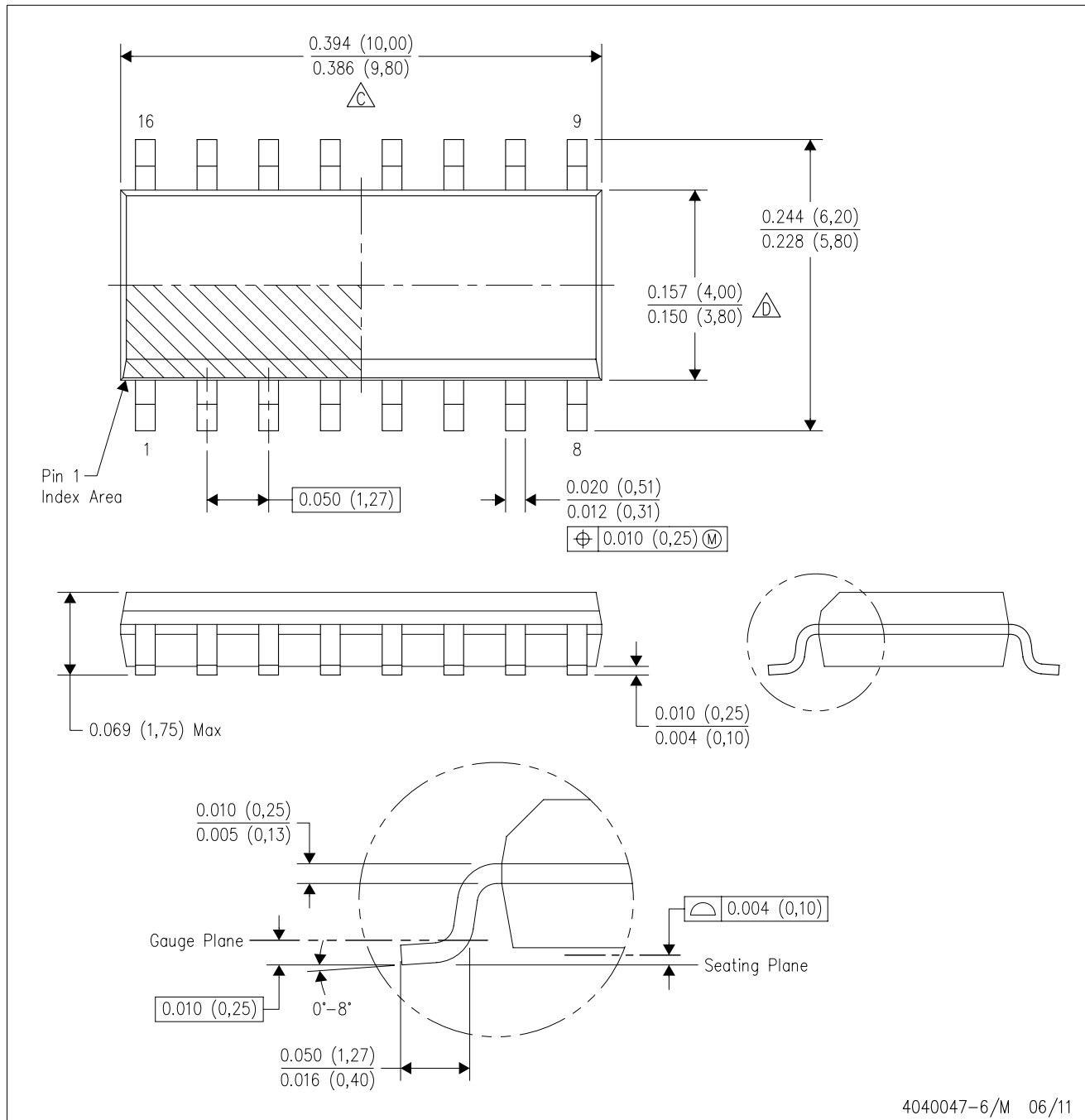
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75138DR	SOIC	D	16	2500	333.2	345.9	28.6
SN75138NSR	SO	NS	16	2000	367.0	367.0	38.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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