TPS92512 2.5A Buck LED Driver with Integrated Analog Current Adjust

1 Features

- Integrated 200-mΩ High-Side MOSFET
- 4.5-V to 42-V Input Voltage Range (4.5 V to 60 V for the TPS92512HV)
- 0 V to 300 mV Adjustable Voltage Reference
- ±5% LED Current Accuracy
- 100-kHz to 2-MHz Switching Frequency Range
- Dedicated PWM Dimming Input
- Adjustable Undervoltage-Lock-Out
- Overcurrent Protection
- Overtemperature Protection
- MSOP-10 Package with PowerPAD™

2 Applications

- Street Lighting
- Emergency/Exit Lighting
- General Industrial and Commercial Illumination
- Retail Lighting
- Appliance Lighting
- Transportation Lighting
- Channel Letters
- Light Bars

3 Description

The TPS92512/HV are 2.5A step-down (buck) current regulators with an integrated MOSFET to drive high current LEDs. Available with 42 V and 60 V (HV) input ranges, these LED drivers operate at a user selected fixed-frequency with peak-current mode control and deliver excellent line and load regulation.

The TPS92512/HV LED drivers feature separate inputs for analog and pulse width modulation (PWM) dimming for no compromise brightness control achieving contrast ratios of greater than 10:1 and greater than 100:1, respectively. The PWM input is compatible with low-voltage logic standards for easy interface to a broad range of microcontrollers. The analog LED current setpoint is adjustable from 0 V to 300 mV using the IADJ input with an external 0 V to 1.8 V signal.

For multi-string applications using two or more TPS92512/HV LED drivers, the internal oscillator can be overdriven by an external clock ensuring all of the converters operate at a common frequency thereby reducing the potential for beat frequencies and simplifying system EMI filtering. An adjustable input under-voltage lockout (UVLO) with hysteresis provides flexibility in setting start/stop voltages based upon supply voltage conditions.

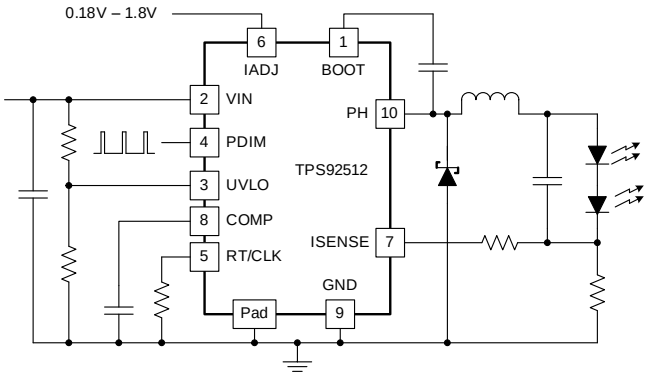
The TPS92512 includes cycle-by-cycle overcurrent protection and thermal shutdown protection. It is available in a 10-pin HVSSOP PowerPAD™ package.

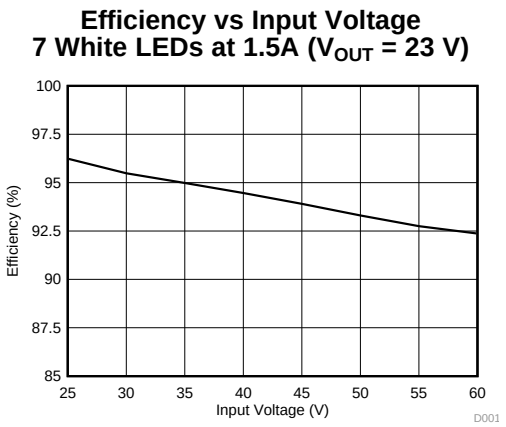
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS92512	HVSSOP (10)	5.00 mm x 3.00 mm
TPS92512HV		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematics





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5 Revision History

Changes from Revision A (March 2015) to Revision B — **Page**

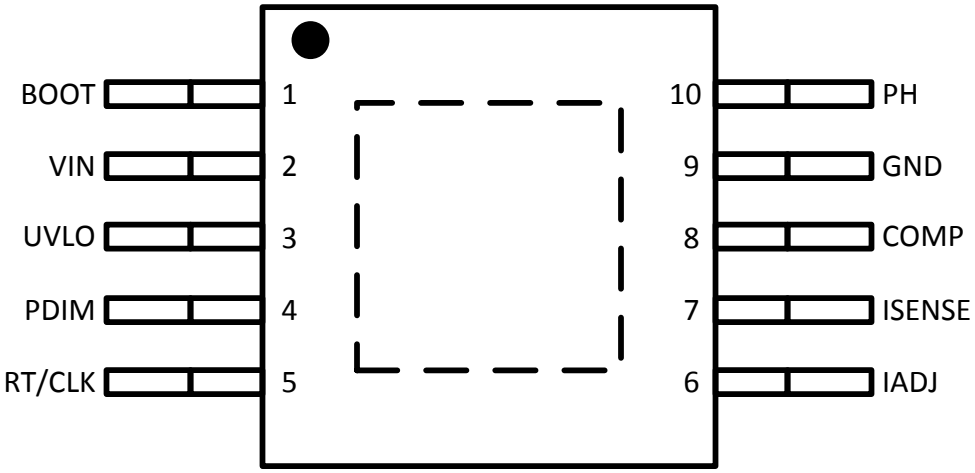
- Changed Equation 16 From: $P_{D(AC)} = 0.73^{-9}$ To: $P_{D(AC)} = 0.73 \times 10^{-9}$ ... 14

Changes from Original (February 2015) to Revision A — **Page**

- Changed the device status From: Product Preview To: Production Data ... 1

6 Pin Configuration and Functions

DGQ (HVSSOP) Package
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the output device, the output is forced to switch off until the capacitor is recharged.
COMP	8	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
GND	9	G	Ground.
IADJ	6	I	Analog current adjust pin. The voltage applied to this pin will set the current sense (ISENSE pin) voltage. The range of the ADJ pin is 180 mV to 1.8 V and the corresponding ISENSE pin voltage is the IADJ pin voltage divided by 6.
ISENSE	7	I	Inverting node of the transconductance (g_M) error amplifier.
PDIM	4	I	PWM dimming input pin. The duty cycle of the PWM signal linearly controls the average output current of the converter.
PH	10	O	The source of the internal high-side MOSFET.
PowerPAD	PAD	G	GND pin must be electrically connected to the exposed pad directly beneath the device on the printed circuit board for proper operation.
RT/CLK	5	I	Resistor timing and external clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to program the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin becomes a high impedance clock input to the internal PLL. If the clocking edges stop, the internal amplifier is re-enabled and the mode returns to the resistor-programmed function.
UVLO	3	I	Adjustable undervoltage lockout. Set with resistor divider from VIN.
VIN	2	P	Input supply voltage, 4.5V to 42V or 4.5V to 60V for the HV version.

(1) I = Input, O = Output, P = Supply, G = Ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Input voltage	VIN (TPS92512HV)	–0.3	65	V
		VIN (TPS92512)	–0.3	45	
		PDIM, UVLO	–0.3	5	
		BOOT		(PH + 8)	
		ISENSE, IADJ, COMP	–0.3	3	
		RT/CLK	–0.3	3.6	
	Output voltage	PH (TPS92512HV)	–0.6	65	V
		PH (TPS92512)	–0.6	45	
		PH, 10-ns Transient	–2		
	Voltage Difference	PAD to GND		±200	mV
	Source Current	PH		Current Limit	A
	Sink current	VIN		Current Limit	A
		BOOT		1	mA
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM),ESD stress voltage (1)	±2000	V
		Charged-device model (CDM), ESD stress voltage (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2 kV may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±500 V may actually have higher performance.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
VIN	Input voltage (TPS92512HV)	4.5	60	V
	Input voltage (TPS92512)	4.5	42	
f_{SW}	Switching frequency range using RT mode	100	2000	kHz
	Switching frequency range using CLK mode	300	2000	
$t_{MIN(RT/CLK)}$	Minimum RT/CLK input pulse width for switching frequency synchronization	51		ns
T_J	Operating junction temperature	–40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS92512 TPS92512HV	UNIT
		DGQ (10 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	37.5	
ψ_{JT}	Junction-to-top characterization parameter	1.8	
ψ_{JB}	Junction-to-board characterization parameter	37.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

–40°C ≤ T_J ≤ 125°C, V_{VIN} = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN)						
VIN_{UVLO}	VIN undervoltage lockout threshold	No voltage hysteresis, rising and falling		2.94		V
I_{VINSD}	Shutdown supply current	V_{UVLO} = 0 V, 4.5 V ≤ V_{VIN} ≤ 42 V (60 V for HV)			11.5	µA
I_{VIN}	Non-switching supply current	V_{ISENSE} = 220 mV, 4.5V ≤ V_{VIN} ≤ 42 V (60 V for HV)		337	407	µA
UNDER VOLTAGE LOCKOUT (UVLO)						
V_{UVLO}	UVLO threshold voltage	Rising threshold	1.12	1.22	1.30	V
	UVLO pin source current	V_{UVLO} = 1.5 V (device enabled)		3.97		µA
		V_{UVLO} = 1 V (device disabled)		1.05		
ANALOG CURRENT ADJUST (V_{IADJ}, V_{ISENSE})						
V_{IADJ}	IADJ clamp voltage	I_{IADJ} = 1 µA		1.8		V
		I_{IADJ} = 100 µA		2.77		
V_{ISENSE}	Current sense voltage	V_{IADJ} = 1.2 V, T_J = 25°C to 125°C	191	200	210	mV
		V_{IADJ} = 0.18 V, T_J = 25°C to 125°C	21.4	30.0	40.0	
		I_{IADJ} = 1 µA, T_J = 25°C to 125°C	285	300	309	
		I_{IADJ} = 100 µA, T_J = 25°C to 125°C	286	300	309	
	Current sense voltage level	180 mV ≤ V_{IADJ} ≤ 1.8V		V_{IADJ}/6		
HIGH-SIDE MOSFET (BOOT, PH)						
$R_{DS(on)}$	On-resistance	V_{VIN} = 4.5 V, (V_{BOOT} – V_{PH}) = 3.5 V		232		mΩ
		(V_{BOOT} – V_{PH}) = 6 V		200	342	
V_{BOOT}	BOOT-PH voltage	VPDIM = 3V		6		V
I_{BOOT}	BOOT-PH current	VPDIM = 0V, (V_{BOOT} – V_{PH}) = 5V		93.9		µA
V_{BOOTUV}	BOOT-PH under voltage lockout	Rising threshold		2.25	2.81	V
		Falling threshold		1.99	2.40	
$t_{ON(min)}$	Minimum on time	V_{COMP} = 0		140		ns
ERROR AMPLIFIER (ISENSE, COMP)						
	Input bias current	V_{ISENSE} = 200 mV		20		nA
$g_{M(ea)}$	Transconductance gain	V_{IADJ} = 1.2 V, 180 mV < V_{ISENSE} < 220 mV, V_{COMP} = 1 V		331		µA/V
	DC gain	V_{IADJ} = 1.2 V , V_{ISENSE} = 0.2 V		10		kV/V
	Bandwidth			2.7		MHz
	Source/sink current	V_{IADJ} = 1.2 V , V_{COMP} = 1 V, V_{ISENSE} = 200 mV ± 100 mV		±28		µA
CURRENT LIMIT						
	Current limit threshold			6		A

Electrical Characteristics (continued)

–40°C ≤ T_J ≤ 125°C, V_{VIN} = 12V (unless otherwise noted)

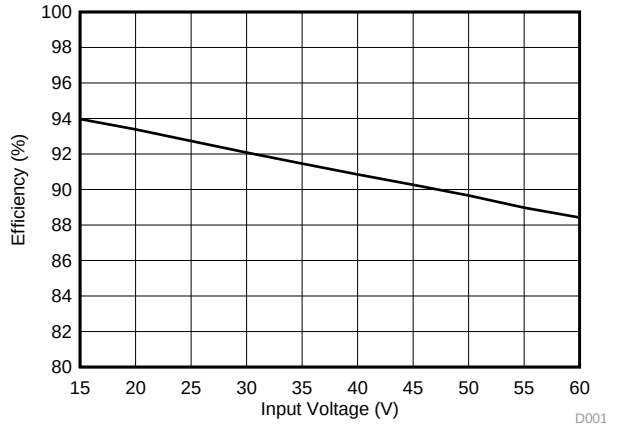
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown			165		°C
	Thermal shutdown hysteresis			20		
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK)						
V_{RT}	RT/CLK regulated voltage	R_{RT} = 200 kΩ	474	500	513	mV
f_{SW}	Switching frequency	V_{VIN} = 6 V, R_{RT} = 200 kΩ	447	557	648	kHz
	RT/CLK high threshold	V_{VIN} = 6 V		1.49	1.81	V
	RT/CLK low threshold	V_{VIN} = 6 V	0.63	1.02		V
PWM DIMMING (PDIM)						
I_{PDIM}	PDIM source current	V_{PDIM} = 0		1.04		µA
V_{IH}	High-level input voltage			1.34	1.45	V
V_{IL}	Low-level input voltage		0.79	0.88		

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK)						
	RT/CLK falling edge to PH rising edge delay	Measured at 500 kHz with RT resistor in series, V_{VIN} = 6 V		92.1		ns
	Phase loop (PLL) lock-in time	f_{SW} = 500 kHz		100		µs
PWM DIMMING (PDIM)						
t_{RISE}	Rising propagation delay			305		ns
t_{FALL}	Falling propagation delay			535		

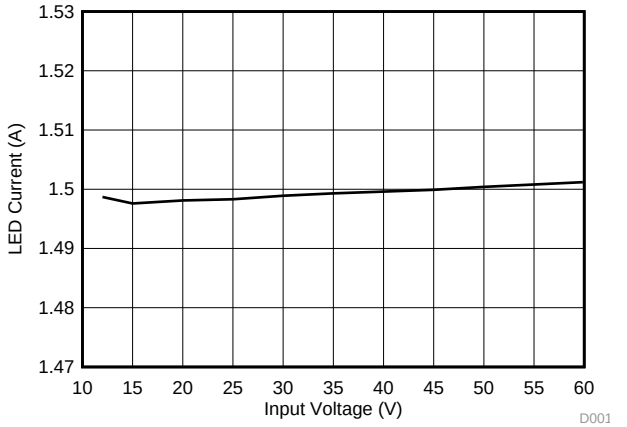
7.7 Typical Characteristics

VIN = 24V, Unless otherwise specified



1.5 A LED Current 4 LEDs in Series V_{IADJ} = 1.8 V
f_{SW} = 570 kHz V_{OUT} = 13.1 V

Figure 1. Efficiency vs Input Voltage



1.5 A LED Current 3 LEDs in Series V_{IADJ} = 1.8 V
V_{OUT} = 9.9 V

Figure 2. Line Regulation

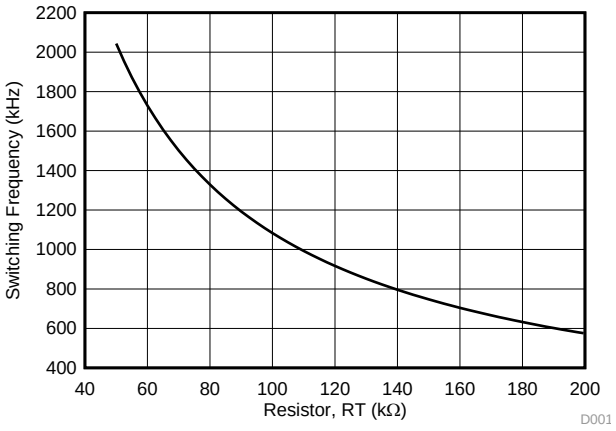


Figure 3. Switching Frequency vs RT Resistor

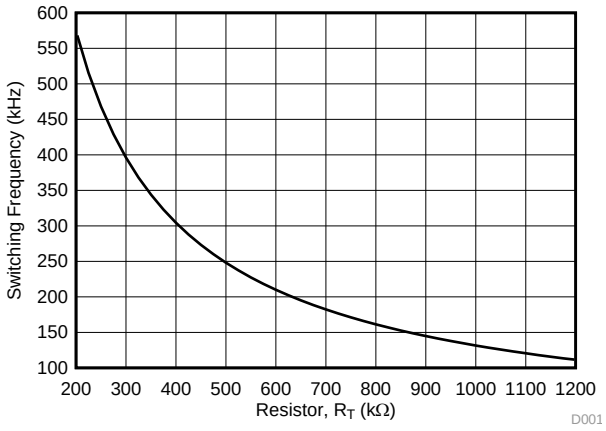
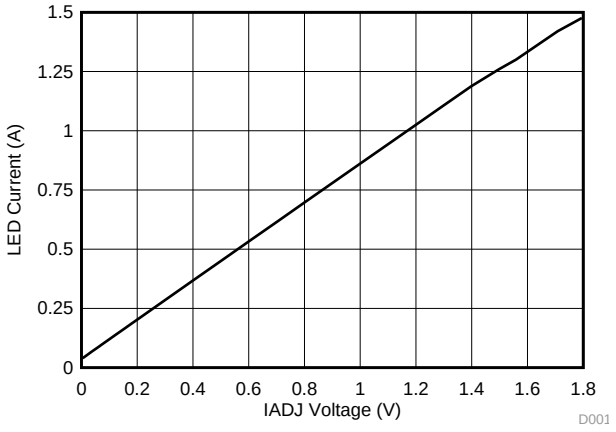
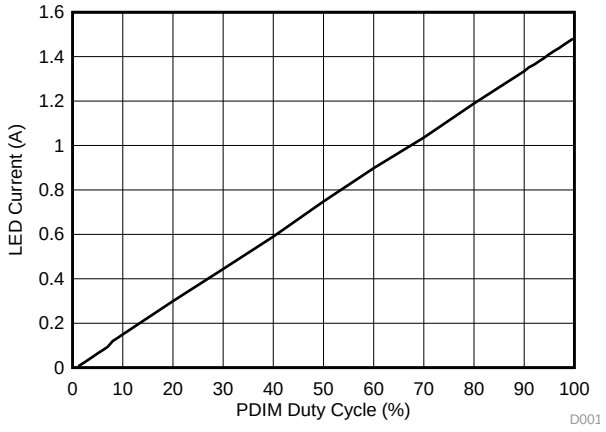


Figure 4. Switching Frequency vs RT Resistor



1.5 A LED Current 3 LEDs in Series
V_{OUT} = 9.9 V

Figure 5. LED Current vs IADJ Voltage

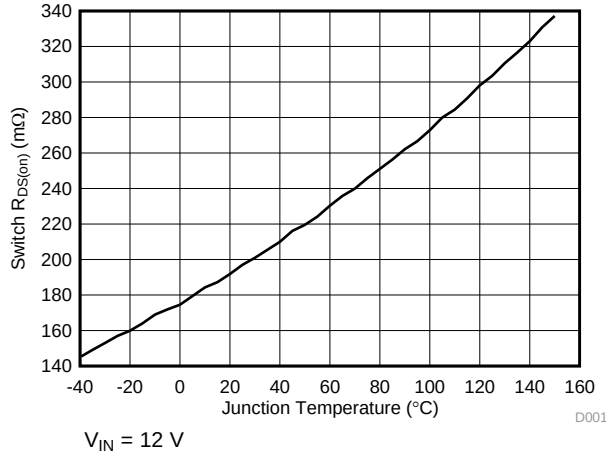


1.5 A LED Current 3 LEDs in Series V_{IADJ} = 1.8 V
250 Hz PWM Frequency V_{OUT} = 9.9 V

Figure 6. LED Current vs PDIM Duty Cycle

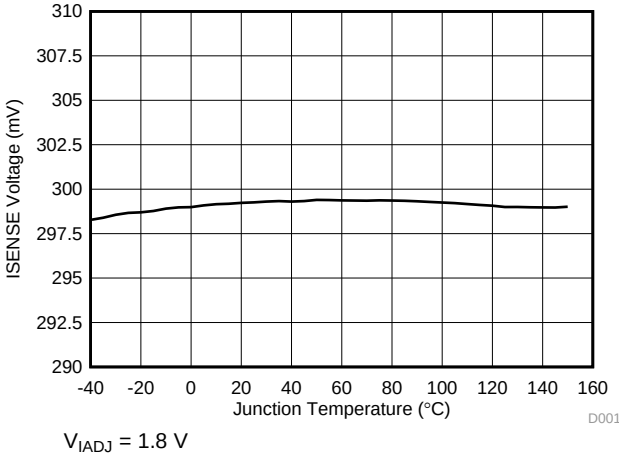
Typical Characteristics (continued)

VIN = 24V, Unless otherwise specified



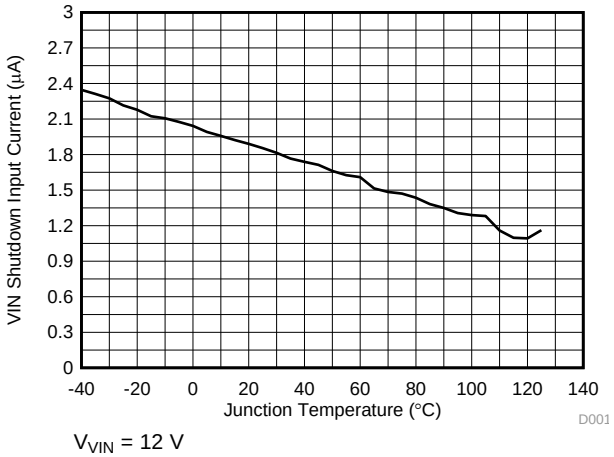
V_{IN} = 12 V

Figure 7. PH Switch $R_{DS(on)}$ vs Junction Temperature



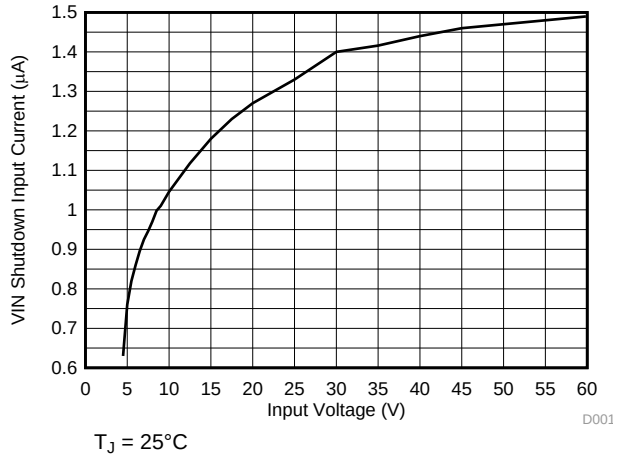
V_{IADJ} = 1.8 V

Figure 8. V_{ISENSE} vs Junction Temperature



V_{VIN} = 12 V

Figure 9. Shutdown Input Current vs Junction Temperature



T_J = 25°C

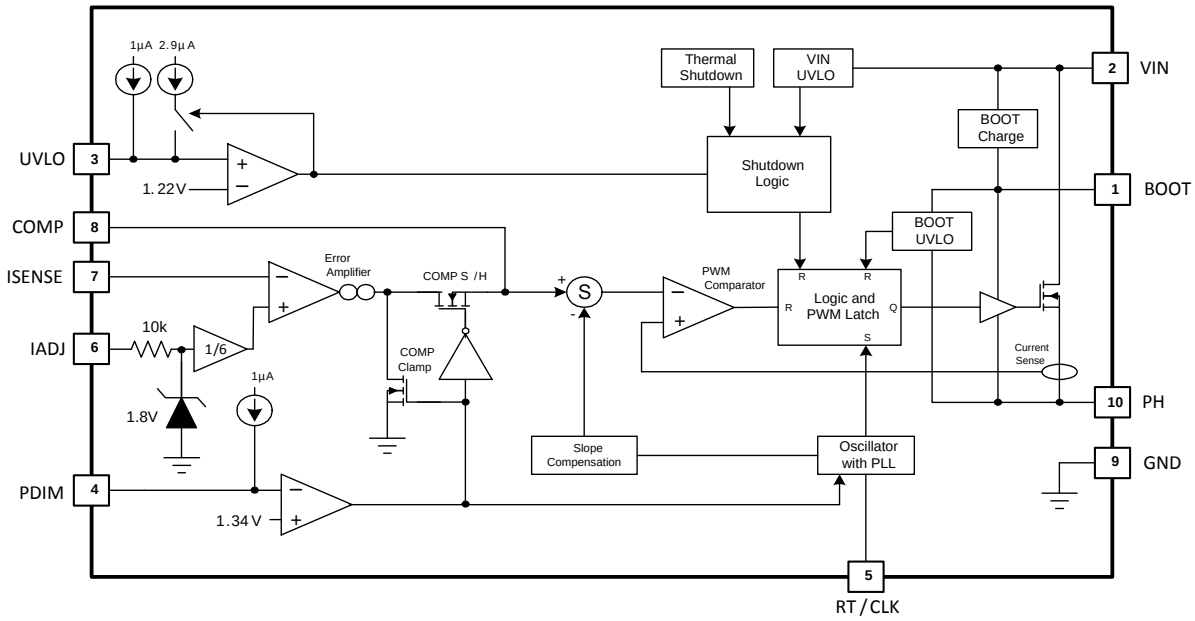
Figure 10. Shutdown Input Current vs Input Voltage

8 Detailed Description

8.1 Overview

The TPS92512 is a high voltage, up to 2.5-A, step-down (buck) regulator with an integrated high-side N-channel MOSFET. To improve performance during line and load transients the device implements a constant frequency, peak-current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency of 100 kHz to 2000 kHz allows for efficiency and size optimization when selecting the output filter components.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Undervoltage Lockout and Low Power Shutdown (UVLO Pin)

The TPS92512 contains an internal under-voltage lockout circuit on the VIN pin of the device. However, this internal UVLO is for device protection only and does not contain hysteresis. The UVLO pin of the device should always be used to set the minimum VIN voltage that the circuit operates at. This level should be set using the minimum input voltage expected for the application with a minimum setting of 4.5 V.

The UVLO pin has an internal pull-up current source of 1 µA (I1) that will provide a default ON state in the event the UVLO pin is left floating (not recommended). When the UVLO pin voltage exceeds 1.22 V (V_{EN}), an additional 2.9 µA of hysteresis current is added (see Figure 11). This additional current provides the input voltage hysteresis. Use Equation 1 to set the external hysteresis (V_{HYS}) for the input voltage. Use Equation 2 to set the input rising start voltage, V_{START}. When the UVLO pin is pulled low, the internal regulators are shut down, the device enters a low-power shutdown mode and the compensation capacitor on the COMP pin, C_{COMP}, is discharged.

Feature Description (continued)

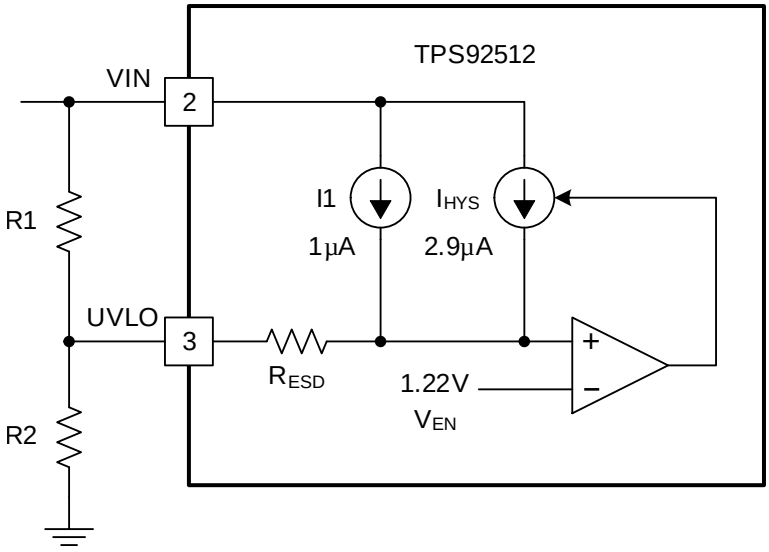


Figure 11. Adjustable Undervoltage Lockout (UVLO)

$$R1 = \frac{V_{HYS} \times \left(V_{EN} - \left(I1 \times R_{ESD}\right)\right) - I_{HYS} \times R_{ESD} \times V_{START}}{I_{HYS} \times V_{EN}} \quad (1)$$

$$R2 = \frac{R1 \times \left(V_{EN} - \left(R_{ESD} \times \left(I1 + I_{HYS}\right)\right)\right)}{\left(V_{STOP} - V_{EN}\right) + \left(I1 + I_{HYS}\right) \times \left(R1 + R_{ESD}\right)} \quad (2)$$

$$V_{HYS} = V_{START} - V_{STOP} \quad (3)$$

$$R_{ESD} = 10\ k\Omega \quad (4)$$

8.3.2 Adjustable Switching Frequency (RT/CLK Pin)

The switching frequency of the TPS92512 is adjustable over a wide range from 100 kHz to 2 MHz by placing a resistor, R_{RT}, on the RT/CLK pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 5 or the curves in Figure 3 or Figure 4. To reduce the solution size one typically sets the switching frequency as high as possible, but tradeoffs of the supply efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time, $t_{ON(min)}$, limits the maximum operating input voltage.

$$R_{RT}\left(k\Omega\right) = \frac{206033}{\left(f_{SW}\right)^{1.092}\left(kHz\right)} \quad (5)$$

$$f_{SW} = \left(\frac{206033}{R_{RT}(k\Omega)}\right)^{\left(\frac{1}{1.092}\right)} \quad (6)$$

8.3.3 Synchronizing the Switching Frequency to an External Clock (RT/CLK Pin)

The RT/CLK pin can be used to synchronize the regulator to an external system clock by connecting a square wave to the RT/CLK pin through the circuit network as shown in Figure 12. The square wave amplitude must transition lower than 0.63 V and higher than 1.81 V on the RT/CLK pin and have an on-time greater than 51 ns and an off-time greater than 100 ns. The synchronization frequency range is 300 kHz to 2 MHz. The rising edge of the PH is synchronized to the falling edge of RT/CLK pin signal. The internal oscillator provides default switching frequency set by connecting the resistor from the RT/CLK pin to ground should the synchronization signal turn off.

Feature Description (continued)

It is required to AC couple the synchronization signal through a 470 pF ceramic capacitor and a 4 kΩ series resistor to the RT/CLK pin. The series resistor reduces PH jitter in heavy load applications when synchronizing to an external clock and in applications which transition from synchronizing to RT mode. The first time the RT/CLK pin is pulled above the CLK threshold the device switches from the RT resistor frequency to PLL mode. The internal 0.5 V voltage source is removed and the CLK pin becomes high impedance as the PLL starts to lock onto the external signal. Since there is a PLL on the regulator, the switching frequency can be higher or lower than the frequency set with the external resistor. The device transitions from the resistor mode to the PLL mode and then increases or decreases the switching frequency until the PLL locks onto the CLK frequency within 100 microseconds.

When the device transitions from the PLL to resistor mode, the switching frequency slows down from the CLK frequency to 150 kHz, then reapplies the 0.5 V voltage and the resistor then sets the switching frequency. It is not recommended that a system transition from PLL mode to resistor mode repeatedly during operation. When the PLL loses the external clock input the default 150 kHz switching frequency creates long on-times, which result in higher inductor ripple currents. This can lead to inductor saturation if the system is not designed to operate at this frequency.

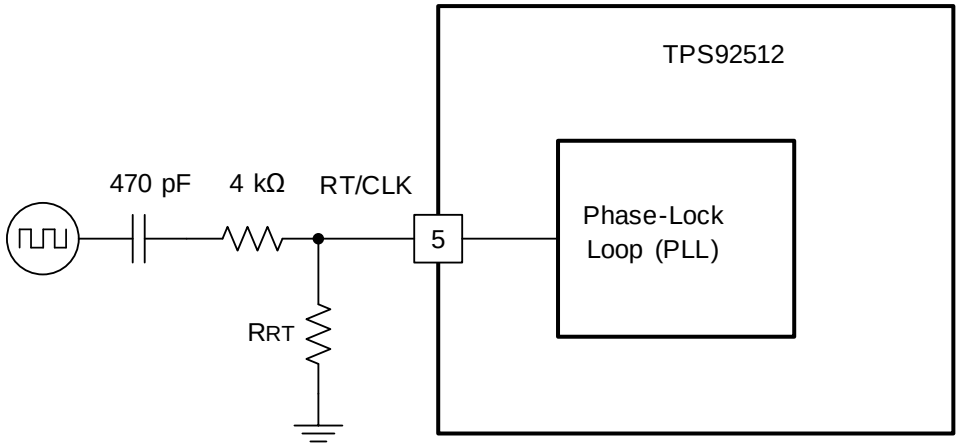


Figure 12. Frequency Synchronization

8.3.4 Adjustable LED Current (IADJ and ISENSE Pins)

The LED current can be set, and controlled dynamically, by using the IADJ pin of the TPS92512. Equation 7 shows the relationship between the voltage applied to IADJ (V_{IADJ}) and the regulation setpoint at the ISENSE pin. Equation 8 shows how to calculate the value of the current setting resistor (R_{ISENSE}) from the ISENSE pin to ground for the desired LED current.

$$V_{ISENSE} = \frac{V_{IADJ}}{6} \quad (7)$$

$$R_{ISENSE} = \frac{V_{ISENSE}}{I_{LED}} \quad (8)$$

The IADJ pin voltage range is 0 V to 1.8 V and is internally clamped at 1.8 V. If analog current adjustment will not be used, the IADJ pin can be connected to VIN through a resistor for a default ISENSE voltage of 300 mV. This resistor should be sized so that the current into the IADJ pin is limited to 100 µA or less at the maximum input voltage. A precision reference between 0 V and 1.8 V can also be used on IADJ to control the ISENSE voltage. If no external voltage source is available, the IADJ pin can be tied to the RT/CLK pin either directly or using a resistor divider to generate a voltage between 0 V and 500 mV. If a resistor divider is used off the RT/CLK pin to generate the IADJ voltage it will introduce a parallel resistance with the RT resistor. High value resistors are recommended in that case and the parallel combination must be used to calculate the switching frequency. The current sense voltage is most accurate with IADJ voltages between 180 mV and 1.8 V for a dimming range of 10:1. Below 180 mV the TPS92512 dims well but may have more variation between circuits. Due to internal offsets pulling IADJ to 0 V will not result in a current sense voltage of 0 V. Some small current will continue to run unless the PDIM pin is pulled low or the device is disabled using the UVLO pin. Analog dimming

Feature Description (continued)

is also most accurate when the device is in continuous conduction mode (CCM). If the highest accuracy possible is desired during analog dimming, size the inductor so that 1/2 the peak-to-peak inductor ripple is less than the minimum LED current to remain in CCM. The IADJ pin should be decoupled with a 10 nF capacitor to ground. A 1 kΩ resistor should be used between the ISENSE pin and R_{ISENSE} to protect the pin in the event R_{ISENSE} opens or there is a transient due to one or more LEDs shorting.

8.3.5 PWM Dimming (PDIM Pin)

The TPS92512 incorporates a PWM dimming input pin, which directly controls the enable/disable state of the internal gate driver. When PDIM is low, the gate driver is disabled. The PDIM pin has a 1 µA pull-up current source, which creates a default ON state when the PDIM pin is floating. When PDIM goes low, the gate driver shuts off and the LED current quickly reduces to zero. A square wave of variable duty cycle should be used and should have a low level below 0.79 V and a high level of 1.45 V or above.

The TPS92512 uses a sample-and-hold switch on the error amplifier output. During the PDIM off-time the COMP voltage remains unchanged. Also, the error amplifier output is internally clamped low. These techniques help the system recover to its regulation duty cycle quickly. The dimming frequency range is 100 Hz to 1 kHz and the minimum duty cycle is only limited in cases where the BOOT capacitor can discharge below its under-voltage threshold of 2 V (VIN is within 2 V of the total output voltage).

8.3.6 External Compensation (COMP Pin)

The TPS92512 error amplifier output is connected to the COMP pin. The TPS92512 is a simple device to stabilize and only requires a capacitor from the COMP pin to ground (C_{COMP}). A 0.1 µF capacitor is recommended and will work well for most all applications. If an application requires faster response to input voltage transients, a capacitor as small as 0.01 µF will work for most applications if needed. The overall system bandwidth can be approximated using Equation 9.

$$BW = \frac{g_{M(ea)}}{2\pi \times C_{COMP}} \tag{9}$$

8.3.7 Overcurrent Protection

Overcurrent can be the result of a shorted sense resistor or a direct short from VOUT to GND. In either case, the voltage at the ISENSE pin is zero and this causes the COMP pin voltage to rise. When V_{COMP} reaches approximately 2.2 V, it is internally clamped and functions as a MOSFET current limit. The TPS92512 limits the MOSFET current to 6 A (typical). If the shorted condition persists, the TPS92512 junction temperature increases. If it increases above 165°C, the thermal shutdown protection is activated.

8.3.8 Overtemperature Protection

The TPS92512 includes a thermal shutdown circuit to protect the device from over-temperature conditions. The device can overheat due to high ambient temperatures, high internal power dissipation, or both. In the event the die temperature reaches 165°C the device will shut down until the die temperature falls 20°C at which point it will turn back on.

8.4 Device Functional Modes

8.4.1 Start-Up

To reduce inrush current and to keep the regulator in control during all startup conditions the TPS92512 employs a startup mode that behaves differently than during normal operation (*regulation mode*). The UVLO conditions must be satisfied before the TPS92512 is allowed to switch. When the UVLO pin is held low the device enters a low-power shutdown mode, and some internal circuits are deactivated to conserve power. When UVLO returns high these circuits are enabled, which results in a delay of approximately 50 µs (typical) before switching starts. During start-up the TPS92512 operates in a *minimum pulse width* mode which is an open-loop control. At the start of each switching cycle the internal oscillator initiates a SET pulse. The high-side MOSFET turns on with a minimum pulse width of 140 ns (typical), independent of the COMP voltage. The device does not pulse skip. While operating in minimum pulse width mode, the LED bypass capacitor is being charged causing an in-rush current. Also, the COMP voltage begins to rise as the error amplifier output current charges the compensation capacitor. When the COMP voltage reaches approximately 0.7 V, the error amplifier is ensured to be out of saturation and to have sufficient gain to regulate the loop. The TPS92512 then transitions from *minimum pulse width* mode to *regulation* mode. During regulation mode the error amplifier is now in closed-loop control of the system. The gain of the error amplifier quickly increases the duty cycle, which causes the output voltage to increase. Once the output voltage approaches the forward voltage of the LED string, the LED current quickly begins to increase until it reaches regulation.

There is a slight delay from the time the VIN and EN UVLO conditions are satisfied until the time the error amplifier has control of the feedback loop. This delay is a result of the time it takes COMP to charge the compensation capacitor to 0.7 V. This delay can be approximated as shown in Equation 10.

$$t_{DELAY} = C_{COMP} \times \frac{0.7\ V}{28\ \mu A} \tag{10}$$

The peak inrush current, I_{PEAK}, can be calculated to a first order approximation using Equation 11 and the value of the output capacitor, C_{OUT}.

$$I_{PEAK} = \frac{V_{IN} \times t_{ON(min)} \times f_{SW}}{\sqrt{\frac{L}{C_{OUT}}} + R_{ISENSE}} \tag{11}$$

8.4.2 Minimum Pulse Width and Limitations

The TPS92512 is designed to output a minimum pulse width during each switching cycle of 140 ns (typical). The control loop cannot regulate the system to an on-time less than this amount, and it does not skip pulses. When attempting to operate below the minimum on-time the system loses regulation and the LED current increases. This puts a practical limitation on the system operating conditions, as shown in Equation 12.

$$V_{IN} = \frac{V_{OUT}}{f_{SW} \times t_{ON(min)}} \tag{12}$$

Where V_{OUT} equals the forward voltage of the LED string plus the reference voltage V_{ISENSE}.

The system can avoid this operating condition by limiting the maximum input voltage as shown in Equation 12. If the input voltage cannot be limited due to application, then the switching frequency can be lowered, or the output voltage increased. This region of operation typically occurs with high input voltages, high operating frequencies, and low output voltages.

8.4.3 Maximum Duty Cycle and Bootstrap Voltage (BOOT)

The TPS92512 requires a small 0.1 µF ceramic capacitor between the BOOT and PH pins to provide the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET turns off, and the freewheeling rectifier diode conducts. A ceramic capacitor with an X7R or X5R dielectric and a minimum voltage rating of 10 V is recommended.

Device Functional Modes (continued)

The TPS92512 is designed to operate up to 100% duty cycle as long as the BOOT to PH voltage is greater than at least 2 V. If the BOOT capacitor voltage drops below 2 V, then the BOOT UVLO circuit turns off the MOSFET, which allows the BOOT capacitor to be recharged. The current required from the BOOT capacitor to keep the MOSFET on is quite low. Therefore, many switching cycles occur before the BOOT capacitor is refreshed. In this way, the effective duty cycle of the converter is quite high.

Attention must be taken in maximum duty cycle applications which experience extended time periods with little or no load current such as during PWM dimming. When the voltage across the BOOT capacitor falls below the 2 V UVLO threshold, the high-side MOSFET is turned off, but there may not be enough inductor current to pull the PH pin down to recharge the BOOT capacitor. The high-side MOSFET of the regulator stops switching because the voltage across the BOOT capacitor is less than 2 V. The output capacitor then decays until the difference between the input voltage and output voltage is greater than 2 V, at which point the BOOT UVLO threshold is exceeded, and the device starts switching again until the desired output current is reached. This operating condition persists until the input voltage and/or the load current increases. It is recommended to adjust the VIN stop voltage, V_{STOP}, to be greater than the BOOT UVLO trigger condition at the minimum load of the application using the adjustable UVLO feature.

8.4.4 Thermal Shutdown and Thermal Limitations

The TPS92512 is a high current density device in a small package. Therefore; it is not capable of providing the full 2.5 A of output current under all conditions without the die reaching the thermal shutdown temperature. To ensure the device will not get too hot the package power dissipation should be calculated and used in conjunction with the device *Thermal Information* to estimate the maximum die temperature for a given application. The total device power dissipation can be closely approximated using the following equations:

$$D = \frac{V_{OUT}}{VIN} \tag{13}$$

$$P_{D(sw)} = D \times R_{DS(on)} \times I_{LED}^{2} \tag{14}$$

$$P_{D(IQ)} = V_{IN} \times \left(400\ \mu A + \frac{2\ mA \times f_{SW}}{1\ MHz} \right) \tag{15}$$

$$P_{D(AC)} = 0.73 \times 10^{-9} \times f_{SW} \times VIN^{2} \times I_{LED} \tag{16}$$

$$P_{TOT} = P_{D(SW)} + P_{D(IQ)} + P_{D(AC)} \tag{17}$$

Where each are in Watts and

- D is the maximum duty cycle (at minimum input voltage)
- V_{OUT} is the LED stack voltage plus the reference voltage V_{ISENSE}
- $P_{D(SW)}$ is the power dissipated in the MOSFET
- $P_{D(IQ)}$ is the power dissipated by the internal circuitry
- $P_{D(AC)}$) are the approximate AC losses due to the MOSFET transitions
- P_{TOT} is the total device dissipation

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section describes power component selection not discussed in the *Feature Description* section.

9.1.1 Inductor Selection

The value of the buck inductor impacts the peak-to-peak ripple-current amplitude. The peak inductor current is used in current mode control and to maintain a good signal to noise ratio it is recommended that the peak-to-peak ripple current (I_R Equation 18) is greater than 75 mA for dependable operation. This allows the control system to have an adequate current signal even at the lowest input voltage. Equation 18 calculates the value for the buck inductance given the minimum ripple current of I_R = 75 mA. Enter the lowest input voltage and the highest output voltage to yield the maximum inductance value.

$$L = \frac{V_{OUT} \times (VIN - V_{OUT})}{I_R \times VIN \times f_{SW}} \quad (18)$$

Calculate the maximum inductor value for the particular application and choose the next lowest standard value for applications requiring low ripple current. Choose a lower value for size sensitive applications that can tolerate higher LED current ripple or use larger output capacitors. With the chosen value the user can calculate the actual inductor current ripple using Equation 19.

$$I_{RIPPLE} = \frac{V_{OUT} \times (VIN - V_{OUT})}{L \times VIN \times f_{SW}} \quad (19)$$

The inductor RMS current and saturation current ratings must be greater than those seen in the application. This ensures that the inductor does not overheat or saturate. During power-up, transient conditions, or fault conditions, the inductor current can exceed its normal operating current. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the converter current limit. This is not always possible due to application size limitations. The peak inductor current and the RMS current equations are shown in Equation 20 and Equation 21.

$$I_{L\_PEAK} = I_{LED} + \frac{I_{RIPPLE}}{2} \quad (20)$$

$$I_{L\_RMS} = \sqrt{I_{LED}^2 + \frac{I_{RIPPLE}^2}{12}} \quad (21)$$

9.1.2 Input Capacitor Selection

The TPS92512 requires a high-quality ceramic, type X5R or X7R, input decoupling capacitor of at least 2 µF of effective capacitance per 1 A of output current. Ceramic capacitance tends to decrease as the applied dc voltage increases. This depreciation must be accounted for to ensure that the minimum input capacitance is satisfied. In some applications, additional capacitance is needed to provide bulk energy storage such as high current PWM dimming applications. The input capacitor voltage rating must be greater than the maximum input voltage and have a ripple current rating greater than the maximum input current ripple of the converter. The RMS input ripple current is calculated in Equation 22, where D is the duty cycle (output voltage divided by input voltage). The maximum RMS input ripple current can be calculated by using the minimum input voltage for the application.

$$I_{IN\_RMS} = I_{LED} \times \sqrt{D \times (1 - D)} \quad (22)$$

Application Information (continued)

The input capacitance (C_{IN}) is inversely proportional to the input ripple voltage of the converter. The peak-to-peak input ripple voltage can be calculated as shown in Equation 23. Additionally, this equation can be used to solve for the required input capacitance to keep the input ripple voltage to a defined limit.

$$\Delta VIN = \frac{I_{LED} \times D \times (1 - D)}{C_{IN} \times f_{SW}} \quad (23)$$

9.1.3 Output Capacitor Selection

During start-up, the TPS92512 uses the discharged output capacitor as a charging path for the BOOT capacitor. In order to ensure that the BOOT capacitor charges and that the converter begins switching immediately, the value of the output capacitor should be 10 times larger than the BOOT capacitor. If the BOOT capacitor is 0.1 µF, then the minimum output capacitor should be 1 µF for the fastest startup time. If the output capacitor is chosen to be a smaller value or none at all, then the BOOT capacitor can charge through the LED string itself. However, this method of charging the BOOT capacitor will result in longer startup times.

The output capacitor also reduces the high-frequency ripple current through the LED string. Various guidelines disclose how much high-frequency ripple current is acceptable in the LED string. Excessive ripple current in the LED string increases the RMS current in the LED string, and therefore the LED temperature also increases. First, calculate the total dynamic resistance of the LED string (R_{LED}) using the LED manufacturer's data sheet. Second, calculate the required impedance of the output capacitor (Z_{OUT}) given the acceptable peak-to-peak ripple current through the LED string, ΔI_{LED}. I_{RIPPLE} is the peak-to-peak inductor ripple current as calculated previously in *Inductor Selection*. Third, calculate the minimum effective output capacitance required. Finally, increase the output capacitance appropriately due to the derating effect of applied dc voltage. See Equation 24, Equation 25, and Equation 26.

$$R_{LED} = \frac{\Delta V_F}{\Delta I_F} \times \#\ \text{of LEDs} \quad (24)$$

$$Z_{COUT} = \frac{R_{LED} \times \Delta I_{LED}}{I_{RIPPLE} - \Delta I_{LED}} \quad (25)$$

$$C_{OUT} = \frac{1}{2 \times \pi \times f_{SW} \times Z_{COUT}} \quad (26)$$

9.1.4 Rectifier Diode Selection

The rectifier diode conducts the inductor current only during the high-side MOSFET off-time. The rectifier diode must have a reverse voltage rating greater than the maximum input voltage and a current rating greater than the peak inductor current. A Schottky diode is recommended for highest efficiency and optimal performance. The package size chosen for the rectifier diode must be capable of handling the power dissipation of the diode. The diode power dissipation is equal to the average diode current times the diode forward voltage, V_F. See Equation 27 and Equation 28.

$$I_{D\_AVE} = I_{LED}(1 - D) \quad (27)$$

$$P_{DIODE} = I_{D\_AVE} \times V_F \quad (28)$$

When calculating the diode average current, the worst case duty cycle, D, for the diode should be used. D should be calculated using the maximum input voltage for the application in this case.

9.1.5 Output Protection Clamp (Optional)

In the event of an output open circuit during normal operation the output voltage will rise up to the input voltage. This is a safe operating mode provided the output capacitor can sustain the voltage without damage. However, the inductor will still have energy stored at the moment of the event. This can cause significant ringing between the inductor and output capacitor that can shoot higher than VIN. To prevent this, a single Schottky diode from V_{OUT} to VIN can be used to clamp the ringing. This diode should be rated for at least 500 mA and have a voltage rating greater than or equal to the voltage rating of the rectifier diode. A zener diode across the output capacitor can also be used to clamp the output voltage to a lower level. The output will clamp at the zener voltage plus the ISENSE voltage since when the zener begins to conduct it will pull the ISENSE pin up and reduce the duty cycle.

9.2 Typical Application

The TPS92512 is a switching regulator designed to provide tight current regulation and high performance over a wide range of conditions. The following application is a design example for a wide input voltage range, high current regulator.

Figure 13 shows the schematic for the wide input voltage range converter with the design requirements below. A detailed design procedure to calculate various component values follows.

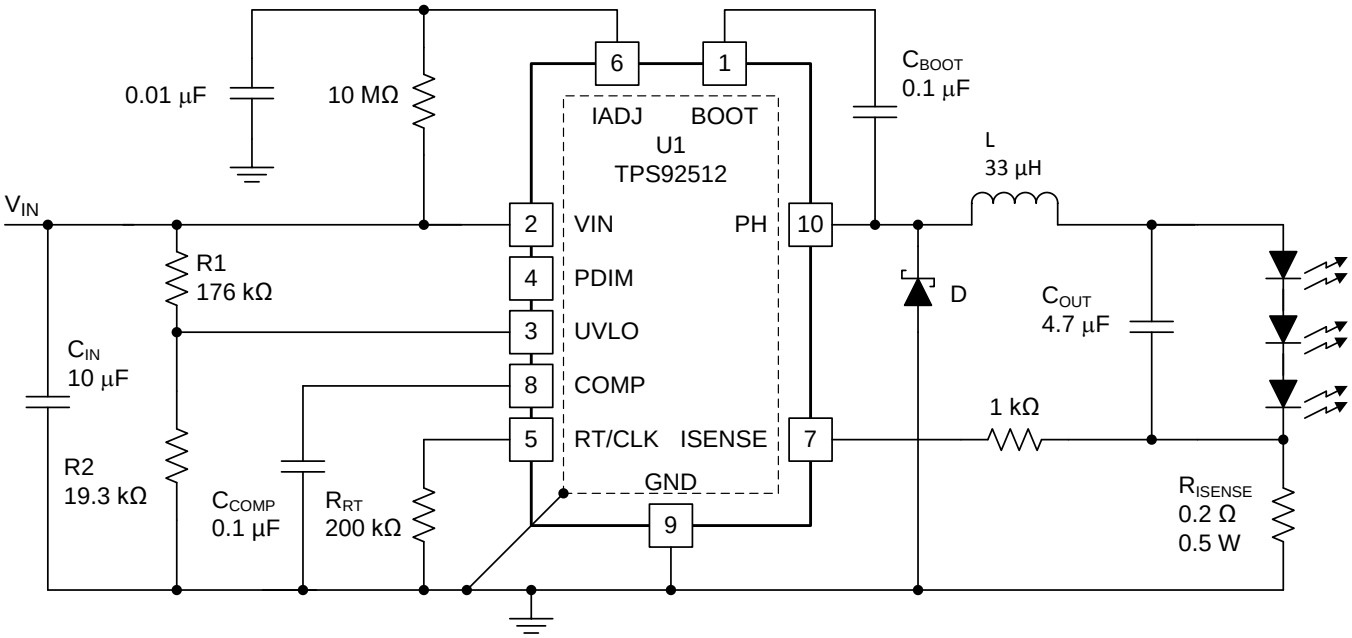


Figure 13. High Current, Low LED Current Ripple Buck Converter

9.3 Design Requirements

- VIN range of 12 V to 48 V
- UVLO set to 12 V with 0.8 V hysteresis
- 3 LED output, 9.7 V stack, V_{OUT} = 10 V
- 1.5A LED current (at V_{ISENSE} = 300 mV for best accuracy)
- Switching frequency of 570 kHz
- LED current ripple of 10 mA or less

9.4 Detailed Design Procedure

This section provides a detailed design procedure for selecting the component values for the application with the given design requirements.

9.4.1 Standard Component Selection

Choose a 0.1 µF ceramic capacitor with a 10 V or greater rating for C_{COMP} and C_{BOOT}. Connect IADJ to VIN through a 10 MΩ resistor to clamp it at 1.8 V and provide an ISENSE voltage regulation point of 300 mV. Connect a 10 nF capacitor from IADJ to ground. Connect ISENSE to $R_{(ISENSE)}$ through a 1 kΩ resistor.

9.4.2 Calculate UVLO Resistor Values

Using Equation 1 and Equation 2 the UVLO resistors R1 and R2 can be calculated using Equation 29, Equation 30, and the following parameters:

- V_{START} = 12 V
- V_{STOP} = 11.2 V
- V_{HYS} = 0.8 V

$$R1 = \frac{0.8 \times \left(1.22\ V - \left(1\ \mu A \times 10\ k\Omega\right)\right) - 2.9\ \mu A \times 10\ k\Omega \times 12\ V}{2.9\ \mu A \times 1.22\ V} = 175\ k\Omega \quad (29)$$

Choose the closest standard 1% value of 176 kΩ for R1. This value can then be used to calculate the value of R2 as shown in Equation 30.

$$R2 = \frac{174\ k\Omega \times \left(1.22\ V - \left(10\ k\Omega \times \left(1\ \mu A + 2.9\ \mu A\right)\right)\right)}{\left(11.2\ V - 1.22\ V\right) + \left(1\ \mu A + 2.9\ \mu A\right) \times \left(174\ k\Omega + 10\ k\Omega\right)} = 19.2\ k\Omega \quad (30)$$

Choose the closest standard 1% value of 19.3 kΩ for R2.

9.4.3 Calculate the RT Resistor Value (R_{RT})

The desired switching frequency is 570 kHz, so the value of R_{RT} can be calculated using Equation 5 as shown in Equation 31.

$$R_{RT}\left(k\Omega\right) = \frac{206033}{\left(570\right)^{1.092}} = 201.6\ k\Omega \quad (31)$$

Choose the closest standard 1% value of 200 kΩ for R_{RT}.

9.4.4 Calculate the ISENSE Resistor Value ($R_{(ISENSE)}$)

This design uses a V_{ISENSE} voltage of 300 mV and the desired LED current (I_{LED}) is 1.5 A. Given these values the sense resistor value can be calculated using Equation 8 as shown in Equation 32.

$$R_{ISENSE} = \frac{300\ mV}{1.5\ A} = 0.2\ \Omega \quad (32)$$

0.2 Ω is a standard 1% resistor value. The power dissipation is V_{ISENSE} multiplied by I_{LED}, in this case 0.45 W. Choose a 0.5 W or greater resistor.

9.4.5 Calculate the Inductor Value and Operating Parameters (L)

For this application, low LED ripple current is important. One way to reduce LED ripple current is to reduce inductor ripple current. For this low ripple current application, the maximum inductor value (minimum 75 mA current ripple I_R) will be calculated and the next lower value will be used. The maximum inductor value can be calculated using Equation 18 as shown in Equation 33.

$$L = \frac{10\ V \times \left(12\ V - 10\ V\right)}{75\ mA \times 12\ V \times 570\ kHz} = 39\ \mu H \quad (33)$$

Choose the next lowest standard value of 33 µH. Now the actual inductor current ripple, the peak inductor current, and the RMS inductor current can be calculated using Equation 19, Equation 20, and Equation 21 as shown in Equation 34, Equation 35, and Equation 36.

Detailed Design Procedure (continued)

$$I_{RIPPLE} = \frac{10\ V \times (12\ V - 10\ V)}{33\ \mu H \times 12\ V \times 570\ kHz} = 89\ mA \quad (34)$$

$$I_{L\_PEAK} = 1.5\,A + \frac{88\,mA}{2} = 1.544\,A \quad (35)$$

$$I_{L\_RMS} = \sqrt{1.5\,A^2 + \frac{88\,mA^2}{12}} = 1.5002\,A \quad (36)$$

The inductor chosen should have a saturation current rating higher than I_{L_PEAK} and a DC current rating higher than I_{L_RMS}.

9.4.6 Calculate the Minimum Input Capacitance and the Required RMS Current Rating (C_{IN})

Given a minimum of 2 µF of capacitance for every 1 A of LED current, a 1.5 A design would require a minimum of 3 µF. To account for ceramic capacitor tolerances and capacitance drops due to bias voltage this capacitance should be at least doubled. Higher values will also give better overall performance. Choose a 10 µF capacitor with a voltage rating of 50 V or greater. Using Equation 13, Equation 22, and Equation 23 the user can calculate the RMS current rating required for the capacitor and the resulting input voltage ripple as shown in Equation 38 and Equation 39.

$$D = \frac{10\,V}{12\,V} = 0.83 \quad (37)$$

$$I_{IN\_RMS} = 1.5\,A \times \sqrt{0.83 \times (1 - 0.83)} = 0.56\,A \quad (38)$$

$$\Delta VIN = \frac{1.5\ A \times 0.83 \times (1 - 10.83)}{10\ \mu F \times 570\ kHz} = 37\ mV \quad (39)$$

9.4.7 Calculate the Output Capacitor Value (C_{OUT})

The required output capacitor value to get the required LED ripple current can be calculated by first determining the dynamic resistance of the LEDs used, R_{LED}, by using the forward voltage versus forward current graph in the manufacturer's datasheet. Place a tangent line on the curve at the forward current required to get the slope and the corresponding ΔV and ΔF. For this design example, the R_{LED} is 0.22 Ω per LED. So the total R_{LED} is 0.22 Ω X 3, or 0.66 Ω. Then find the required output impedance, Z_{COUT}, using Equation 25 as shown in Equation 40. Using the required Z_{COUT} calculate the minimum output capacitance using Equation 26 as shown in Equation 41.

$$Z_{COUT} = \frac{0.66\,\Omega \times 10\,mA}{89\,mA - 10\,mA} = 0.0835\,\Omega \quad (40)$$

$$C_{OUT} = \frac{1}{2 \times \pi \times 570\,kHz \times 0.0835\,\Omega} = 3.34\,\mu F \quad (41)$$

Choose a 4.7 µF ceramic capacitor with a X5R or X7R dielectric and 16 V or greater voltage rating.

9.4.8 Calculate the Diode Power Dissipation (D)

The maximum input voltage is 48 V, so a 60 V or greater Schottky diode should be used for this application. Calculate the required current rating and power dissipation to size the diode correctly. This should be done at the maximum input voltage since that is where the diode conducts for the most time and will have the highest power dissipation. The duty cycle, D, at the maximum input voltage is 10 V/48 V, or 0.208. Using this duty cycle and Equation 27 calculate the average diode current, I_{D_AVE}, as shown in Equation 42. Then calculate the diode power dissipation, P_{DIODE}, using Equation 28 as shown in Equation 43.

$$I_{D\_AVE} = 1.5\ A \times (1 - 0.208) = 1.19\ A \quad (42)$$

$$P_{DIODE} = 1.19\ A \times 0.7\ V = 0.833\ W \quad (43)$$

The power dissipation calculation is assuming a diode forward voltage drop, V_F, of 0.7 V. If a diode with a different forward drop is chosen the calculation should be re-done. Choose a Schottky diode with a 1.5 A or greater current rating that can dissipate at least 1 W of power.

9.5 Application Curves

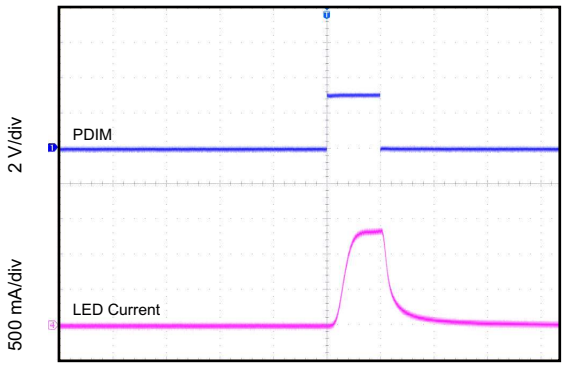


Figure 14. 1% Duty Cycle, 250 Hz PWM Dimming

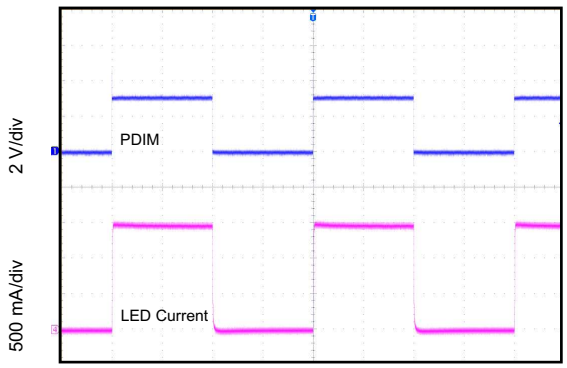


Figure 15. 50% Duty Cycle, 250 Hz PWM Dimming

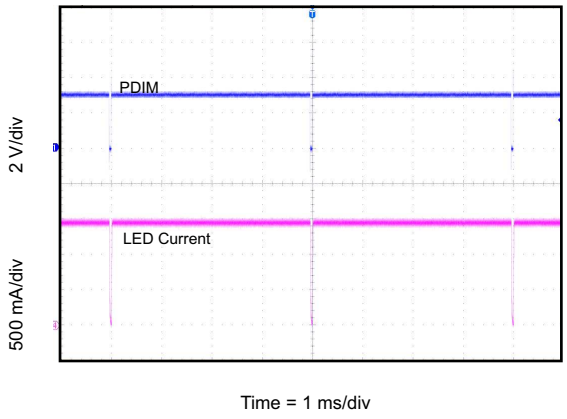


Figure 16. 99% Duty Cycle, 250 Hz PWM Dimming

10 Power Supply Recommendations

Use any DC output power supply with a maximum voltage high enough for the application. The power supply should have a current limit of at least 3A.

11 Layout

The TPS92512 requires a proper layout for optimal performance. The following section gives some guidelines to ensure a proper layout.

11.1 Layout Guidelines

An example of a proper layout for the TPS92512 is shown in Figure 17. Creating a large GND plane under the integrated circuit (IC) for good electrical and thermal performance is important.

- The GND pin of the device must connect to the GND plane directly beneath the IC.
- Thermal vias can be used to connect the topside GND plane to additional printed-circuit board (PCB) layers for heat spreading and more solid grounding.
- The input capacitors must be located as close as possible to the VIN pin and the GND plane and should be tied to a solid backside ground plane using multiple vias.
- The compensation components must be located as close as possible to the COMP and GND pins in order to minimize noise sensitivity.
- The PH trace must be kept as short as possible to reduce the possibility of radiated noise/EMI.
- The ISENSE node should be kept as short as possible and shielded from noise.
- The RT/CLK pin is sensitive and its routing must be kept as short as possible.
- In higher current applications, routing the load current of the current-sense resistor to the junction of the input capacitor and rectifier diode GND node may be necessary. The easiest way to accomplish this is to use a backside ground plane and arrays of vias to connect the top side ground connections solidly to the backside plane. This steers the high current away from the sensitive RT/CLK to GND connection.
- If possible, the current loop created when the internal MOSFET is on should be in the same direction as the current loop when the internal MOSFET is off and the schottky diode is conducting. This will prevent magnetic field reversal, reduce radiated noise, and simplify EMI filtering.

11.2 Layout Example

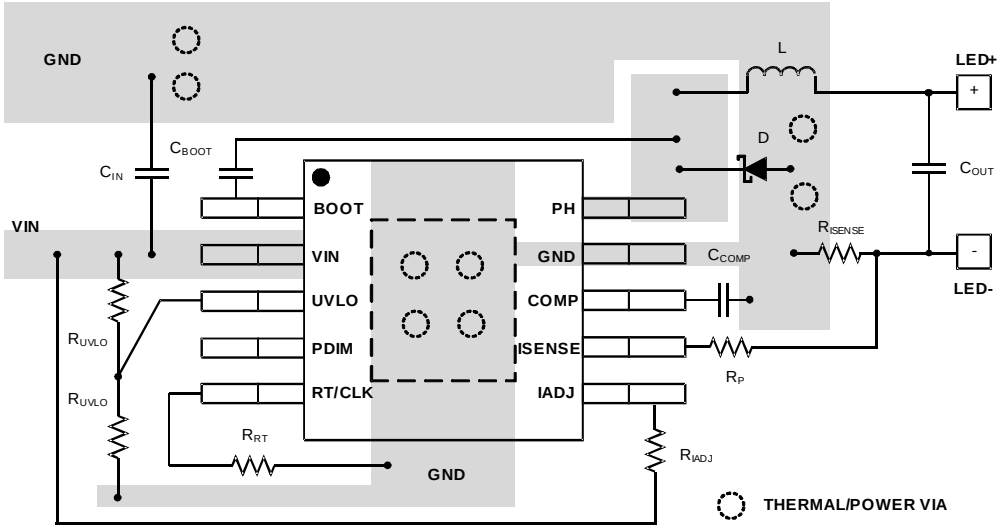


Figure 17. Layout Example

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS92512	Click here	Click here	Click here	Click here	Click here
TPS92512HV	Click here	Click here	Click here	Click here	Click here

12.2 Trademarks

PowerPAD is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92512DGQR	ACTIVE	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	92512	Samples
TPS92512DGQT	ACTIVE	HVSSOP	DGQ	10	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	92512	Samples
TPS92512HVDGQR	ACTIVE	HVSSOP	DGQ	10	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	512H	Samples
TPS92512HVDGQT	ACTIVE	HVSSOP	DGQ	10	250	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	512H	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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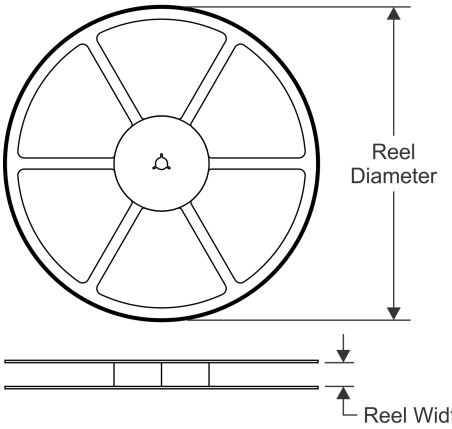
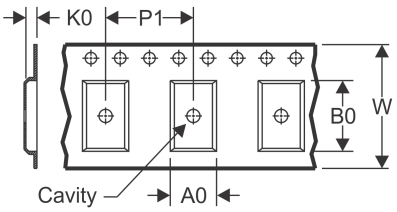
TAPE AND REEL INFORMATION

REEL DIMENSIONS

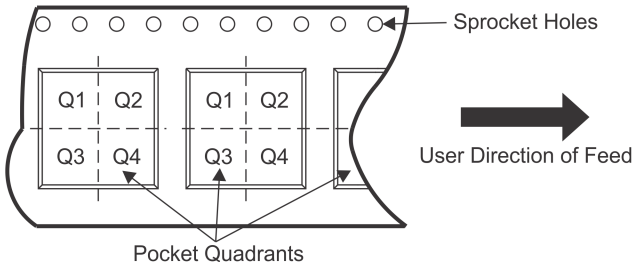


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

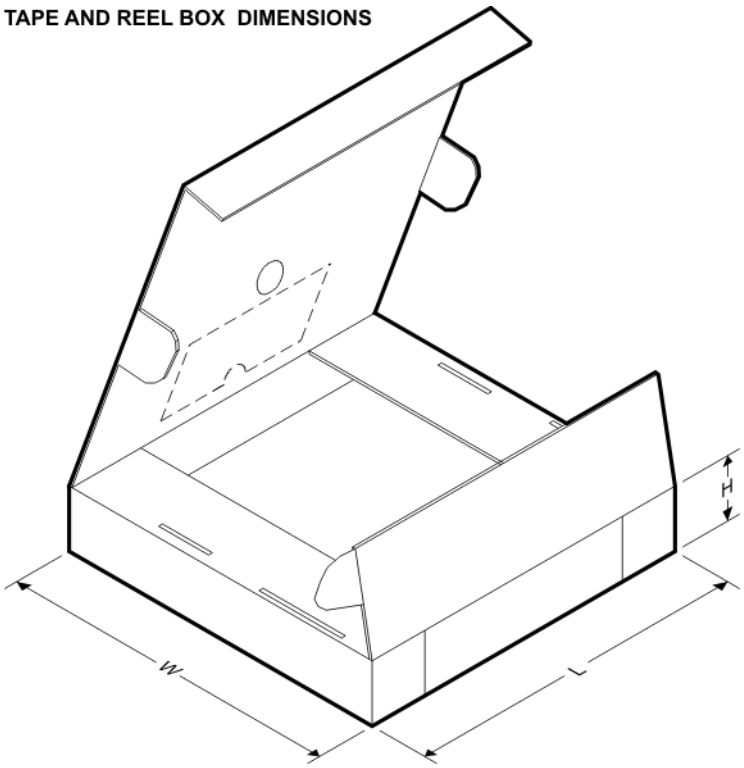
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92512DGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS92512DGQT	HVSSOP	DGQ	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS92512HVDGQR	HVSSOP	DGQ	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS92512HVDGQT	HVSSOP	DGQ	10	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

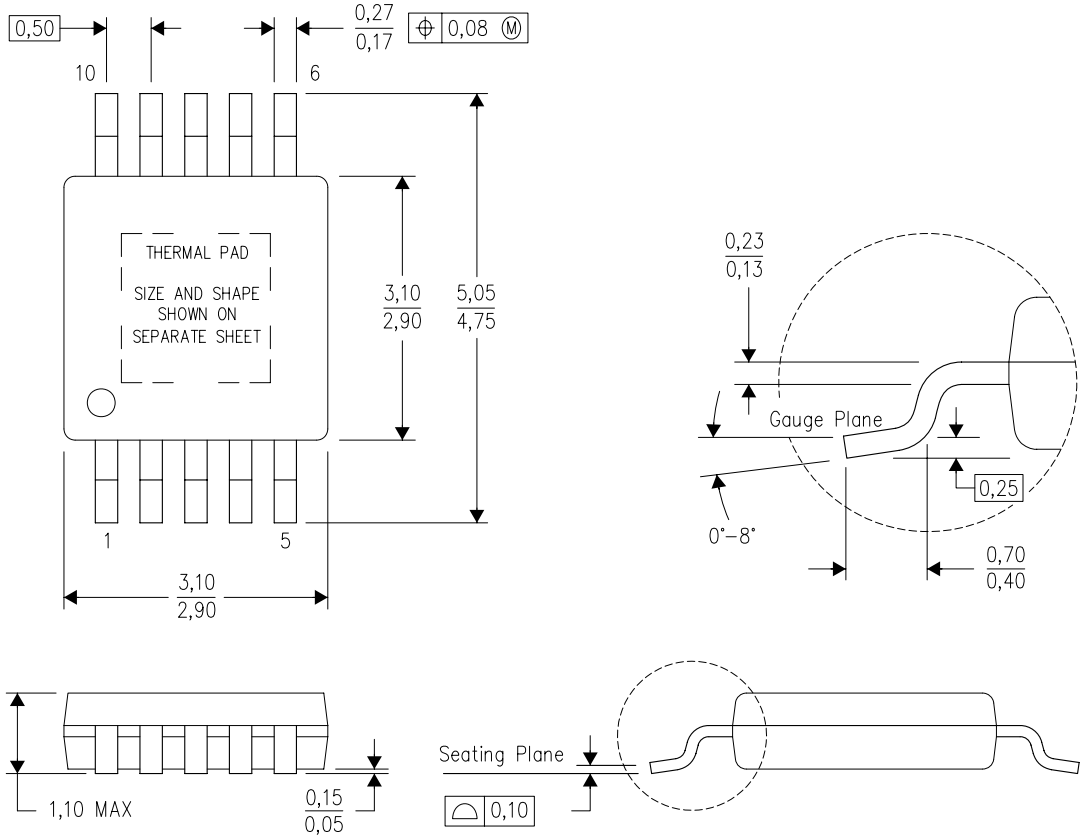
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92512DGQR	HVSSOP	DGQ	10	2500	364.0	364.0	27.0
TPS92512DGQT	HVSSOP	DGQ	10	250	364.0	364.0	27.0
TPS92512HVDGQR	HVSSOP	DGQ	10	2500	364.0	364.0	27.0
TPS92512HVDGQT	HVSSOP	DGQ	10	250	364.0	364.0	27.0

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE



4073273/F 11/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–187 variation BA–T.

PowerPAD is a trademark of Texas Instruments.

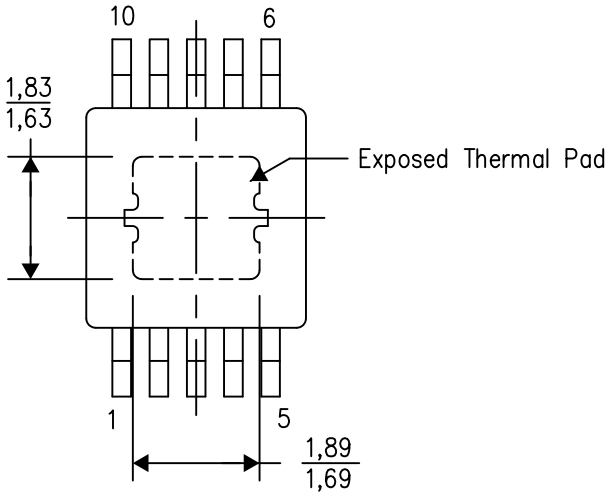
DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

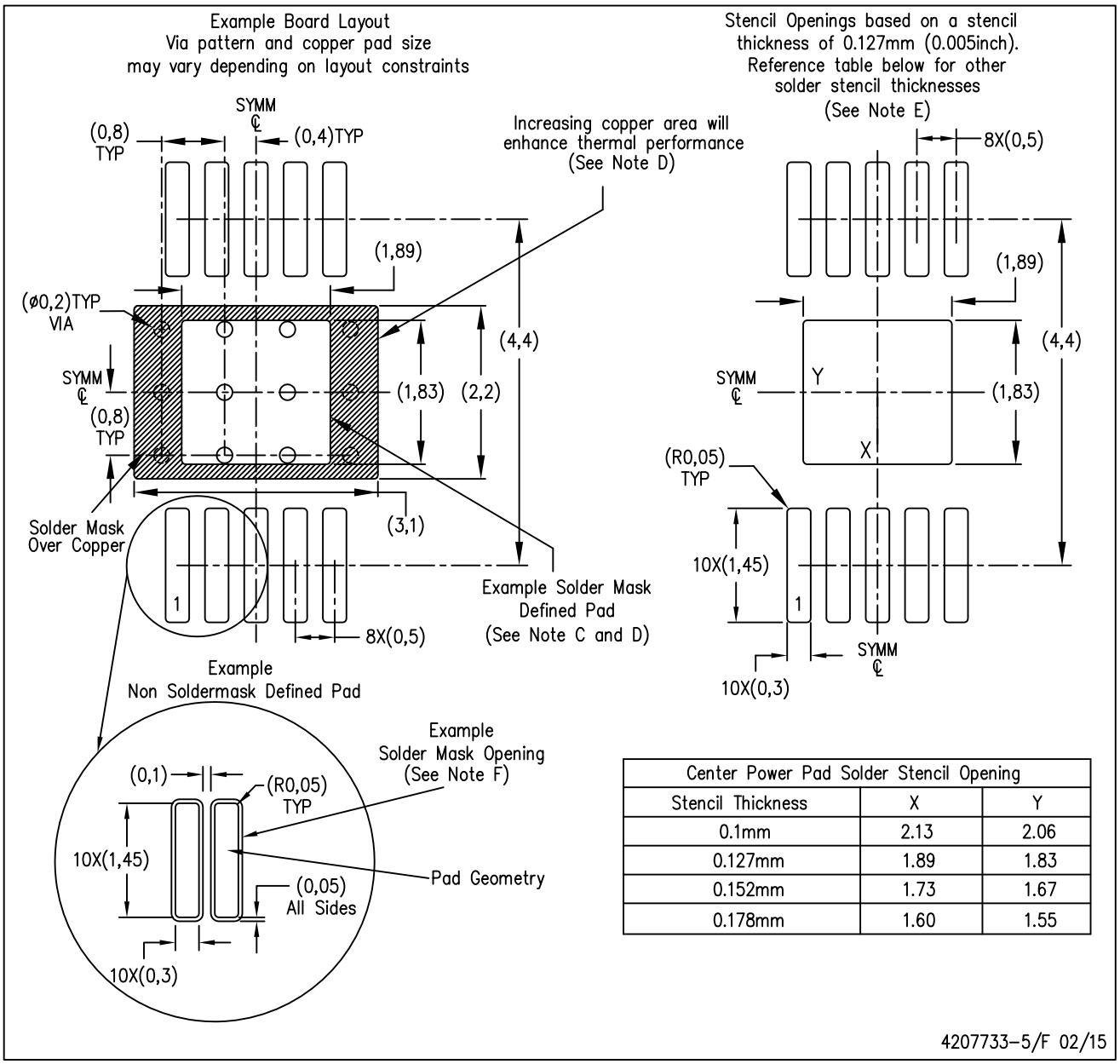
Exposed Thermal Pad Dimensions

4206324–7/H 12/14

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGQ (S–PDSO–G10) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.13	2.06
0.127mm	1.89	1.83
0.152mm	1.73	1.67
0.178mm	1.60	1.55

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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