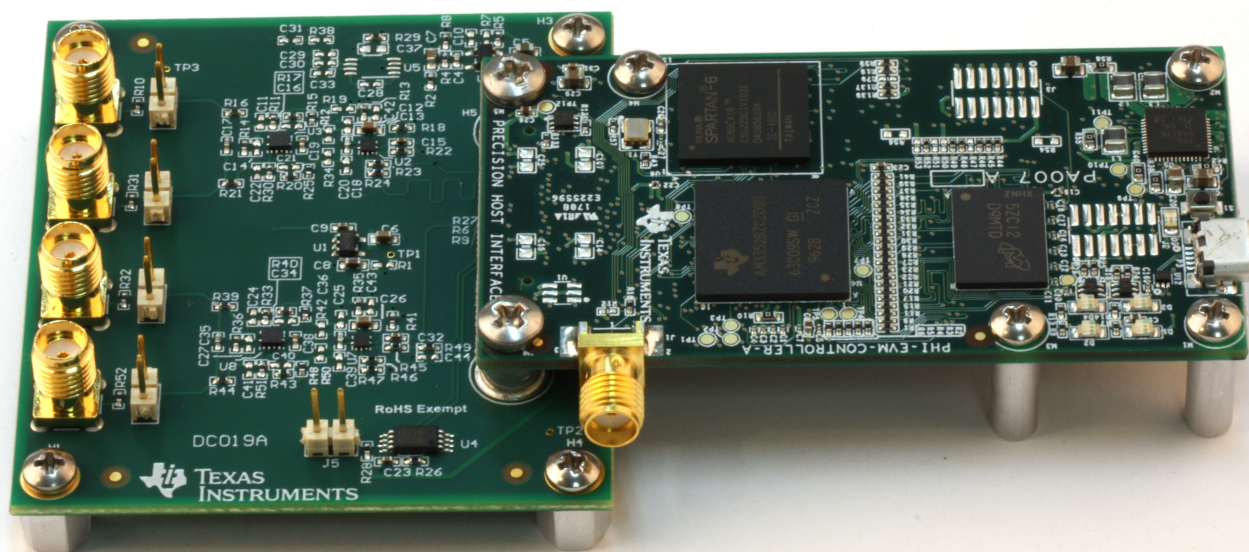


ADS7057 Evaluation Module

This user's guide describes the characteristics, operation, and use of the ADS7057 evaluation module (EVM) performance demonstration kit (PDK). This kit is an evaluation platform for the ADS7057 device, which is a 14-bit, 2.5-MSPS, differential analog input, successive approximation register (SAR) analog-to-digital converter (ADC) that features an easy-to-use SPI. This evaluation module can also be used for performance evaluation of ADS7054 (14-bit, 1-MSPS, differential analog input SAR ADC). The EVM-PDK eases evaluation with hardware, software, and computer connectivity through the universal serial bus (USB) interface. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials (BOM).



The following related documents are available through the [Texas Instruments](https://www.ti.com) website.

Table 1. Related Documentation

Device	Literature Number
ADS7057	SBAS821
ADS7054	SBAS859
THS4551	SBOS778
TPS79901	SBVS056
REF1933	SBOS697

Contents

1	Overview	3
2	Analog Interface	3
3	Digital Interfaces	4
4	Power Supplies	5

5	ADS7057EVM-PDK Initial Setup	6
6	ADS7057EVM-PDK Operation	11
7	Bill of Materials, Printed-Circuit Board Layout, and Schematics	19

List of Figures

1	ADS7057EVM Analog Input Path	4
2	ADS7057EVM-PDK Jumper Locations	6
3	ADS7057EVM Software Installation Prompts	7
4	Device Driver Installation Wizard Prompts	8
5	LabVIEW Run-Time Engine Installation	9
6	ADS7057EVM-PDK Installation Final Step	10
7	EVM-PDK Hardware Setup and LED Indicators	11
8	Launch the EVM GUI Software.....	12
9	EVM GUI Global Input Parameters	13
10	Time Domain Display Tool Options.....	14
11	Spectral Analysis Tool	15
12	Histogram Analysis Tool	16
13	ADS7057 Calibration	17
14	ADS7057EVM PCB Layer 1: Top Layer	21
15	ADS7057EVM PCB Layer 2: GND Plane	21
16	ADS7057EVM PCB Layer 3: Power Planes.....	22
17	ADS7057EVM PCB Layer 4: Bottom Layer	22
18	Schematic Diagram (Page 1) of the ADS7057EVM PCB.....	23
19	Schematic Diagram (Page 2) of the ADS7057EVM PCB.....	24

List of Tables

1	Related Documentation	1
2	Analog Input Connector Description	3
3	Voltage Settings for AVDD and V _{DD} Supplies	5
4	V _{DD} Voltage Selection Settings.....	5
5	Default Jumper Configurations.....	6
6	External Source Requirements for Device Evaluation (SNR and THD)	15
7	ADS7057EVM Bill of Materials	19

Trademarks

Microsoft, Windows are registered trademarks of Microsoft Corporation.

LabVIEW is a trademark of National Instruments.

All other trademarks are the property of their respective owners.

1 Overview

The ADS7057EVM-PDK evaluation kit includes the ADS7057EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis.

The ADS7057EVM board includes the ADS7057 SAR ADC, all the peripheral analog circuits, and the components required to achieve optimum performance from the ADC.

The PHI controller board primarily serves three functions:

- Provide a communication interface from the EVM to the computer through a USB port
- Provide the digital input and output signals necessary to communicate with the ADS7057 device
- Supply power to all active circuitry on the ADS7057EVM board

Along with the ADS7057EVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

1.1 ADS7057EVM-PDK Features

The ADS7057EVM-PDK showcases the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS7057 ADC
- USB powered — no external power supply is required
- The PHI controller board that provides a convenient communication interface to the ADS7057 ADC over USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for Microsoft® Windows® 7, 64-bit operating systems

1.2 ADS7057EVM Features

The ADS7057EVM showcases the following features:

- Onboard low-noise, low-distortion ADC input drivers optimized to meet ADC performance
- Onboard ultra-low noise, low-dropout (LDO) regulators, to generate supplies for the operation amplifier and voltage reference to generate the power supply for ADC

2 Analog Interface

The ADS7057 is a low-power, small ADC that supports differential analog inputs. The ADS7057EVM uses a THS4551 fully differential amplifier to drive the inputs of the ADC. The ADS7057EVM is designed for easy interfacing to analog sources. This section describes the front-end driver circuitry details, including jumper configurations for the analog input signal source.

2.1 Connectors for Differential Analog Input

The ADS7057EVM is designed for easy interfacing to an external, analog, differential source through either a subminiature version A (SMA) connectors or 100-mil headers. The ADS7057EVM has two ADS7057 ADCs on board. The ADS7057EVM GUI can either be configured for individual ADC data sampling or simultaneous sampling with both ADCs. Jumpers J1, J2, J7, and J10 are the SMA connectors that allow for differential analog source connectivity through coaxial cables. Alternatively, 100-mil jumper cables or mini-grabbers can be used to connect analog sources to the pin 1 of connectors J3, J6, J8, and J9. [Table 2](#) lists the analog input connectors for the individual ADCs.

Table 2. Analog Input Connector Description

Pin Number	Signal	Description
J1 and J2	INP	Differential analog input provided at the SMA for ADC A
J3:1 and J6:1	INP	Alternate location to provide the differential input for ADC A
J7 and J10	INP	Differential analog input provided at the SMA for ADC B
J8:1 and J9:1	INP	Alternate location to provide the differential input for ADC B

2.2 ADC Differential Input Signal Driver

The SAR ADC inputs terminate in switched-capacitor networks that create large instantaneous current loads when the switches are closed, which effectively makes the ADC inputs dynamically low impedance. The differential inputs of the ADC are therefore driven by a THS4551 fully differential amplifier in a small gain configuration to maintain ADC performance with maximum loading at full device throughput of the ADS7057 of 2.5 MSPS.

2.2.1 Input Signal Path

Figure 1 shows the signal path for the positive differential inputs applied to the ADS7057EVM. A separate THS4551 amplifier is used in a fully differential configuration to drive the differential input of each ADC. An RC filter with values of 10 Ω and 680 pF was selected to achieve a SINAD greater than 79 dB and a THD less than -85 dB for a 2-kHz sine wave input at full throughput of the ADS7057 of 2.5 MSPS.

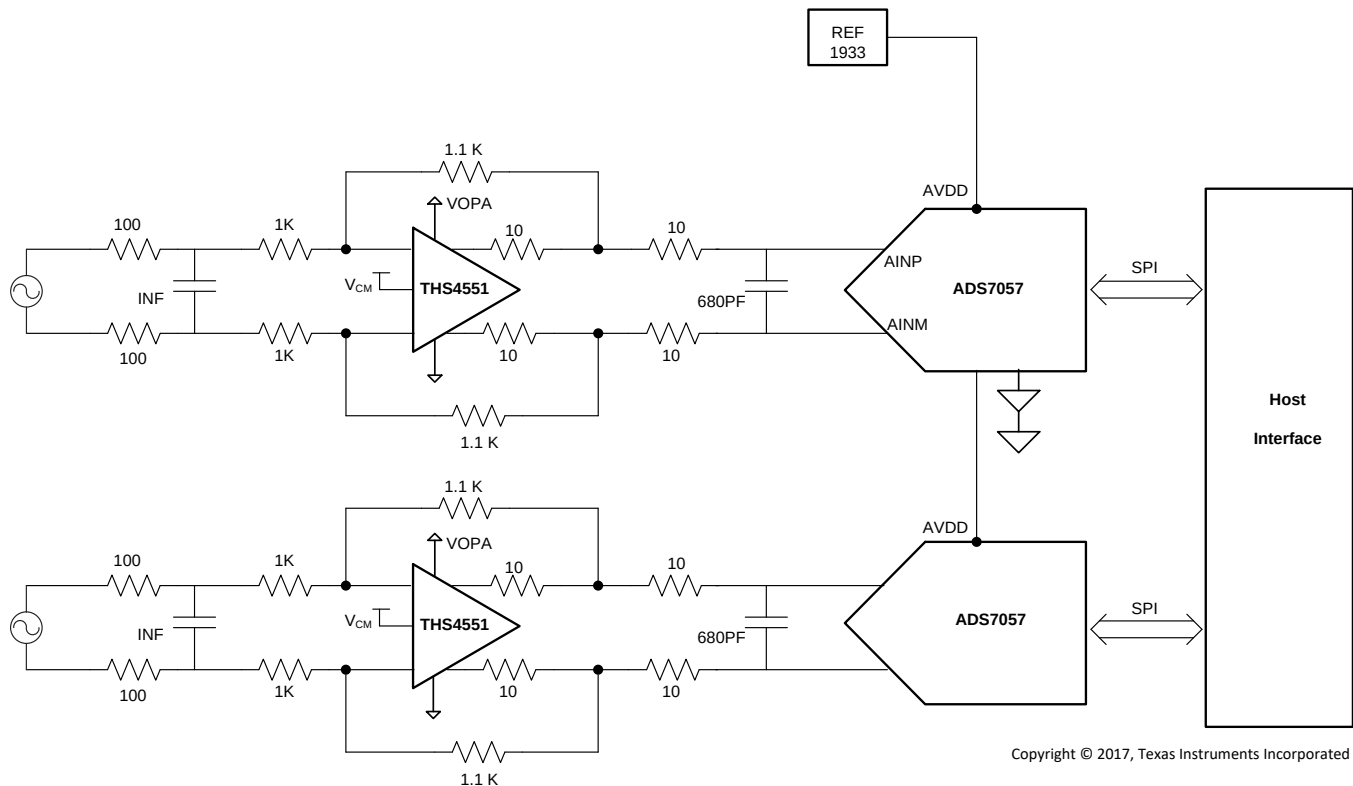


Figure 1. ADS7057EVM Analog Input Path

3 Digital Interfaces

As noted in Section 1, the ADS7057EVM interfaces with the PHI, which in turn communicates with the computer over USB. The three devices on the EVM that the PHI communicates with are the two ADS7057 ADCs (over SPI) and the EEPROM (over I²C). The EEPROM comes preprogrammed with the information required to configure and initialize the ADS7057EVM-PDK platform. When the hardware is initialized, the EEPROM is no longer used.

3.1 SPI for ADC Digital I/O

The ADS7057EVM-PDK supports the interface and calibration modes detailed in [ADS7056 Ultra-Low Power, Ultra-Small Size, 14-Bit, High-Speed SAR ADC](#). The PHI is capable of operating at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC.

4 Power Supplies

The ADS7057 supports a wide range of operation on its analog supplies. The AVDD operates from 2.35 V to 3.6 V. The DVDD operates from 1.65 V to 3.6 V, independent of the AVDD supply. The analog portion of the ADS7057EVM operates from a 5.5-V supply, which in turn generates the 5-V V_{OPA} supply for the THS4551 fully differential amplifier using the TPS79901, which is a low-noise, fixed-voltage regulator. The 3.3-V AVDD supply for the ADS7057 is generated using the REF1933 which is a low-drift, low-power, voltage reference.

The TPS79901 regulator can be configured to generate a V_{OPA} supply other than 5 V by replacing resistors R4 and R8 with appropriate values. [Table 3](#) lists the nearest feedback resistor values that should be populated to generate the desired V_{DD} supply voltage.

Table 3. Voltage Settings for AVDD and V_{DD} Supplies

V_{OPA} Supply Voltage	Device (U6)	R4	R8
5 V (default)	TPS79901	100 k Ω	31.6 k Ω
3.3 V	TPS79901	56 k Ω	31.6 k Ω
3.6 V	TPS79901	63.4 k Ω	31.6 k Ω

There is a provision given for operating the THS4551 operational amplifier and the ADS7057 ADC from a common power supply. [Table 4](#) lists the modifications required to select a common power supply for the THS4551 and ADS7057 devices.

Table 4. V_{DD} Voltage Selection Settings

OPA836 Supply Source	R19	R29
V_{OPA} (default 5 V)	Not installed	Assemble (0 Ω)
AVDD	Assemble (0 Ω)	Not installed

The digital portion of the ADC operates from 3.3-V EVM_DVDD supply from the PHI.

5 ADS7057EVM-PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for proper operation of the ADS7057EVM-PDK.

5.1 Default Jumper Settings

Figure 2 shows the silkscreen plot, which details the jumper locations for ADS7057EVM-PDK.

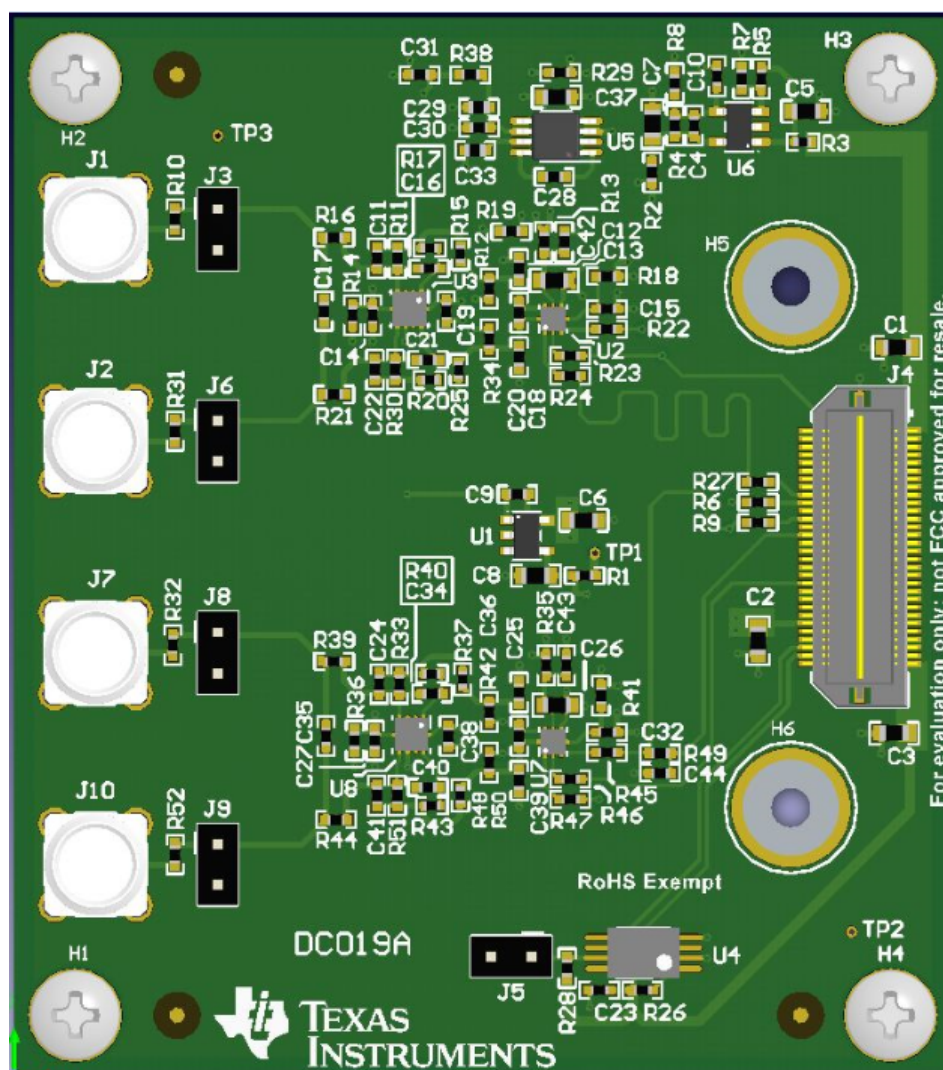


Figure 2. ADS7057EVM-PDK Jumper Locations

Table 5 lists the functionality and default configuration of each jumper. No jumpers are required to be populated on any location of the EVM for normal operation. Remove any jumpers that may be present at locations J3, J5, J6, J8, and J9.

Table 5. Default Jumper Configurations

Reference Designator	Default Configuration	Description
J5	Open	Connect this jumper for EEPROM write protection
J3, J6, J8, J9	Open	Use pin 1 of these jumpers as an alternate location to provide the differential input to ADC A (U2) and ADC B (U7)

5.2 EVM Graphical User Interface Software Installation

The following steps describe how to install the software for the ADS7057 EVM graphical user interface (GUI).

1. Download the latest version of the EVM GUI installer from the *Software* section of the [ADS7057EVM-PDK Tool Folder](#), and run the GUI installer to install the EVM GUI software on your computer.

CAUTION

Manually disable any antivirus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Failure to disable antivirus software, depending on the antivirus settings, may cause an error message to appear or the *installer.exe* file may be deleted.

2. Accept the License Agreements and follow the on-screen instructions to complete the installation (see [Figure 3](#)).

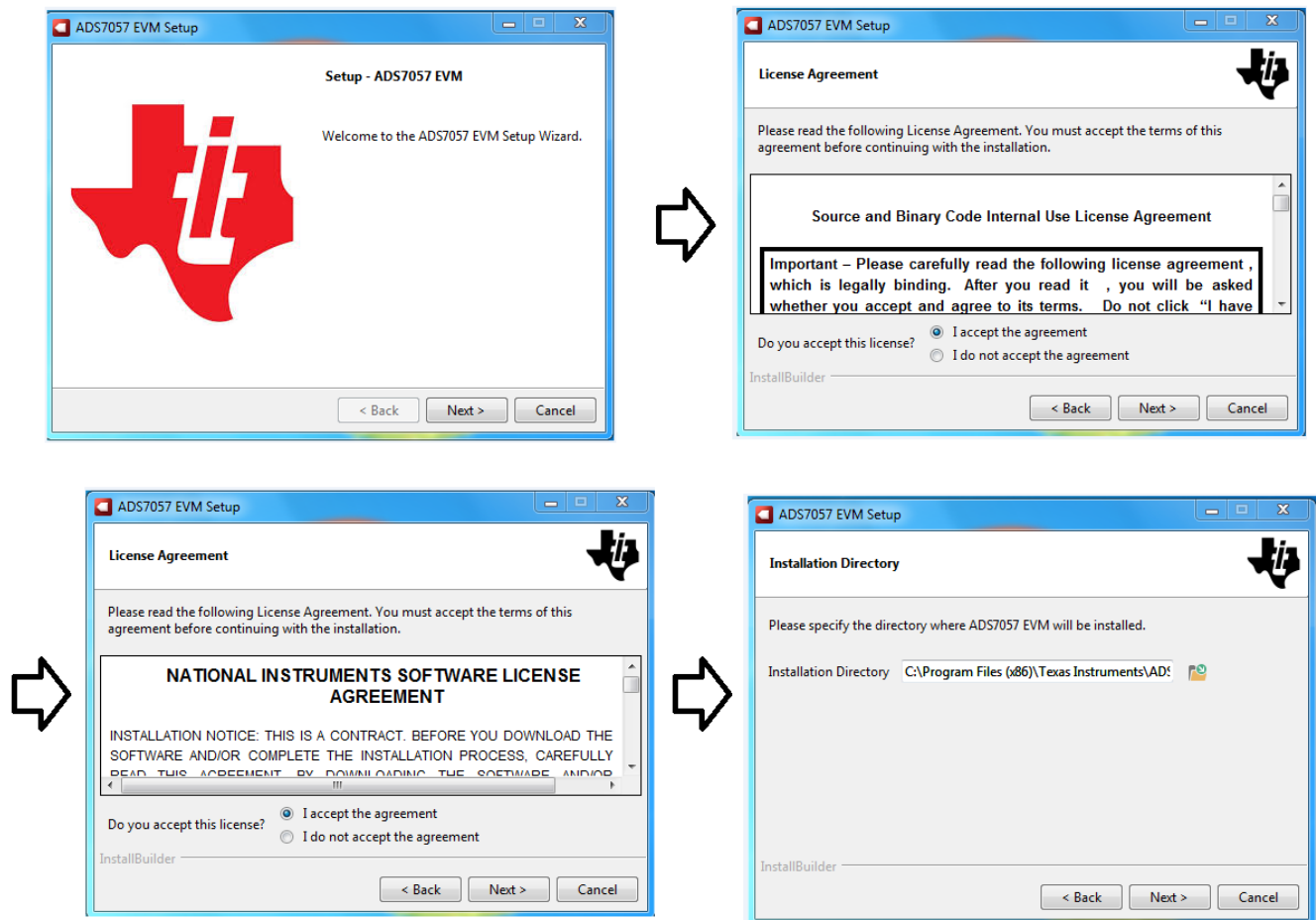


Figure 3. ADS7057EVM Software Installation Prompts

3. As a part of the ADS7057EVM GUI installation, a prompt with a Device Driver Installation Wizard appears on the screen (see [Figure 4](#)). Click the *Next* button to proceed, then click the *Finish* button when the installation is complete.

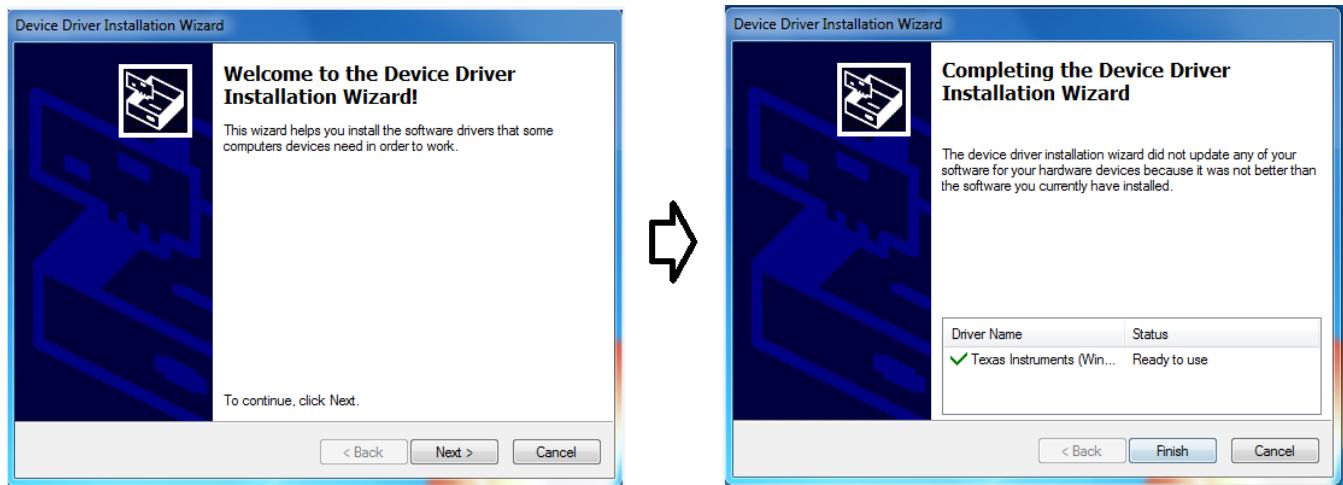


Figure 4. Device Driver Installation Wizard Prompts

NOTE: A notice may appear on the screen stating that Windows cannot verify the publisher of this driver software. Select the *Install this driver software anyway* option.

The device requires the LabVIEW™ Run-Time Engine (see Figure 5) and may prompt for the installation of this software, if not already installed.

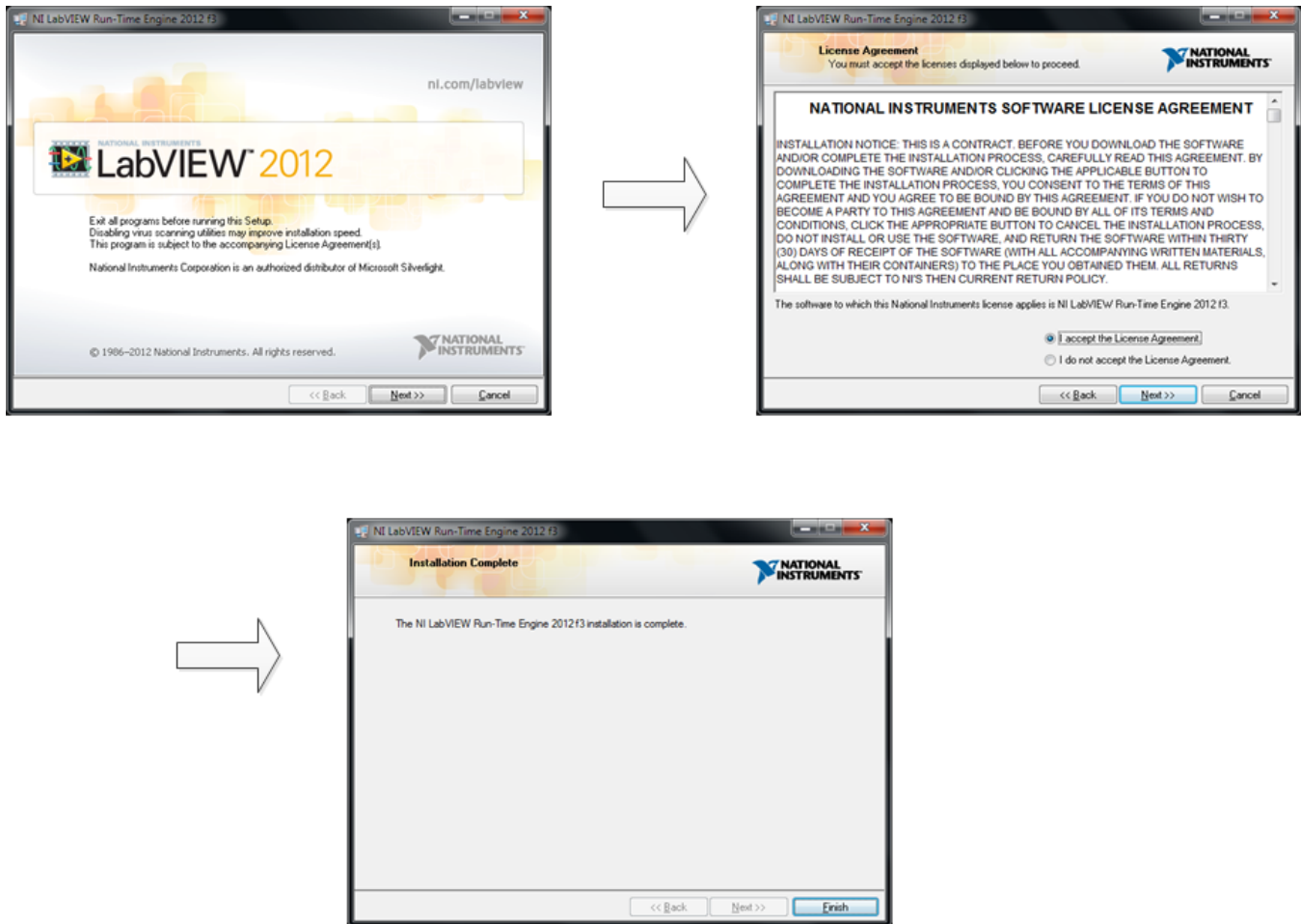


Figure 5. LabVIEW Run-Time Engine Installation

4. After these installations, check the *Create Desktop Shortcut* box, as [Figure 6](#) shows.

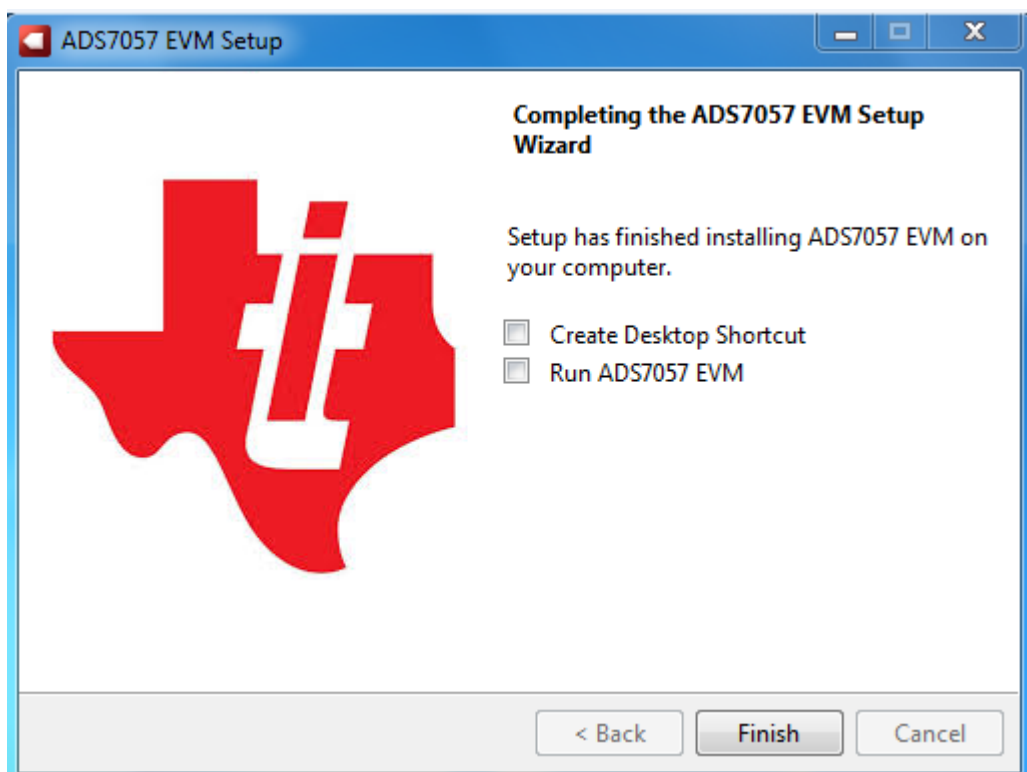


Figure 6. ADS7057EVM-PDK Installation Final Step

6 ADS7057EVM-PDK Operation

The following instructions are a step-by-step guide for connecting the device to a computer and evaluating the performance of the device.

1. Connect the device EVM to the PHI board. Install the two screws as indicated in [Figure 7](#).
2. Use the provided USB cable to connect the PHI to the computer.
 - LED D5 on the PHI lights up, indicating that the PHI is powered up.
 - LEDs D1 and D2 on the PHI start flashing, indicating that the PHI is booted up and communicating with the PC.

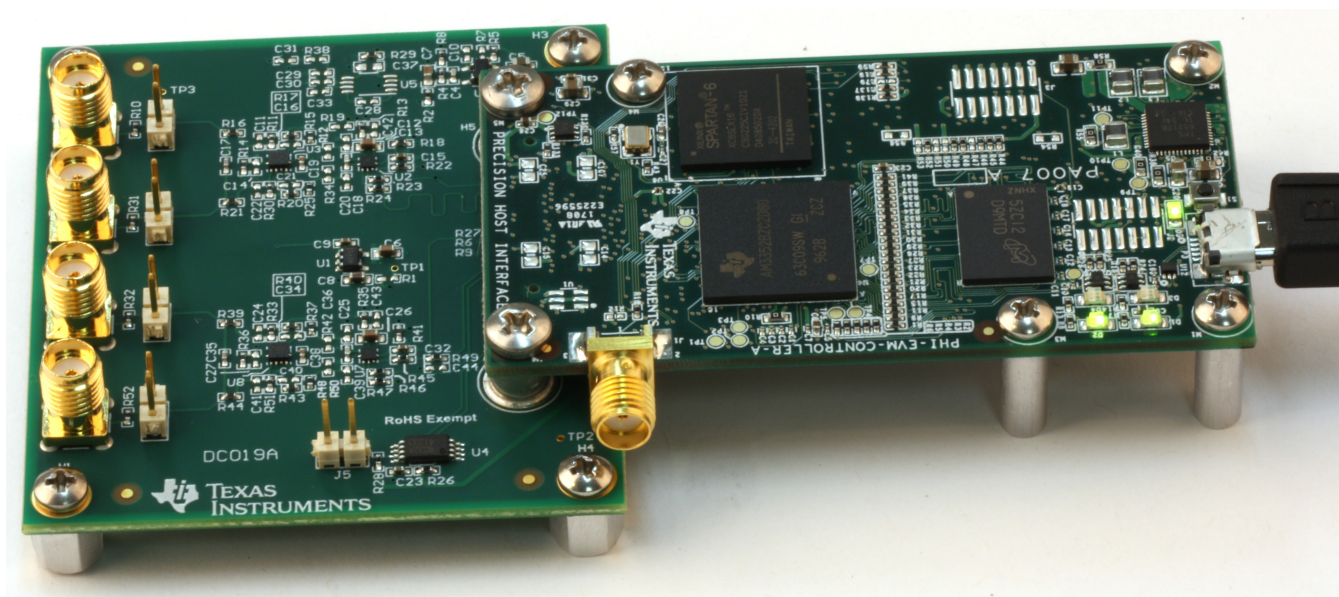


Figure 7. EVM-PDK Hardware Setup and LED Indicators

3. Launch the device EVM GUI software from the installed path, as [Figure 8](#) shows, or using the desktop shortcut created during installation.

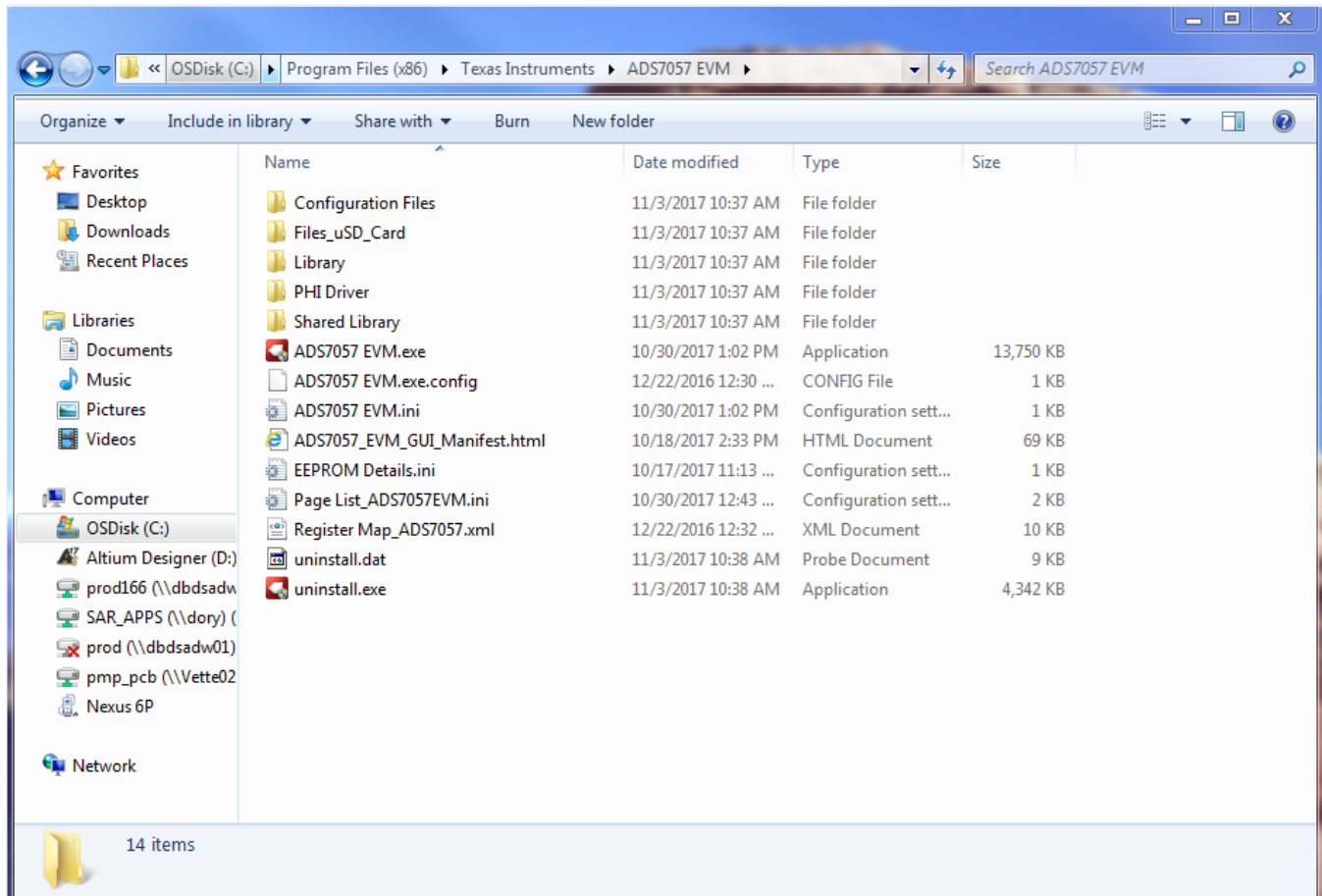


Figure 8. Launch the EVM GUI Software

6.1 EVM GUI Global Settings for ADC Control

Figure 9 shows the input parameters of the GUI (as well as their default values), through which the various functions of the ADS7057EVM-PDK can be exercised. These settings are global and persist across the GUI tools listed in the top left pane (or from one page to another).

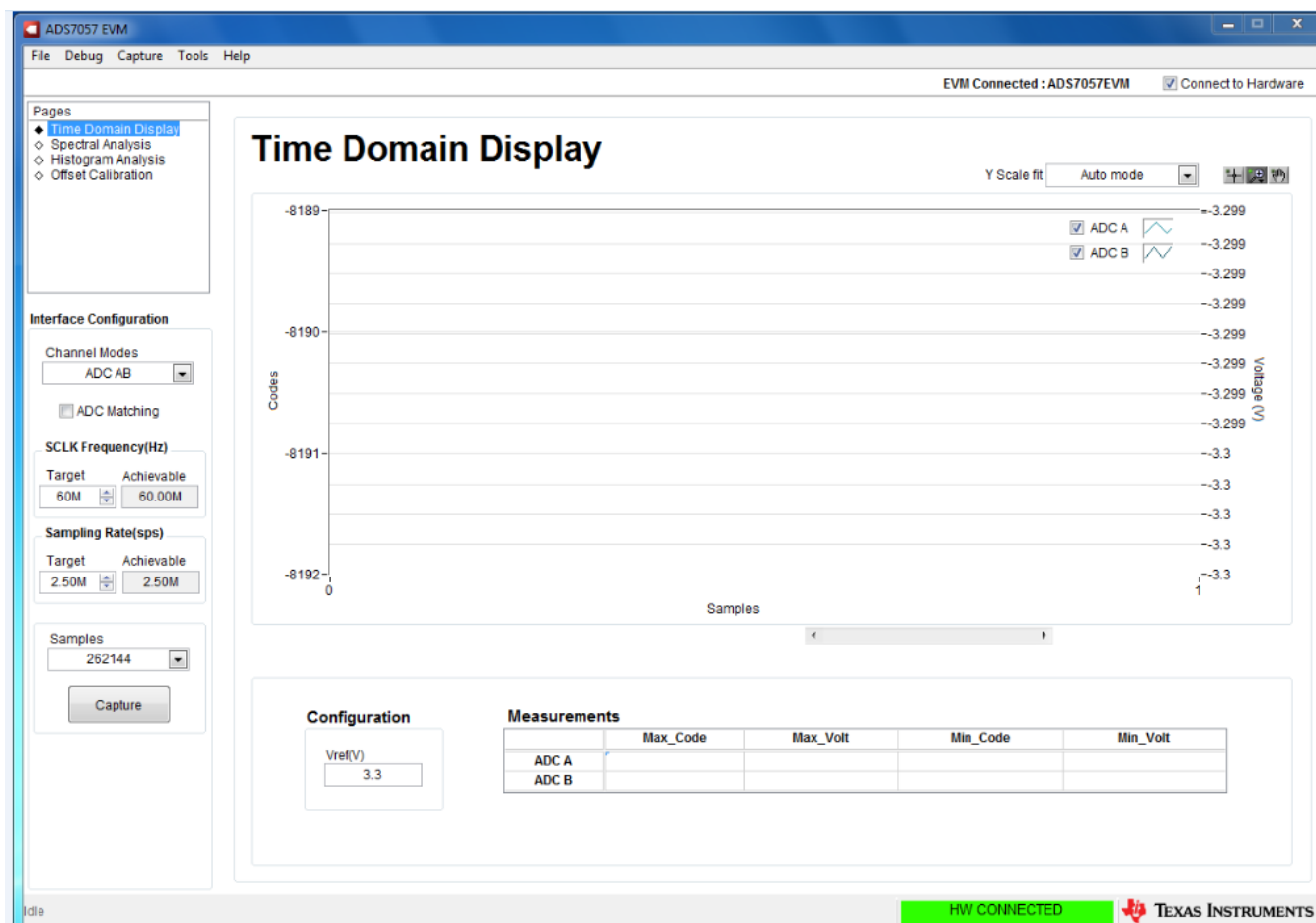


Figure 9. EVM GUI Global Input Parameters

The *SCLK Frequency* and *Sampling Rate* are selected on this page. The GUI lets the user enter the target values for these two parameters, and the GUI computes the closest value that can be achieved, considering the timing constraints of the device.

Select either one of the ADCs or both of the ADCs if they are configured in the simultaneous sampling scheme described in [Section 2.1](#) by clicking on the drop-down menu titled *Channel Modes*. Specify a target SCLK frequency (Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings; however, the achievable frequency may differ from the target value entered. Similarly, the sampling rate of the ADC can be adjusted by modifying the *Target Sampling Rate* argument (Hz). The achievable ADC sampling rate can differ from the target value, depending on the applied SCLK frequency and the closest match achievable is displayed. This page, therefore, allows various settings available on the device to be tested in a repetitive fashion until arriving at the best settings for the corresponding test scenario.

6.2 Time Domain Display Tool

The *Time Domain Display* tool provides a visualization of the ADC response to a given input signal. This tool is useful for both studying the behavior and debugging any gross problems with the ADC or front-end drive circuits.

The user can trigger a capture of the data of the selected number of samples from the ADS7057EVM-PDK, as per the selected interface mode settings using the *Capture* button as indicated in [Figure 10](#). The sample indices are on the x-axis, and two y-axes show the corresponding output codes as well as the equivalent analog voltages based on the specified reference voltage. Switching pages to any of the analysis tools described in the subsequent sections triggers calculations to be performed on the same set of data.

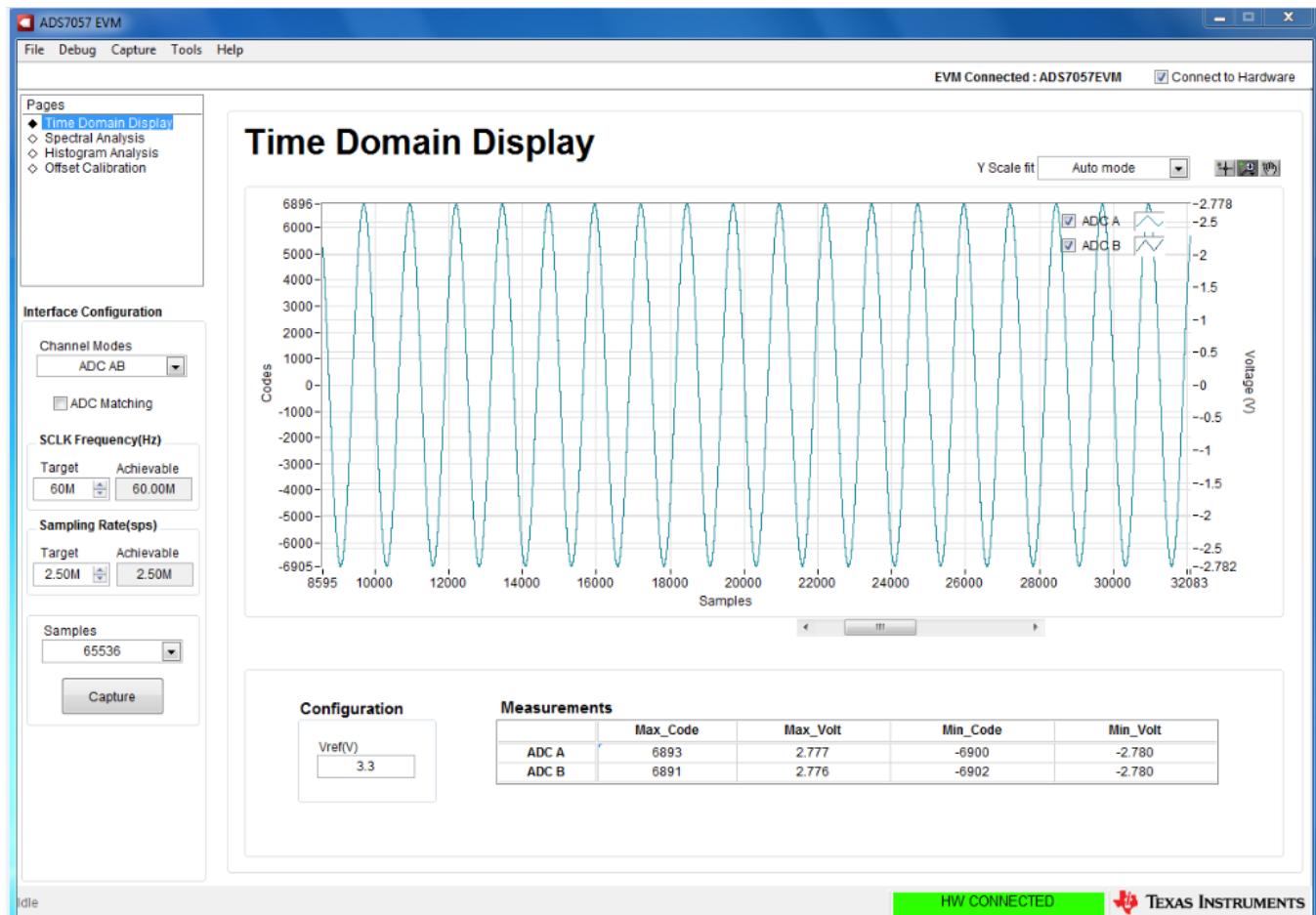


Figure 10. Time Domain Display Tool Options

6.3 Spectral Analysis Tool

The *Spectral Analysis* tool (see [Figure 11](#)) is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of the ADS7057 SAR ADC through the use of a single-tone, sinusoidal signal FFT analysis, using the 7-term Blackman-Harris window setting. Alternatively, the window setting of *None* can be used to search for noise spurs over frequency in DC inputs.

For dynamic performance evaluation, the external, single-ended source must have better specifications than the ADC to ensure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements listed in [Table 6](#).

Table 6. External Source Requirements for Device Evaluation (SNR and THD)

Specification Description	Specification Value
Signal frequency	2 kHz
External source type	Single-ended
External source common-mode	1.65 V
Minimum SNR	90 dB
Minimum THD	-105 dB

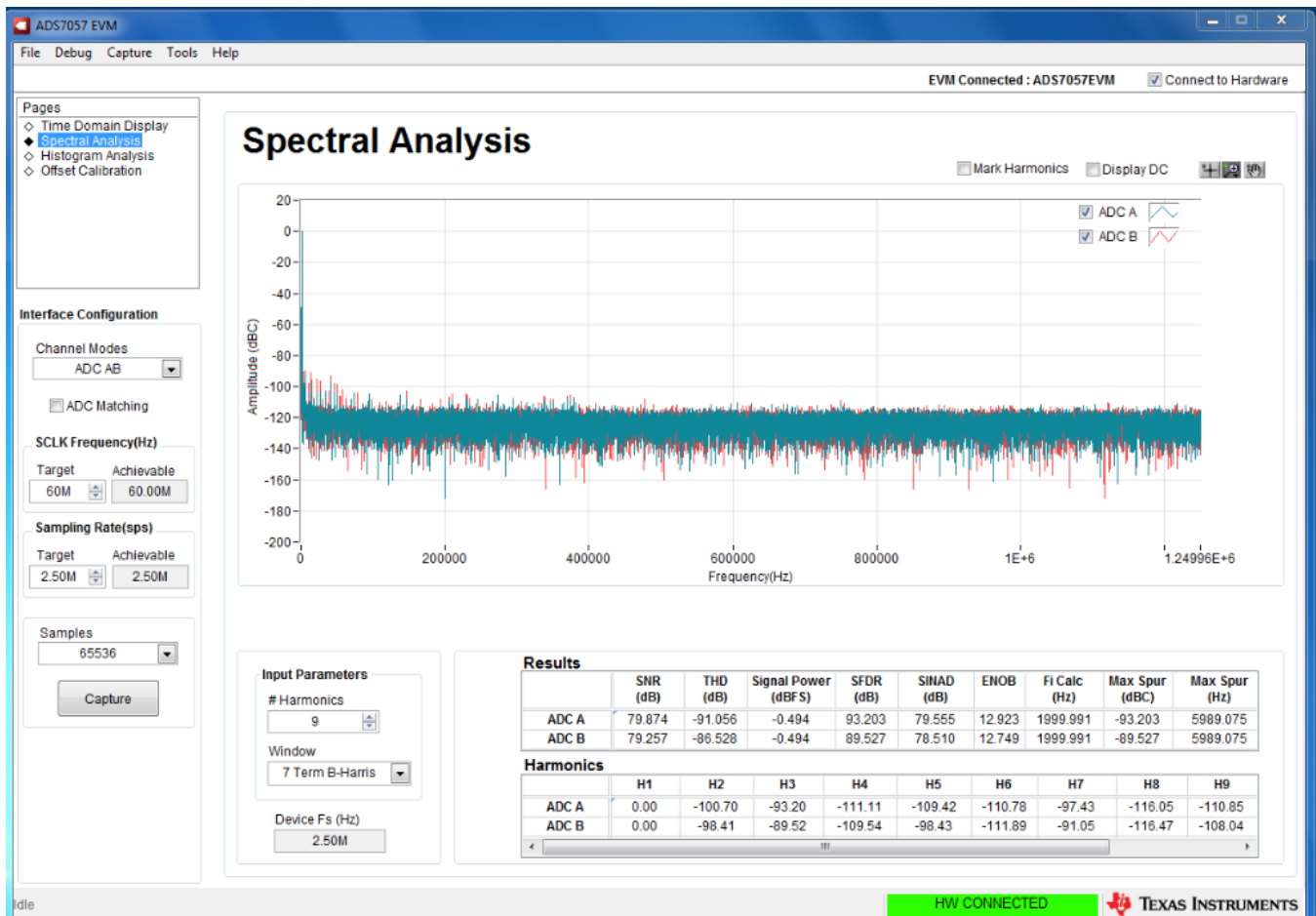


Figure 11. Spectral Analysis Tool

6.4 Histogram Analysis Tool

The *Histogram Analysis* tool can be used to estimate the effective resolution of the ADC due to the performance degradation caused by noise. Effective resolution is an indicator of the number of bits of ADC measurement resolution resulting from performance losses due to noise generated by the various sources connected to the ADC when measuring a DC signal. The cumulative effect of noise coupling to the ADC output (from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself) is reflected in the standard deviation of the ADC output code histogram obtained by performing multiple conversions of a DC input applied to a given channel.

The histogram corresponding to a DC input is displayed by clicking the *Capture* button, as [Figure 12](#) shows.

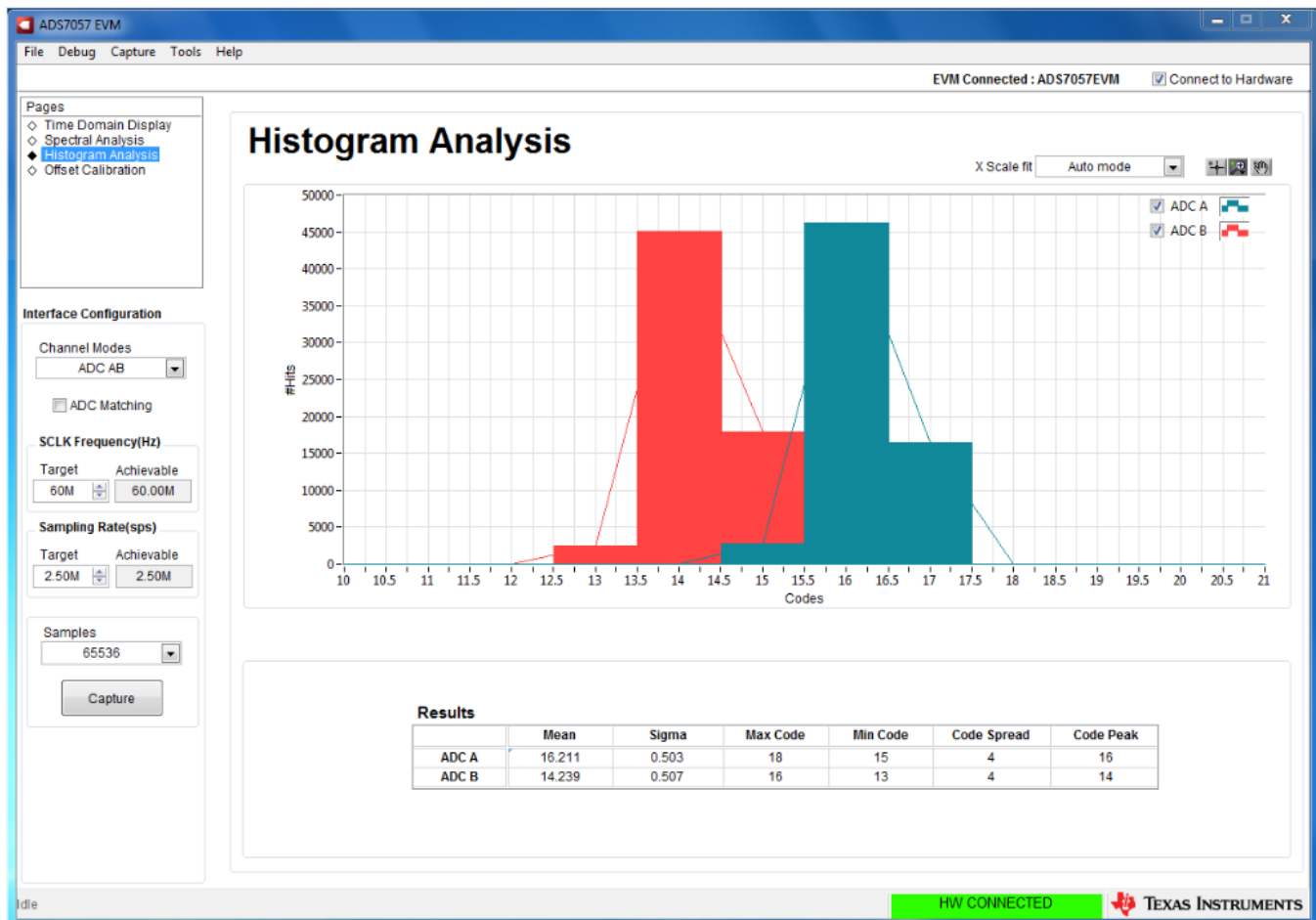


Figure 12. Histogram Analysis Tool

6.5 Offset Calibration

The ADS7057 device can calibrate its own internal offset. The offset calibration can be initiated by the user either on power up or during normal operation. During offset calibration, the analog input pins (AINP and AINM) are disconnected from the sampling stage and connected to an internal reference. The result of the offset calibration is stored in an internal register. For subsequent conversions, the device adjusts the conversion results provided on the SDO output with the value stored in this internal register.

The ADS7057 GUI implements offset calibration, described in the *Offset Calibration During Normal Operation* section of [ADS7056 Ultra-Low Power, Ultra-Small Size, 14-Bit, High-Speed SAR ADC](#). Figure 13 shows the *Offset Calibration* page of the GUI.

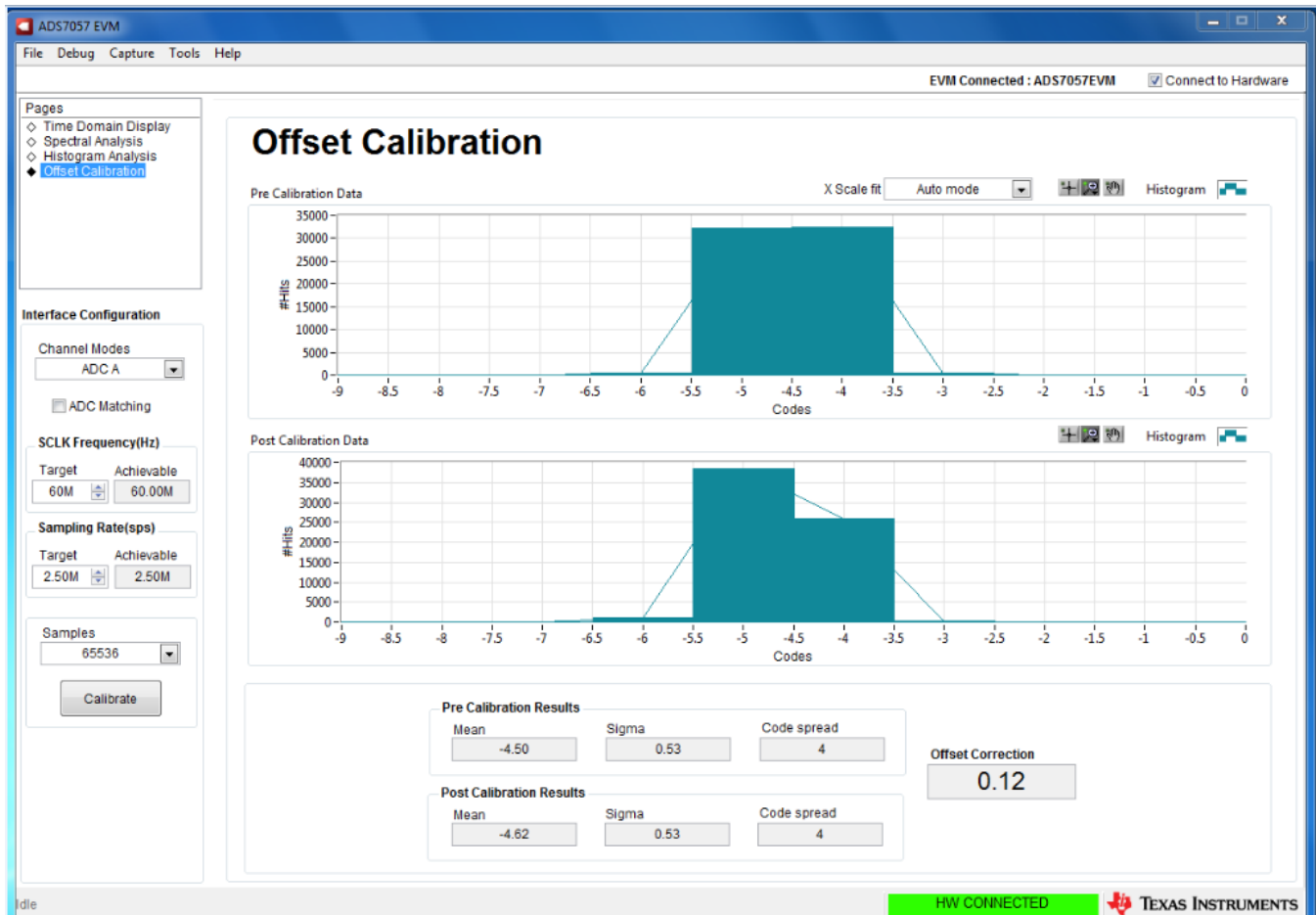


Figure 13. ADS7057 Calibration

The offset calibration test is conducted regardless of the input signal applied to ADC input pin. Users can keep the ADC input floating or apply a fixed DC voltage to the ADC input. Click the *Calibrate* button to initiate the internal self-calibration routine on the ADC. The GUI first performs a histogram test for the device as described in [Section 6.4](#) and populates the top graph. The pre-calibrated *Mean* code is displayed in the *Pre Calibration Results* box. Next, the SPI calibration frame is sent to the ADS7057 device that enables the internal offset calibration logic. The GUI performs the histogram test for a second time and the bottom graph is populated and the *Mean* value is displayed in the *Post Calibration Results* box. Finally, the difference between the first and second mean is displayed in the *Offset Correction* box.

The computed offset for all subsequent attempts to calibrate the device always yields a result within the limits specified in the data sheet. This indicates that after the calibration is performed for the first time, the offset is actually being applied on all subsequent conversions. This computed offset will remain fixed unless the device is reset or there is a significant change in operating temperature or analog supply voltage.

6.6 Performance Evaluation of ADS7054 Using ADS7057 EVM

The ADS7054 is a slower sampling variant of the ADS7057 (1 MSPS vs 2.5 MSPS). Therefore, the ADS7054 performance can be inferred using the ADS7057 EVM GUI by restricting the *Sample Rate(sps)* *Target* value to no greater than 1M. The performance numbers achieved on the *Time Domain Display*, *Spectral Analysis*, and *Histogram Analysis* pages will be representative of the ADS7054 performance parameters under similar operating conditions.

7 Bill of Materials, Printed-Circuit Board Layout, and Schematics

This section contains the ADS7057EVM bill of materials (BOM), printed-circuit board (PCB) layout, and schematics.

7.1 Bill of Materials

Table 7 lists the ADS7057EVM BOM.

Table 7. ADS7057EVM Bill of Materials

Manufacturer Part Number	Quantity	Reference Designators	Manufacturer	Description
DC019	1	PCB	Any	Printed Circuit Board
PA007A	1	PCB2	Any	PHI-EVM-CONTROLLER
1891	4	@H1, @H2, @H3, @H4	Keystone	Hex Standoff, #4-40, Aluminum, 1/4"
RM3X4MM 2701	2	@H5, @H6	APM HEXSEAL	Machine Screw Pan PHILLIPS M3
GRM188R61A106ME69D	4	C1, C2, C3, C5	Murata	CAP, CERM, 10 μ F, 10 V, +/- 20%, X5R, 0603
04025A181FAT2A	1	C4	AVX	CAP, CERM, 180 pF, 50 V, +/- 1%, C0G/NP0, 0402
C1608X7R1A225K080AC	4	C6, C7, C13, C26	TDK	CAP, CERM, 2.2 μ F, 10 V, +/- 10%, X7R, 0603
GRM185C81A105KE36D	1	C8	Murata	CAP, CERM, 1 μ F, 10 V, +/- 10%, X6S, 0603
GRM155R61A105KE15D	3	C9, C15, C32	Murata	CAP, CERM, 1 μ F, 10 V, +/- 10%, X5R, 0402
C1005NP01H102J050BA	2	C17, C35	TDK	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0402
GRM1555C1H681JA01D	2	C18, C36	Murata	CAP, CERM, 680 pF, 50 V, +/- 5%, C0G/NP0, 0402
GRM155R71E104KE14D	2	C19, C38	Murata	CAP, CERM, 0.1 μ F, 25 V, +/- 10%, X7R, 0402
GRM155R61A104KA01D	1	C23	Murata	CAP, CERM, 0.1 μ F, 10 V, +/- 10%, X5R, 0402
PMSSS 440 0025 PH	4	H1, H2, H3, H4	B&F Fastener Supply	MACHINE SCREW PAN PHILLIPS 4-40
9774050360R	2	H5, H6	Würth Elektronik	ROUND STANDOFF M3 STEEL 5MM
5-1814832-1	4	J1, J2, J7, J10	TE Connectivity	SMA Straight PCB Socket Die Cast, 50 Ohm, TH
PEC02SAAN	5	J3, J5, J6, J8, J9	Sullins Connector Solutions	Header, 100mil, 2x1, Tin, TH
QTH-030-01-L-D-A	1	J4	Samtec	Header(Shrouded), 19.7mil, 30x2, Gold, SMT
CRCW04020000Z0ED	11	R2, R5, R6, R9, R13, R14, R27, R29, R35, R36, R49	Vishay-Dale	RES, 0, 5%, 0.063 W, 0402
CPF0402B10RE1	9	R3, R15, R17, R20, R25, R37, R40, R43, R48	TE Connectivity	RES, 10.0, 0.1%, 0.063 W, 0402
CRCW0402100KJNED	1	R4	Vishay-Dale	RES, 100 k, 5%, 0.063 W, 0402
CRCW040231K6FKED	1	R8	Vishay-Dale	RES, 31.6 k, 1%, 0.063 W, 0402
RC0402FR-07100RL	4	R10, R31, R32, R52	Yageo America	RES, 100, 1%, 0.063 W, 0402
CRCW04021K10FKED	4	R11, R30, R33, R51	Vishay-Dale	RES, 1.10 k, 1%, 0.063 W, 0402
ERJ-2RKF1001X	4	R16, R21, R39, R44	Panasonic	RES, 1.00 k, 1%, 0.1 W, 0402
ERJ-2GE0R00X	2	R18, R41	Panasonic	RES, 0, 5%, 0.063 W, 0402
ERJ-2RKF49R9X	6	R22, R23, R24, R45, R46, R47	Panasonic	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0402
CRCW040210K0FKED	2	R26, R28	Vishay-Dale	RES, 10.0 k, 1%, 0.063 W, 0402
REF1933AIDDCR	1	U1	Texas Instruments	Dual Output Vref and Vref/2 Voltage Reference, DDC0005A (SOT-23-T-5)
ADS7057IRUGR	2	U2,U7	Texas Instruments	Ultra-Low Power, Ultra-Small Size, 14-Bit, High-Speed SAR ADC, RUG0008A (X2QFN-8)
THS4551IRUNR	2	U3, U8	Texas Instruments	Low Noise, Precision, 150MHz, Fully Differential Amplifier, RUN0010A (WQFN-10)
BR24G32FVT-3AGE2	1	U4	Rohm	I2C BUS EEPROM (2-Wire), TSSOP-B8
TPS79901DDCR	1	U6	Texas Instruments	Single Output High PSRR LDO, 200 mA, Adjustable 1.2 to 6.5 V Output, 2.7 to 6.5 V Input, with Low IQ, 5-pin SOT (DDC), -40 to 85 degC, Green (RoHS & no Sb/Br)
0402ZC103KAT2A	0	C10	AVX	CAP, CERM, 0.01 μ F, 10 V, +/- 10%, X7R, 0402
C1005NP01H102J050BA	0	C11, C22, C24, C41	TDK	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0402

Table 7. ADS7057EVM Bill of Materials (continued)

Manufacturer Part Number	Quantity	Reference Designators	Manufacturer	Description
GRM1555C1H681JA01D	0	C12, C20, C25, C39	Murata	CAP, CERM, 680 pF, 50 V, +/- 5%, C0G/NP0, 0402
GRM155R71E104KE14D	0	C14, C27, C42, C43	Murata	CAP, CERM, 0.1 uF, 25 V, +/- 10%, X7R, 0402
C1005C0G1H220J050BA	0	C16, C21, C34, C40, C44	TDK	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0402
C1005X5R1A475M050BC	0	C28	TDK	CAP, CERM, 4.7 uF, 10 V, +/- 20%, X5R, 0402
LDK105EBJ226MV-F	0	C29, C33	Taiyo Yuden	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0402
GRM155R61A104KA01D	0	C30	Murata	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402
CL05A106MP5NUNC	0	C31	Samsung Electro-Mechanics	CAP, CERM, 10 uF, 10 V, +/- 20%, X5R, 0402
C1608X7R1A225K080AC	0	C37	TDK	CAP, CERM, 2.2 uF, 10 V, +/- 10%, X7R, 0603
CRCW04020000Z0ED	0	R1, R7, R12, R19, R34, R42, R50	Vishay-Dale	RES, 0, 5%, 0.063 W, 0402
CRCW04024R70JNED	0	R38	Vishay-Dale	RES, 4.7, 5%, 0.063 W, 0402
	0	U5	Texas Instruments	Low Noise Negative Bias Generator, 8-pin Mini SOIC, Pb-Free

7.2 PCB Layout

Figure 14 through Figure 17 show the EVM PCB layout.

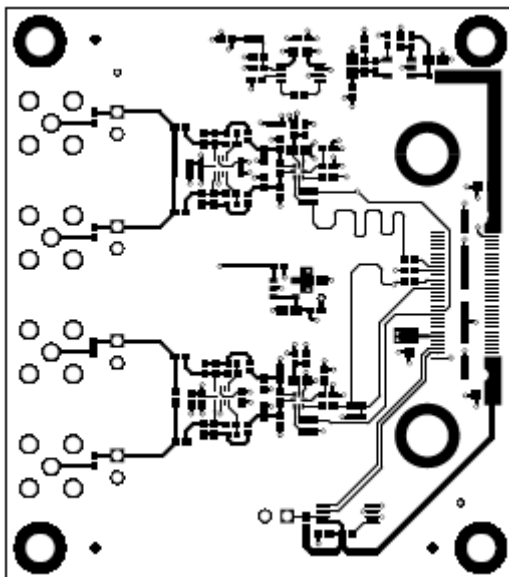


Figure 14. ADS7057EVM PCB Layer 1: Top Layer

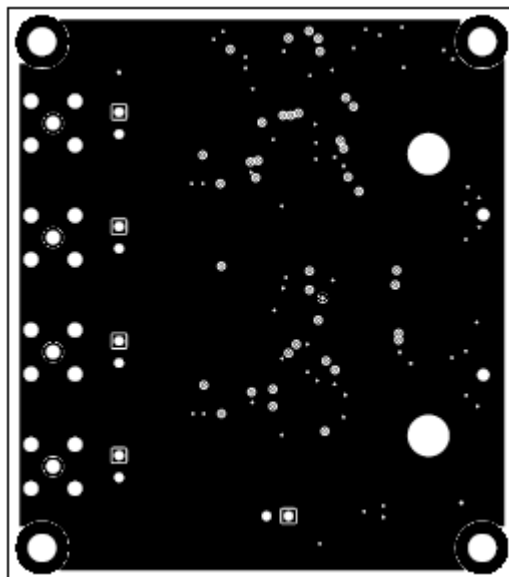


Figure 15. ADS7057EVM PCB Layer 2: GND Plane

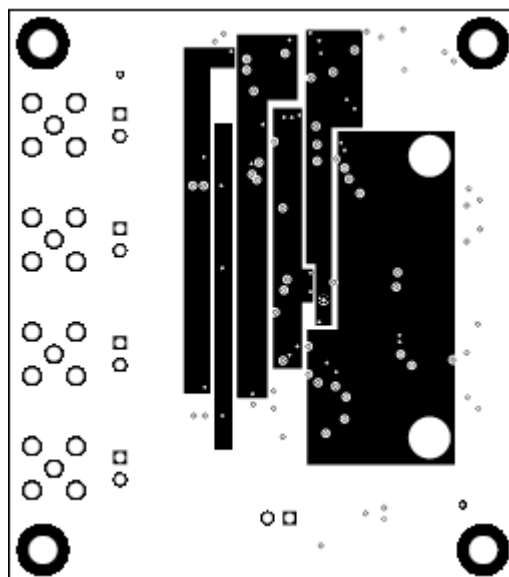


Figure 16. ADS7057EVM PCB Layer 3: Power Planes

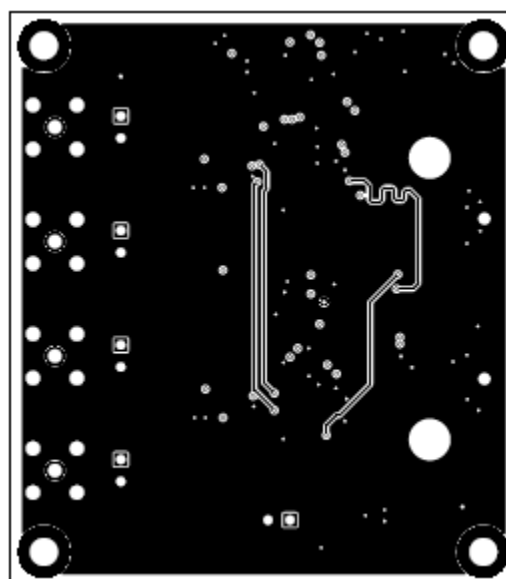
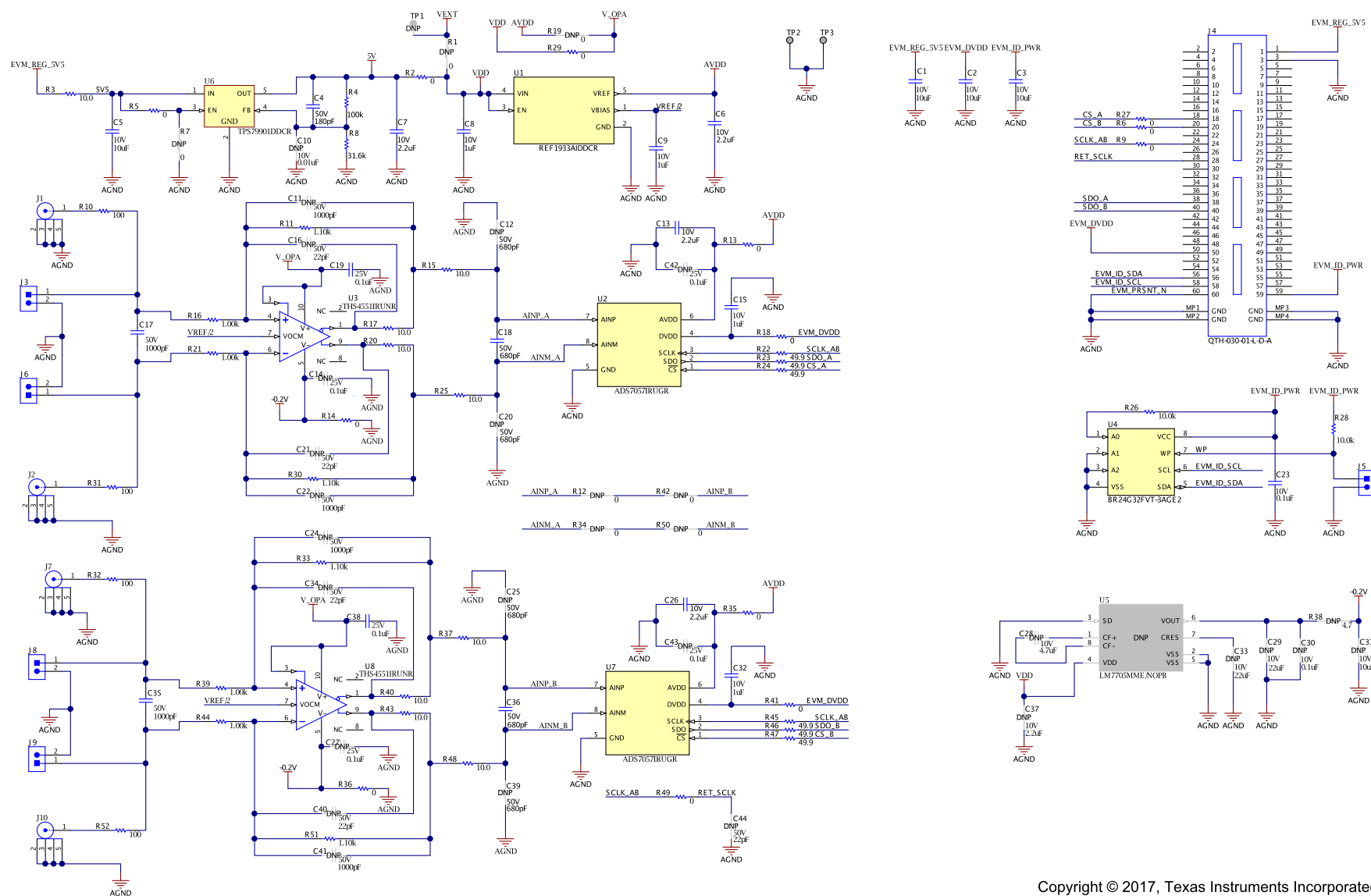


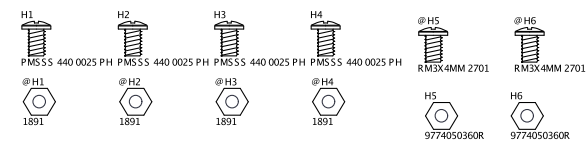
Figure 17. ADS7057EVM PCB Layer 4: Bottom Layer

7.3 Schematics



Copyright © 2017, Texas Instruments Incorporated

Figure 18. Schematic Diagram (Page 1) of the ADS7057EVM PCB



PCB Number: DC019
PCB Rev: A

PCB
LOGO
Texas Instruments

PCB
LOGO
EU RoHS Exempt Logo

PCB
LOGO
FCC disclaimer

PCB: PA007A
PHI-EVM-CONTROLLER

ZZ1
Assembly Note
These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2
Assembly Note
These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3
Assembly Note
These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Copyright © 2017, Texas Instruments Incorporated

Figure 19. Schematic Diagram (Page 2) of the ADS7057EVM PCB

STANDARD TERMS FOR EVALUATION MODULES

1. **Delivery:** TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
 - 1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductor products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM ("Software") shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software
 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. **Limited Warranty and Related Remedies/Disclaimers:**
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.
3. **Regulatory Notices:**
 - 3.1 **United States**
 - 3.1.1 **Notice applicable to EVMs not FCC-Approved:**

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.
 - 3.1.2 **For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:**

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/llds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/llds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿 6 丁目 2 4 番 1 号
西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page
電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。 http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

8.1 *General Limitations.* IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS, REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMNITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2017, Texas Instruments Incorporated