Burr-Brown Products from Texas Instruments



SBAS342B − DECEMBER 2004 − REVISED APRIL 2006

Low Power, 24-Bit, Single Channel Audio Analog-to-Digital Converter

FEATURES

- High Performance Delta-Sigma Analog-to-Digital Converter
- Differential Voltage Inputs
- Dynamic Performance:
  - Dynamic Range (A-Weighted): Up to 112dB
  - THD+N: As low as −105dB
- Three Sampling Modes:
  - Supports Output Sampling Rates Up to 108kHz
  - Choose from Low Power, High Performance, or Double Speed Modes
- Audio Serial Port Interface:
  - Master or Slave Mode Operation
  - 24-Bit Linear PCM Output Data
  - Left-Justified/DSP-Compatible Data Format
- Digital High-Pass Filter for DC Removal:
  - Includes a High-Pass Filter Disable Pin
- Power Supplies:
  - Requires a +5V Analog Power Supply
  - Supports a +1.8V to +3.3V Digital Power Supply Range
- Low Power Dissipation
  - 49mW Typical (Low Power Mode with V_{DD} = +3.3V)
  - 39mW Typical (Low Power Mode with V_{DD} = +1.8V)
- Power Down Mode
  - Less than 50μW total power dissipation
- Available in a small TSSOP-16 Package

APPLICATIONS

- Digital Wireless Microphones
- Battery-Powered Audio Recording and Processing Equipment

DESCRIPTION

The PCM4201 is designed for digital audio applications that require a combination of high dynamic range, low distortion, and low power consumption. The primary applications for the PCM4201 include digital wireless microphones and battery-operated audio recording or processing equipment. The PCM4201 outputs 24-bit linear PCM audio data at sampling rates up to 108kHz. Three sampling modes allow the user to trade off power for performance, dependent upon the intended system requirements. An on-chip voltage reference reduces the number of external components needed for operation.

The PCM4201 includes dedicated control pins for configuration of all programmable functions. The device requires a +5.0V analog power supply, in addition to a digital supply operating from +1.8V to +3.3V. The PCM4201 is available in a small TSSOP-16 package.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		PCM4201	UNIT
Supply voltage	V_{CC}	+6.0	V
	V_{DD}	+3.6	V
Ground voltage differences	AGND to DGND	±0.1	V
Digital input voltage	RATE, S/$\overline{M}$, $\overline{RST}$, HPFD SCKI, BCK, FSYNC	−0.3 to (V_{DD} + 0.3)	V
Analog input voltage	$V_{IN}+$, $V_{IN}-$	−0.3 to (V_{CC} + 0.3)	V
Input current (any pin except supplies)		±10mA	mA
Operating temperature range		−10 to +70	°C
Storage temperature range, T_{STG}		−65 to +150	°C

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

PACKAGE/ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum located at the end of this datasheet, or see the TI website at www.ti.com.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, all characteristics are measured with T_A = +25°C, V_{CC} = +5V, and V_{DD} = +3.3V. System clock frequency is set to 24.576 MHz. Device is operated in Slave mode.

PARAMETER		CONDITIONS	PCM4201 MIN	PCM4201 TYP	PCM4201 MAX	UNITS
RESOLUTION				24		Bits
AUDIO DATA FORMAT						
Format		Two's complement, MSB first data		Left-Justified / DSP Compatible		
Word length				24		Bits
DIGITAL I/O						
Input logic level	V_{IH}		0.7 x V_{DD}		V_{DD}	V
	V_{IL}		0		0.3 x V_{DD}	V
Output logic level	V_{OH}	I_{OH} = −2mA	0.8 x V_{DD}			V
	V_{OL}	I_{OL} = +2mA			0.2 x V_{DD}	V
Input current	I_{IH}	V_{IN} = V_{DD}			+10	µA
	I_{IL}	V_{IN} = 0V			−10	µA
Input current(1)	I_{IH}	V_{IN} = V_{DD}			+25	µA
	I_{IL}	V_{IN} = 0V			−25	µA
DIGITAL SWITCHING						
Output sampling frequency	f_S	Normal speed, low power	8		54	kHz
		Normal speed, high performance	8		54	kHz
		Double speed	54		108	kHz
System clock duty cycle			45	50	55	%
System clock frequency			2.048		27.65	MHz
AUDIO SERIAL-PORT TIMING						
Delay from FSYNC rising to BCK rising	t_{DBK}		5			ns
Delay from BCK rising to FSYNC rising	t_{DLK}		5			ns
BCK high pulse width	t_{BCKH}		72			ns
BCK low pulse width	t_{BCKL}		72			ns
Data setup time	t_S		10			ns
Data hold time	t_H		10			ns
ANALOG INPUTS						
Input voltage, full-scale range (FSR)		Differential input		5.0		V_{PP}
Input impedance		Per analog input pin		15		kΩ
Common-mode rejection				100		dB
DC PERFORMANCE						
Output offset error		High-pass filter disabled		±4		% of FSR
Gain error				±4		% of FSR

(1) Applies to RATE (pin 5) and S/$\overline{M}$ (pin 6) inputs.

(2) All typical dynamic performance specifications were measured using an Audio Precision System Two Cascade or Cascade Plus test system and a PCM4201EVM evaluation module. For Normal Speed operation, the measurement bandwidth is limited using the Audio Precision 22Hz high-pass filter and 20kHz low-pass filter. For Double Speed mode, the measurement bandwidth is limited using the Audio Precision 22Hz high-pass filter and a user-defined 40kHz low-pass filter (the f_S/2 low pass filter may be utilized with similar results). All A-weighted measurements are made using the Audio Precision A-weighting filter in combination with the filters previously noted here. Minimum and maximum dynamic performance limits are based upon the capability of the production test solution.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all characteristics are measured with T_A = +25°C, V_{CC} = +5V, and V_{DD} = +3.3V. System clock frequency is set to 24.576 MHz. Device is operated in Slave mode.

PARAMETER	CONDITIONS	PCM4201 MIN	PCM4201 TYP	PCM4201 MAX	UNITS
DYNAMIC PERFORMANCE(2) with V_{CC} = +5V and V_{DD} = +1.8V					
Normal Speed, Low Power, f_S = 48kHz, BW = 22Hz to 20kHz					
Total harmonic distortion + noise THD+N	V_{IN} = −0.5dB, f_{IN} = 1kHz		−103	−100	dB
Dynamic range	V_{IN} = −60dB, f_{IN} = 1kHz, A-weighted	104	109		dB
Dynamic range, no weighting	V_{IN} = −60dB, f_{IN} = 1kHz		106		dB
Normal Speed, High Performance, f_S = 48kHz, BW = 22Hz to 20kHz					
Total harmonic distortion + noise THD+N	V_{IN} = −0.5dB, f_{IN} = 1kHz		−105	−100	dB
Dynamic range	V_{IN} = −60dB, f_{IN} = 1kHz, A-weighted	105	112		dB
Dynamic range, no weighting	V_{IN} = −60dB, f_{IN} = 1kHz		110		dB
Double Speed, f_S = 96kHz, BW = 22Hz to 40kHz					
Total harmonic distortion + noise THD+N	V_{IN} = −0.5dB, f_{IN} = 1kHz		−103	−100	dB
Dynamic range	V_{IN} = −60dB, f_{IN} = 1kHz, A-weighted	105	112		dB
Dynamic range, no weighting	V_{IN} = −60dB, f_{IN} = 1kHz		106		dB
DYNAMIC PERFORMANCE(2) with V_{CC} = +5V and V_{DD} = +3.3V					
Normal Speed, Low Power, f_S = 48kHz, BW = 22Hz to 20kHz					
Total harmonic distortion + noise THD+N	V_{IN} = −0.5dB, f_{IN} = 1kHz		−102	−100	dB
Dynamic range	V_{IN} = −60dB, f_{IN} = 1kHz, A-weighted	104	106		dB
Dynamic range, no weighting	V_{IN} = −60dB, f_{IN} = 1kHz		104		dB
Normal Speed, High Performance, f_S = 48kHz, BW = 22Hz to 20kHz					
Total harmonic distortion + noise THD+N	V_{IN} = −0.5dB, f_{IN} = 1kHz		−105	−100	dB
Dynamic range	V_{IN} = −60dB, f_{IN} = 1kHz, A-weighted	105	112		dB
Dynamic range, no weighting	V_{IN} = −60dB, f_{IN} = 1kHz		109		dB
Double Speed, f_S = 96kHz, BW = 22Hz to 40kHz					
Total harmonic distortion + noise THD+N	V_{IN} = −0.5dB, f_{IN} = 1kHz		−103	−100	dB
Dynamic range	V_{IN} = −60dB, f_{IN} = 1kHz, A-weighted	105	111		dB
Dynamic range, no weighting	V_{IN} = −60dB, f_{IN} = 1kHz		106		dB
DIGITAL DECIMATION FILTER					
Passband edge				$0.453f_S$	Hz
Passband ripple				±0.005	dB
Stop band edge		$0.547f_S$			Hz
Stop band attenuation		−100			dB
Group delay			$37/f_S$		sec

(1) Applies to RATE (pin 5) and S/$\overline{M}$ (pin 6) inputs.

(2) All typical dynamic performance specifications were measured using an Audio Precision System Two Cascade or Cascade Plus test system and a PCM4201EVM evaluation module. For Normal Speed operation, the measurement bandwidth is limited using the Audio Precision 22Hz high-pass filter and 20kHz low-pass filter. For Double Speed mode, the measurement bandwidth is limited using the Audio Precision 22Hz high-pass filter and a user-defined 40kHz low-pass filter (the $f_S/2$ low pass filter may be utilized with similar results). All A-weighted measurements are made using the Audio Precision A-weighting filter in combination with the filters previously noted here. Minimum and maximum dynamic performance limits are based upon the capability of the production test solution.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise specified, all characteristics are measured with T_A = +25°C, V_{CC} = +5V, and V_{DD} = +3.3V. System clock frequency is set to 24.576 MHz. Device is operated in Slave mode.

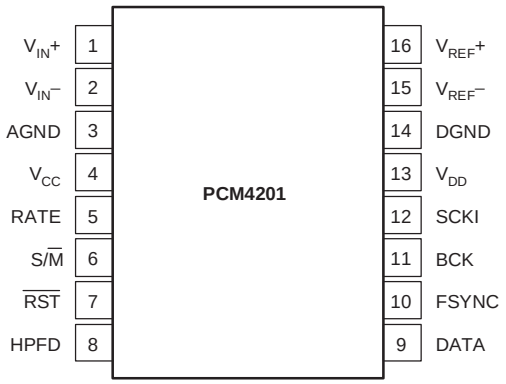
PARAMETER		CONDITIONS	PCM4201 MIN	PCM4201 TYP	PCM4201 MAX	UNITS
DIGITAL HIGH PASS FILTER						
Frequency response (−3dB)				f_S/48000		Hz
POWER SUPPLY						
Supply voltage range	V_{CC}		+4.75	+5.0	+5.25	V
	V_{DD}		+1.65	+3.3	+3.6	V
Operating supply current with V_{CC} = +5V, V_{DD} = +1.8V	I_{CC}	Normal speed, low power		7	8.2	mA
		Normal speed, high performance		13	15	mA
		Double speed		13	16	mA
	I_{DD}	Normal speed, low power		2	3.2	mA
		Normal speed, high performance		2.5	4.5	mA
		Double speed		3.5	6.0	mA
Operating supply current with V_{CC} = +5V, V_{DD} = +3.3V	I_{CC}	Normal speed, low power		7	8.2	mA
		Normal speed, high performance		13	15	mA
		Double speed		13	16	mA
	I_{DD}	Normal speed, low power		4	6.0	mA
		Normal speed, high performance		5	8.5	mA
		Double speed		7.5	10.5	mA
Power-Down mode current with V_{CC} = +5V, V_{DD} = +1.8V or +3.3V	I_{CC}				5	µA
	I_{DD}				5	µA
Total power dissipation with V_{CC} = +5V, V_{DD} = +3.3V		Normal speed, low power		49	61	mW
		Normal speed, high performance		82	103	mW
		Double speed		90	115	mW
Total power dissipation with V_{CC} = +5V, V_{DD} = +1.8V		Normal speed, low power		39	47	mW
		Normal speed, high performance		70	83	mW
		Double speed		72	91	mW

(1) Applies to RATE (pin 5) and S/$\overline{M}$ (pin 6) inputs.

(2) All typical dynamic performance specifications were measured using an Audio Precision System Two Cascade or Cascade Plus test system and a PCM4201EVM evaluation module. For Normal Speed operation, the measurement bandwidth is limited using the Audio Precision 22Hz high-pass filter and 20kHz low-pass filter. For Double Speed mode, the measurement bandwidth is limited using the Audio Precision 22Hz high-pass filter and a user-defined 40kHz low-pass filter (the f_S/2 low pass filter may be utilized with similar results). All A-weighted measurements are made using the Audio Precision A-weighting filter in combination with the filters previously noted here. Minimum and maximum dynamic performance limits are based upon the capability of the production test solution.

PIN ASSIGNMENT

PW PACKAGE
TSSOP-16
(TOP VIEW)



Terminal Functions

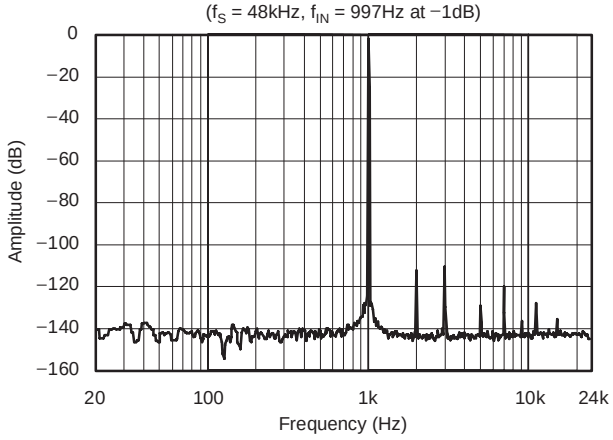
TERMINAL		I/O	DESCRIPTION
PIN NO.	NAME		
1	$V_{IN}+$	Input	Noninverting Analog Input
2	$V_{IN}-$	Input	Inverting Analog Input
3	AGND	Ground	Analog Ground
4	V_{CC}	Power	Analog Supply, +5V
5	RATE	Input	Sampling Mode Configuration (Tri-Level Input): 0 = Double Speed; 1 = Normal Speed, Low Power; Z = Normal Speed, High Performance. Maximum external capacitive load is 100pF.
6	S/$\overline{M}$	Input	Audio Serial Port Slave/Master Mode (0 = Master, 1 = Slave)
7	$\overline{RST}$	Input	Reset/Power Down (Active Low)
8	HPFD	Input	High Pass Filter Disable (Active High)
9	DATA	Output	Audio Serial Port Data
10	FSYNC	I/O	Audio Serial Port Frame Synchronization Clock
11	BCK	I/O	Audio Serial Port Bit (or Data) Clock
12	SCKI	Input	System Clock
13	V_{DD}	Power	Digital Supply, +3.3V Typical(1)
14	DGND	Ground	Digital Ground
15	$V_{REF}-$	Output	Voltage Reference Low Output, Connect to AGND
16	$V_{REF}+$	Output	Voltage Reference High Output, De-Coupling Only(2)

(1) The V_{DD} supply may be operated from +1.8V to +3.6V.
(2) Unbuffered output. Do not use to drive external circuitry.

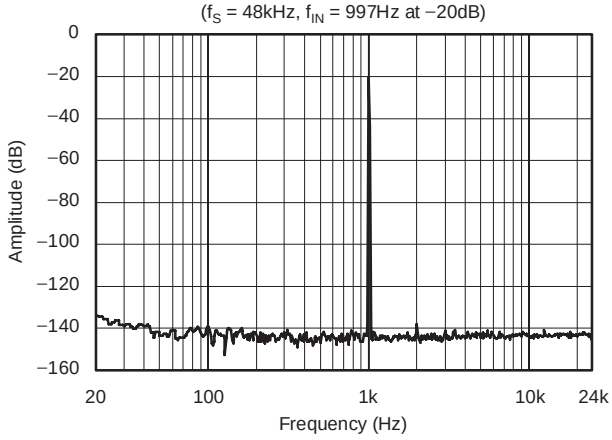
TYPICAL CHARACTERISTICS

At T_A = 25°C, V_{DD} = 1.8V, V_{CC} = 5.0V, Master Mode, SCKI = 24.576MHz, unless otherwise noted.

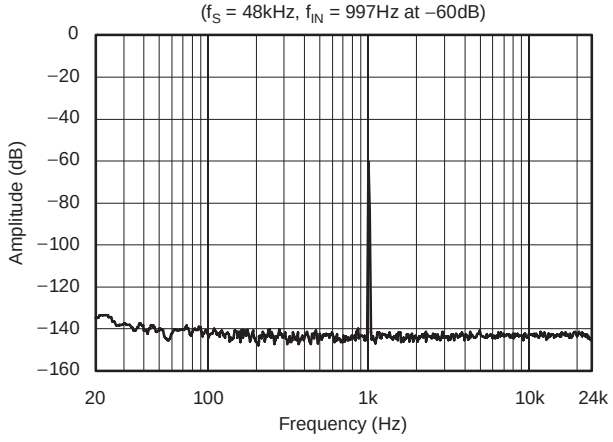
HIGH−PERFORMANCE FFT PLOT
(f_S = 48kHz, f_{IN} = 997Hz at −1dB)



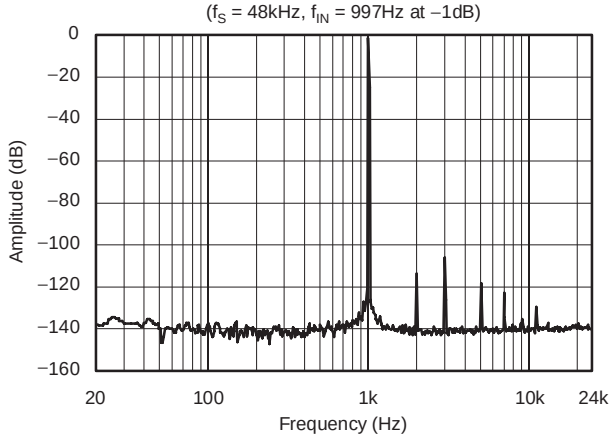
HIGH−PERFORMANCE FFT PLOT
(f_S = 48kHz, f_{IN} = 997Hz at −20dB)



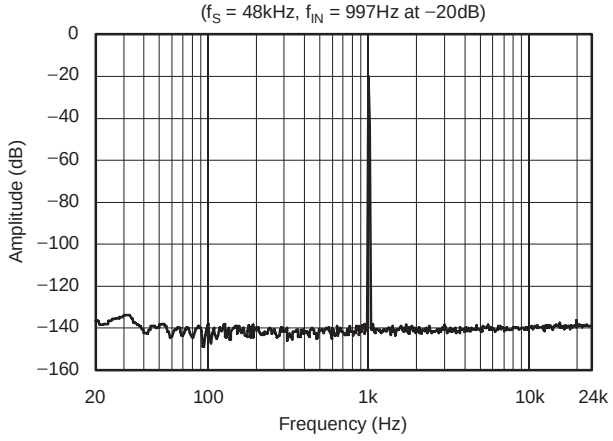
HIGH−PERFORMANCE FFT PLOT
(f_S = 48kHz, f_{IN} = 997Hz at −60dB)



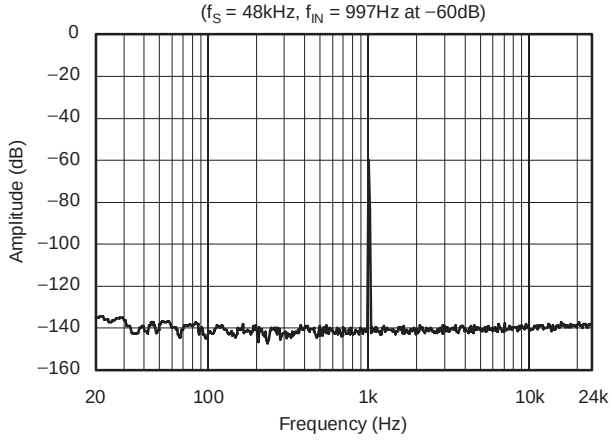
LOW−POWER FFT PLOT
(f_S = 48kHz, f_{IN} = 997Hz at −1dB)



LOW−POWER FFT PLOT
(f_S = 48kHz, f_{IN} = 997Hz at −20dB)



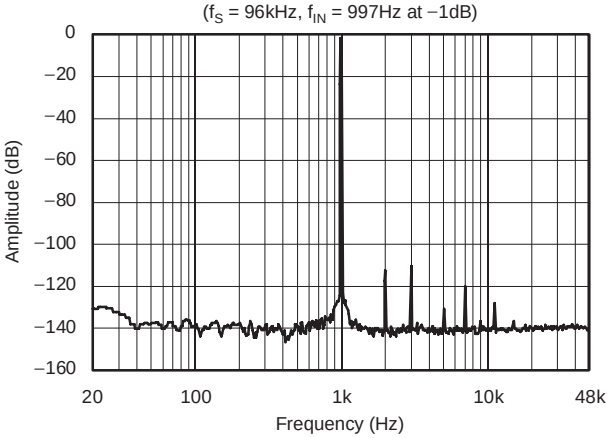
LOW−POWER FFT PLOT
(f_S = 48kHz, f_{IN} = 997Hz at −60dB)



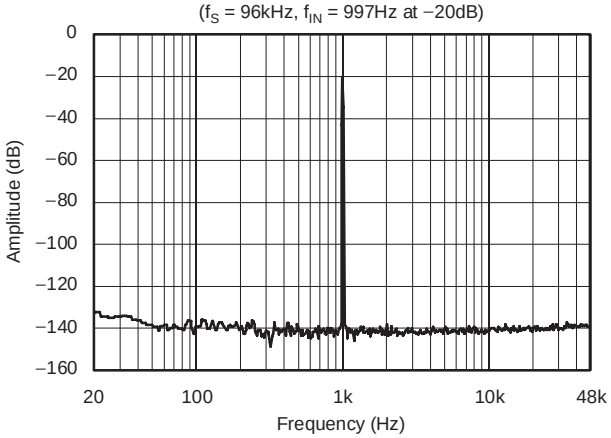
TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, V_{DD} = 1.8V, V_{CC} = 5.0V, Master Mode, SCKI = 24.576MHz, unless otherwise noted.

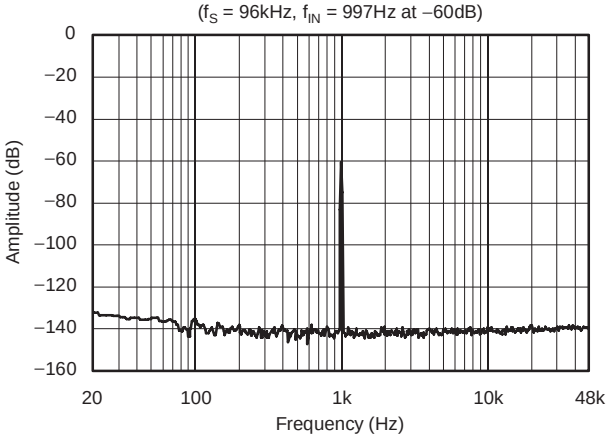
DOUBLE−SPEED FFT PLOT
(f_S = 96kHz, f_{IN} = 997Hz at −1dB)



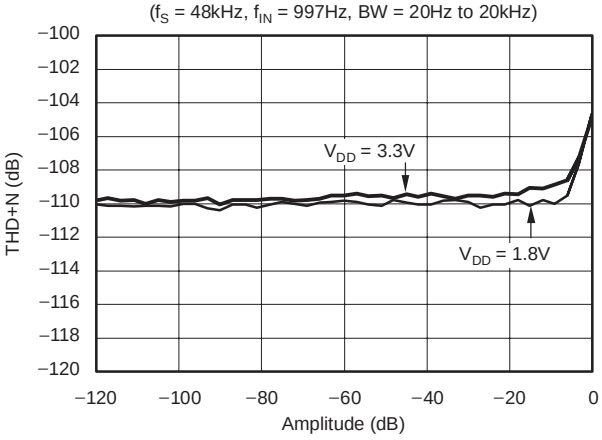
DOUBLE−SPEED FFT PLOT
(f_S = 96kHz, f_{IN} = 997Hz at −20dB)



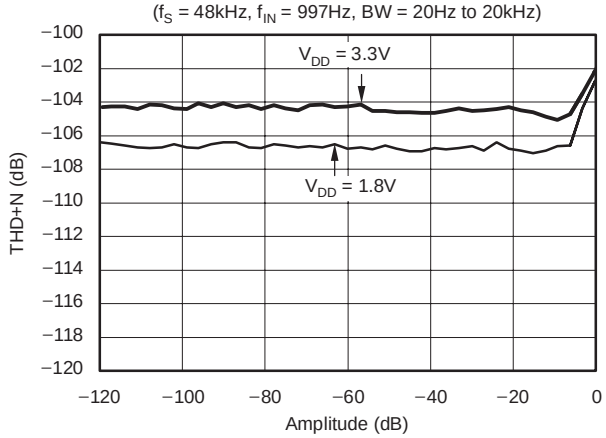
DOUBLE−SPEED FFT PLOT
(f_S = 96kHz, f_{IN} = 997Hz at −60dB)



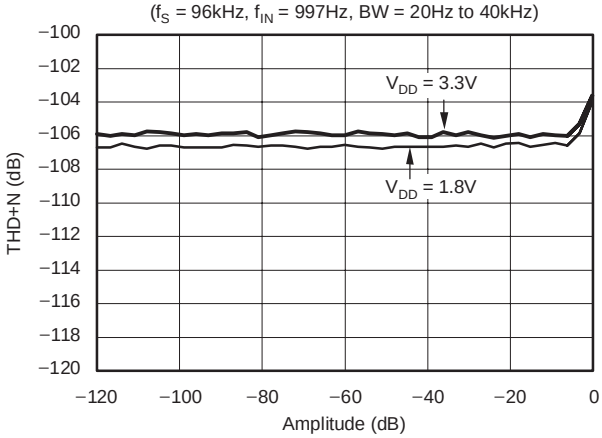
THD+N vs AMPLITUDE, HIGH PERFORMANCE
(f_S = 48kHz, f_{IN} = 997Hz, BW = 20Hz to 20kHz)



THD+N vs AMPLITUDE, LOW POWER
(f_S = 48kHz, f_{IN} = 997Hz, BW = 20Hz to 20kHz)



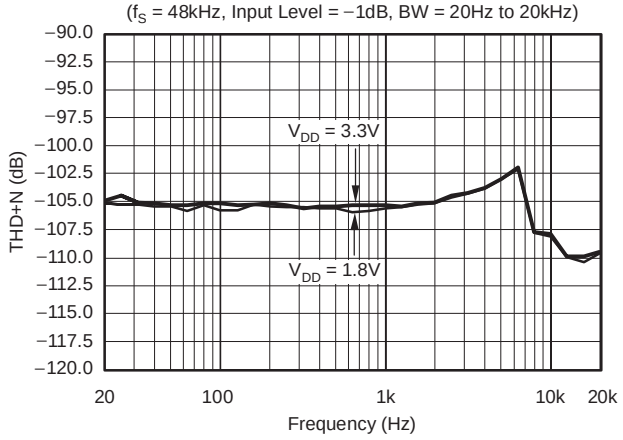
THD+N vs AMPLITUDE, DOUBLE SPEED
(f_S = 96kHz, f_{IN} = 997Hz, BW = 20Hz to 40kHz)



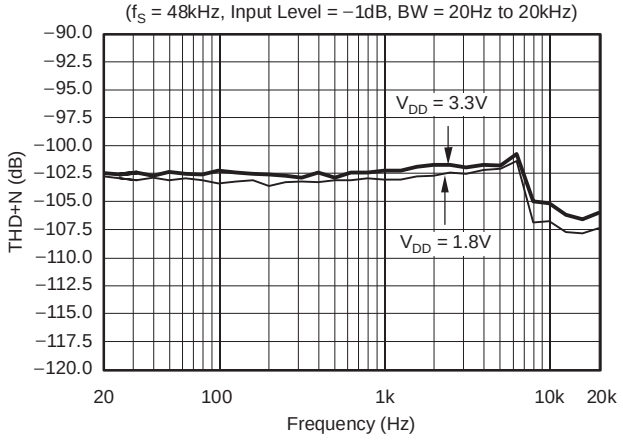
TYPICAL CHARACTERISTICS (continued)

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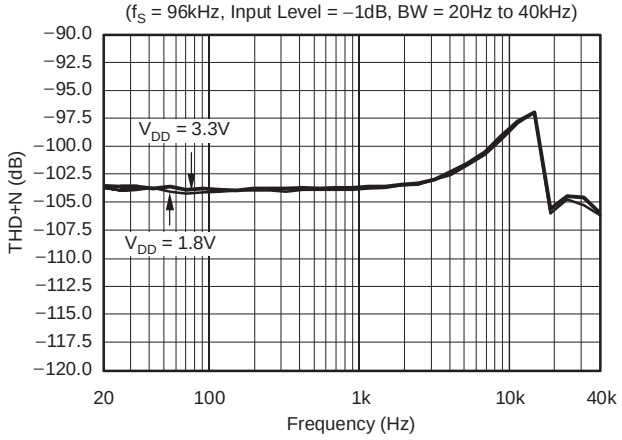
THD+N vs FREQUENCY, HIGH PERFORMANCE
(f_S = 48kHz, Input Level = −1dB, BW = 20Hz to 20kHz)



THD+N vs FREQUENCY, LOW POWER
(f_S = 48kHz, Input Level = −1dB, BW = 20Hz to 20kHz)



THD+N vs FREQUENCY, DOUBLE SPEED
(f_S = 96kHz, Input Level = −1dB, BW = 20Hz to 40kHz)



PRODUCT OVERVIEW

The PCM4202 is a single channel audio analog-to-digital converter (ADC) designed for use in low power, battery-operated or portable professional audio equipment. Target applications include digital wireless microphones and portable digital audio recorders/processors. The PCM4201 features 24-bit linear PCM output data, with a format compatible with digital signal processors, digital audio interface transmitters, and programmable logic devices.

The PCM4201 includes three sampling modes, supporting sampling rates up to 108kHz. The Normal Speed, Low Power mode supports sampling rates up to 54kHz, and employs 64x oversampling to reduce overall converter power. The Normal Speed, High Performance mode supports sampling rates up to 54kHz with 128x oversampling, resulting in improved dynamic range and THD+N when compared to the Low Power mode, at the expense of increased power dissipation. The Double Speed mode supports sampling frequencies up to 108kHz and is provided for those applications where higher sampling rates may be required.

A digital high-pass filter is included for DC removal. Dedicated control pins are included for sampling mode selection, Slave/Master mode audio serial port operation, digital high-pass filter enable/disable, and reset/power-down functions.

A +5V power supply is required for the analog section of the device, while a +3.3V power supply is typically utilized for the digital section. The digital supply may be operated at voltages as low as +1.8V, with a corresponding 10 to 20 milliwatt (mW) reduction in power dissipation, depending upon the sampling mode selection. Figure 1 shows the functional block diagram for the PCM4201.

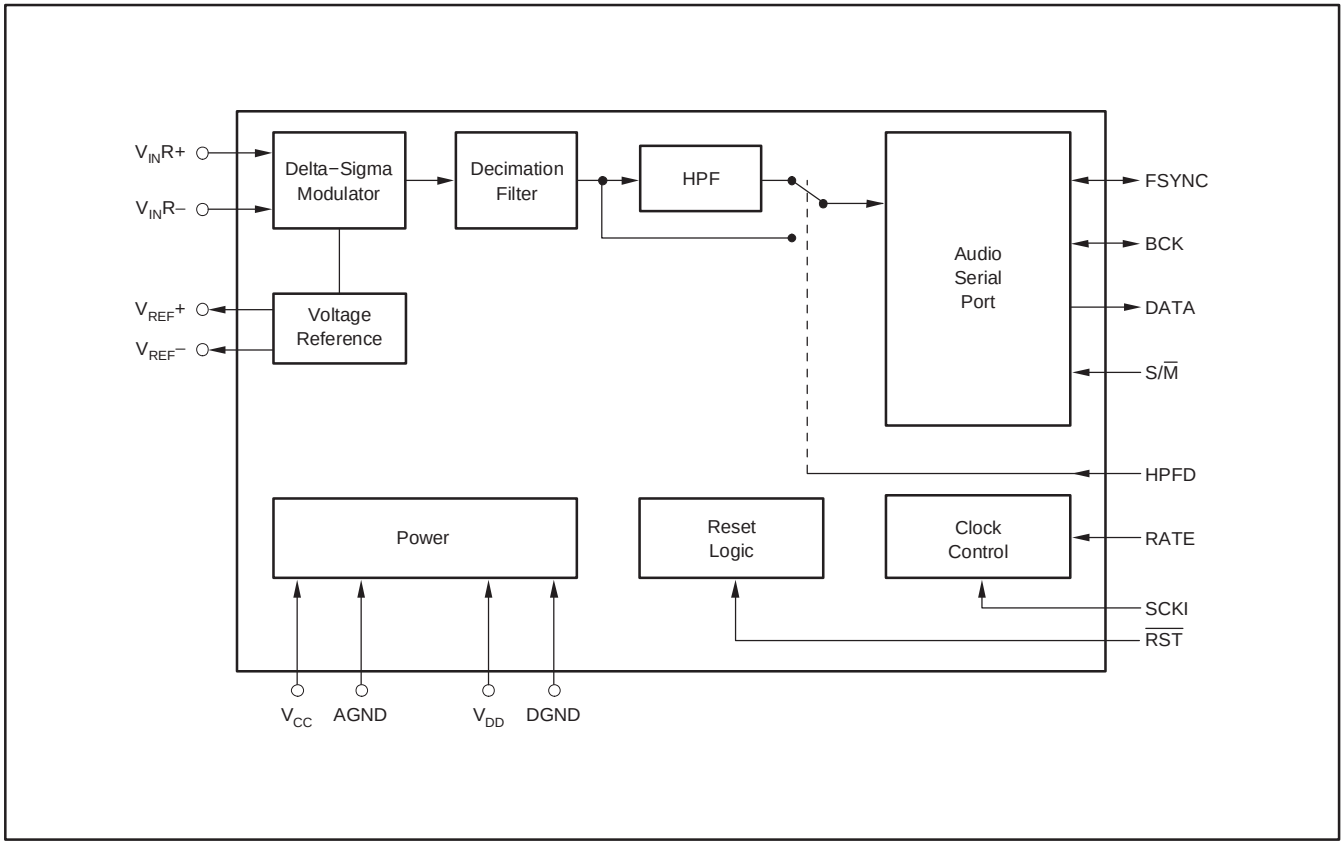


Figure 1. PCM4201 Functional Block Diagram

ANALOG INPUTS

The PCM4201 features differential voltage inputs. V_{IN}+ (pin 1) and V_{IN}− (pin 2) provide the noninverting and inverting inputs, respectively. The full-scale input voltage, measured differentially across these two pins, is approximately $5.0V_{PP}$. The input impedance is approximately 15kΩ per input pin.

In applications where the analog inputs can be driven beyond the analog supply rails of the PCM4201, the input buffer circuit should incorporate clamping or limiting circuitry to ensure that the analog inputs are not driven beyond the absolute maximum input levels for these pins. Refer to the ***Absolute Maximum Ratings*** table of this datasheet.

VOLTAGE REFERENCE

The PCM4201 includes an on-chip band gap reference for the delta-sigma modulator, eliminating the need for external reference circuitry. The reference voltage is set to +2.5V nominal. The V_{REF}+ (pin 16) and V_{REF}− (pin 15) outputs provide connections for reference decoupling capacitors, which are connected between these two pins. The V_{REF}− output is then connected to analog ground. Figure 2 shows the recommended decoupling capacitor connections and values.

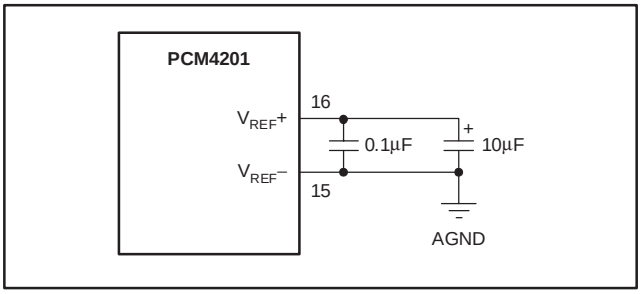


Figure 2. Voltage Reference Connections

The voltage reference output is not buffered, and should not be connected to external circuitry other than the decoupling capacitors. DC common-mode voltage for the input buffer circuitry may be set using an external voltage divider circuit, as shown in the ***Applications Information*** section of this datasheet.

SYSTEM CLOCK

The PCM4201 requires an external system clock, which is used internally to derive the modulator oversampling and digital subsystem clocks. The system clock is input at SCKI (pin 12). The acceptable system clock frequency and duty cycle range are listed in the Electrical Characteristics table of this datasheet.

The PCM4201 supports specific system clock rates, which are multiples of the desired output sampling frequency. The supported system clock rate is also dependent upon the audio serial port mode. Table 1 and Table 2 specify the system clock rates required for common output sampling frequencies for both Slave and Master mode audio serial-port operation.

Table 1. System Clock Rates for Common Audio Sampling Frequencies—Slave Mode Operation

SAMPLING MODE	SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHZ)	
		SCKI = 256f_S	SCKI = 512f_S
Normal	32	8.192	16.384
Normal	44.1	11.2896	22.5792
Normal	48	12.288	24.576
Double	88.2	22.5792	N/A
Double	96	24.576	N/A

Table 2. System Clock Rates for Common Audio Sampling Frequencies—Master Mode Operation

SAMPLING MODE	SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (MHZ)	
		SCKI = 256f_S	SCKI = 512f_S
Normal	32	N/A	16.384
Normal	44.1	N/A	22.5792
Normal	48	N/A	24.576
Double	88.2	22.5792	N/A
Double	96	24.576	N/A

SAMPLING MODES

The PCM4201 supports three sampling modes, allowing the user to select the most appropriate power/performance combination for a given application. The following paragraphs describe the operation and tradeoffs for the three sampling modes. For all cases, f_S is defined as the desired output sampling rate at the audio serial port interface.

Normal Speed, Low Power mode provides the lowest overall power dissipation, while supporting sampling rates up to 54kHz. The modulator oversampling rate is $64f_S$ for this mode, which results in lower dynamic range and THD+N when compared to Normal Speed, High Performance mode. For best dynamic performance and lowest power consumption when using Low Power mode, it is recommended to operate the PCM4201 from a +1.8V digital power supply.

Normal Speed, High Performance mode provides the best overall dynamic performance at the expense of increased power dissipation. Sampling rates up to 54kHz are supported. The modulator oversampling rate is $128f_S$ for this mode, improving the overall dynamic range and THD+N when compared to Low Power mode.

Double Speed mode supports sampling frequencies up to 108kHz with power dissipation that is somewhat higher than Normal Speed, High Performance mode. The modulator oversampling rate is $64f_S$ for this mode.

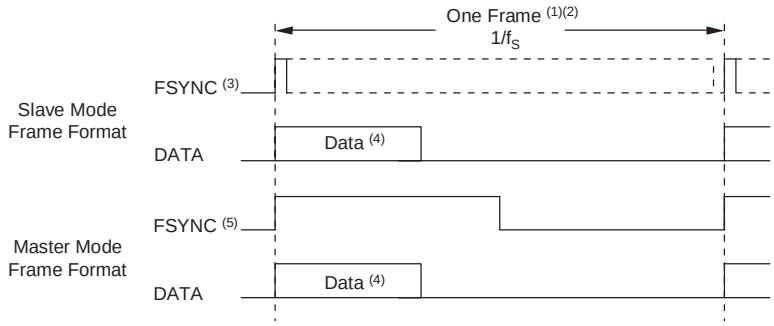
The sampling mode is selected using the RATE input (pin 5). The RATE pin is a tri-level logic input, with the ability to detect low, high, and floating (or high-impedance) states. Table 3 shows the available sampling mode configurations using the RATE pin. For the floating or high-impedance case, it is best to drive the RATE pin with a tri-state buffer, such as the Texas Instruments SN74LVC1G125 or equivalent. This allows the buffer to be disabled, setting the output to a high-impedance state.

Table 3. Sampling Mode Configuration

RATE (PIN 5)	SAMPLING MODE SELECTION
0	Double Speed
1	Normal Speed, Low Power
Float or Hi Z	Normal Speed, High Performance

AUDIO SERIAL PORT

The PCM4201 audio serial port is a 3-wire synchronous serial interface comprised of the audio serial data output, DATA (pin 9); a frame synchronization clock, FSYNC (pin 10); and a bit or data clock, BCK (pin 11). The FSYNC and BCK clocks may be either inputs or outputs, supporting either Slave or Master mode interfaces, respectively. The audio data format is 24-bit linear PCM, represented as two's complement binary data with the MSB being the first data bit in the frame. Figure 3 illustrates the audio frame format, while Figure 4 and the Electrical Characteristics table highlight the important timing parameters for the audio serial port interface.



NOTES: (1) One Frame = 128 BCK clock cycles for Normal Speed modes and 64 BCK clock cycles for Double Speed mode.
(2) If BCK = $128f_S$ when Normal Speed, Low Power sampling is enabled, then the frame will begin on the falling edge of the FSYNC clock input. The FSYNC clock is inverted for this case.
(3) For Slave Mode operation, the FSYNC pulse width high period must be at least one BCK clock cycle in length, while the FSYNC pulse low period must be at least one BCK clock cycle in length. Best performance is achieved when the FSYNC duty cycle is 50%.
(4) The audio data word length is 24 bits and is Left−Justified in the frame. The audio data is always presented in two's complement binary format with the MSB being the first data bit in the frame.
(5) For Master mode operation, the FSYNC clock duty cycle is equal to 50%.

Figure 3. Audio Serial-Port Frame Format

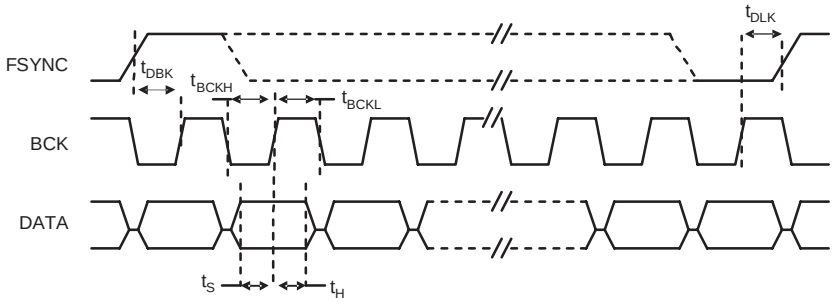


Figure 4. Audio Serial-Port Timing

Slave mode operation requires that the FSYNC and BCK clocks be generated from an external audio processor or master timing generator, as shown in Figure 5. Both clocks are inputs in Slave mode. The FSYNC clock rate is the equal to the desired output sampling frequency, f_S. The FSYNC high pulse width must be equal to at least one BCK clock period. The BCK clock rate should be $128f_S$ for Normal Speed, High Performance sampling mode. A BCK rate equal to $64f_S$ results in no output for this sampling mode. For Normal Speed, Low Power sampling mode, the BCK rate may be $64f_S$ or $128f_S$. See Note (2) in Figure 3 regarding the FSYNC edge used for start of frame when BCK = $128f_S$ for this sampling mode. For Double Speed sampling mode, the BCK rate should be $64f_S$.

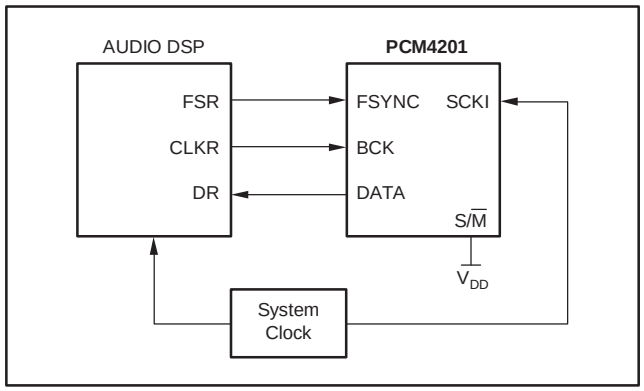


Figure 5. PCM4201 Slave Mode Configuration

For Master mode operation, the PCM4201 generates the FSYNC and BCK clocks, deriving them from the system clock input, SCKI (pin 12), as shown in Figure 6. The FSYNC clock rate is equal to the output sampling frequency, f_S. The FSYNC clock duty cycle is 50% in Master mode. The BCK clock rate is fixed at $128f_S$ for Normal Speed, High Performance sampling mode. For Normal Speed, Low Power, and Double Speed sampling modes, the BCK rate is fixed at $64f_S$.

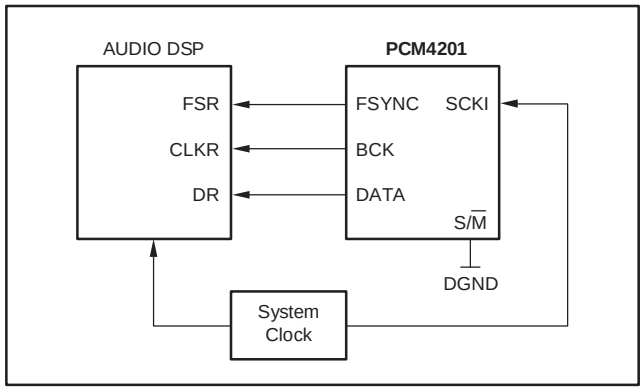


Figure 6. PCM4201 Master Mode Configuration

DIGITAL HIGH-PASS FILTER

The PCM4201 includes a digital high-pass filter, which is located at the output of the digital decimation filter block. The purpose of the high-pass filter is to remove the DC component from the digitized signal. The corner, or −3dB frequency, for the digital high-pass filter is calculated using the following relationship:

$$f_{-3dB} = \frac{f_S}{48000} \quad (1)$$

where f_S = the output sampling frequency.

The digital high-pass filter may be enabled or disabled using the HPFD input (pin 8). When HPFD is forced low, the high-pass filter is enabled. Forcing HPFD high disables the high-pass filter. Distortion for signal frequencies less than 100Hz may increase slightly when the high-pass filter is enabled.

RESET OPERATION

The PCM4201 includes two reset functions: power-on and externally controlled. This section describes the operation of each of these functions.

On power up, the internal reset signal is forced low, forcing the PCM4201 into a reset state. The power-on reset circuit monitors the V_{DD} (pin 13) and V_{CC} (pin 4) power supplies. When the digital supply exceeds $0.6 \times V_{DD}$ nominal ±400mV, and the V_{CC} supply exceeds +4.0V ±400mV, the internal reset signal is forced high. The PCM4201 will then wait for the system clock input (SCKI) to become active. Once the system clock has been detected, the initialization sequence begins. The initialization sequence requires 1024 system clock periods for completion. During the initialization sequence, the ADC output data pin will be forced low. Once the initialization sequence is completed, the PCM4201 outputs valid data. Figure 7 shows the power-on reset sequence timing.

The user may force a reset initialization sequence at any time while the system clock input is active by utilizing the $\overline{RST}$ input (pin 7). The $\overline{RST}$ input is active low, and requires a minimum low pulse width of 40ns. The low-to-high transition of the applied reset signal will force an initialization sequence to begin. As in the case of the power-on reset, the initialization sequence requires 1024 system clock periods for completion. Figure 8 illustrates the reset sequence initiated when using the $\overline{RST}$ input.

Figure 9 shows the state of the audio data output (DATA) for the PCM4201 before, during, and after the reset operations.

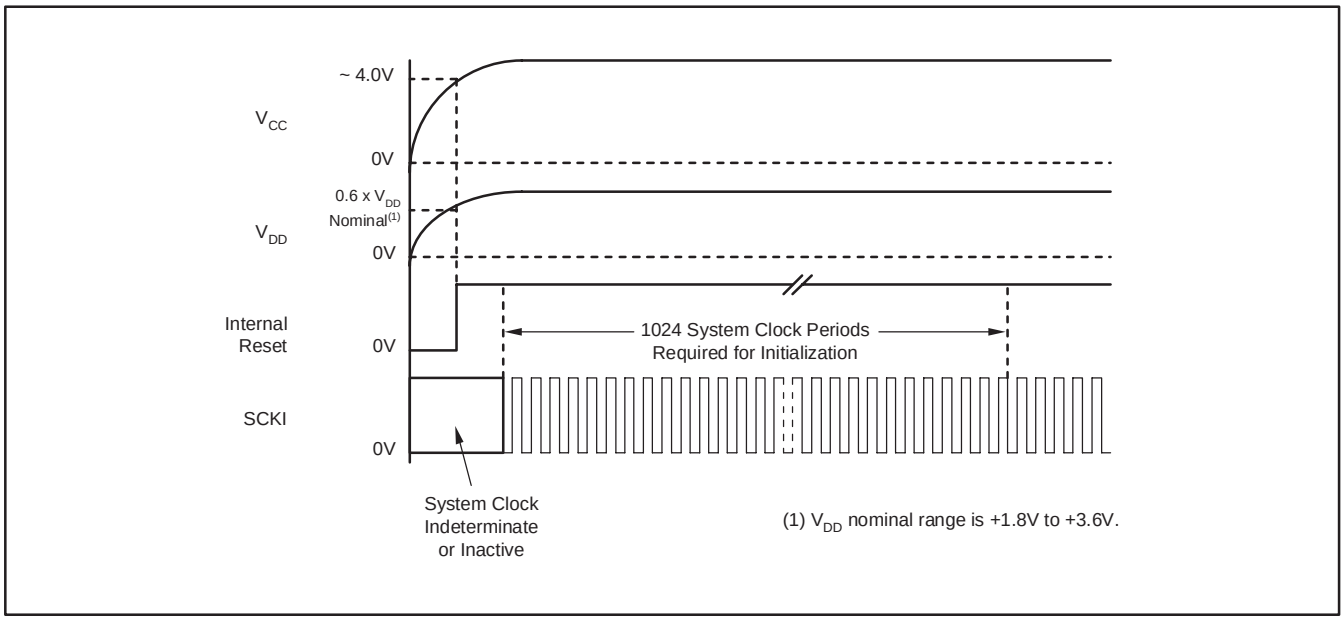


Figure 7. Power-On Reset Sequence

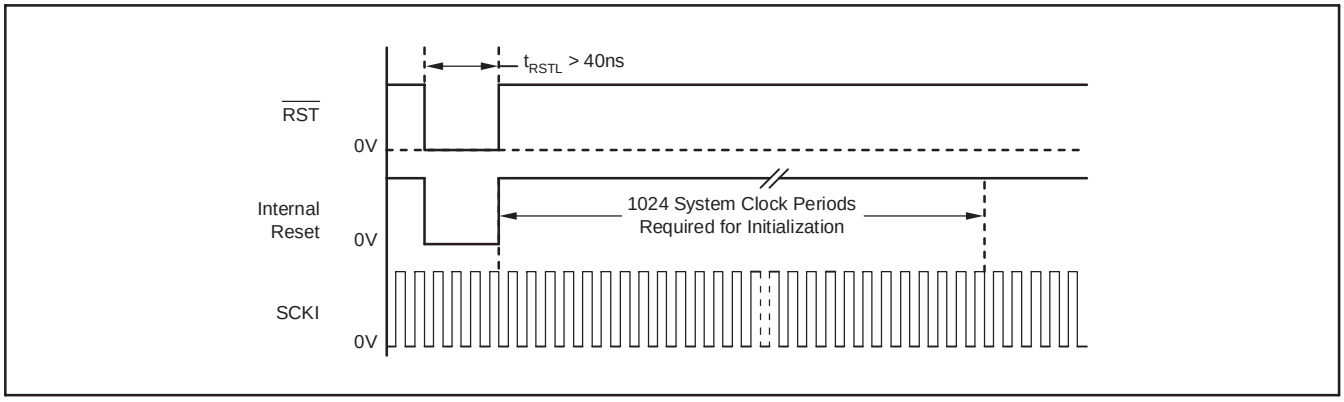


Figure 8. External Reset Sequence

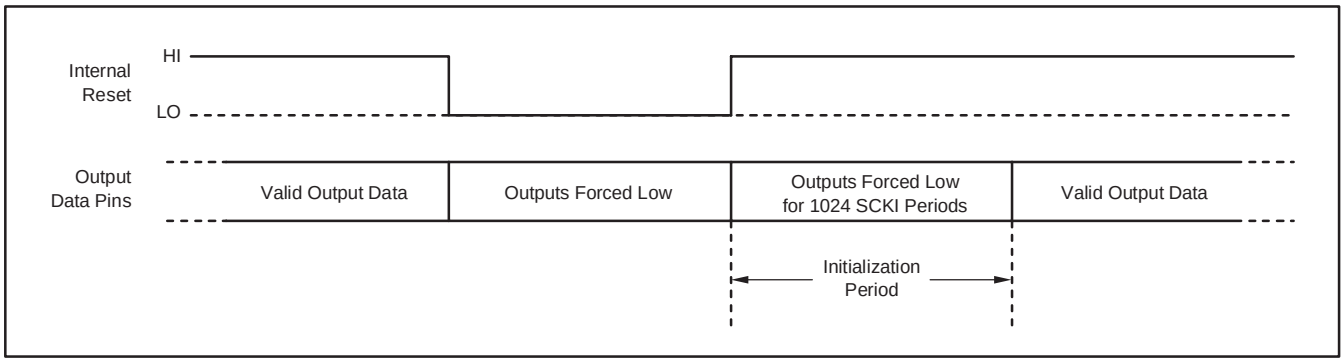


Figure 9. ADC Digital Output State for Reset Operation

POWER-DOWN OPERATION

The PCM4201 can be forced to a power-down state by applying a low level to the $\overline{RST}$ input (pin 7) for a minimum of 65,536 system clock cycles. In power-down mode, all internal clocks are stopped, and the output data pin is forced low. The system clock may then be removed to conserve additional power. Before exiting power-down mode, the system and audio clocks should be restarted. Once the clocks are active, the $\overline{RST}$ input may be driven high, which initiates a reset initialization sequence. Figure 10 illustrates the state of the output data pins before, during, and upon exiting the power-down state.

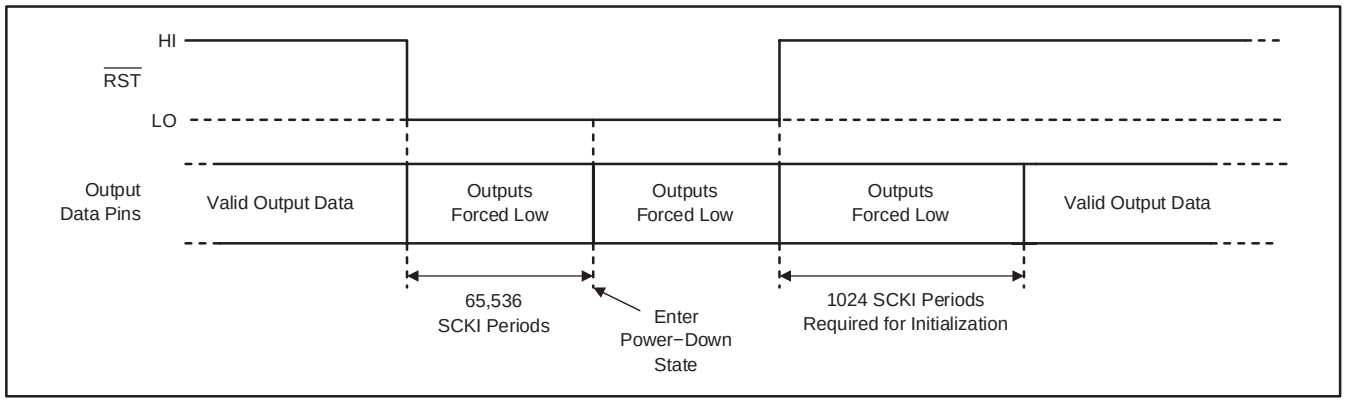


Figure 10. ADC Digital Output State for Power-Down Operation

APPLICATIONS INFORMATION

A typical connection diagram for the PCM4201 is shown in Figure 11. Power supply bypass and reference decoupling capacitors are included, and are labeled with recommended values. The 0.1µF capacitors should be X7R ceramic chip type, although other low ESR capacitor types may also be used. The 10µF capacitors may be low ESR tantalum, multilayer ceramic, or aluminum electrolytic capacitors. Analog and digital ground pins should be connected at a common point, preferably beneath the PCM4201 package.

Printed circuit board layout is critical for best performance. Please refer to the PCM4201EVM User's Guide (TI literature number SBAU108) for an example of a design and layout that meets the published specifications for the PCM4201.

INPUT BUFFER CIRCUIT EXAMPLES

The PCM4201 analog input requires some type of input buffer or signal conditioning circuitry, especially when interfacing to a microphone capsule. The input buffer or amplifier must incorporate at least a single pole, RC low-pass filter in order to provide antialias filtering for the delta-sigma modulator. A filter with a −3dB corner frequency in the range of 100kHz to 150kHz should be sufficient for common audio output sampling rates equal to or greater than 44.1kHz. However, a low-pass filter with a lower corner frequency and possibly a higher filter order will be required when running at the lower sampling rates, depending upon the system requirements. Examples of single-ended and differential input circuits are shown in Figure 12 and Figure 13, respectively.

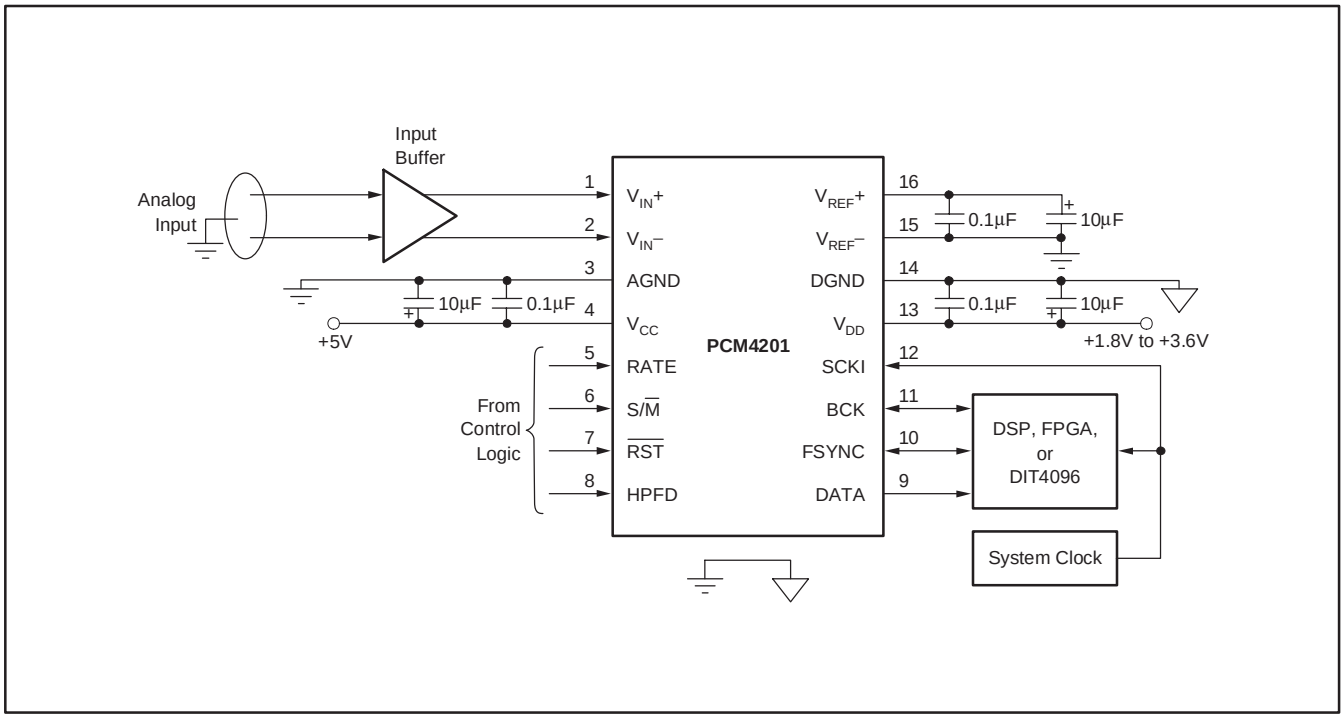


Figure 11. Typical Connections for the PCM4201

For single-ended or unbalanced inputs, the input buffer circuit shown in Figure 12 provides the conversion to a differential signal required for the PCM4201 analog inputs. The buffer circuit may be configured for the appropriate gain/attenuation using resistors R1 and R2. Capacitor C1 is chosen to provide the low-pass corner frequency. Additional low-pass filtering is provided by the RC network at the output of the buffer.

A differential input buffer circuit is shown in Figure 13. Like the unbalanced circuit, the differential buffer gain/attenuation may be set by using the R1/R2 and R3/R4 resistor pairs. The resulting gain or attenuation must be the same for both pairs. Filtering is provided by the feedback capacitors and the capacitors at the buffer output. This circuit configuration is used for the PCM4201EVM evaluation module.

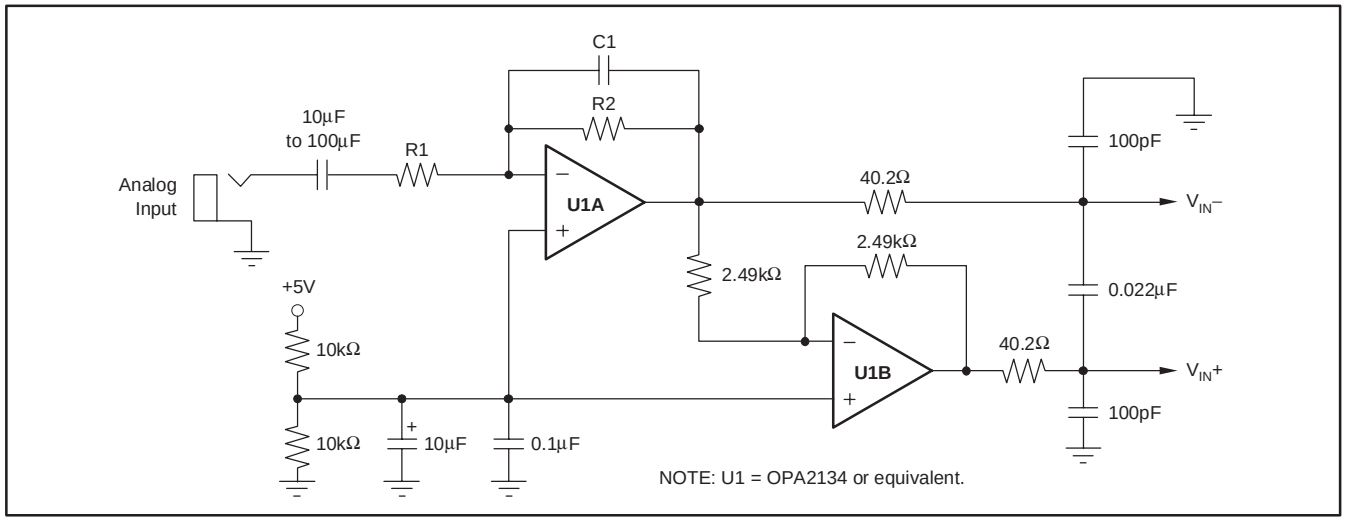


Figure 12. Single-Ended Input Buffer Circuit

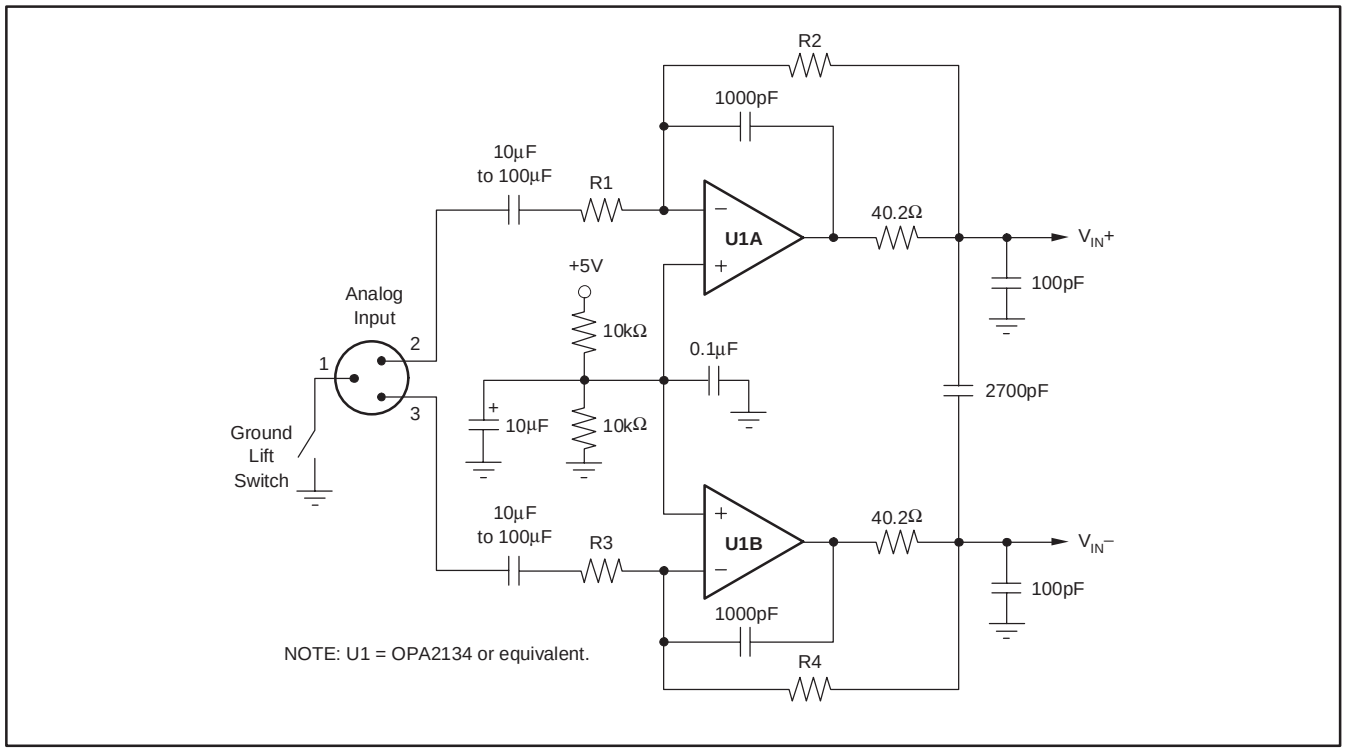
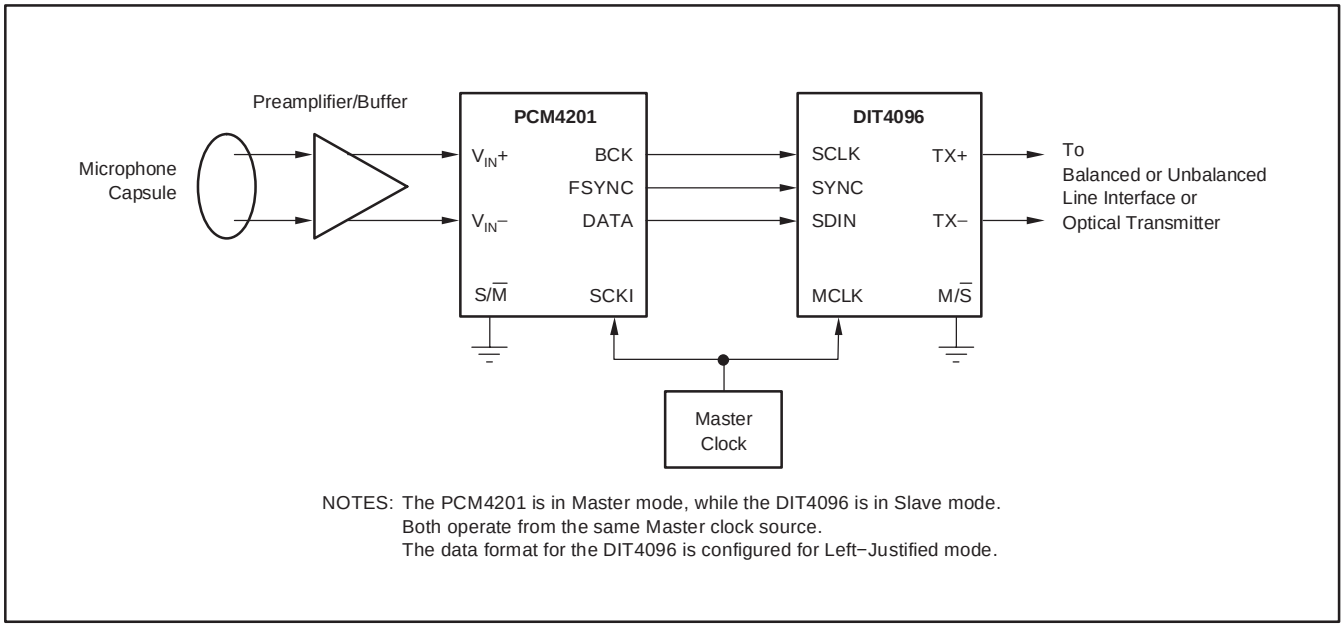


Figure 13. Differential Input Buffer Circuit

INTERFACING TO THE DIT4096 DIGITAL AUDIO TRANSMITTER

The Texas Instruments DIT4096 digital audio transmitter encodes linear PCM audio data into AES3 standard formatted data, which is compatible with a number of professional and consumer audio specifications and interfaces. This encoding provides a convenient, standard transmission format over which the audio data from the PCM4201 may be carried. The physical interface may be twisted pair or coaxial cable, or all-plastic optical fiber. The combination of the PCM4201, the DIT4096, and the appropriate microphone element and preamplifier circuit may be used to create a cost-effective, digital-interface microphone solution.

The PCM4201 output data format is equivalent to the Left-Justified data format supported by the DIT4096 transmitter. Although this format supports two channels for stereo operation, the PCM4201 provides only one channel, which corresponds to the left data channel of the DIT4096 Left-Justified data format, and channel A of the AES3 frame format. Figure 14 shows the physical interface between the PCM4201 and the DIT4096 transmitter. The digital supply for the PCM4201 (V_{DD}) and the digital I/O supply for the DIT4096 (V_{IO}) must be set to the same voltage in order to ensure logic level compatibility.



NOTES: The PCM4201 is in Master mode, while the DIT4096 is in Slave mode.
Both operate from the same Master clock source.
The data format for the DIT4096 is configured for Left−Justified mode.

Figure 14. Digital Interface Microphone Example

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
4/12/06	B	12	Product Overview	Added new Note (2) to Figure 3.
				Changed order of notes in Figure 3 to accommodate new Note (2).
		13	Product Overview	Replaced last sentence of first paragraph, left column to clarify BCK rate. Several sentences used to replace original sentence.
				Changed last sentence of second paragraph, left column to clarify BCK rate. Several sentences used to replace original sentence.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM4201PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-10 to 70	PCM 4201	Samples
PCM4201PWR	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-10 to 70	PCM 4201	Samples
PCM4201PWRG4	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-2-260C-1 YEAR	-10 to 70	PCM 4201	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

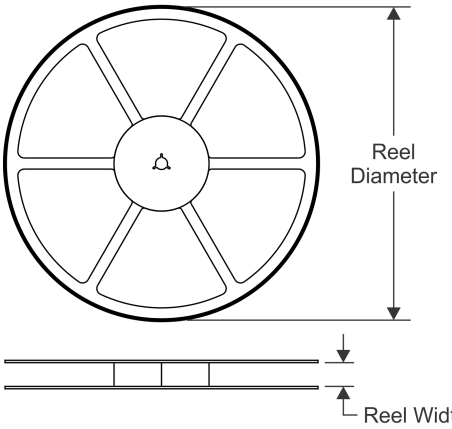
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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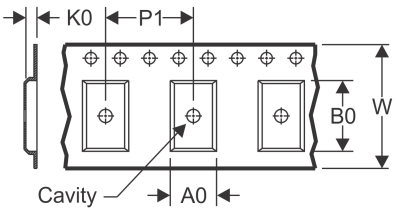
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

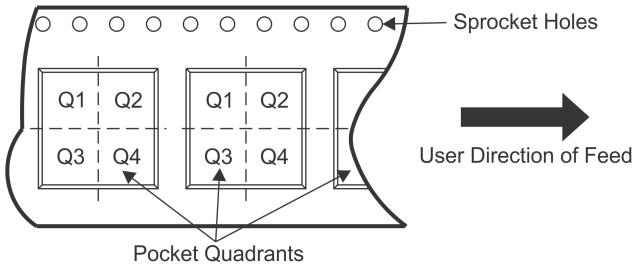


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

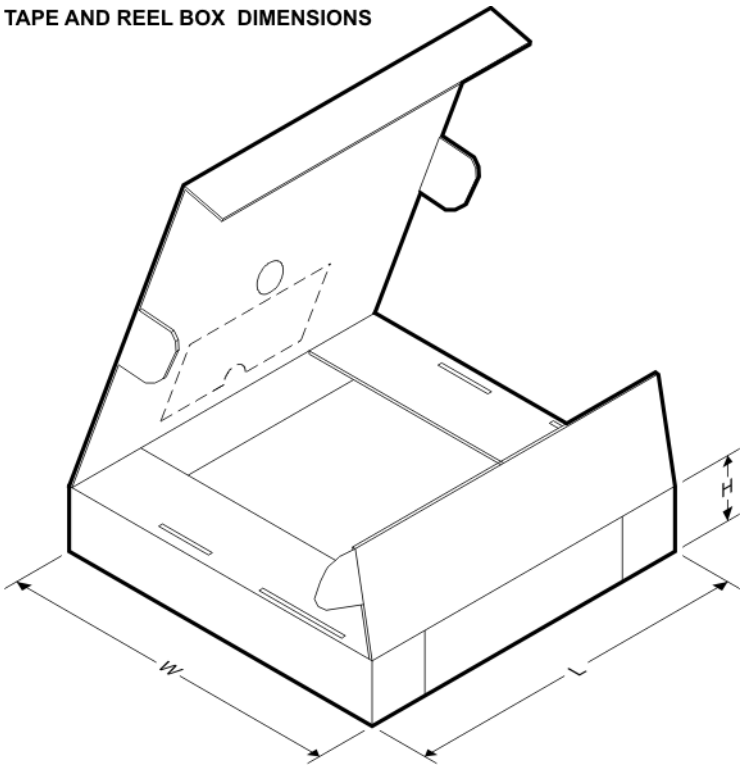
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM4201PWR	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

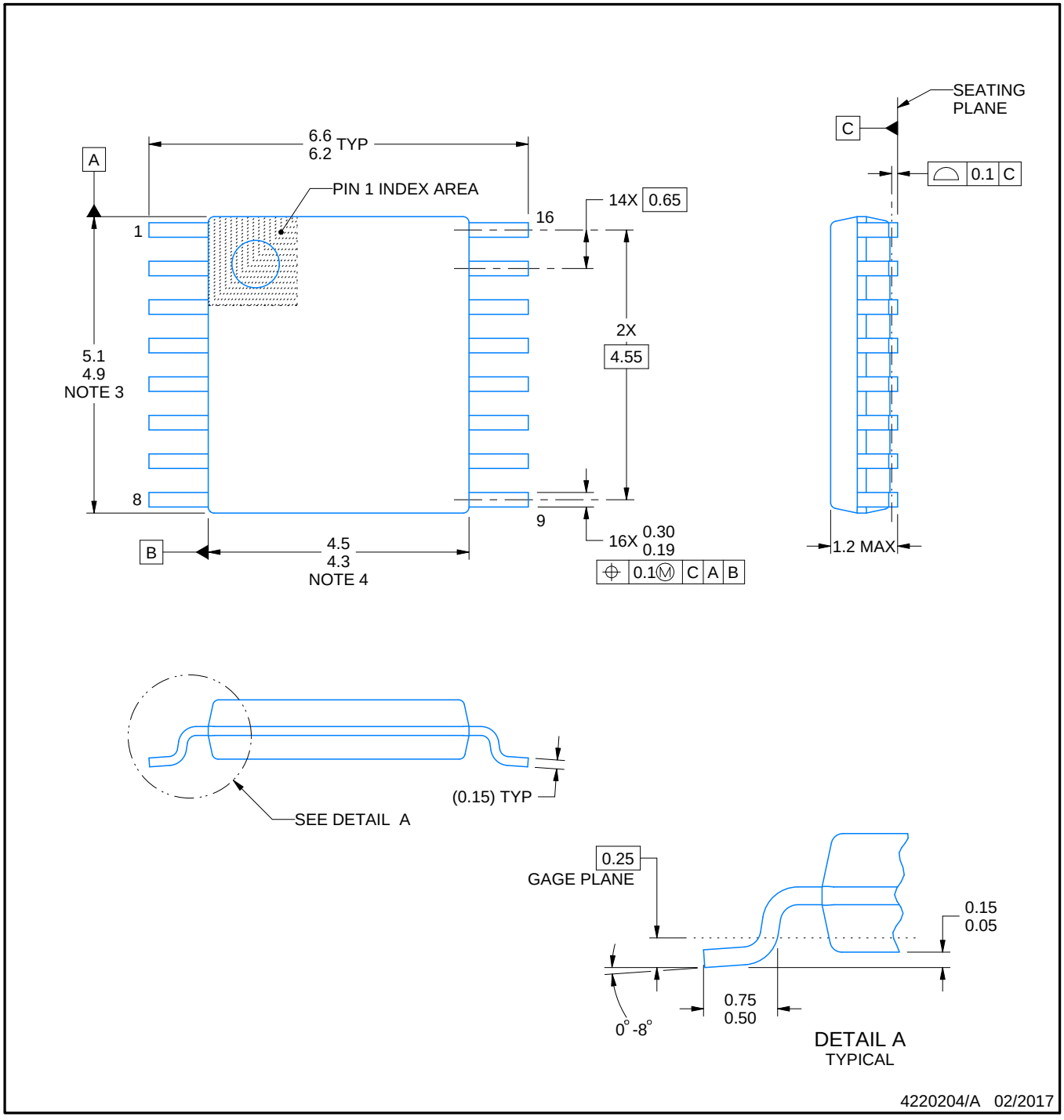
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM4201PWR	TSSOP	PW	16	2500	350.0	350.0	43.0

PACKAGE OUTLINE

PW0016A

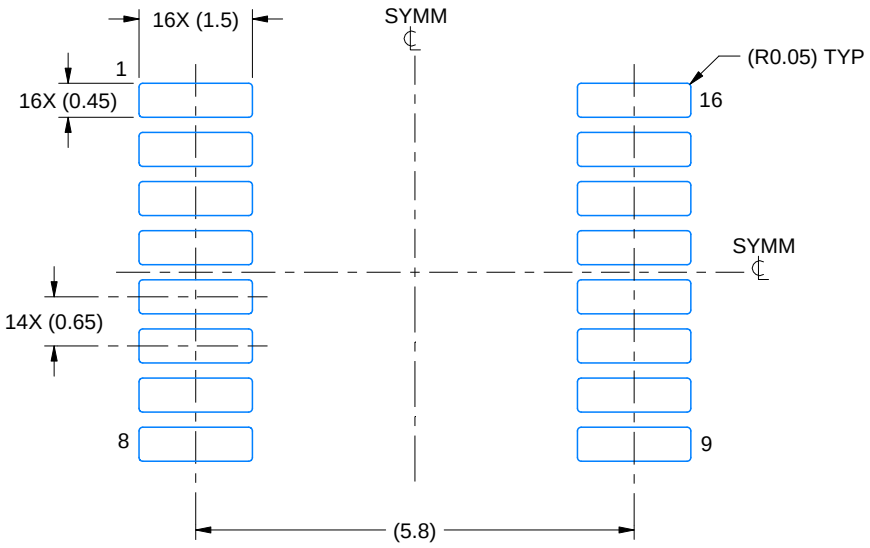
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

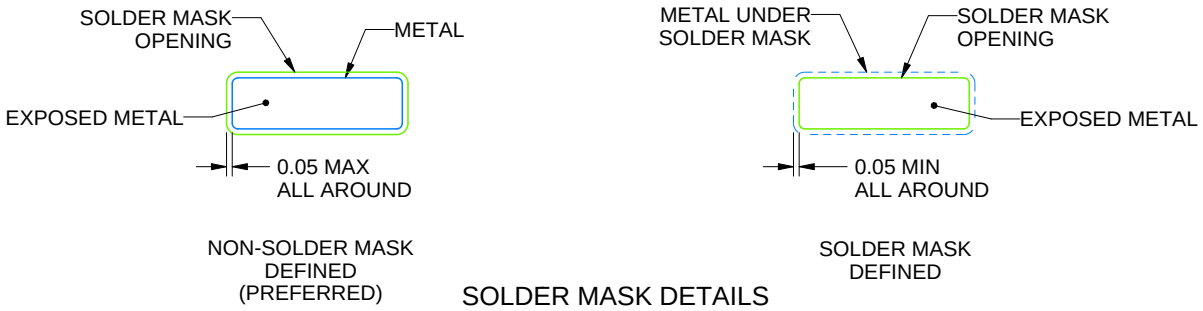


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

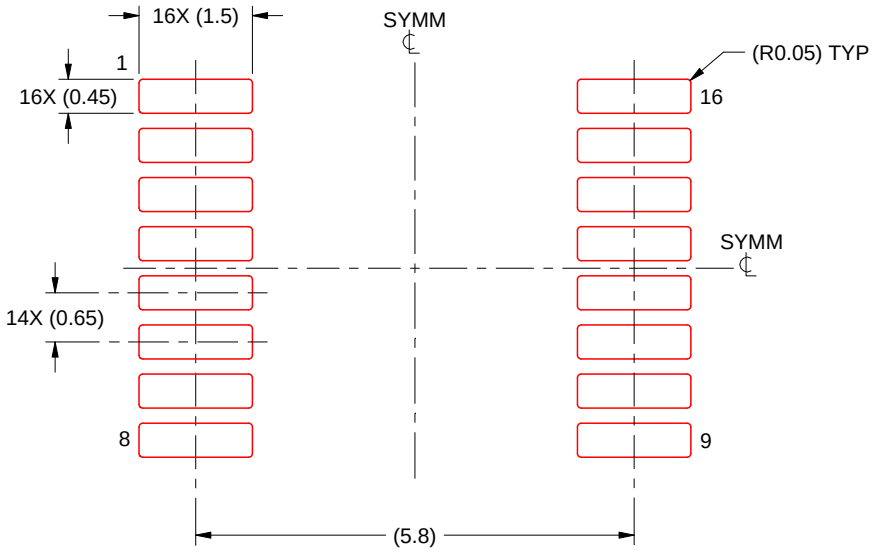


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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