

DS3170DK

DS3/E3 Single-Chip Transceiver Design Kit

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GENERAL DESCRIPTION

The DS3170DK is a fully integrated design kit for the DS3170 DS3/E3 single-chip transceiver (SCT). This design kit contains all the necessary circuitry to evaluate the DS3170 in all modes of operation. The design kit also includes an on-board microprocessor to run real-time code for further part evaluation.

DESIGN KIT CONTENTS

DS3170DK Board

Download:

ChipView Software

DS3170DK.DEF Definition File

DS3170DK Data Sheet

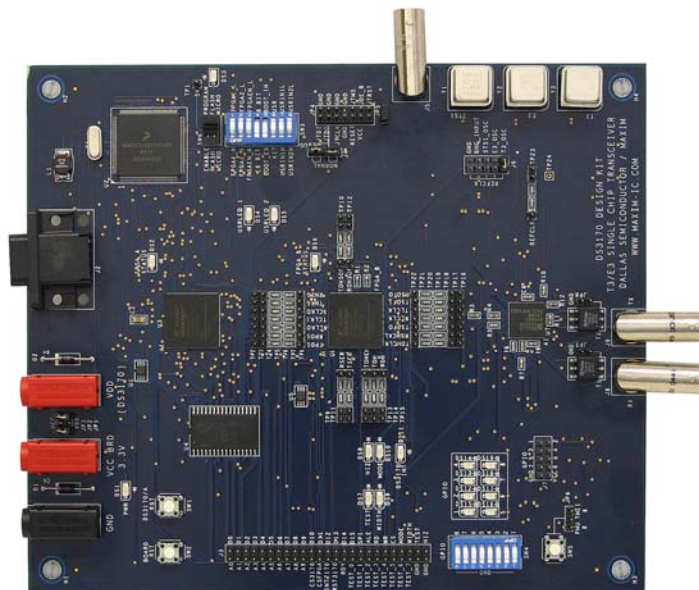
ORDERING INFORMATION

PART	DESCRIPTION
DS3170DK	Design Kit for the DS3170 DS3/E3 Single-Chip Transceiver

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FEATURES

- Expedites New Designs by Eliminating First-Pass Prototyping
- Demonstrates Key Functions of the DS3170 DS3/E3 Single-Chip Transceiver (SCT)
- Includes DS3170 Single-Chip Transceiver (SCT), Transformers, 75Ω BNC, and Termination Passives
- Interfaces with Any PC with an RS-232 Serial Interface
- High Level Windows®-Based Software Provides Visual Access to All Registers
- Software Controlled (Register) Mapped Configuration Switches Facilitate Real-Time Clock and Signal Routing
- Precision Test Points for All Clocks and Signals
- On-Board DS3 and E3 Crystal Oscillators for Stable Clock Generation
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs



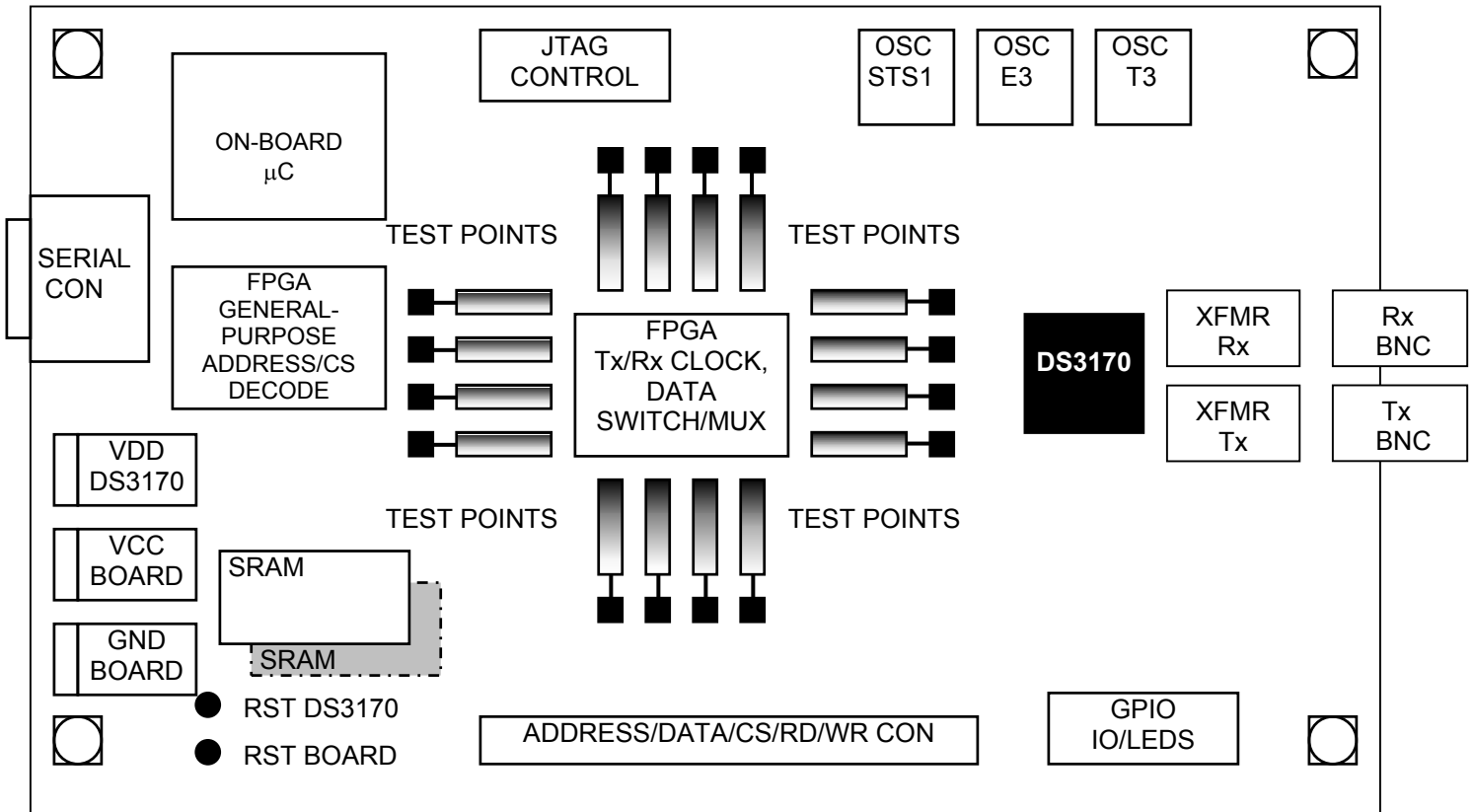
COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART NUMBER
C1, C4, C5, C10, C14, C15, C18, C19, C21, C24, C25–C32, C36–C38, C39–C44, C47–C49, C50, C52–C56, C59–C61, C66, C68, C70, C73, C74	44	0.1 μ F 20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
C2, C3, C16, C17, C20, C22, C23, C33, C34, C51, C57, C69, C75	13	1 μ F 10%, 16V ceramic capacitors (1206)	Panasonic	ECJ-3YB1C105K
C6, C62, C65	3	0.001 μ F 10%, 50V ceramic capacitors (0603)	Panasonic	ECJ-1VB1H102K
C7, C8, C9, C11, C35, C58, C76	7	68 μ F 20%, 16V tantalum capacitors (D case)	Panasonic	ECS-T1CD686R
C12, C13	2	10pF 5%, 50V ceramic capacitors (tall case)	Phycomp	1206CG100J9B200
C45, C46	2	10,000pF 10%, 16V ceramic capacitors (0603)	Panasonic	ECJ-1VB1C103K
C63, C64, C67	3	0.01 μ F 10%, 50V X7R ceramic capacitors (0603)	AVX	06035C103KAT
C71, C72	2	56,000pF 10%, 16V ceramic capacitors (0603)	Panasonic	ECJ-1VB1C563K
D1, D2	2	1A 50V general-purpose silicon diodes	General Semiconductor	1N4001
DS1, DS2, DS6–DS10	7	LED, green, SMD	Panasonic	LN1351C
DS3, DS4, DS5, DS11–DS19	12	LED, red, SMD	Panasonic	LN1251C
J1, PWR_CONNBAN1	2	Banana plug sockets (horizontal, black)	Mouser Electronics	164-6218
J2	1	DB9 right-angle connector (long case)	AMP	747459-1
J3	1	50-pin, dual-row, vertical terminal strip	Samtec	TSW-125-07-T-D
J4	1	100-mils 4-position jumper	Samtec	NA
J5	1	50 Ω BNC connector (5-pin right-angle header)	Trompeter	CBJR220
J6, J7	2	Terminal strip, 10-pin, dual row, vertical	Samtec	NA
J8, J9	2	75 Ω BNC connectors (5-pin right-angle)	Trompeter	UCBJR220
JP1, JP2, JP3, JP5, JP7, JP8	6	2-pin headers, 0.100" centerline (vertical)	Samtec	TSW-102-07-T-S
JP4	1	14-pin connector (dual row, vertical)	Samtec	NA
JP6	1	100-mils 3-position jumper	Samtec	NA
L1	1	1.0 μ H 20% 2-pin surface-mount inductor	Coiltronics	UP1B-1R0
PWR_CONNBAN2	1	Banana plug socket (horizontal, red)	Mouser Electronics	164-6219

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART NUMBER
R1–R4, R12, R42, R43, R54–R56, R59, R63, R68, R69, R70, R73, R74, R83, R93, R107	20	150Ω 1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF1500V
R5–R8, R10, R15, R51, R57, R62, R71, R81, R85, R92, R94, R95, R100, R101, R103–R106, R109	22	33Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ330V
R9, R11, R16, R22, R30, R32, R38, R46, R60, R61, R64, R65, R72, R77–R80, R89, R90, R91, R96	22	330Ω 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V
R13	1	1.0MΩ 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ105V
R14, R17–R21, R23–R29, R31, R33–R37, R39, R40, R41, R44, R45, R47, R48, R49, R52, R53, R58, R67, R75, R76, R82, R86, R87, R98, R99, R102, R108, R110	41	10kΩ 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
R50	1	1.0kΩ 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ102V
R66, R88, R97	3	0Ω 1%, 1/16W resistors (0603)	AVX	CJ10-000F
R84	1	51.1Ω 1%, 1/16W resistor (0603)	Panasonic	ERJ-3EKF51R1V
SW1, SW2, SW5	3	4-pin single-pole switch MOM	Panasonic	EVQPAE04M
SW3, SW4	2	8-position switch, 16-pin DIP, low profile	AMP	435668-7
SW6	1	Slide switch (DPDT) 6-pin through-hole	Tyco	SSA22
T1, T2	2	1:2 XFMR T3/E3/STS-1 (industrial)	Pulse	T3012
TP1–TP24	24	Test points, compensated, 3pF, 953Ω, 3 plated holes	NA	KIT1
U1, U5	2	8-pin power-μMAX (1.8V or Adj)	Maxim	MAX1792EUA18
U2	1	M-CORE 32-bit microcontroller	Motorola	MMC2107
U3, U6	2	Spartan-IIe 200K gate, 1.8V FPGA, 256 PIN BGA	Xilinx	XC2S200E-6FT256C
U4, U11	2	128K x 8 SRAM	Cypress	CY62128V
U7	1	DS3/E3 SCT 100-pin CSBGA (11mm x 11mm)	Dallas Semiconductor	DS3170
U8	1	3.3V RS-232 20-pin SO	Maxim	MAX3233EEWP
U9, U14, U16–U20, U23	8	High-speed buffer	Fairchild	NC7SZ86

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART NUMBER
U10, U12	2	2Mb flash-based configuration memory	Xilinx	XCF02SV020C
U13	1	Quad 2-input NAND gate 14-pin SO	Toshiba	TC74HC00AFN
U15, U21, U24	3	Hex inverter, SO	Toshiba	TC74HC04AFN
U22	1	SOT switch debouncer	Maxim	MAX6816
X1	1	8.0MHz low-profile crystal	Dove Electronic	EC1-8.000M
Y1	1	3.3V 51.840MHz oscillator, crystal clock	SaRonix	NTH089AA3-51.840
Y2	1	3.3V 34.368MHz oscillator, crystal clock	SaRonix	NTH089AA3-34.368
Y3	1	3.3V 44.736MHz oscillator, crystal clock	SaRonix	NTH089AA3-44.736

BOARD FLOORPLAN



BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/telecom. See the DS3170DK QuickView page for files.

The support files are used with an evaluation program called ChipView with is available for download at www.maxim-ic.com/telecom.

HARDWARE CONFIGURATION

Quick Start (Hardware Settings)

- For single power-supply operation, short jumpers JP1-JP3. This connects VDD of the DS3170 to the board VCC.
- Ensure that *PROGRAM FLASH MICRO* is selected (SW6). DS3 should not be on.
- Connect reference clock. See [Table 1](#).
- DIP switches (SW3) can be in either the ON or OFF position depending on the desired configuration. See [Table 6](#).
- Connect serial cable from DS3170DK (J2) to PC.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V.

Reference Clock Configuration

The reference clock for the DS3170 (SCT) can be configured a number of ways depending on the application's need. This is done by shorting the REFCLK signal on J6 to the signal inputs, which are also connected to J6.

Table 1: Reference Clock Configuration

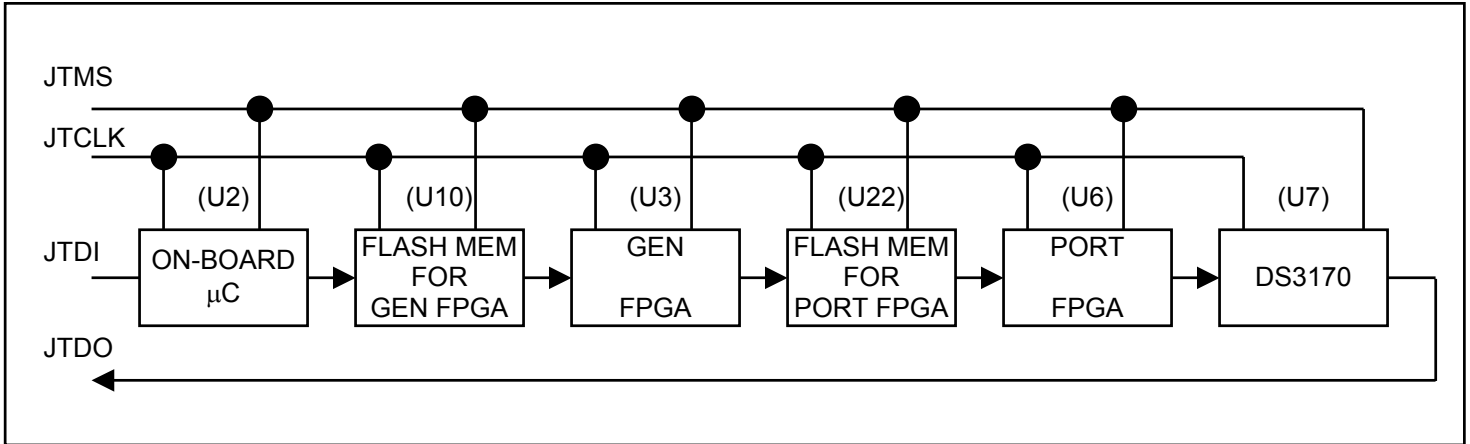
REFERENCE CLOCK	DESCRIPTION
GND	Short pins J6.1 and J6.2 together. Open all other pins on J6.
BNC Input	Short pins J6.3 and J6.4 together. Open all other pins on J6.
STS1 OSC	Short pins J6.5 and J6.6 together. Open all other pins on J6.
E3 OSC	Short pins J6.7 and J6.8 together. Open all other pins on J6.
T3 OSC	Short pins J6.9 and J6.10 together. Open all other pins on J6.

JTAG Configuration

The JTAG chain is controlled by the following connectors: J4, JP4, and JP5. Depending on the function, such as programming the internal microcontroller flash or performing boundary scan operations, the three connectors can be configured to accomplish the desired task. For information on programming the internal flash of the microcontroller, refer to the microcontroller user manual and board schematic.

For most purposes, having the complete JTAG chain is sufficient. [Figure 1](#) shows the complete chain as well as what order the devices will appear during boundary scan. To set up this configuration, perform the following:

- Connect JTDI to JP4.1
- Connect JTDO to JP4.3
- Connect JTMS to JP4.10
- Connect JCLK to JP4.5
- Connect J4.1 to J4.2
- Connect J4.3 to J4.4
- Connect JP5.1 to JP5.2

Figure 1. JTAG Chain

Address/Data BUS Connector

The DS3170DK has a connector (J3) to monitor all local bus activity for the design kit. All the signals can be captured with a high-impedance probe and displayed on an oscilloscope or logic analyzer. **Note:** If FPGA_ENABLE (SW3.3) is logic 0, the on-board microcontroller will no longer drive any data onto the local bus. Therefore, the user can now connect the local bus of the DS3170 into another system without making any modifications to the hardware. See [Table 2](#) for specific pin information for connector J3.

Table 2. Address/Data Connector

PIN NUM	PIN NAME	DESCRIPTION		PIN NUM	PIN NAME	DESCRIPTION
1	A0	Local Address Bit 0		2	D0	Local Data Bit 0
3	A1	Local Address Bit 1		4	D1	Local Data Bit 1
5	A2	Local Address Bit 2		6	D2	Local Data Bit 2
7	A3	Local Address Bit 3		8	D3	Local Data Bit 3
9	A4	Local Address Bit 4		10	D4	Local Data Bit 4
11	A5	Local Address Bit 5		12	D5	Local Data Bit 5
13	A6	Local Address Bit 6		14	D6	Local Data Bit 6
15	A7	Local Address Bit 7		16	D7	Local Data Bit 7
17	A8	Local Address Bit 8		18	D8	Local Data Bit 8
19	A9	Local Address Bit 9		20	D9	Local Data Bit 9
21	CS3170	Chip Select DS3170		22	D10	Local Data Bit 10
23	CSFPGA	Chip Select Port FPGA		24	D11	Local Data Bit 11
25	INT3170	INT PIN DS3170		26	D12	Local Data Bit 12
27	RST3170	RST PIN DS3170		28	D13	Local Data Bit 13
29	RDY	Ready Handshake DS3170		30	D14	Local Data Bit 14
31	TEST0	Generic I/O Bit 0		32	D15	Local Data Bit 15
33	TEST1	Generic I/O Bit 1		34	SPI	DS3170 Serial/Parallel Bus Mode
35	TEST2	Generic I/O Bit 2		36	ALE	Address Latch Enable
37	TEST3	Generic I/O Bit 3		38	RD_DS	Read (Intel)/Data Strobe (MOT)
39	TEST4	Generic I/O Bit 4		40	WR_W/R	Write (Intel)/Write_READ (MOT)
41	TEST5	Generic I/O Bit 5		42	CS_OUT	Programmable CS_OUT Pin
43	TEST6	Generic I/O Bit 6		44	MODE	Mot/Intel Mode
45	TEST7	Generic I/O Bit 7		46	WIDTH	Data Bus Width
47	GND	GND		48	TEST	Test Enable (Active Low)
49	GND	GND		50	HIZ	High Impedance (Active Low)

High Impedance and Compensated Test Points

The test points for all the clock and data lines are unique for this board such that each test point listed in [Table 3](#) have a relative high-impedance pin and a compensated pin. The compensated pin is part of a (20:1) voltage divider that when used with the standard 50Ω load of an oscilloscope provides a very clean signal. If you are making critical timing and or slew rate measurements, the compensated test points are very useful. [Figure 2](#) shows the relationship between the high-impedance and compensated test point pins.

Figure 2. Test Point Logical and Physical View

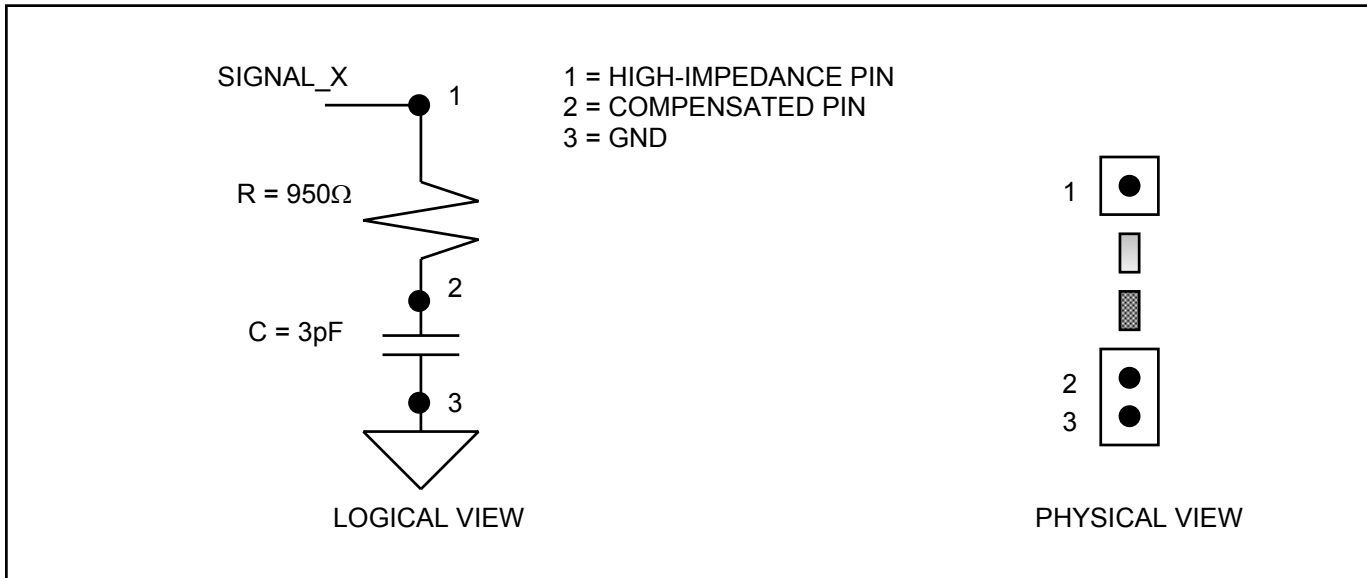


Table 3. Test Points

REF DES	SIGNAL NAME	REF DES	SIGNAL NAME
TP5	TCLKI	TP7	TNEG
TP6	TCLKO	TP8	RNEG
TP4	RCLKO	TP2	TPOS
TP20	TLCLK	TP3	RPOS
TP19	RLCLK	TP11	TSER
TP10	TOHSOF	TP9	RSER
TP12	ROHSOF	TP13	TOHEN
TP16	TOHCLK	TP14	TOH
TP17	ROHCLK	TP15	ROH
TP19	TSOFO	TP23	REFCLK
TP22	RSOFO	TP21	TSOFI

General Purpose Input/Output for DS3170

The DS3170 SCT has an 8-bit port that can be bit configured as either general-purpose I/O or specific alarms, a TEMI input, or PMU input. Refer to the DS3170 data sheet for specific questions about the operation of the DS3170 GPIO port.

Each GPIO pin has two types of inputs and an LED for easy identification of the pin's state. The first input type for the GPIO port is an 8-bit switch (SW4). Each pin on SW4 corresponds to the bit in the GPIO. When the switch is in the "On" position, the pin for the switch is grounded and provides logic 0 to the port. When the switch is in the "Off" position, the pin for the switch floats to VDD and provides logic 1 to the port.

The second input type for the GPIO port is a straight 10-pin header (J7). This can be simply a monitoring pin for the GPIO port or used as input stimulus. **Note:** If you plan to drive a bit to a value other than GND, the GPIO bit in SW4 must be in the "Off" position. See the DS3170DK schematic for questions on the connection of the GPIO port.

[Table 4](#) provides a description of pin out of SW4 and J7.

Table 4. GPIO Header and Switch Pinout

PIN NUMBER		PIN NAME
SW4.1	J7.1	GPIO Bit 1
SW4.2	J7.2	GPIO Bit 2
SW4.3	J7.3	GPIO Bit 3
SW4.4	J7.4	GPIO Bit 4
SW4.5	J7.5	GPIO Bit 5
SW4.6	J7.6	GPIO Bit 6
SW4.7	J7.7	GPIO Bit 7
SW4.8	J7.8	GPIO Bit 8

TEMI and PMU Inputs

GPIO Bit 6 and GPIO Bit 8 can be configured to be the TEMI and PMU inputs respectively. A pushbutton (SW5) and 3-position jumper (JP6) are available to provide a glitch-free input to either of these inputs. **Note:** When using the pushbutton (SW5) and 3-position jumper (JP6) as an input to the GPIO pins, you must have the appropriate switch in SW4 in the "Off" position.

Table 5. TEMI and PMU Configuration

SIGNAL NAME	SETUP PROCEDURE
TEMI	Set SW4.6 to the "Off" position
	Short (Jumper) JP6.3 and JP2
PMU	Set SW4.8 to the "Off" position
	Short (Jumper) JP6.1 and JP2

User Input Switch (SW3)

SW3 is an 8-pin DIP switch that controls the function of the on-board microcontroller and the two on-board FPGAs, and offers a number of generic inputs for user programs.

Table 6. User Input Switch Pinout

PIN	NAME	FUNCTION
1	FPGA INPUT 1	Generic Input-Only Pin to the General-Purpose FPGA. Value of pin is copied to general-purpose register XXXXXXXX. Can be used for user programs. This pin has no effect if FPGA ENABLE is logic 0.
2	FPGA INPUT 2	Generic Input-Only Pin to the General-Purpose FPGA. Value of pin is copied to general-purpose register XXXXXXXX. Can be used for user programs. This pin has no effect if FPGA ENABLE is logic 0.
3	FPGA ENABLE	Input-Only Pin to the General-Purpose FPGA (U3). When this pin is logic 1 (SW3.3 is OFF), the FPGA is enabled and will transfer data from the DS3170 and FPGA as directed from the on-board microcontroller. When this pin is logic 0 (SW3.3 is ON), the FPGA is disabled. All inputs and outputs to the DS3170 and port FPGA are tri-stated. Note: This pin does not cause a hardware enable for the PORT FGPA.
4	DATA BUS SELECT	Input-Only Pin to the General-Purpose FPGA (U3). When this pin is logic 1 (SW3.4 is OFF), the DS3170 and the port FPGA are set up such that they use the 16-bit bus from the on-board microcontroller. When this pin is logic 0 (SW3.4 is ON), the DS3170 and the port FPGA are set up such that they use the 8-bit bus from the on-board microcontroller. This pin has no effect if FPGA ENABLE is logic 0.
5	BOOT SEL	Input-Only Pin to the On-Board Microcontroller. When this pin is logic 1 (SW3.5 is OFF), the on-board microcontroller loads the firmware from an external source rather than the internal flash bank. When this pin is logic 0 (SW3.5 is ON), the microcontroller loads the firmware from the internal flash bank. If you choose to load code from an external source, refer to the user manual for the on-board microcontroller (U2) to ensure that all the timing and data are correct to run this program. This option should only be used by the advanced user.
6	KIT	Input-Only Pin to the On-Board Microcontroller. Not implemented with the firmware shipped from Dallas Semiconductor. This pin can be used by a user program.
7	USER INPUT 1	Input/Output Pin to the General-Purpose FPGA (U3). This pin has an LED (DS4) to track the value of this signal. This pin has no effect if FPGA ENABLE is logic 0. Note: If you choose to use this as an output, USER INPUT 1 (SW3.7) must be in the off position.
8	USER INPUT 2	Input/Output Pin to the General-Purpose FPGA (U3). This pin has an LED (DS5) to track the value of this signal. This pin has no effect if FPGA ENABLE is logic 0. Note: If you choose to use this as an output, USER INPUT 1 (SW3.8) must be in the off position.

SOFTWARE CONFIGURATION

Quick Start (Software—ChipView)

- Perform steps in the Quick Start (Hardware Settings).
- Load ChipView software.
- Select COM port.
- Select Register View.
- From the Programs menu, launch the host application named ChipView.EXE. If the default installation options were used, click the Start button on the Windows toolbar and select Programs → ChipView → ChipView.
- Load the DS3170DK.DEF file.
- Make sure that all the register settings are correct for the proper function desired for the DS3170DK.
- Refer to the DS3170 data sheet for all questions pertaining to device functionality.

MEMORY MAP

The on-board microcontroller is configured to start the user address space at 0x81000000. All offsets given in [Table 7](#) are relative to the beginning of the user address space. All device registers can be easily modified using ChipView.EXE host-based user-interface software.

Table 7. Relative Address Map

REF DES	DEVICE	OFFSET
U3	General-purpose FPGA	0x0000
U6	FPGA Tx/Rx clock, data switch/mux	0x1000
U7	DS3170 DS3/E3 single-chip transceiver	0x2000

Table 8. General-Purpose Memory Map

OFFSET	REGISTER NAME	TYPE	DESCRIPTION
0x00	BRDID	Read Only	Board ID
0x02	DSIDH	Read Only	Dallas Extended ID Upper Nibble
0x03	DSIDM	Read Only	Dallas Extended ID Middle Nibble
0x04	DSIDL	Read Only	Dallas Extended ID Lower Nibble
0x05	BRDREV	Read Only	Board Rev
0x06	ASMREV	Read Only	Assembly Rev
0x07	FPGAREV	Read Only	FPGA Firmware Rev
0x08	CTRL1	Control	Control Reg #1

ID REGISTERS

BID: BOARD ID (Offset=0X0000)

BID is read only with a value of 0xD.

XBIDH: HIGH NIBBLE EXTENDED BOARD ID (Offset=0X0002)

XBIDH is read only with a value of 0x00.

XBIDM: MIDDLE NIBBLE EXTENDED BOARD ID (Offset=0X0003)

XBIDM is read only with a value of 0x07.

XBIDL: LOW NIBBLE EXTENDED BOARD ID (Offset=0X0004)

XBIDL is read only with a value of 0x00.

BREV: BOARD FAB REVISION (Offset=0X0005)

BREV is read only and displays the current fab revision.

AREV: BOARD ASSEMBLY REVISION (Offset=0X0006)

AREV is read only and displays the current assembly revision.

PREV: PLD REVISION (Offset=0X0007)

PREV is read only and displays the current PLD firmware revision.

CONTROL REGISTERS

Register Name: **CTRL1**

Register Description: **Control Register 1**

Register Offset: **0x0008**

Bit #	7	6	5	4	3	2	1	0
Name	SPI_CPOL	SPI_CPHA	SPI_SWAP	SPI	HIZ	WIDTH	MOT	MUX
Default	0	0	0	0	1	0	0	0

Bit 7: SPI_CPOL: This bit controls the SPI Interface Clock Polarity pin, which is muxed with the D7 pin on the DS3170. Bit 7 is only active when bit 4 (SPI) is a logic 1. Refer to the DS3170 data sheet for pin operation.

Bit 6: SPI_CPHA: This bit controls the SPI Interface Clock Phase pin, which is muxed with the D6 pin on the DS3170. Bit 6 is only active when Bit 4 (SPI) is a logic 1. Refer to the DS3170 data sheet for pin operation.

Bit 5: SPI_SWAP: This bit controls the SPI Interface Bit Order Swap pin, which is muxed with the D5 pin on the DS3170. Bit 5 is only active when Bit 4 (SPI) is a logic 1. Refer to the DS3170 data sheet for pin operation.

Bit 4: SPI: This bit controls the SPI Bus Mode bit.
0 = parallel bus mode
1 = SPI bus mode

Bit 3: HIZ: This bit controls the high-impedance test-enable bit (active low). This signal puts all the digital outputs and bidirectional outputs to a high-impedance state when pulled low and also when the JTRST is pulled low. For normal operation, keep it as a logic 1.

Bit 2: WIDTH: This bit controls the databus width pin for parallel bus mode.
0 = 8-bit parallel mode
1 = 16-bit parallel mode

Bit 1: MOT: This bit controls the MODE pin for the DS3170.
0 = RD/WR strobe mode (Intel)
1 = DS strobe mode (Motorola)

Bit 0: MUX: This bit determines if the ALE pin on the DS3170 is in mux mode or nonmux mode (constantly high).
0 = nonmux mode
1 = mux mode

Register Name: **CTRL2**Register Description: **Control Register 2–Line IO**Register Offset: **0x0009**

Bit #	7	6	5	4	3	2	1	0
Name	RNEG3	RNEG2	RNEG1	RNEG0	RPOS3	RPOS2	RPOS1	RPOS0
Default	0	0	0	0	1	0	0	0

Bits 7 to 4: RNEGx: These bits control the source of the RNEG signal.**Bits 3 to 0: RPOSx:** These bits control the source of the RPOS signal.

RPOSx	DESCRIPTION
0x00	HI-Z
0x01	TPOS
0x02	T3 OSC
0x03	E3 OSC
0x04	STS1 OSC
0x05	BNC_INPUT
0x06	Logic 0
0x07	Logic 1
0x08–0xFF	HI-Z

RNEGx	DESCRIPTION
0X00	HI-Z
0X01	TNEG
0X02	T3 OSC
0X03	E3 OSC
0X04	STS1 OSC
0X05	BNC_INPUT
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

Register Name: **CTRL3**

Register Description: **Control Register 3—Line RCLK**

Register Offset: **0x000A**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	RLCLK3	RLCLK2	RLCLK1	RLCLK0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: These bits are unused.

Bits 3 to 0: RLCLKx: These bits control the source of the RLCLK signal.

RLCLKx	DESCRIPTION
0X00	HI-Z
0X01	TLCLK
0X02	T3 OSC
0X03	E3 OSC
0X04	STS1 OSC
0X05	BNC_INPUT
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

Register Name: **CTRL4**Register Description: **Control Register 4 Overhead Interface**Register Offset: **0x000B**

Bit #	7	6	5	4	3	2	1	0
Name	TOHEN3	TOHEN2	TOHEN1	TOHEN0	TOH3	TOH2	TOH1	TOH0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: TOHENx: These bits control the source of the TOHEN signal.**Bits 3 to 0: TOHx:** These bits control the source of the TOH signal.

TOHENx	DESCRIPTION
0X00	HI-Z
0X01	TOHSOF
0X02	ROHSOF
0X03	Not used
0X04	Not used
0X05	Not used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

TOHx	DESCRIPTION
0X00	HI-Z
0X01	ROH
0X02	Not used
0X03	Not used
0X04	Not used
0X05	Not used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

Register Name: **CTRL5**

Register Description: **Control Register 5 Serial Data Overhead Interface**

Register Offset: **0x000C**

Bit #	7	6	5	4	3	2	1	0
Name	—	—	—	—	TSER3	TSER2	TSER1	TSER0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: These bits are unused.

Bits 3 to 0: TSERx: These bits control the source of the TSER signal.

TSERx	DESCRIPTION
0X00	HI-Z
0X01	RSER
0X02	Not Used
0X03	Not Used
0X04	Not Used
0X05	Not Used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

Register Name: **CTRL6**

Register Description: **Control Register 6 Serial Data Overhead Interface**

Register Offset: **0x000D**

Bit #	7	6	5	4	3	2	1	0
Name	TSOFI3	TSOFI2	TSOFI1	TSOFI0	TCLKI3	TCLKI2	TCLKI1	TCLKI0
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: TSOFIx: These bits control the source of the TSOFI signal.

Bits 3 to 0: TCLKIx: These bits control the source of the TCLKI signal.

TSOFIx	DESCRIPTION
0X00	HI-Z
0X01	TSOFO
0X02	RSOFO
0X03	Not Used
0X04	Not Used
0X05	Not Used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

TCLKIx	DESCRIPTION
0X00	HI-Z
0X01	TCLKO
0X02	RCLKO
0X03	Not Used
0X04	Not Used
0X05	Not Used
0X06	Logic 0
0X07	Logic 1
0X08–0XFF	HI-Z

DS3170 INFORMATION

For more information about the DS3170, refer to the DS3170 data sheet available on our website at www.maxim-ic.com/DS3170. Software downloads are also available for this design kit.

DS3170DK INFORMATION

For more information about the DS3170DK including software downloads, consult the DS3170DK data sheet available on our website at www.maxim-ic.com/DS3170DK.

TECHNICAL SUPPORT

For additional technical support, e-mail your questions to telecom.support@dalsemi.com.

SCHEMATICS

The DS3170DK schematics are featured in the following 23 pages.

DS3170 DESIGN KIT

CREATED BY
DALLAS SEMICONDUCTOR
JUNE 26, 2004

- Page 1. COVER PAGE
- Page 2. DS3170 BGA
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- Page 5. DS3170 RESET / GPIO
- Page 6. MISC TELECOM SIGNALS
- Page 7. REF OSC
- Page 8. PORT FPGA CONTROL / FLASH
- Page 9. PORT FPGA BLOCK1
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- Page 13. SERIAL/JTAG CONN
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- Page 18. ADDRESS/DATA HEADERS
- Page 19. MICROCONTROLOR SRAM
- Page 20. POWER CONN
- Page 21. NOTES

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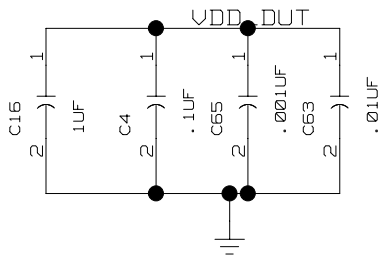
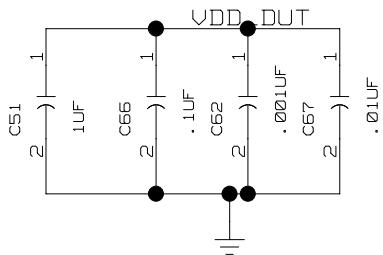
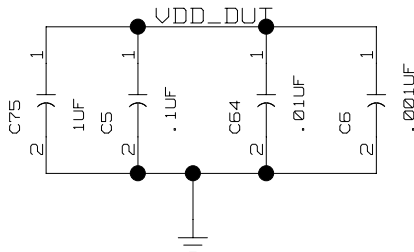
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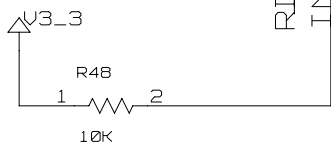
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DS3170
100 PIN BGA



LA0	K5	A<0>/BSWAP
LA1	J2	A<1>
LA2	K2	A<2>
LA3	H3	A<3>
LA4	J3	A<4>
LA5	K3	A<5>
LA6	H4	A<6>
LA7	J4	A<7>
LA8	H5	A<8>
XD0	J5	D<0>/SPI_MISO
XD1	K9	D<1>/SPI_MOSI
XD2	J6	D<2>/SPI_SCLK
XD3	H6	D<3>
XD4	K7	D<4>
XD5	J7	D<5>/SPI_SWAP
XD6	H7	D<6>/SPI_CPHA
XD7	K8	D<7>/SPI_CPOL
XD8	J8	D<8>
XD9	G6	D<9>
XD10	J9	D<10>
XD11	J10	D<11>
XD12	H8	D<12>
XD13	H9	D<13>
XD14	H10	D<14>
XD15	G8	D<15>



RDY*	J1	RDY*
INT*	D8	INT*
MODE	F3	MODE
WIDTH	H2	WIDTH
SPI	C3	SPI
VSS1	C1	VSS1
VSS2	K1	VSS2
VSS3	K6	VSS3
VSS4	G10	VSS4
VSS5	A10	VSS5
VSS6	A2	VSS6
AVSSR	B5	AVSSR
AVSST	E4	AVSST
AVSSJ	D2	AVSSJ
AVSSC	G1	AVSSC
GPIO<1>	E8	GPIO<1>
GPIO<2>	E7	GPIO<2>
GPIO<3>	F7	GPIO<3>
GPIO<4>	G7	GPIO<4>
GPIO<5>	F6	GPIO<5>
GPIO<6>	G5	GPIO<6>
GPIO<7>	D3	GPIO<7>
GPIO<8>	D4	GPIO<8>
TEST*	F5	TEST*
HIZ_70	B4	HIZ_70
RST*	E6	RST*

ALE	G4	ALE
CS*	A1	CS3170
RD*/DS*	B2	RD_DS
WR*/RW	C2	WR_W/R
JTCLK	A5	JTCLK
JTMS	B3	JTMS
JTDI	C4	JTDI_X11_INXB_2_DS3170
JTDO	D5	JTDO
JTRST*	E5	JTRST
VDD1	B1	VDD_DUT
VDD2	D1	VDD_DUT
VDD3	K4	VDD_DUT
VDD4	K10	VDD_DUT
VDD5	D10	VDD_DUT
VDD6	A7	VDD_DUT
AVDDR	C5	VDD_DUT
AVDDT	F4	VDD_DUT
AVDDJ	E3	VDD_DUT
AVDDC	G3	VDD_DUT
REFCLK	H1	REFCLK70
CLKO	G2	CLKO
NC	D6	

I1
ND1
DS3170
U7
DS3170_BGA_U

TLCLK	B7	TLCLK70
TPOS/TDAT	E9	TPOS_70
TNEG	D9	TNEG_70
TXP1	E1	TXP_70
TXP2	E2	
TXN1	F1	TXN_70
TXN2	F2	
RLCLK	A8	RLCLK70
RPOS/RDAT	F10	RPOS_70
RNEG/RLCV	F9	RNEG_70
RXP	A4	RXP_70
RXN	A3	RXN_70
TOH	C7	TOH70
TOHEN	E10	TOHEN70
TOHCLK	D7	TOHCLK70
TOHSOF	G9	TOHSOF70
ROH	B6	ROH70
ROHCLK	C9	ROHCLK70
ROHSOF	F8	ROHSOF70
TCLKI	C10	TCLKI70
TSOFI	A9	TSOFI70
TSER	B10	TSER70
TCLKO/TGCLK	B9	TCLKO70
TSOFO/TDEN	C8	TSOFO70
RSER	C6	RSER70
RCLKO/RGCLK	A6	RCLKO70
RSOFO/RDEN	B8	RSOFO70

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TITLE:	Page 2. DS3170 BGA	DATE:
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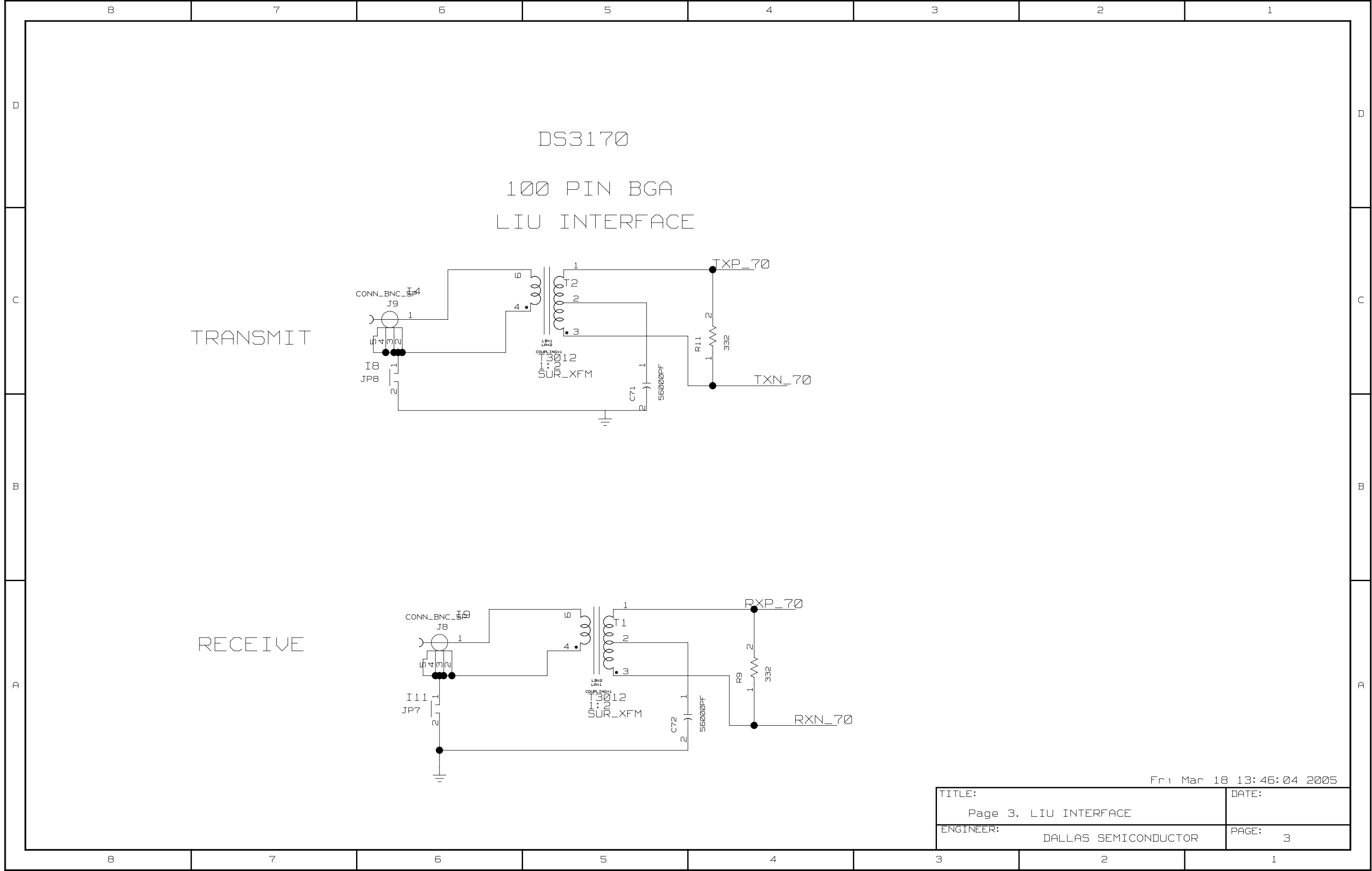
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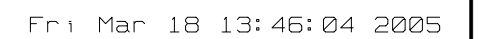


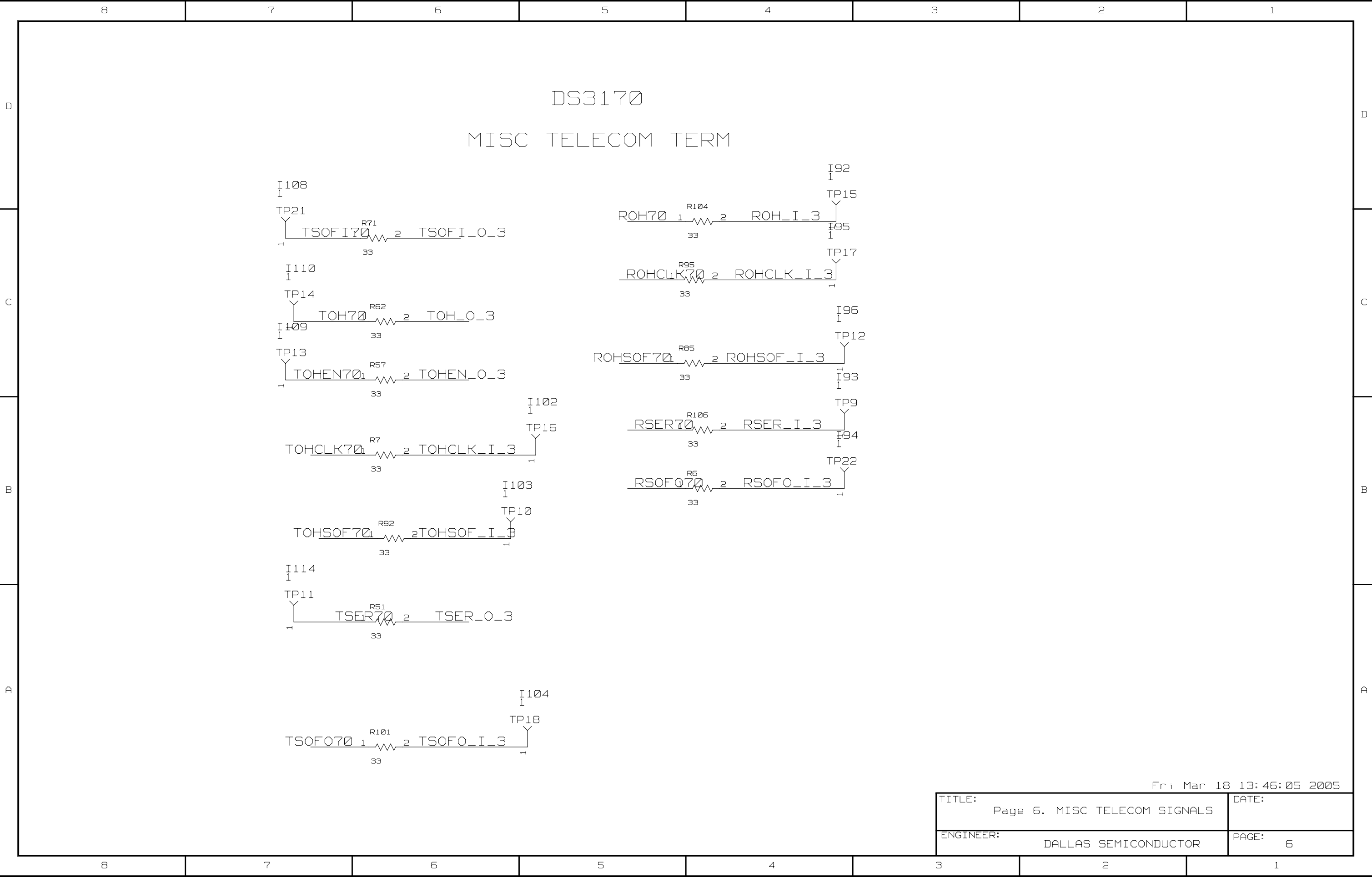
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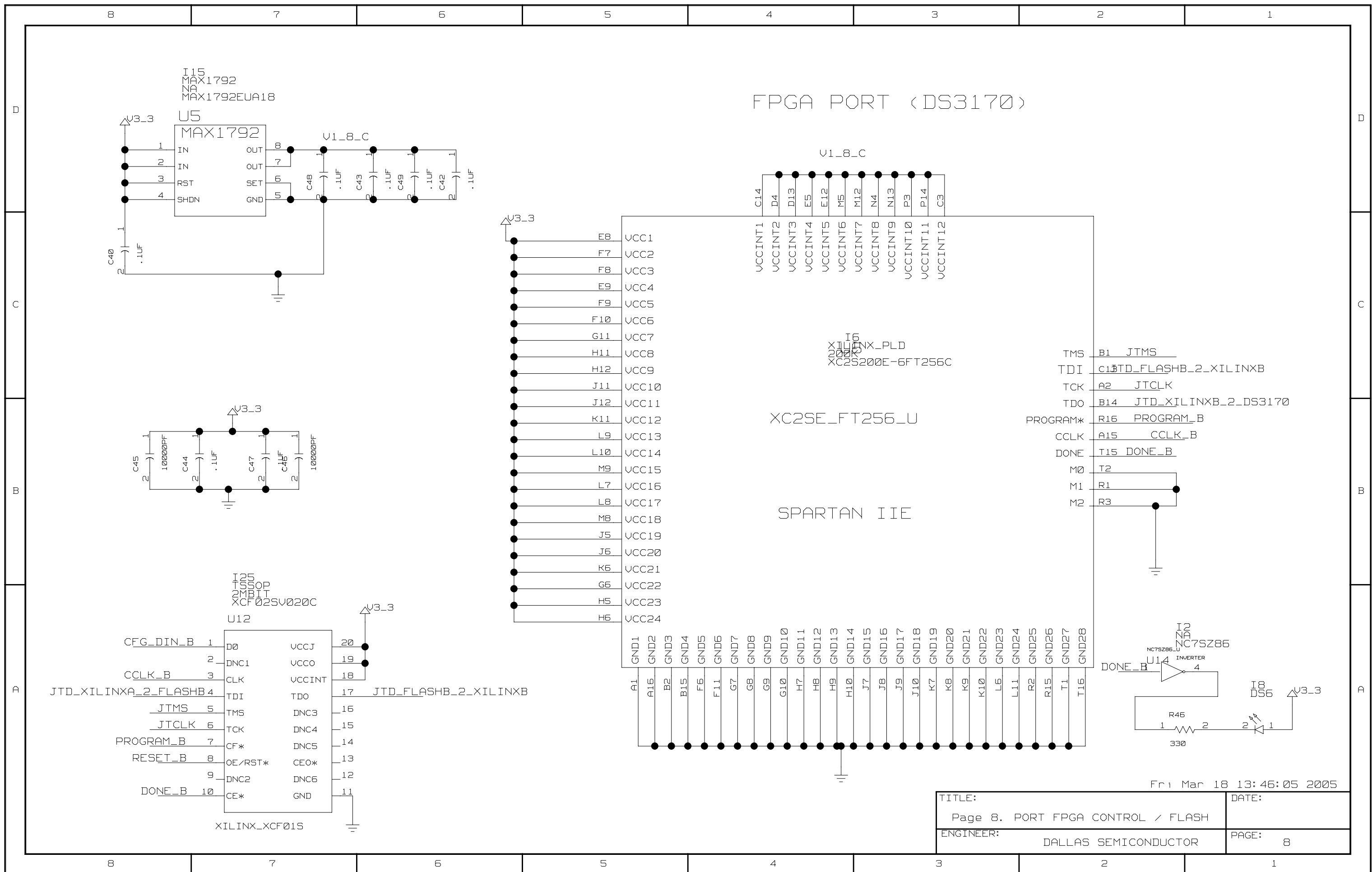
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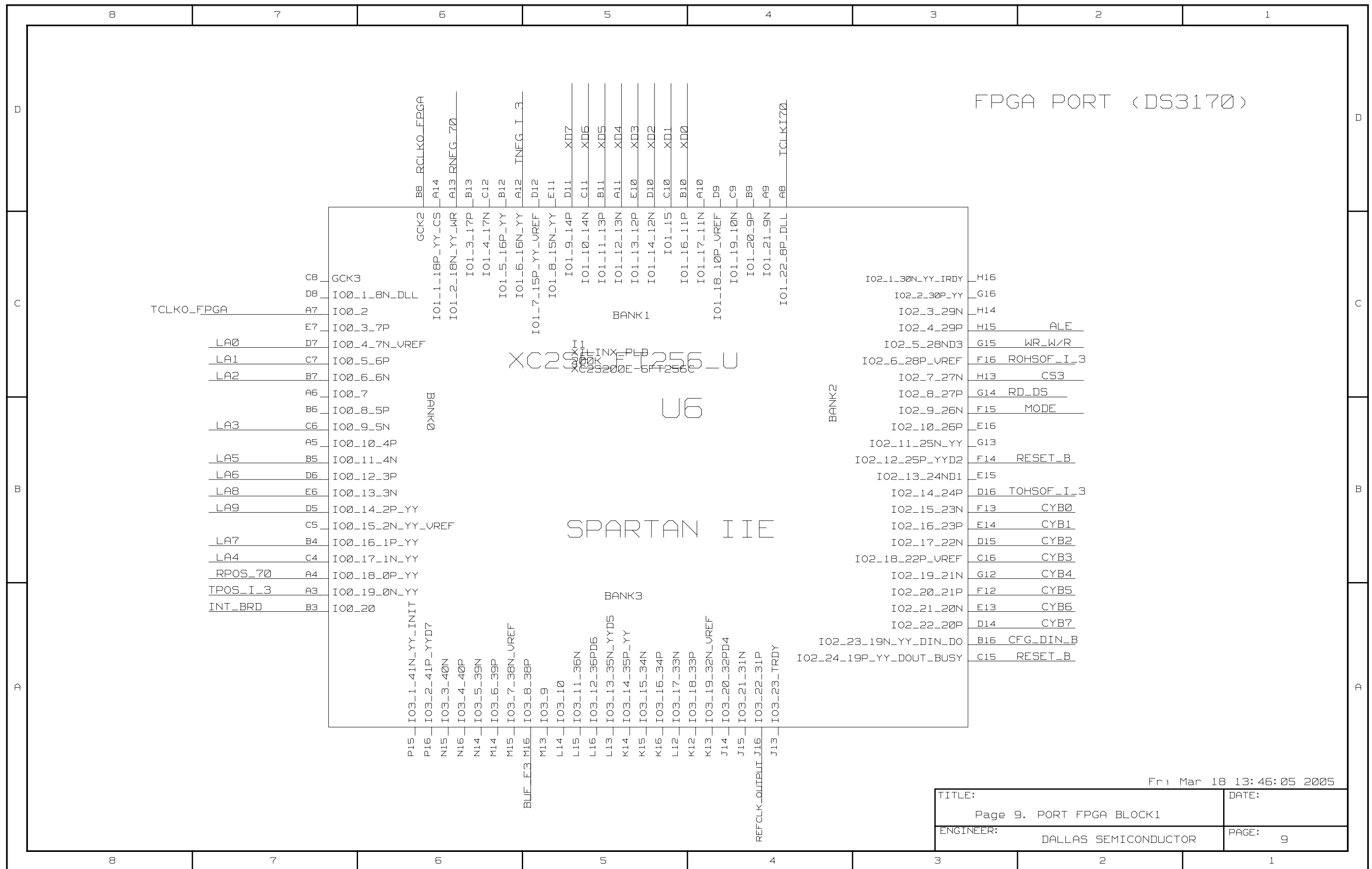


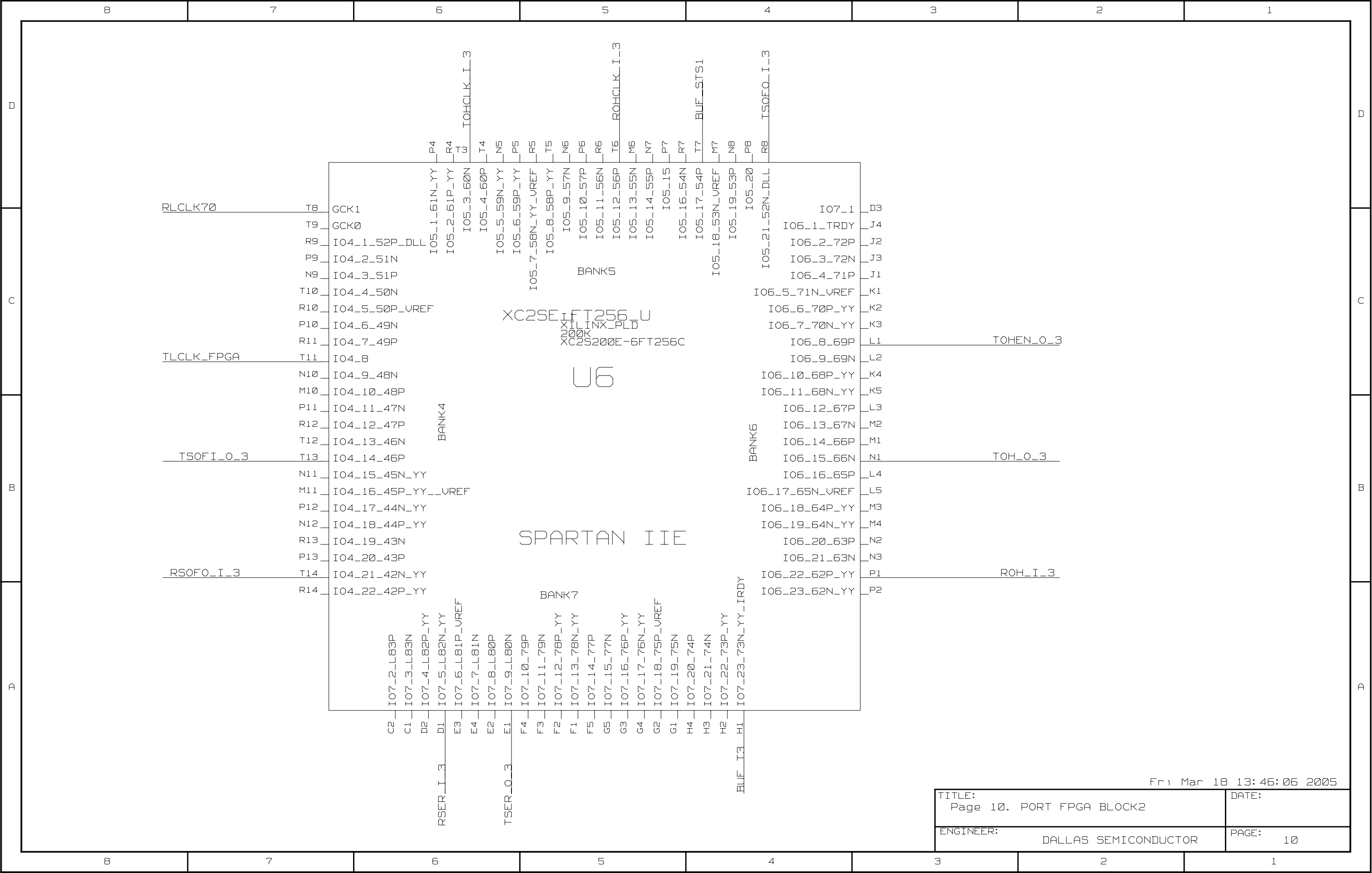
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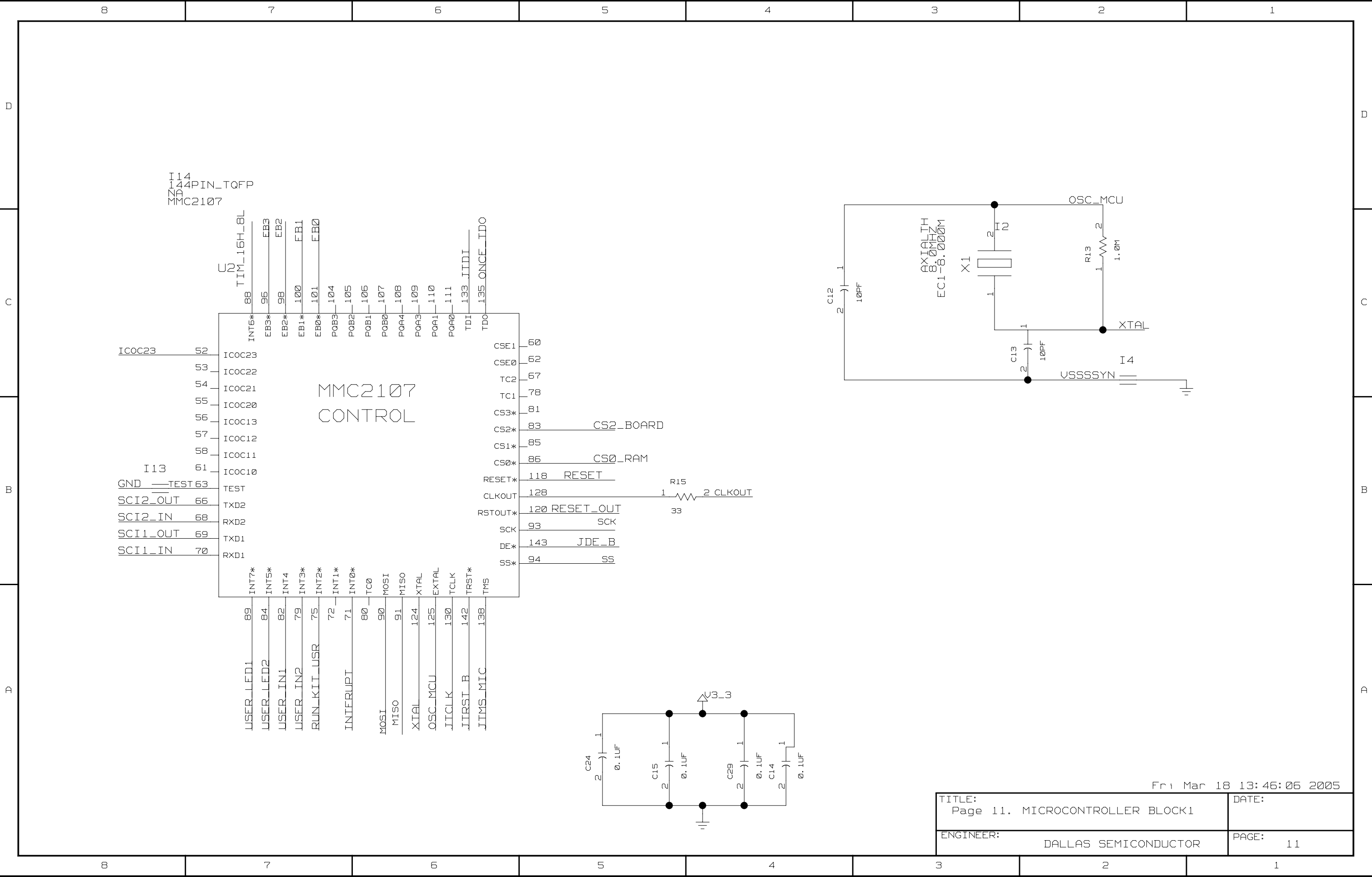
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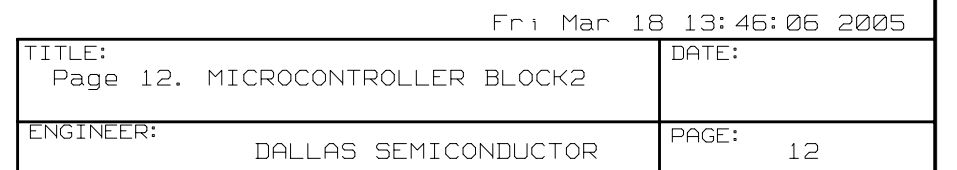


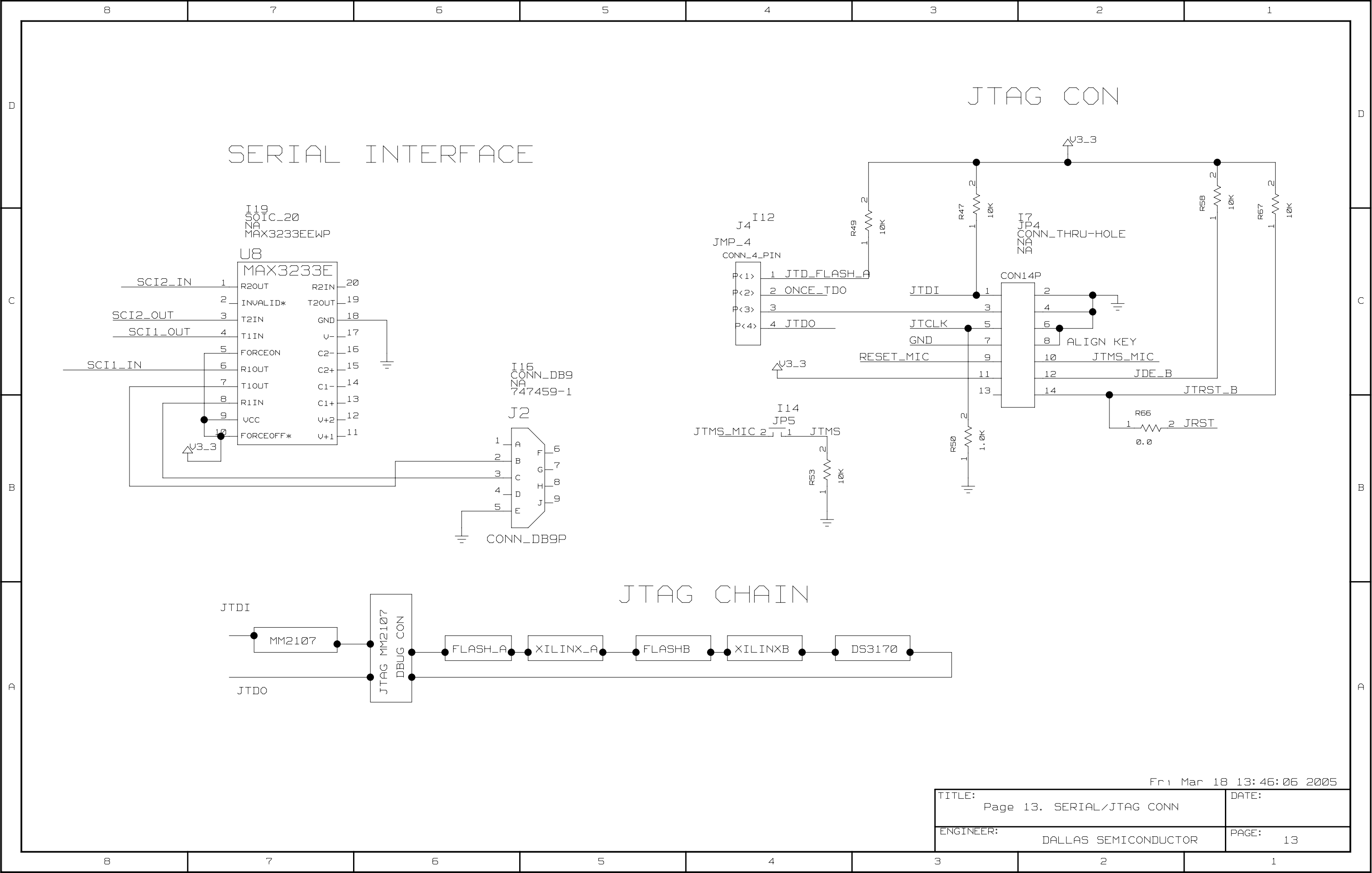




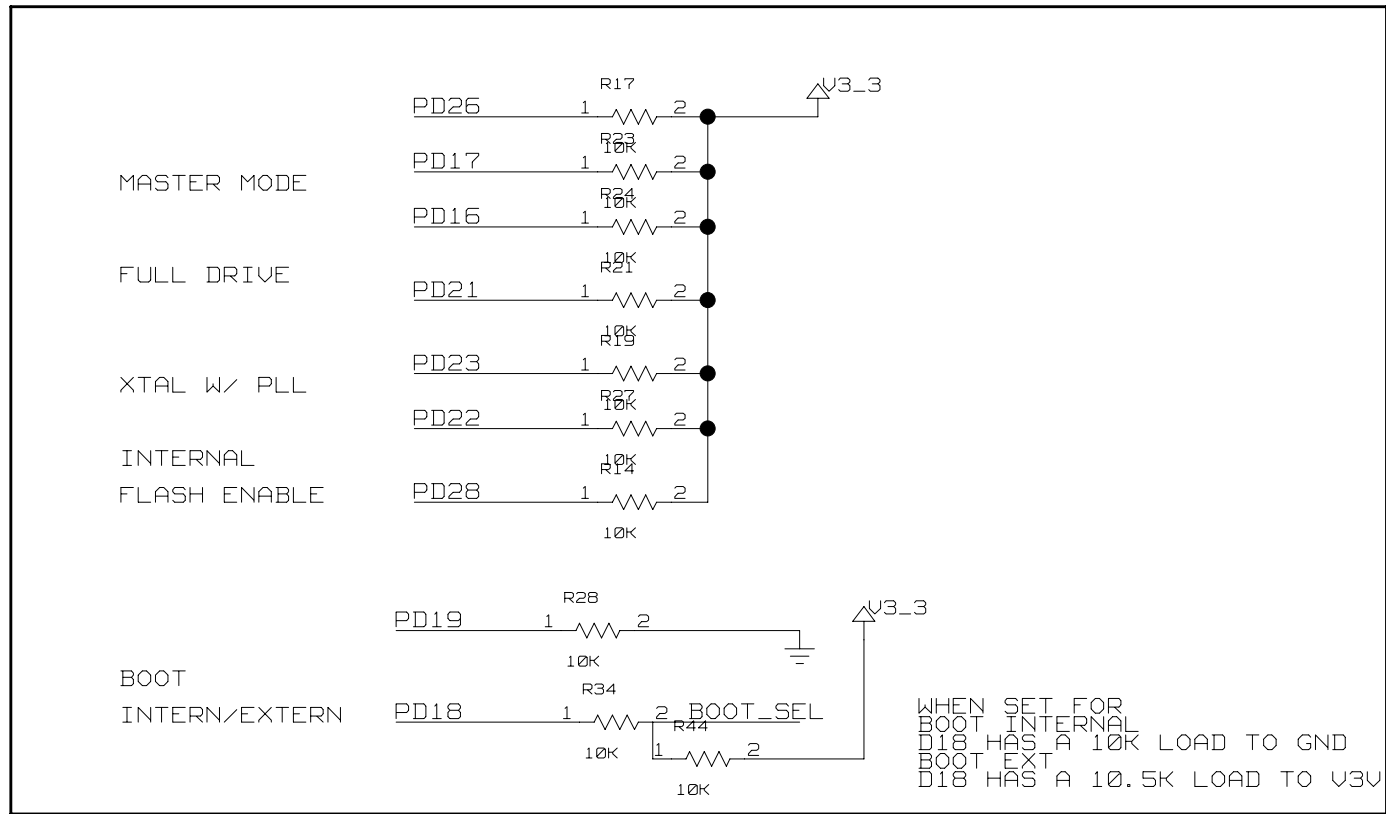
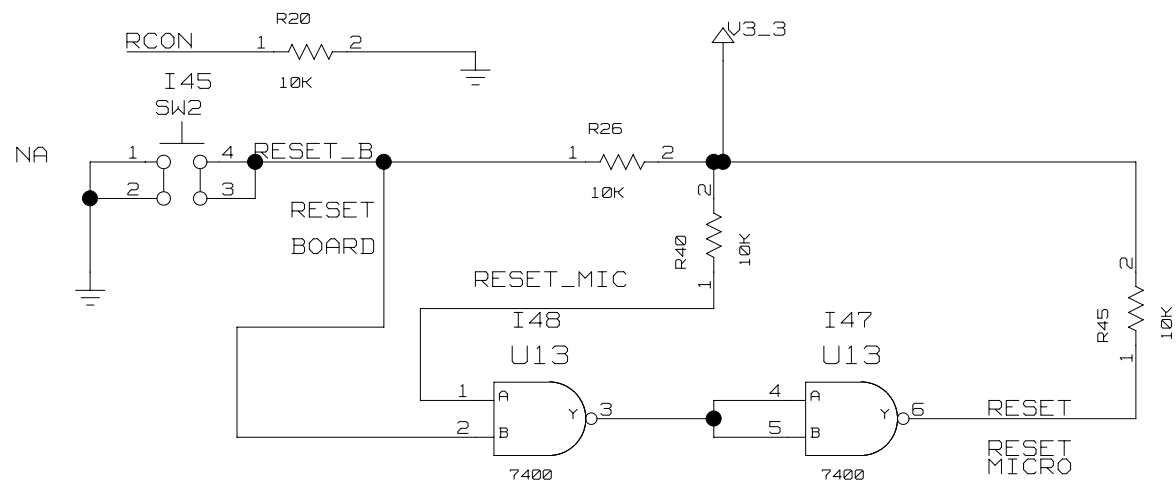
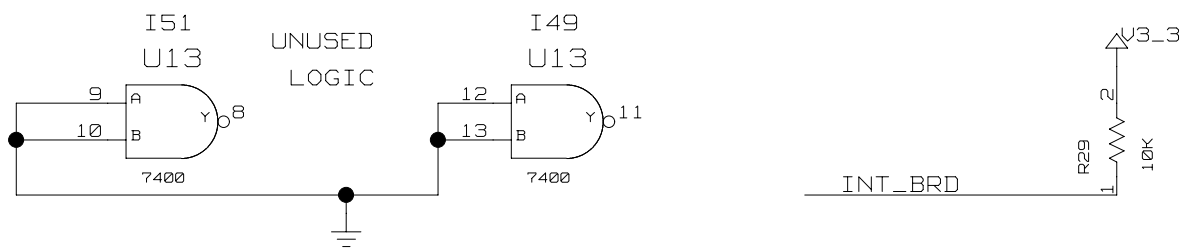
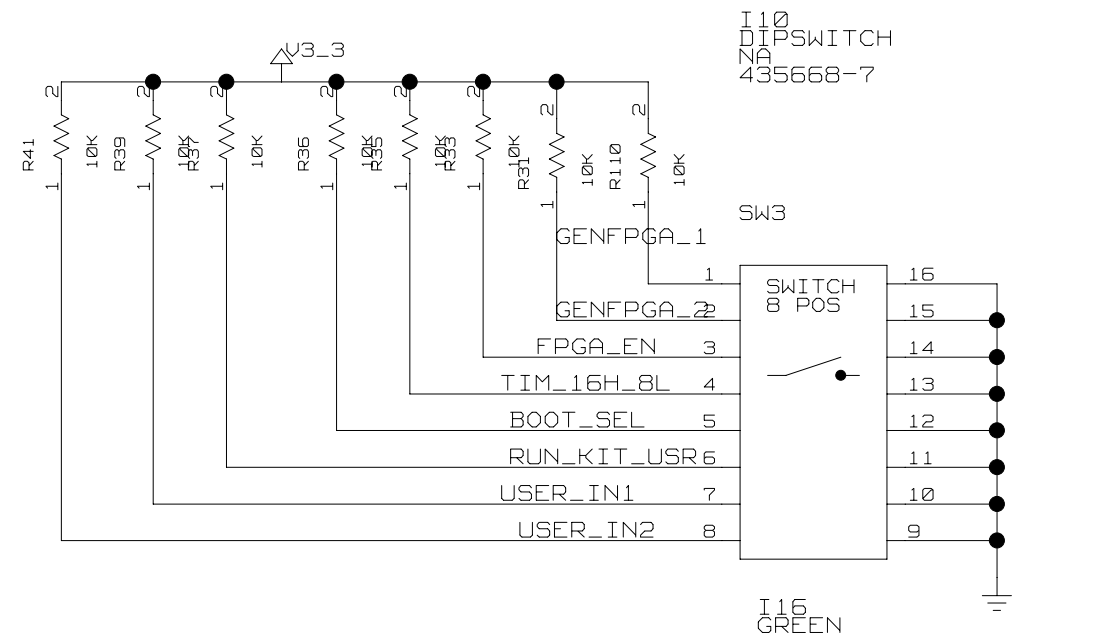
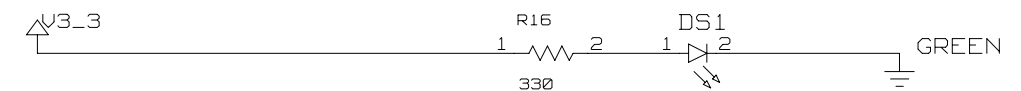
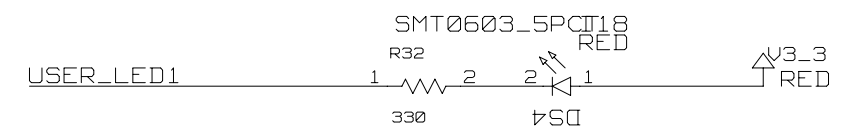
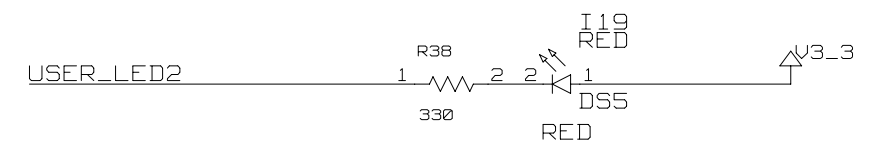
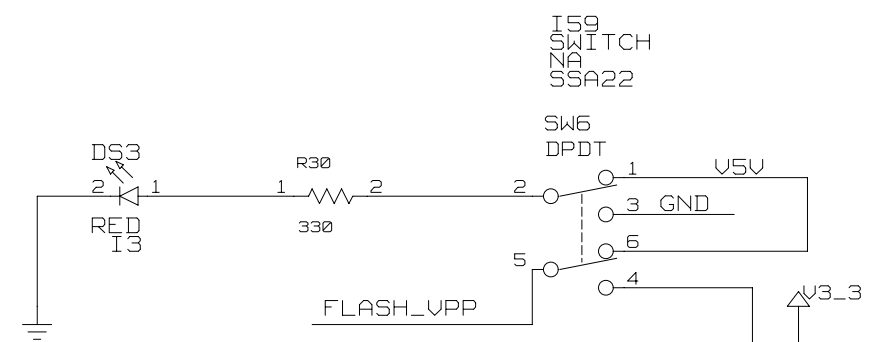






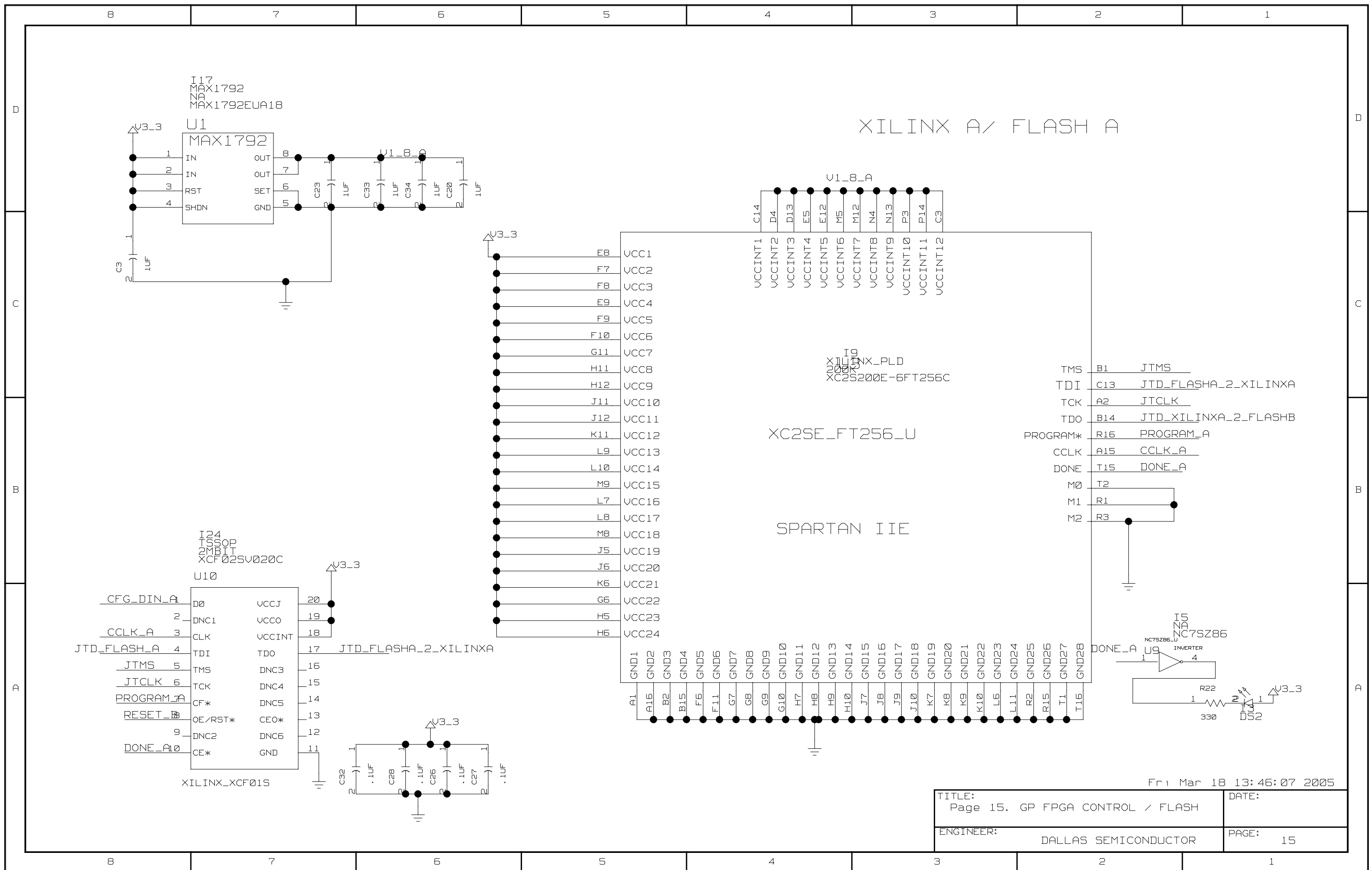


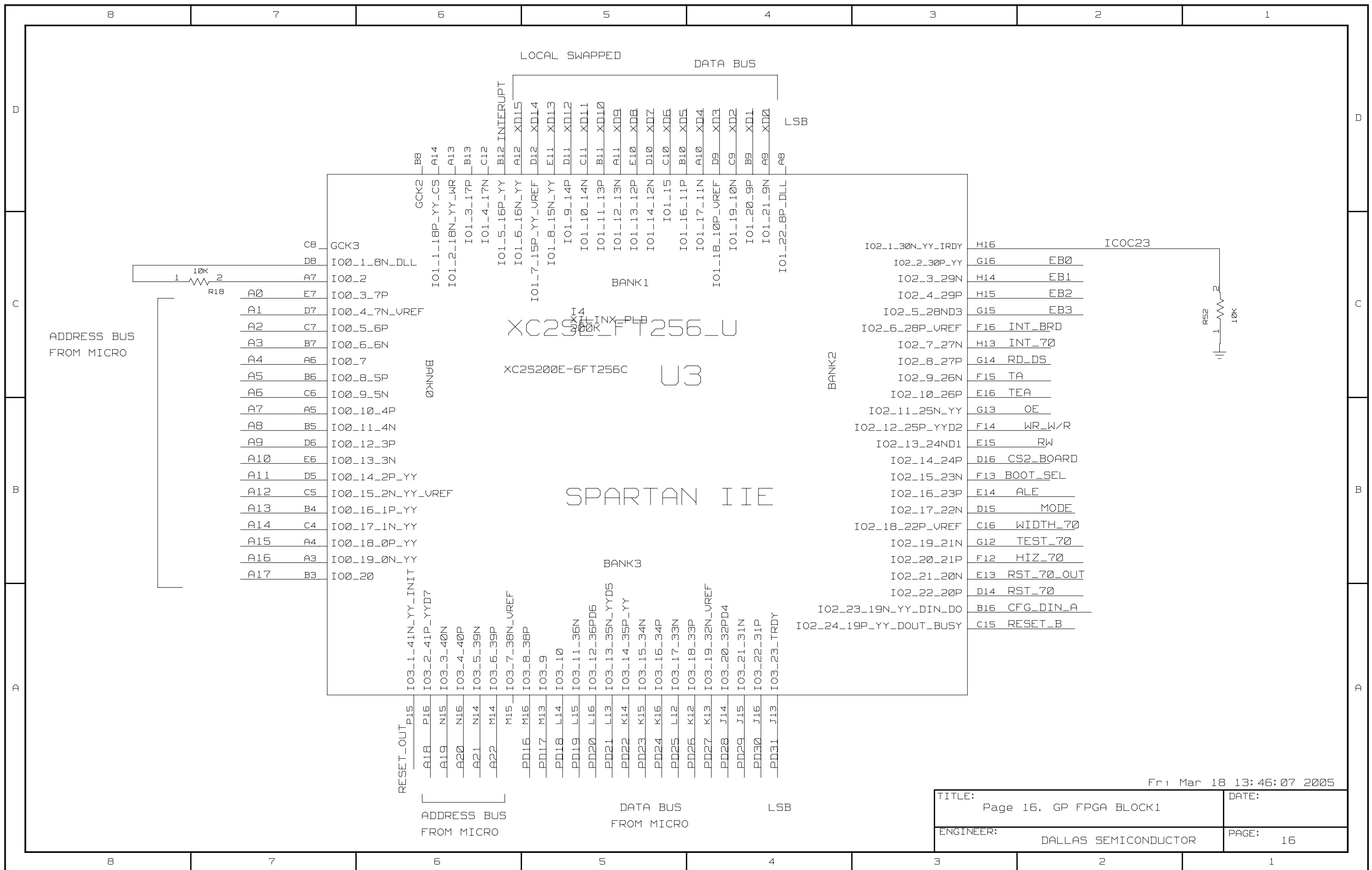
RESET CONFIGURATION

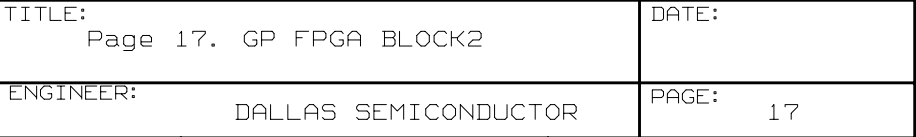


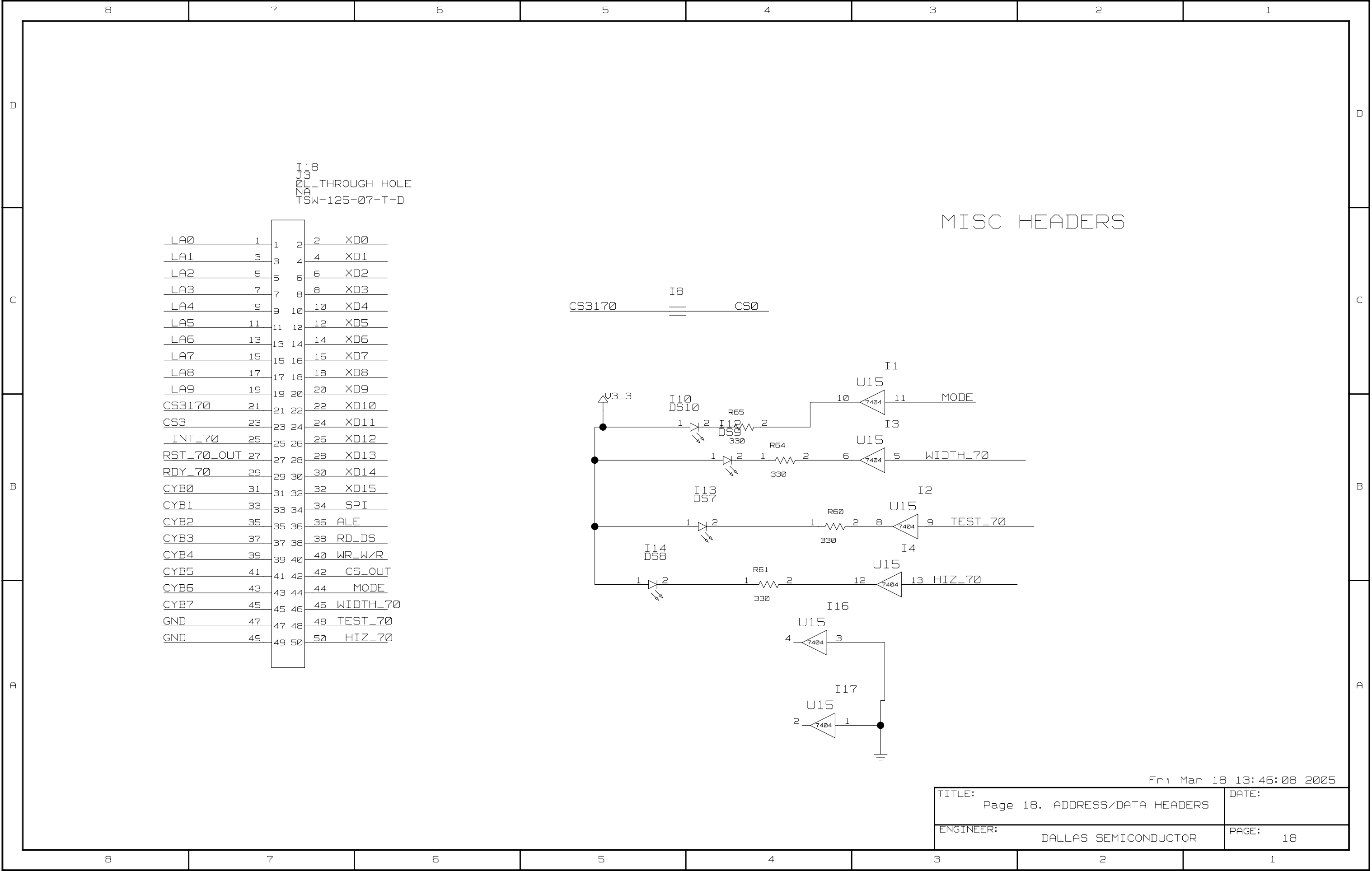
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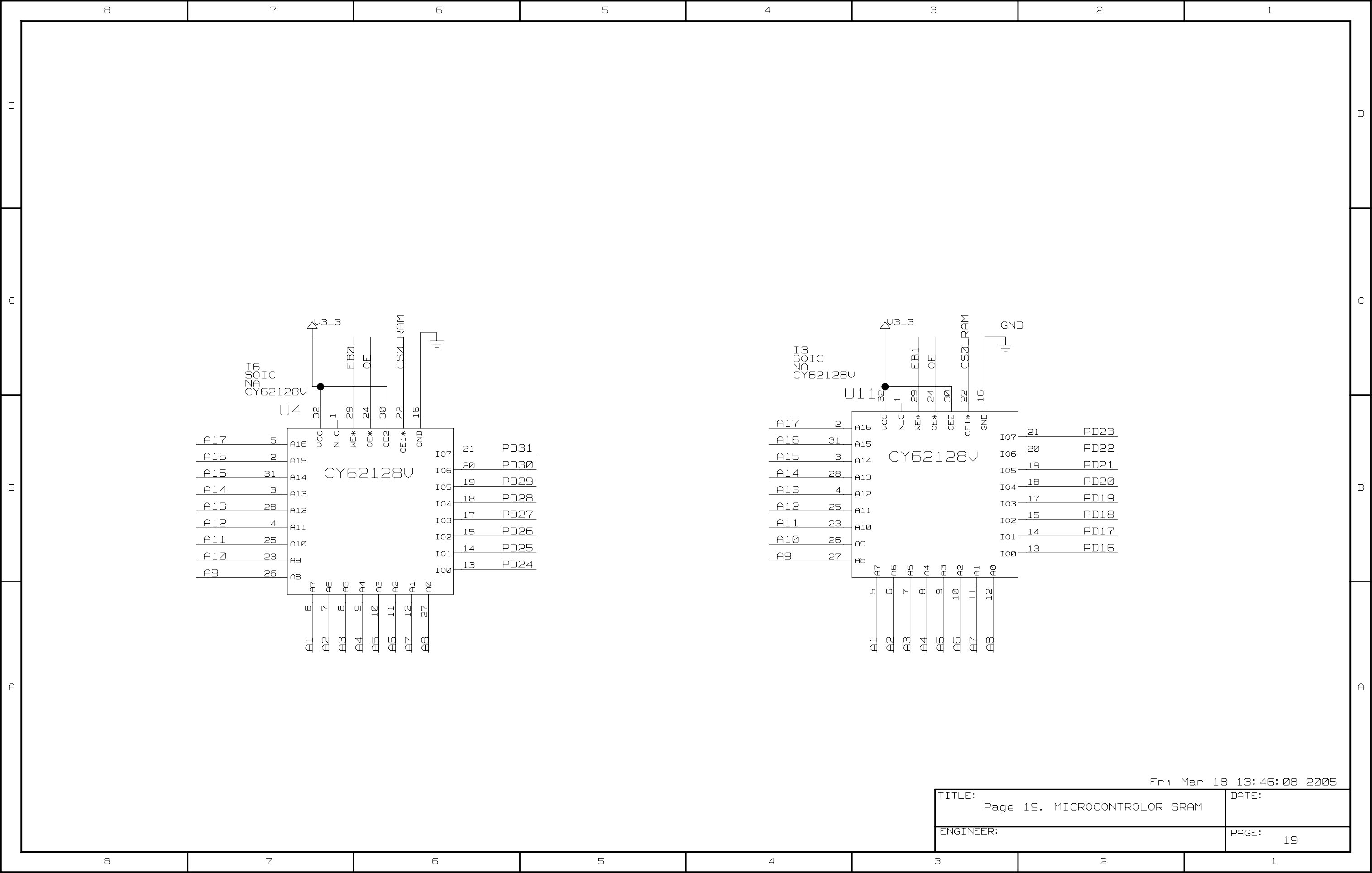
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Page 14. MISC USER INPUTS	
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DALLAS SEMICONDUCTOR	

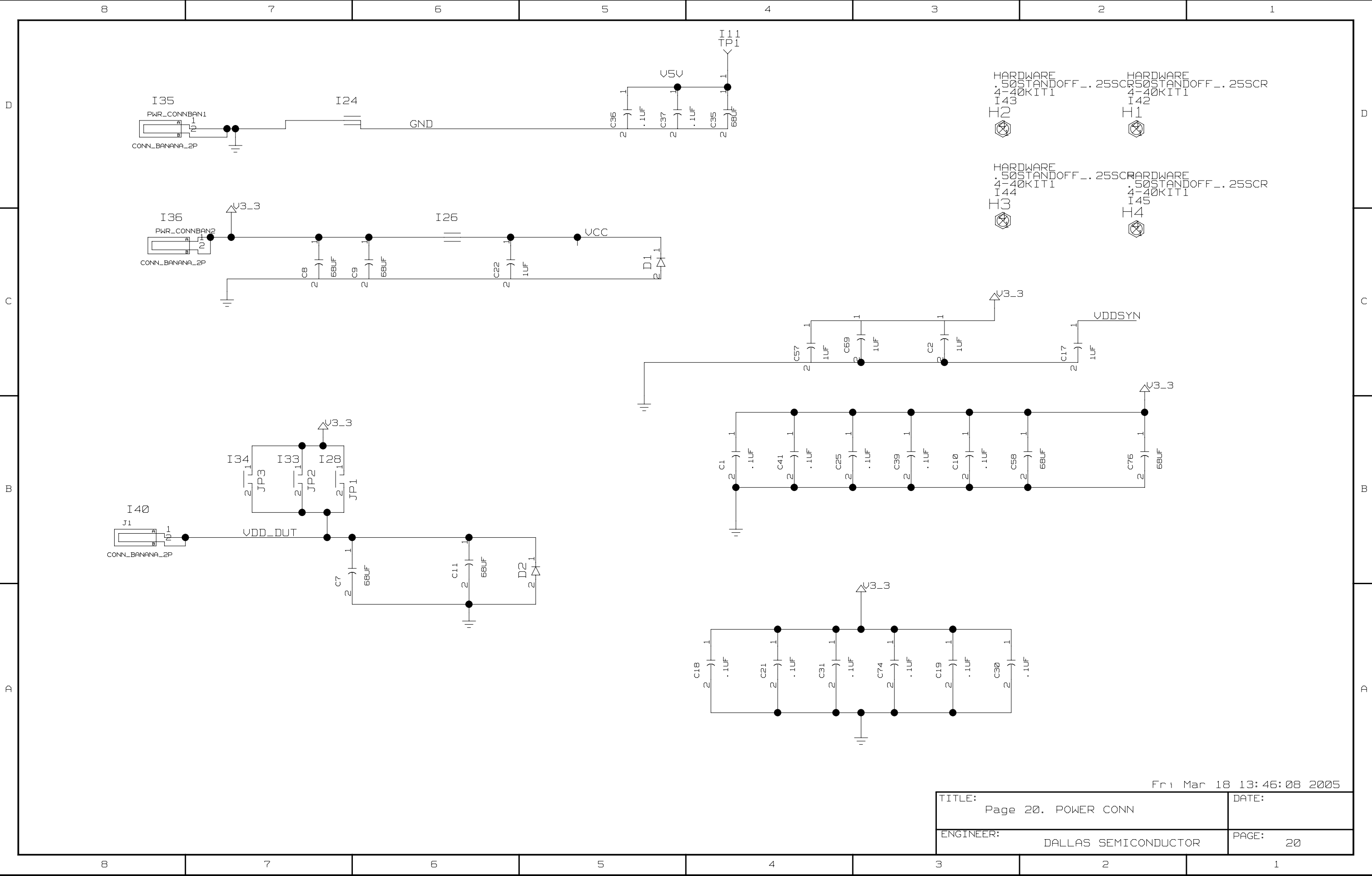












TITLE: Page 20. POWER CONN		DATE:	
ENGINEER: DALLAS SEMICONDUCTOR		PAGE: 20	

DESIGN NOTES:

1. 1/20/05 DESIGN / LAYOUT COMPLETED AND ARCHIEVED

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[illegible]

8			7			6			5			4			3			2			1							
D	*** Part Cross-Reference for the entire design ***																											D
	C1	CAP1	20B4	C76	CAP1	20B2	R32	RES1	14B2	R109	RES1	7C7																
	C2	CAP1	20C3	D1	DIODE	20C5	R33	RES1	14D3	R110	RES1	14D2																
	C3	CAP1	15C8	D2	DIODE	20B5	R34	RES1	14B6	SW1	PUSHBUTTON	5D8																
	C4	CAP1	2C8	DS1	LED	14C2	R35	RES1	14D3	SW2	PUSHBUTTON	14B8																
	C5	CAP1	2B2	DS2	LED	15A1	R36	RES1	14D3	SW3	SWITCH_8POS	14D2																
	C6	CAP1	2B1	DS3	LED	14A3	R37	RES1	14D4	SW4	SWITCH_8POS	5C1																
	C7	CAP1	20B7	DS4	LED	14B2	R38	RES1	14B2	SW5	PUSHBUTTON	5A4																
	C8	CAP1	20C7	DS5	LED	14B2	R39	RES1	14D4	SW6	SWITCH_DPDT_SLIDE_6P	14A2																
	C9	CAP1	20C6	DS6	LED	8A1	R40	RES1	14A6	T1	TRANSFORMER_PULSE	3A5																
C	C10	CAP1	20B3	DS7	LED	18B4	R41	RES1	14D4	T2	TRANSFORMER_PULSE	3C5																
	C11	CAP1	20B6	DS8	LED	18B5	R42	RES1	4B7	TP1	TESTPOINT1	20D4																
	C12	CAP	11C4	DS9	LED	18B4	R43	RES1	4A7	TP2	TESTPOINT1	4C3																
	C13	CAP	11C3	DS10	LED	18B5	R44	RES1	14B6	TP3	TESTPOINT1	4B3																
	C14	CAP1	11A4	DS11	LED	5C7	R45	RES1	14A5	TP4	TESTPOINT1	4A6																
	C15	CAP1	11A5	DS12	LED	5B7	R46	RES1	8A2	TP5	TESTPOINT1	4B7																
	C16	CAP1	2C8	DS13	LED	5B7	R47	RES1	13C3	TP6	TESTPOINT1	4A6																
	C17	CAP1	20C2	DS14	LED	5B7	R48	RES1	2A7	TP7	TESTPOINT1	4C3																
	C18	CAP1	20A4	DS15	LED	5C7	R49	RES1	13C3	TP8	TESTPOINT1	4A3																
	C19	CAP1	20A3	DS16	LED	5A7	R50	RES1	13B3	TP9	TESTPOINT1	6B4																
B	C20	CAP1	15D6	DS17	LED	5A7	R51	RES1	6A6	TP10	TESTPOINT1	6B6																
	C21	CAP1	20A4	DS18	LED	5C5	R52	RES1	16C1	TP11	TESTPOINT1	6A7																
	C22	CAP1	20C6	DS19	LED	5B5	R53	RES1	13B4	TP12	TESTPOINT1	6C4																
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	C24	CAP1	11A5	H2	4_40_HDWR_U	20D3	R55	RES1	7C2	TP14	TESTPOINT1	6C7																
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	C34	CAP1	15D6	J8	CONN_BNC_5P	3A6	R65	RES1	18B4	TP24	TESTPOINT1	7A7																
	C35	CAP	20D4	J9	CONN_BNC_5P	3C6	R66	RES1	13B2	U1	MAX1792	15D8																
	C36	CAP1	20D5	JP1	JMP	20B6	R67	RES1	13C1	U2	MMC2107	11C7 12C6																
	C37	CAP1	20D5	JP2	JMP	20B7	R68	RES1	4C6	U3	XC2SE_FT256_U	15C4 16C5 17B5																
	C38	CAP1	7B2	JP3	JMP	20B7	R69	RES1	7C1	U4	CY62128V	19B7																
	C39	CAP1	20B3	JP4	CON14P	13C3	R70	RES1	7C1	U5	MAX1792	8D8																
			JP5	JMP	13B4	R71	RES1	6C6	U6	XC2SE_FT256_U	8C4 9B5 10C5																	
			JP6	JMP3	5A2	R72	RES1	5C7	U7	DS3170_BGA_U	2C5																	
			JP7	JMP	3A6	R73	RES1	4C7	U8	MAX3233E	13C7																	
			JP8	JMP	3C6	R74	RES1	4C7	U9	NC7SZ86_U	15A2																	
			L1	COIL_2P	12C5	R75	RES1	5B2	U10	XILINX_XCF01S	15B7																	
			PWR_CONNBAN1	CONN_BANANA_2P	20D8	R76	RES1	5B2	U11	CY62128V	19B4																	
			PWR_CONNBAN2	CONN_BANANA_2P	20C8	R77	RES1	5C7	U12	XILINX_XCF01S	8A7																	
			R1	RES1	7D2	R78	RES1	5B7	U13	74_00	14A6 14A7 14A8																	
			R2	RES1	7C2	R79	RES1	5B7	U14	NC7SZ86_U	8A2																	
			R3	RES1	4B4	R80	RES1	5A7	U15	74_04	18A4 18B3 18C3																	
			R4	RES1	4A4	R81	RES1	7B7	U16	NC7SZ86_U	7B5																	
			R5	RES1	4C3	R82	RES1	5B2	U17	NC7SZ86_U	7C5																	
			R6	RES1	6B4	R83	RES1	4B4	U18	NC7SZ86_U	4C7																	
			R7	RES1	6B6	R84	RES1	7B7	U19	NC7SZ86_U	7C5																	
			R8	RES1	4A7	R85	RES1	6C5	U20	NC7SZ86_U	7C3																	
			R9	RES1	3A4	R86	RES1	5B3	U21	74_04	5A7 5B8 5D2 5D3																	
			R10	RES1	7A7	R87	RES1	5C3	U22	MAX6816	5A3																	
			R11	RES1	3C4	R88	RES1	7C4	U23	NC7SZ86_U	7C5																	
			R12	RES1	7C4	R89	RES1	5B5	U24	74_04	5A7 5B5 5B8 5C5 5C8																	
			R13	RES1	11C2	R90	RES1	5C5	X1	XTAL	11C3																	
			R14	RES1	14C6	R91	RES1	5A7	Y1	OSC2	7C8																	
			R15	RES1	11B5	R92	RES1	6B6	Y2	OSC2	7D8																	
			R16	RES1	14C2	R93	RES1	4A4	Y3	OSC2	7C8																	
			R17	RES1	14D6	R94	RES1	4C3																				
			R18	RES1	16C7	R95	RES1	6C5																				
			R19	RES1	14C6	R96	RES1	5A7																				
			R20	RES1	14B7	R97	RES1	7C5																				
			R21	RES1	14C6	R98	RES1	5C2																				
			R22	RES1	15A1	R99	RES1	5C2																				
			R23	RES1	14D6	R100	RES1	4A7																				
			R24	RES1	14D6	R101	RES1	6A6																				
			R25	RES1	5D7	R102	RES1	5C2																				
			R26	RES1	14B6	R103	RES1	4C7																				
			R27	RES1	14C6	R104	RES1	6C4																				
			R28	RES1	14C6	R105	RES1	7D7																				
			R29	RES1	14A5	R106	RES1	6B4																				
			R30	RES1	14A3	R107	RES1	7C4																				
			R31	RES1	14D3	R108	RES1	5A4																				
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