

TLK1221 Ethernet Transceiver Evaluation Module (EVM)

The Texas Instruments TLK1221 SERDES Evaluation Module (EVM) board is used to evaluate the TLK1221 device (40-pin 6-mm × 6-mm QFN PowerPAD™) for point-to-point data transmission applications. The board enables the system designer to connect 50-Ω parallel buses to both transmitter and receiver connectors. Using high-speed PLL technology, the TLK1221 serializes and transmits data along one differential pair. The receiver portion of the device de-serializes and presents data on the parallel bus. The high-speed (up to 1.3 Gbps) data lines interface to four 50-Ω controlled-impedance SMA connectors.

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1 Introduction

The Texas Instruments (TI) TLK1221 SERDES Evaluation Module (EVM) board is used to evaluate the TLK1221 device (40-pin 6-mm x 6-mm QFN PowerPAD). The board enables the designer to connect 50- Ω parallel buses to both the transmitter and receiver parallel connectors. Using high-speed PLL technology, the TLK1221 serializes data and transmits this data along a differential pair. The receiver part of the device de-serializes and presents the data on the parallel bus. For proper use of this device, users must provide dc-balanced encoded data on the parallel bus (that is, 8b/10b). The high-speed (up to 1.3 Gbps) data lines interface to four 50- Ω controlled-impedance SMA connectors. The board can be used to evaluate device parameters while acting as a guide for high-speed board layout. The evaluation board can be used as a daughter board that is plugged into new or existing designs. Since the TLK1221 operates over a wide range of frequencies, the system designer will need to optimize the design for the frequency of interest. Additionally, the designer may wish to use buried transmission lines and provide additional noise attenuation and EMI suppression to optimize the end product.

As the frequency of operation increases, the board designer must take special care to ensure that the highest signal integrity is maintained. To achieve this, the board's impedance is controlled to 50 Ω for both the high-speed differential serial and parallel data connections. In addition, board impedance mismatches are reduced by designing the component pad size to be as close as possible to the width of the connecting transmission lines. Vias are minimized and, when necessary, placed as close as possible to the device drivers. Since the board contains both serial and parallel transmission lines, care was taken to control both impedance and trace-length mismatch (board skew) to less than ± 1 MIL.

Overall, the board layout is designed and optimized to support high-speed operation. Thus, understanding impedance control and transmission-line effects is crucial when designing a high-speed board.

Some of the advanced features offered by this board include:

- PCB (printed-circuit board) is designed for high-speed signal integrity.
- SMA and parallel fixtures are easily connected to test equipment.
- All input/output signals are accessible for rapid prototyping.
- Analog and digital power planes can be supplied through separate banana jacks for isolation, or can be combined by placing jumpers on the supplied header pins.
- Onboard capacitors provide AC coupling of high-speed signals.

2 TLK1221 EVM Kit Contents

The TLK1221 EVM kit contains the following:

- TLK1221 EVM board
- TLK1221 EVM User's Guide (this document)

3 TLK1221 EVM Board Configuration

The TLK1221 EVM board gives the developer various options for operation, many of which are jumper-selectable. Other options can be either soldered into the EVM or connected through input connectors.

The TX and RX parallel connectors, (JMP6), of [Figure 1](#), provide a connection for both transmitted and received parallel data busing. The reference clock is supplied through SMA connector J5 and the high-speed serial data is transmitted through SMA connectors J1 and J2. The received recovered clocks (RBC0 and RBC1) are output through pins on the header JMP8 along with the SYNC pin. Received data connects through SMA connectors J3 and J4 of the board. Header JMP7 provides static control signals (normally pulled high) to configure the device for different modes of operation.

The power planes are split three ways to provide power to different parts of the board. This prevents coupling of switching noise between the analog and digital sections of the TLK1221, and provides voltage isolation for power consumption testing. The VDD, VDDA, and VDDPLL connectors require a nominal 2.5V and are joined together by removable jumpers on headers JMP9 and JMP10 that are installed in the default configuration. Thus only the VDD connection is necessary to energize the TLK1221 device in the default configuration. In all sections of the board, the ground planes are common and each ground plane is tied together at every component ground connection. See the Schematics and Board Layouts for detailed schematic and layout information.

The board is normally delivered in a default configuration that only requires power as well as an external clock and data inputs. The TLK1221 is shipped with jumpers for default operation. Table 1 shows the default configuration for sending data.

The parallel signals on the TLK1221 EVM have been routed to a 0.1 inch header block that is configured as in Figure 1. All RD pins (RD[9:0]) on the header block (JMP6), as well as all TD pins (TD[9:0]) on the header block (JMP6) have matched trace lengths to themselves ± 1 MIL. Due to routing constraints RXD and TXD trace lengths are not matched to each other, but only to themselves.

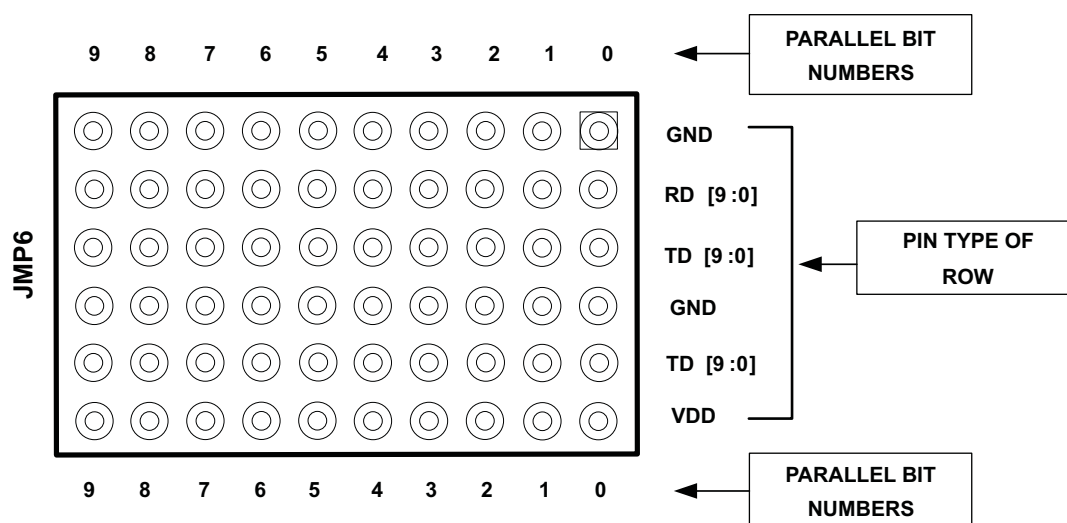


Figure 1. Parallel Signal Header Block

Parallel loop back, shown in Figure 2, can be easily implemented by placing jumpers on the RD/TD pins of the header. For example, placing a jumper on pins 2 and 3 of JMP6 will loop back TD[0] to RD[0].

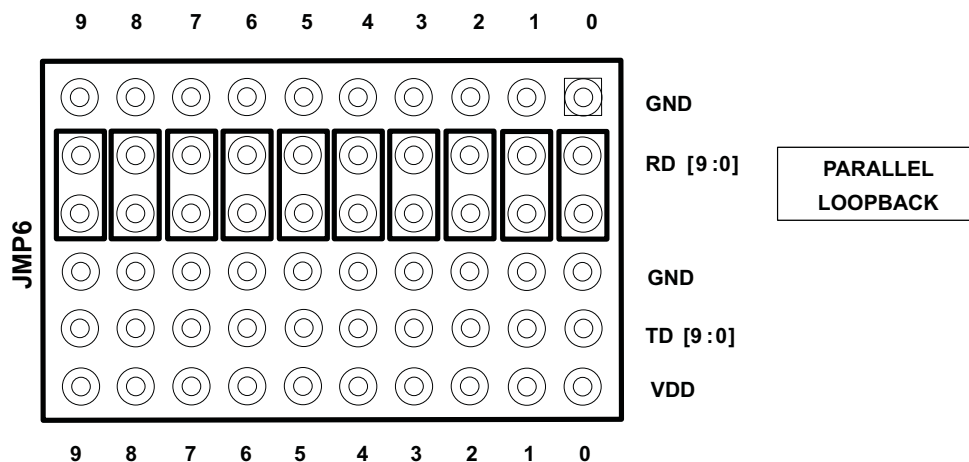


Figure 2. Parallel Signal Header Block

Additional GND and VDD pins have been added into the header block for several reasons. The GND pins

next to the RD and TD pins provide a convenient ground reference for a scope probe or coax cables. The additional TD row and VDD pins allow a static pattern to be driven into the TD bus by placing jumpers across either the TD and VDD pins for a HIGH, or TD and GND pins for a LOW eliminating the need for cables for quick tests. The extra row of TD can also be used to monitor the signals on the TD pins while simultaneously looping back into the RD pins. Figure 3 shows a clock pattern (01010101) on TD[9:0] being looped back onto the RD[9:0] pins.

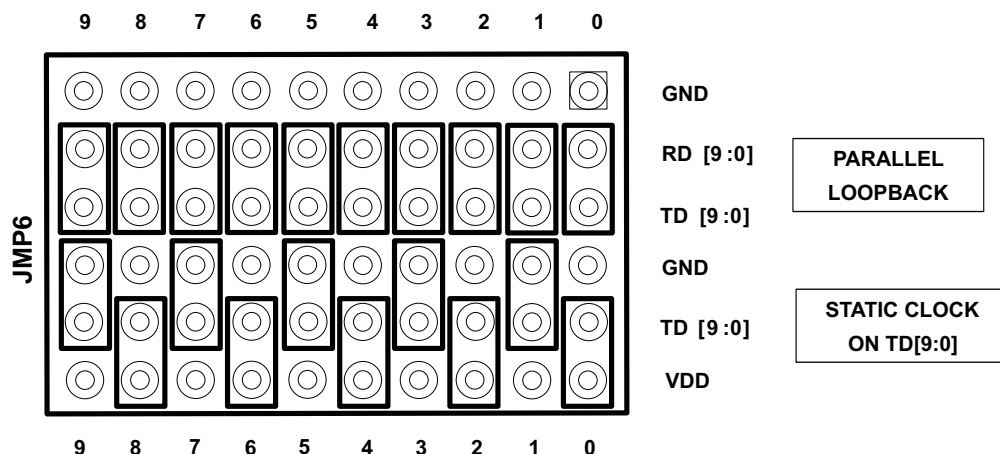


Figure 3. Parallel Loop Back with Static Data Pattern

Table 1. Default Transceiver – Board Configuration as Shipped

Designator	Function	Condition
JMP9	VDD and VDDPLL Bridge	Joins the VDD and VDDPLL power planes
JMP10	VDD and VDDA Bridge	Joins the VDD and VDDA power planes
JMP7	PRBSEN	Jumper installed (logic 0) – disables the TLK1221 PRBS internal production test mode
JMP7	SYNCEN	Jumper installed (logic 0) – disables the TLK1221 comma-detection circuitry
JMP7	ENABLE	Jumper not installed (logic 1) – this pulls up the enable pin for normal operation
JMP7	RBCMODE	Jumper not installed (logic 1) – for a 1/10 baud-rate clock on RBC0 (a non-DDR mode)
JMP7	LOOPEN	Jumper installed (logic 0) – disables the TLK1221 internal loopback mode
C1, C3	TX AC-Coupling Capacitors	These capacitors (normally installed) are provided to ac-couple the transmitted serial signal.
C2, C4	RX AC-Coupling Capacitors	These capacitors (normally installed) are provided to ac-couple the received serial signal.

Table 2. Configuration Changes Necessary for DC-Coupling of the High-Speed Signals

Designator	Function	Condition
C1, C3	TX AC-Coupling Capacitors	Remove capacitors and install 0-Ω resistors
C2, C4	RX AC-Coupling Capacitors	

4 Typical Test and Setup Configurations

This section presents the typical test and setup configuration used to evaluate and test the transceiver. The printed-circuit board construction and characteristics are included in chapter 5.

The following configurations are used to evaluate and test the TLK1221 transceiver. The first configuration is an external serial loopback of the high-speed signals shown in Figure 4. The serial loopback allows the system designer to evaluate most of the functions of the transmitter and receiver sections of the TLK1221 device. To test a system, a parallel Bit Error Rate Tester (BERT) generates a predefined DC-balanced parallel bit pattern. The pattern is connected to the transmitter through parallel connectors TD0-TD9

(TD0-TD4 for DDR mode). The TLK1221 device serializes and presents the data on the high-speed serial pair (TXP/TXN). The serial TX data is then looped back to the receiver side and the device de-serializes and presents the data on the receiver side RD0–RD9 (RD0–RD4 for DDR mode). The data is received by the BERT and compared against the transmitted pattern and monitored for valid data and errors. If any bit errors are received, a bit-error rate is evaluated at the parallel-receive BERT.

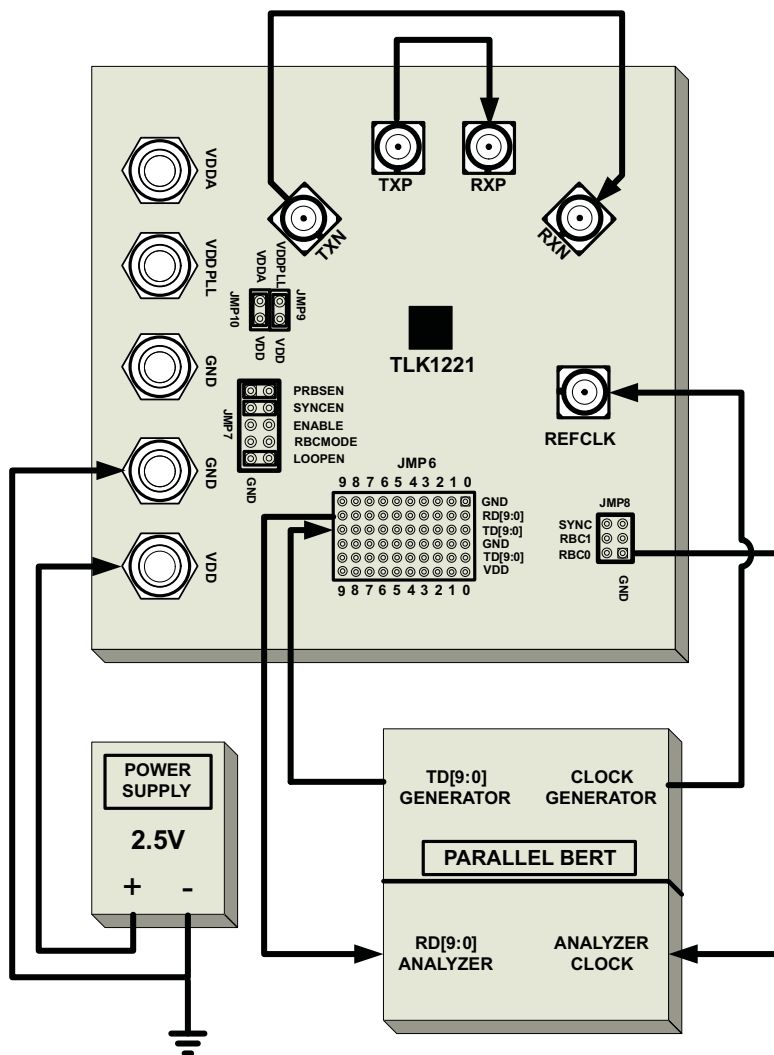


Figure 4. TLK1221 EVM External Serial Loopback Test Configuration

If a parallel data generator is not available, placing jumpers on the additional TD pins of the header block JMP6 will allow a static pattern to be received by the parallel TD bus, serialized, looped back into the serial receiver, and de-serialized where it can be viewed with an analyzer. However, unless the pattern jumpered onto the TD pins includes the comma pattern and the SYNCEN pin is high, the data will be unframed data and the values of the RD[9:0] pins may not be aligned with the corresponding TD[9:0] pins.

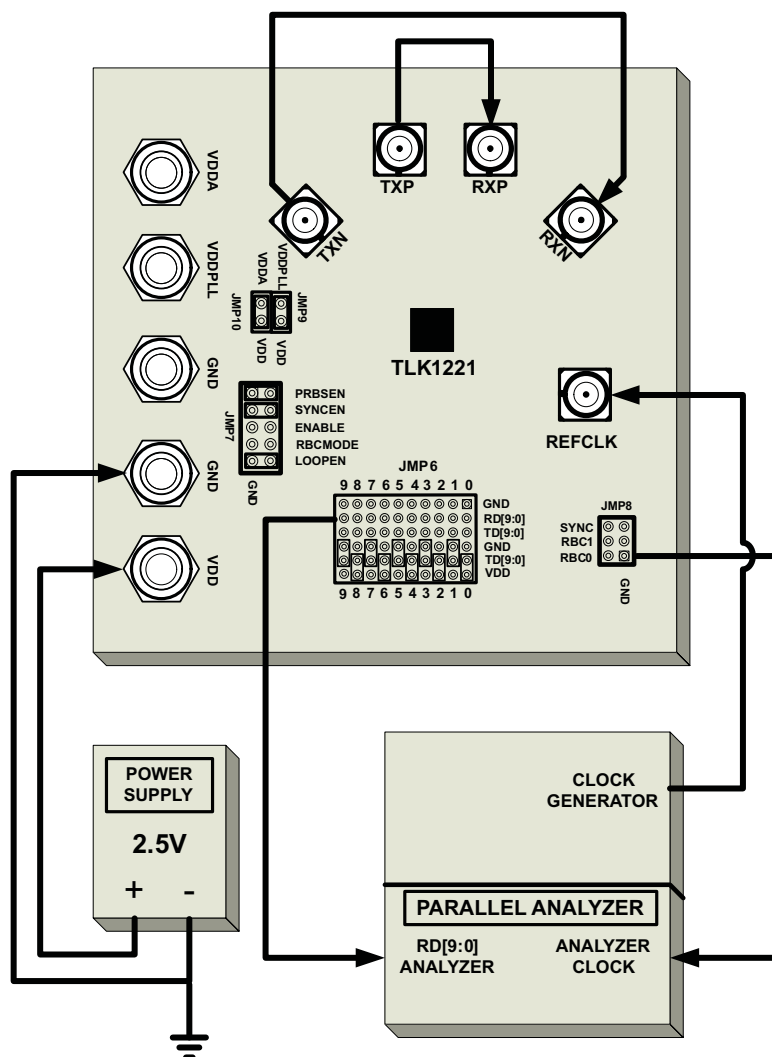


Figure 5. TLK1221 EVM Serial PRBS 2⁷-1 Self-Test Configuration

If a parallel BERT is not available, the system designer can take advantage of the built-in-test mode of the device, see [Figure 6](#). If the designer asserts the PRBSEN pin high, a Pseudo Random Bit Pattern will be transmitted. This pin also puts the receiver in a mode to detect a valid PRBS pattern. A valid pattern is indicated by the SYNC pin indicating high. This test only validates the high-speed serial portion of the device and the system interconnects. The PRBS pattern is compatible with most serial BERT test equipment. This function allows the operator to isolate and test the transmitter and receiver independently. A typical configuration is shown in [Figure 6](#). The dashed lines represent optional connections that can be made for monitoring eye patterns and measuring jitter.

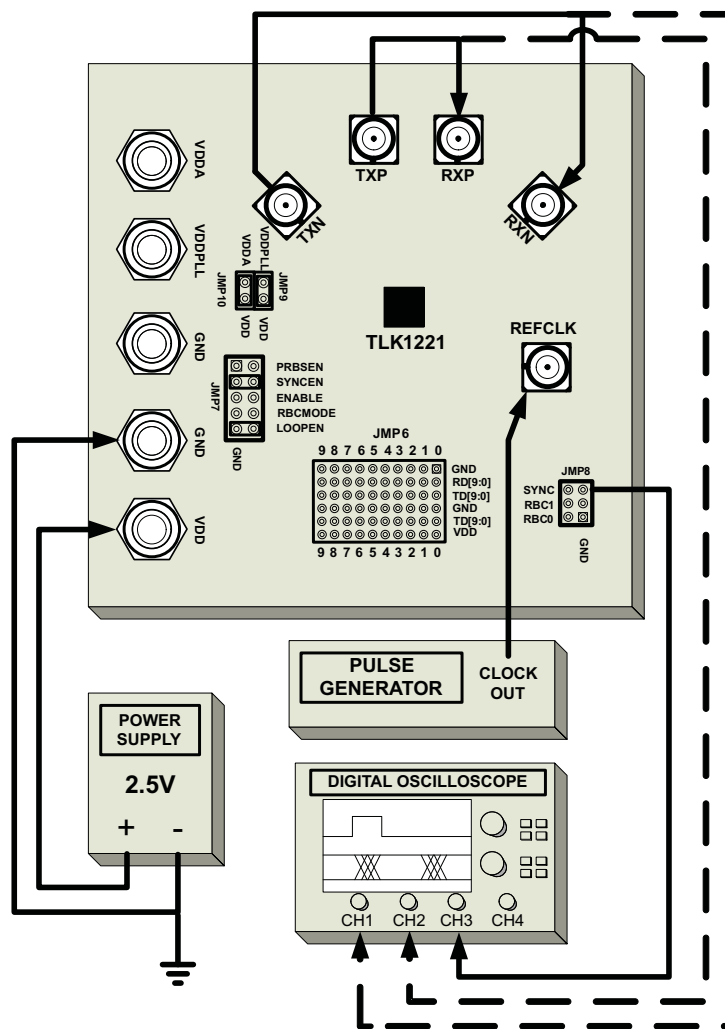


Figure 6. TLK1221 EVM Serial PRBS 2^7-1 Self-Test Configuration

If a serial BERT is available, the system designer can independently test both serial channels of the device with a PRBS 2^7-1 data pattern, see [Figure 7](#). If the designer asserts the PRBSEN pin high, a Pseudo Random Bit Pattern will be transmitted. This pin also puts the receiver in a mode to detect a valid PRBS pattern. A valid pattern is indicated by the SYNC pin indicating high. This test only validates the high-speed serial portion of the device and the system interconnects. The PRBS pattern is compatible with most serial BERT test equipment. This function allows the operator to isolate and test the transmitter and receiver independently. A typical configuration is shown in [Figure 7](#). The dashed lines represent optional connections that can be made for monitoring eye patterns and measuring jitter.

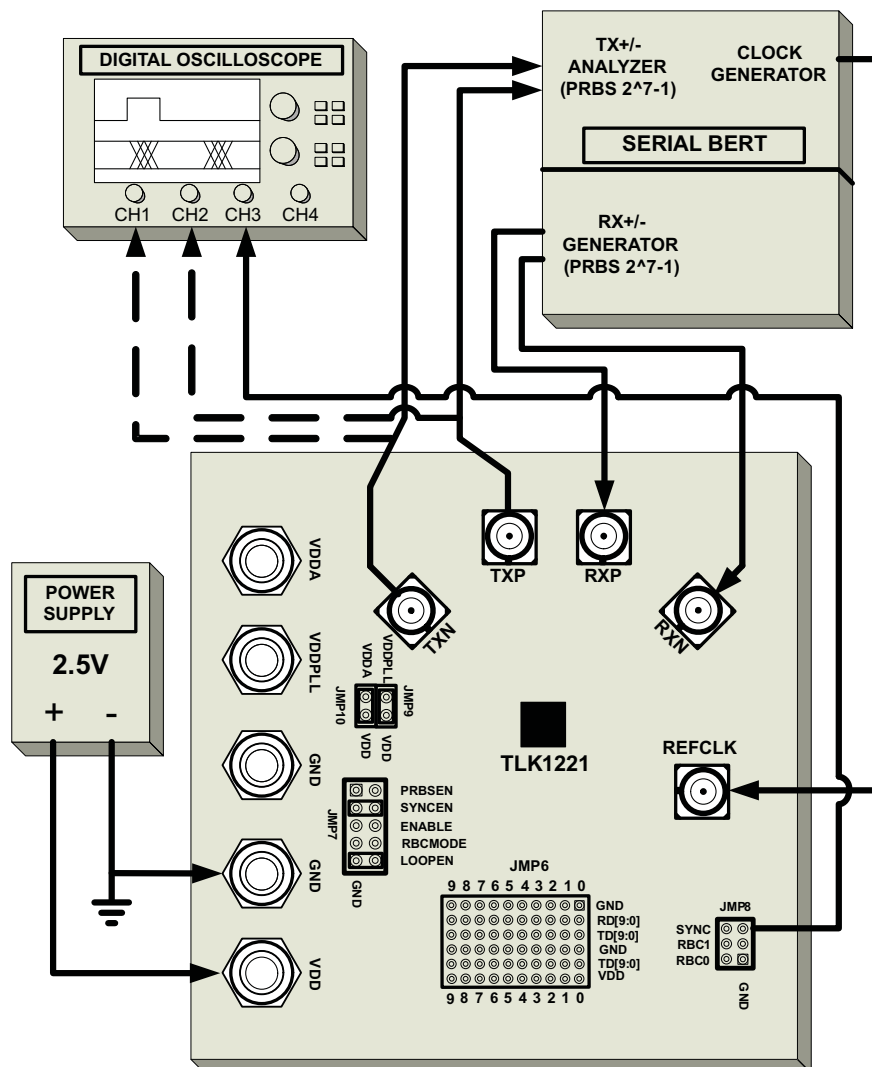


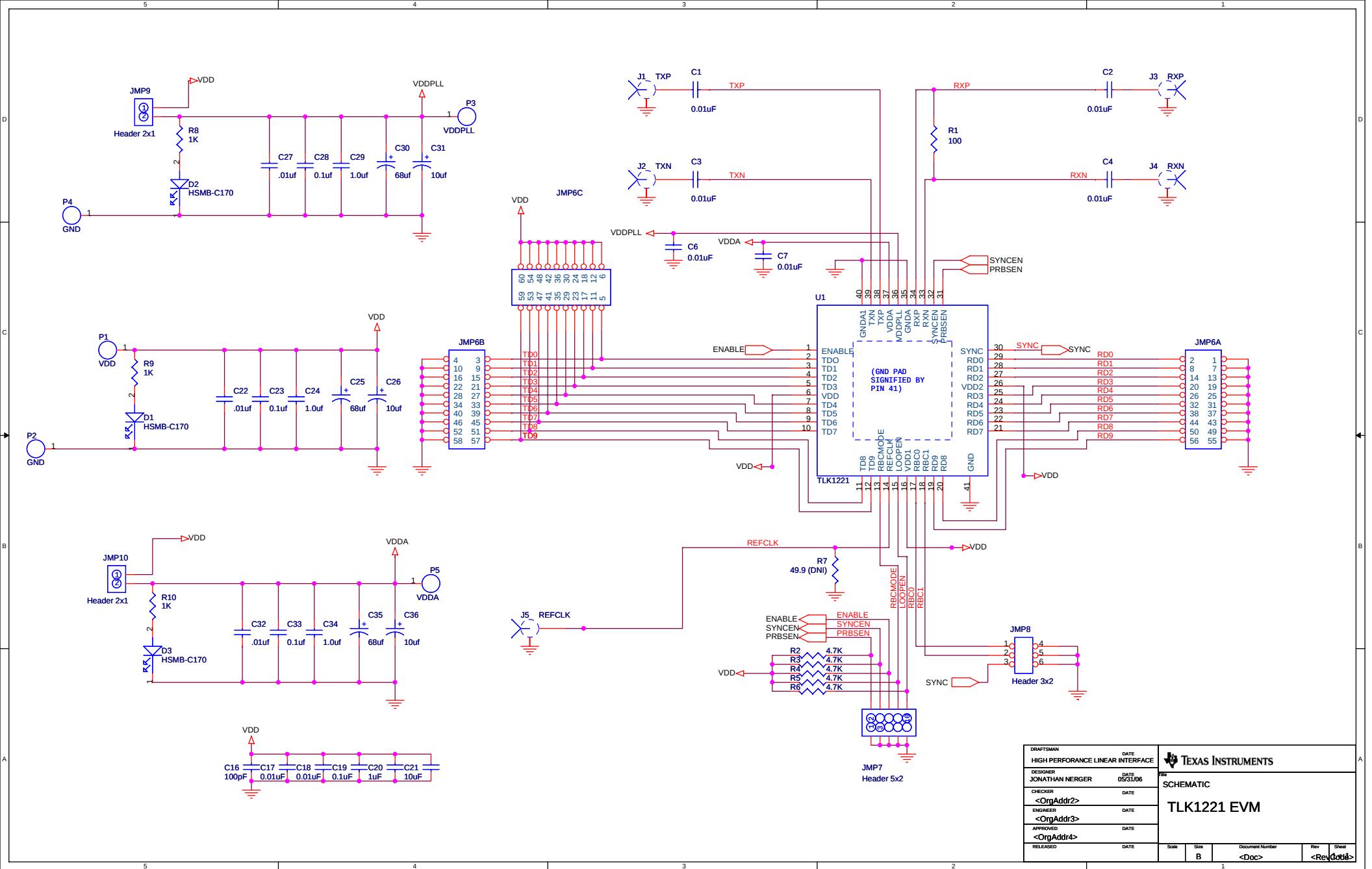
Figure 7. TLK1221 EVM Serial PRBS 2⁷-1 Test Configuration

5 Schematic, Bill of Materials, and Board Layouts

5.1 Schematic

Figure 8. TLK1221 EVM Schematic

The TLK1221 EVM schematic is shown on the following page.



DRAFTSMAN	DATE	 TEXAS INSTRUMENTS
HIGH PERFORMANCE LINEAR INTERFACE	05/31/06	
DESIGNER	DATE	
JONATHAN NERGER	05/31/06	
CHECKER	DATE	
<OrgAddr2>	DATE	SCHEMATIC
ENGINEER	DATE	
<OrgAddr3>	DATE	
APPROVED	DATE	
<OrgAddr4>	DATE	TLK1221 EVM
RELEASED	DATE	

Scale	Size	Document Number	Rev	Sheet
B	B	<Doc>	<Rev>	<Total>

5.2 Bill of Materials

Table 3. TLK1221 EVM Bill of Materials

Item	Qty	Reference	Value	Part	Part Number	Manufacturer
1	8	C1–C4, C6, C7, C17, C18	0.01 μ F	0603 CAP	06031C102JAT2A	Avx Corporation
2	1	C16	100 pF	0603 CAP	06031A101JAT2A	Avx Corporation
3	3	C22, C27, C32	1 μ F	0603 CAP	0603YD105KAT2A	Avx Corporation
4	1	C21	10 μ F	0603 CAP	GRM188R60G106ME47D	Murata Electronics
5	1	C19	0.1 μ F	0603 CAP	C1206C104J5RACTU	Kemet
6	3	C25, C30, C35	68 μ F	7343 CAP	TA025TCM106KDR	Kemet
7	3	C26, C31, C36	10 μ F	7343 CAP	293D106X0035D2W	Venkel
8	3	C24, C29, C34	1.0 μ F	1206 CAP	C1206X7R250-105KNE	Venkel
9	3	C23, C28, C33	0.1 μ F	1206 CAP	C1206C104J5RACTU	Kemet
10	3	C22, C27, C32	0.01 μ F	0805 CAP	GRM21BR72A103KA01L	Murata Electronics
11	3	D1–D3	Red Diffused	0805 LED	HSMH-C170	Avago Technologies
12	2	JMP9, JMP10		2 Pin Header	HTSW-150-07-G-S	Samtec
13	1	JMP7		Header 5x2	HTSW-150-07-G-D	Samtec
14	1	JMP6		Header 10x6	HTSW-150-07-G-T	Samtec
15	1	JMP8		Header 3x2	HTSW-150-07-G-D	Samtec
16	5	J1–J5		SMA Connector	32K141-40ME4	Rosenberger
17	5	P1–P5		Banana Jack	108-0740-001	Emerson Network Power Co.
18	1	R1	100 Ω	0603 RES	ERJ-2RKF1000X	Panasonic – Ecg
19	5	R2–R6	4.7 k Ω	0603 RES	MCR03EZPFX4701	Rohm
20	1	R7	49.9 Ω (DNI)	0603 RES	ERJ-3EKF49R9V	Panasonic – Ecg
21	3	R8–R10	1 k Ω	0603 RES	ERJ-3EKF1001V	Panasonic – Ecg
22	1	U1	TLK1221	IC	TLK1221RHAT	TI

5.3 Board Layouts

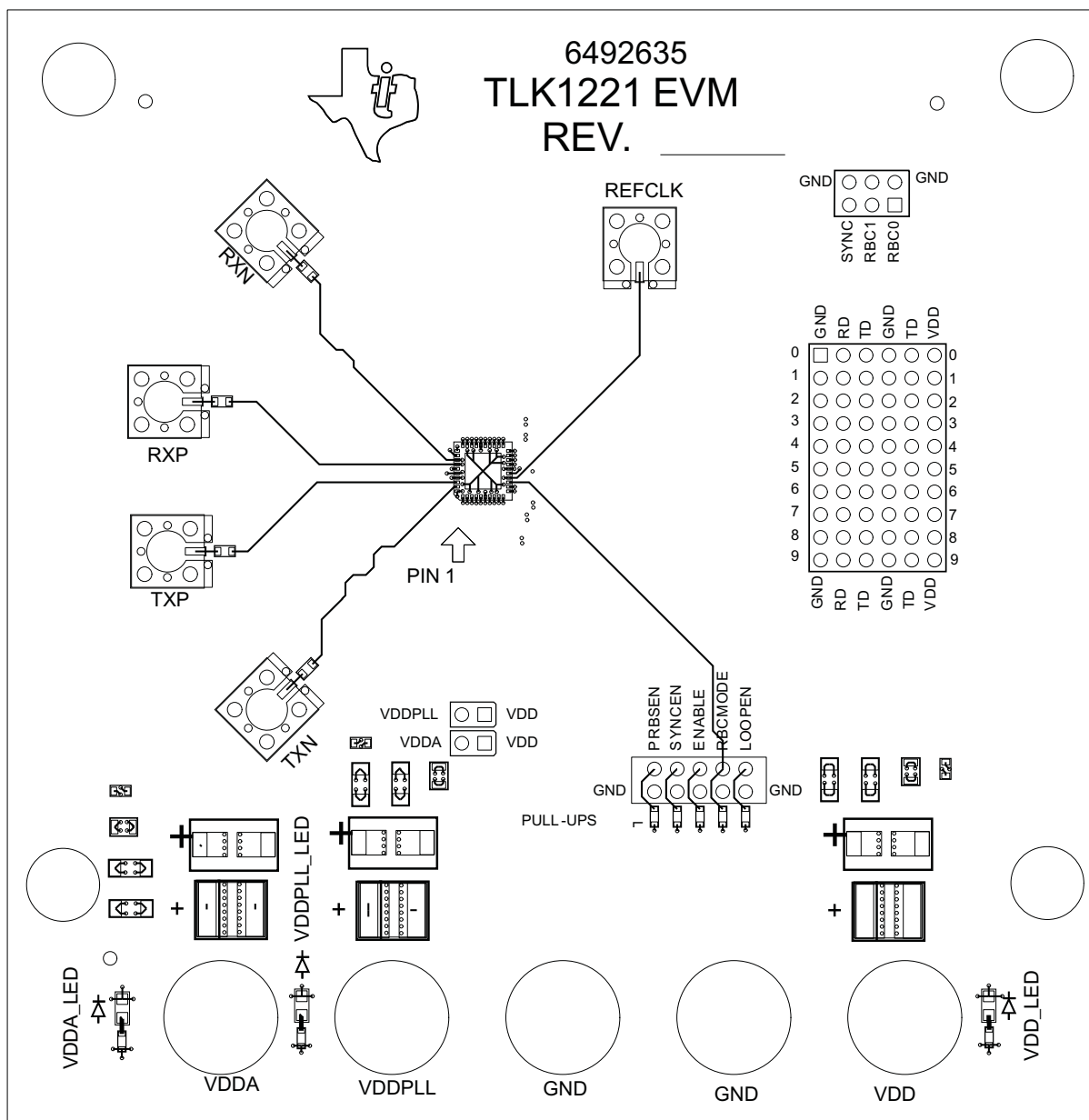


Figure 9. TLK1221 Board Layout: Top (Layer 1)

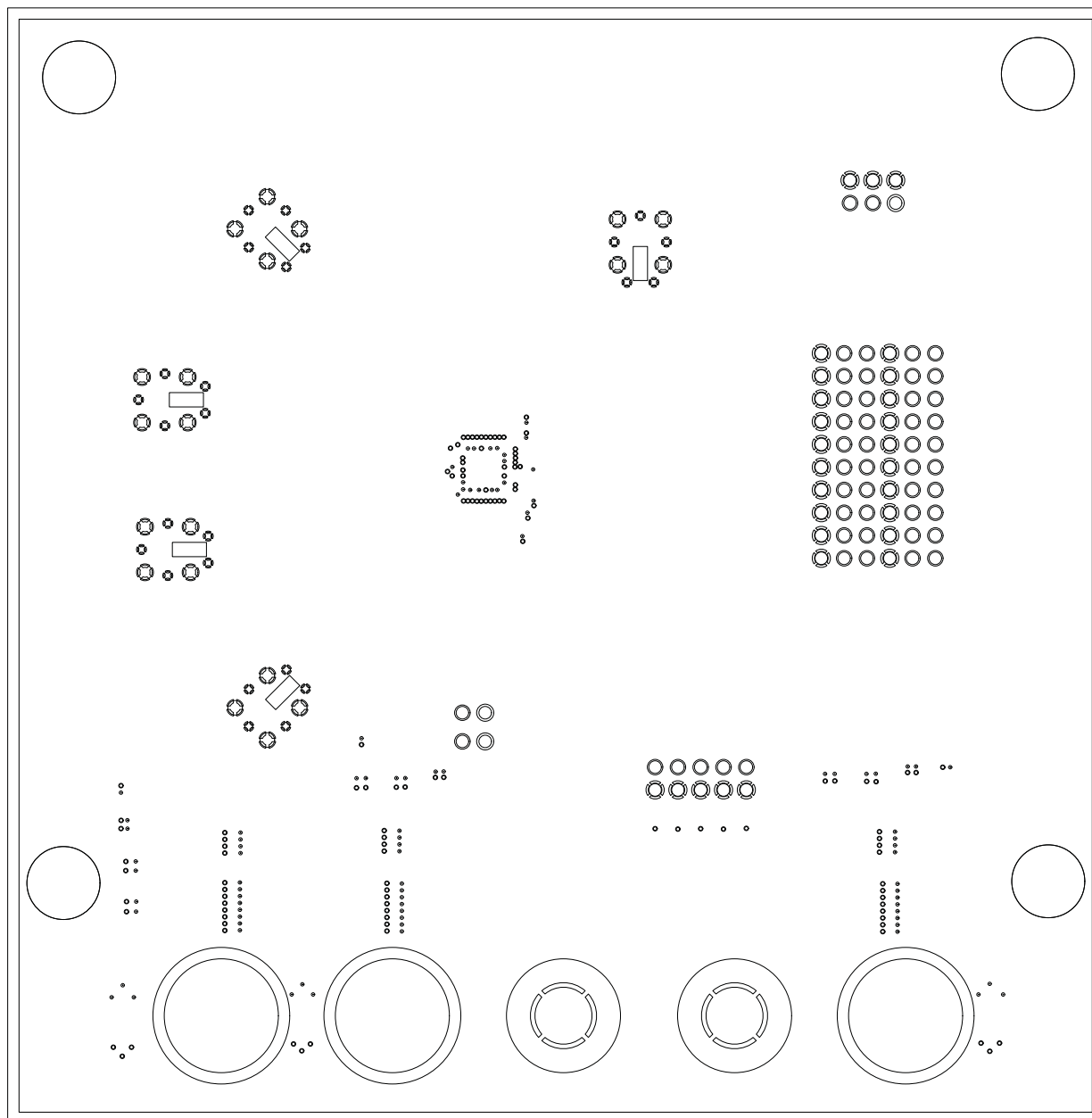


Figure 10. TLK1221 Board Layout: GND (Layer 2)

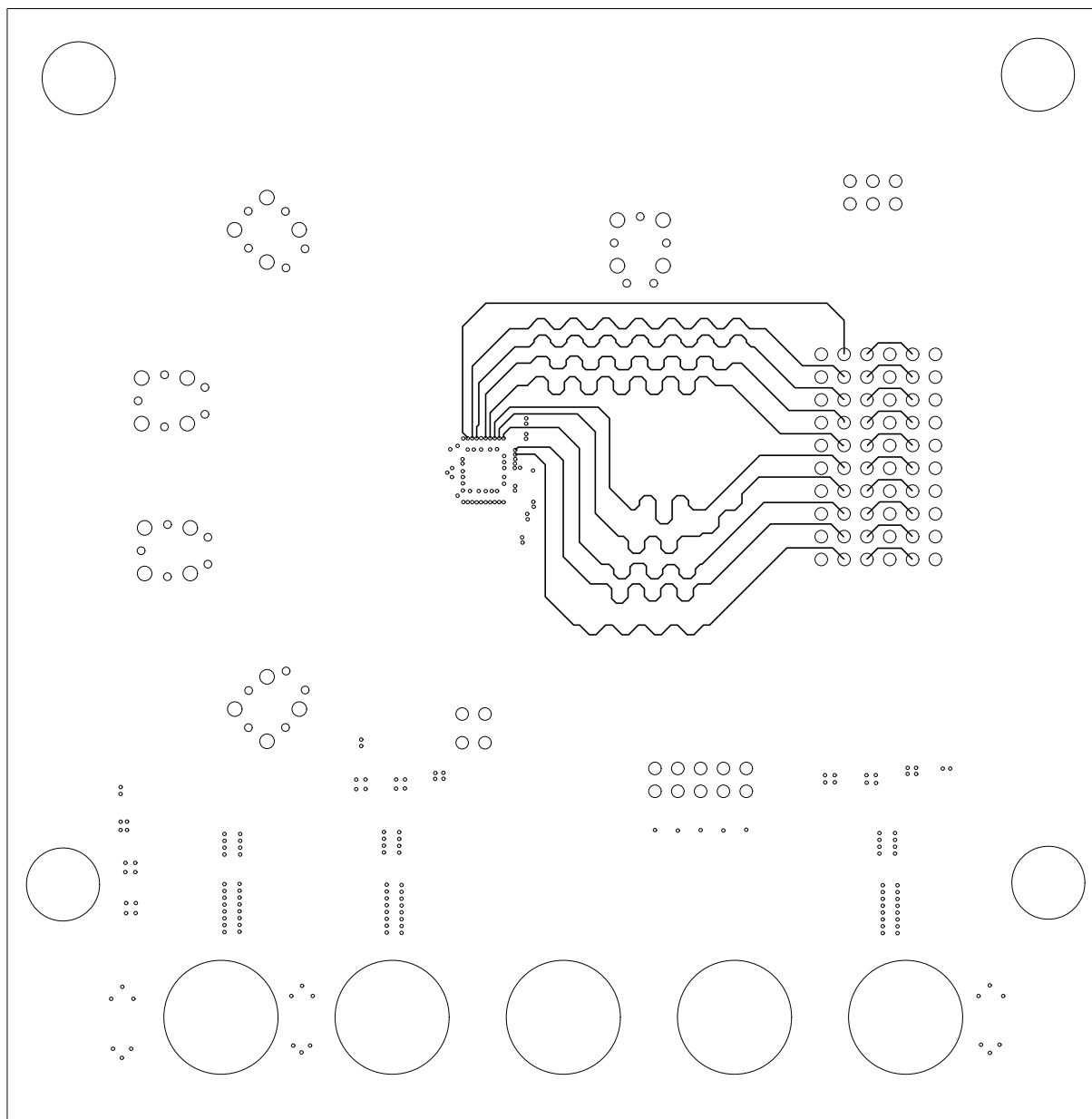


Figure 11. TLK1221 EVM Board Layout: Internal Signal (Layer 3)



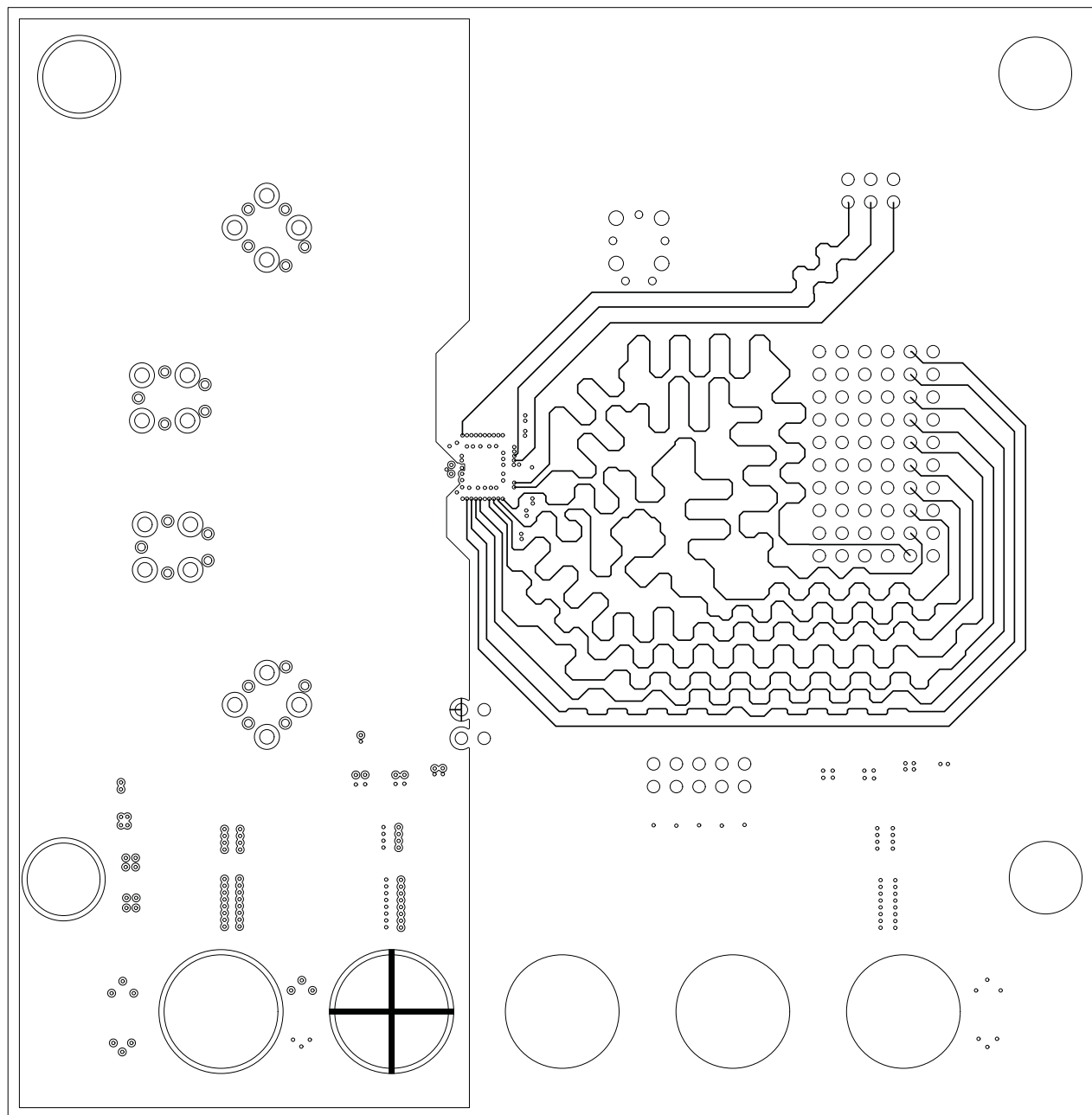


Figure 13. TLK1221 Board Layout: Internal Signal and VDDPLL (Layer 5)

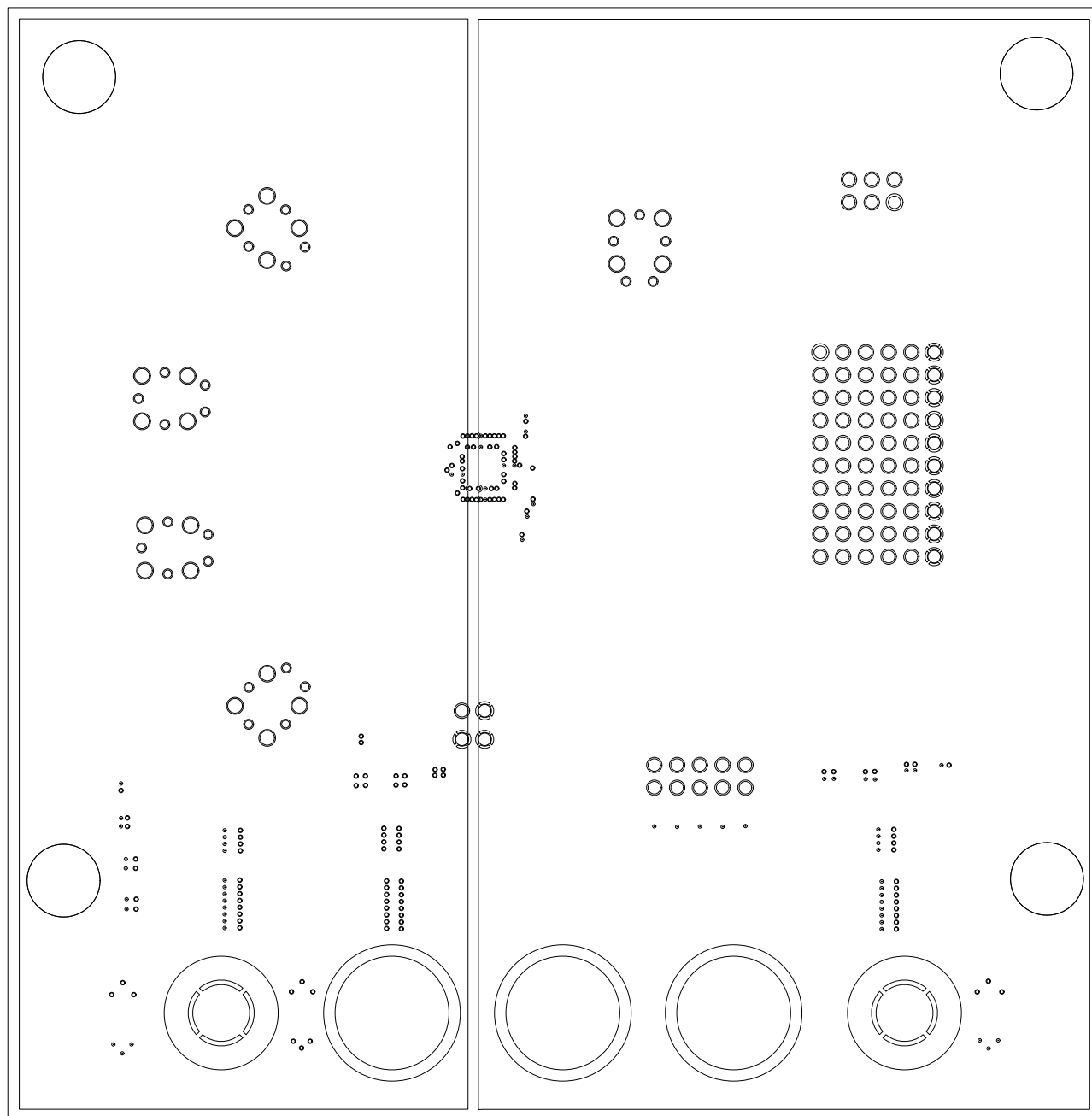


Figure 14. TLK1221 Board Layout: VDDA and VDD (Layer 7)

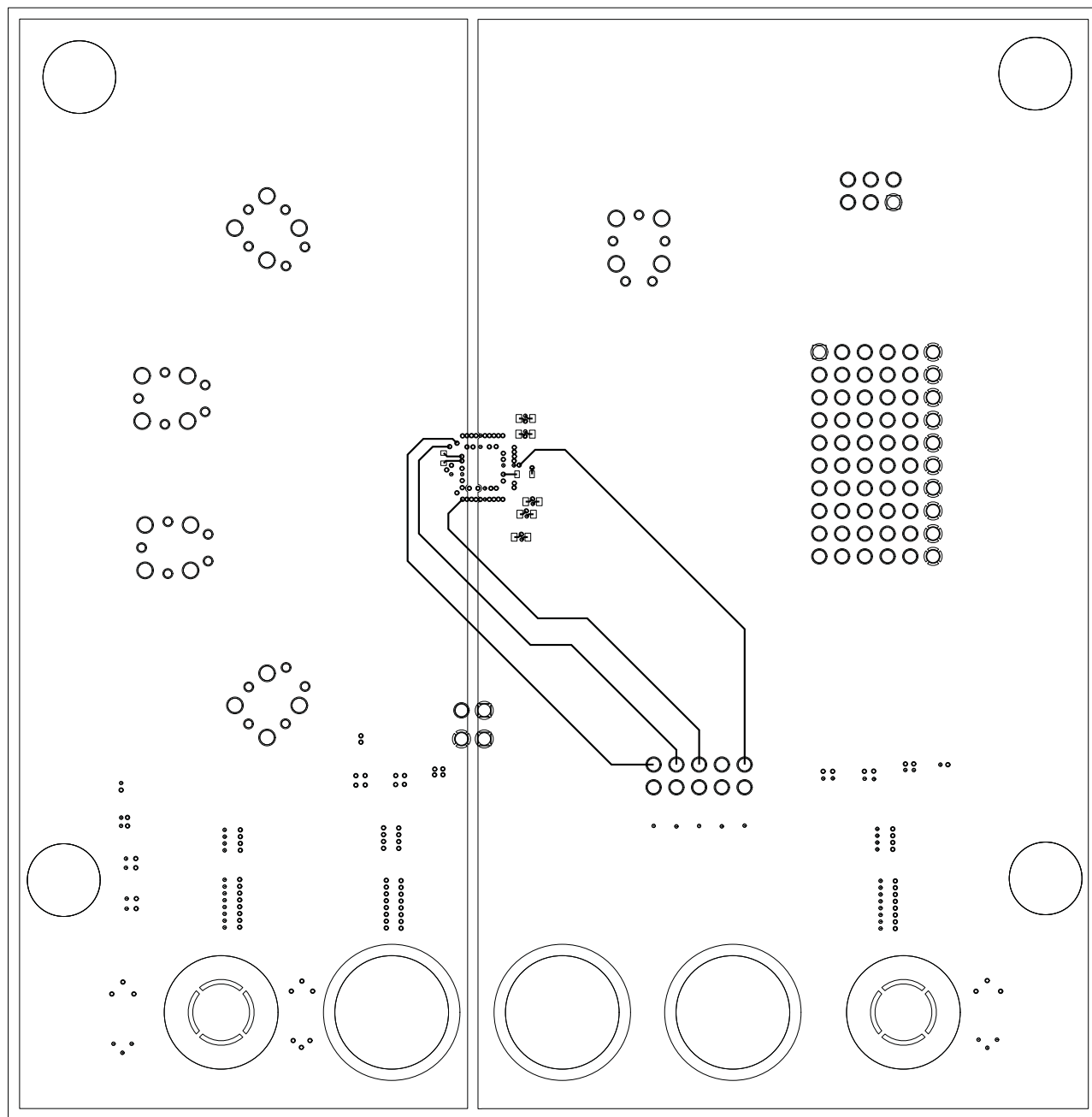


Figure 15. TLK1221 Board Layout: Bottom (Layer 10)

Table 4. TLK1221 EVM PCB Layer Construction

Subclass Name	Type	Material	Thickness (MIL)	Conductivity (mho/cm)	Dielectric Constant	Loss Tangent	Artwork	Width (MIL)	Impedance (Ω)
	SURFACE	AIR							
TOP	CONDUCTOR	COPPER	2.4	595900	1	0	POSITIVE	8	49.307
	DIELECTRIC	FR-4	4.5	0	4.1	0.035			
L2_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	7.5	0	4.1	0.035			
L3_SIG	CONDUCTOR	COPPER	1.2	595900	1	0	POSITIVE	6.5	50.349
	DIELECTRIC	FR-4	7.5	0	4.1	0.035			
L4_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	7.5	0	4.1	0.035			
L5_SIG/VDDPLL	CONDUCTOR	COPPER	1.2	595900	1	0	POSITIVE	6.5	50.349
	DIELECTRIC	FR-4	7.5	0	4.1	0.035			
L6_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	7.5	0	4.1	0.035			
L7_VDD/VDDA	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	7.5	0	4.1	0.035			
L8_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	7.5	0	4.1	0.035			
L9_GND	PLANE	COPPER	1.2	595900	1	0	NEGATIVE		
	DIELECTRIC	FR-4	4.5	0	4.1	0.035			
BOTTOM	CONDUCTOR	COPPER	2.4	595900	1	0	POSITIVE	8	49.307
	SURFACE	AIR							

Note: Always consult with your board manufacturer for their process/design requirements to ensure the desired impedance is achieved.

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It is important to operate this EVM within the input voltage range of 0 V to 3.6 V and the output voltage range of 0 V to 2.9 V or V_{DD} V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 40°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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