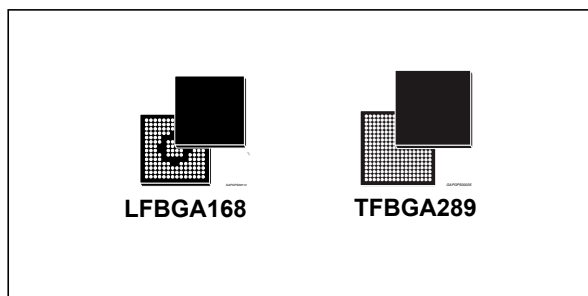


Automotive HD Radio™ baseband receiver

Datasheet - production data



Features



- AEC-Q100 qualified
- IBOC (in-band on-channel) digital audio broadcast signal decoding for AM/FM hybrid and all-digital modes
- Dual-channel HD 1.5 for background scanning and data services
- HD codec (HDC) audio decompression
- Metadata support for HD Radio reception
- MPS (main program service), SPS (supplemental program service) and PAD (program associated data) data decoding
- Advanced HD Radio feature support:
 - Apple ID3 tag
 - Multicasting
 - Electronic program guide (EPG)
 - Real-time traffic
- Automatic Audio Alignment (AAA) algorithm support
- Variable input base-band data-rate I2S-like interface supporting 650, 675, 744.1875, 912 kS/s data rates
- Secondary RF base-band interface for dual tuner applications
- Glueless interface to Synchronous SDRAM addressing up to 512 Mbit of SDRAM in x16 configuration
- Optional Serial Flash memory SPI interface for application code storage
- IIS serial audio interface with programmable sample rate converter
- Primary and secondary serial interfaces for host micro communication based on industry standard IIC and SPI
- Several General purpose IOs
- One Internal clock oscillator and two internal PLLs
- External clock input
- 1.2 V core supply; 3.3 V I/O supply

Description

The STA680 is an HD-radio base-band processor for car-radio applications. The STA680 functionality includes audio decompression and data processing, while multiple interfaces ensure flexible integration into the system.

The STA680 takes full advantage of HD 1.5 Radio benefits including CD-like audio quality from HD Radio FM broadcasts and FM-like audio quality using HD Radio AM, while program associated data or traffic information is received from the second channel.

STA680 supports FM/AM analog/digital AAA algorithm by mean of specific FW.

Table 1. Device summary

Order code	Package ⁽¹⁾	Packing
STA680	LFBGA 168 balls (12x12x1.4 mm)	Tray
STA680TR		Tape & Reel
STA680D	TFBGA 289 balls (15x15x1.2 mm)	Tray
STA680DTR		Tape & Reel

1. ECOPACK® compliant.

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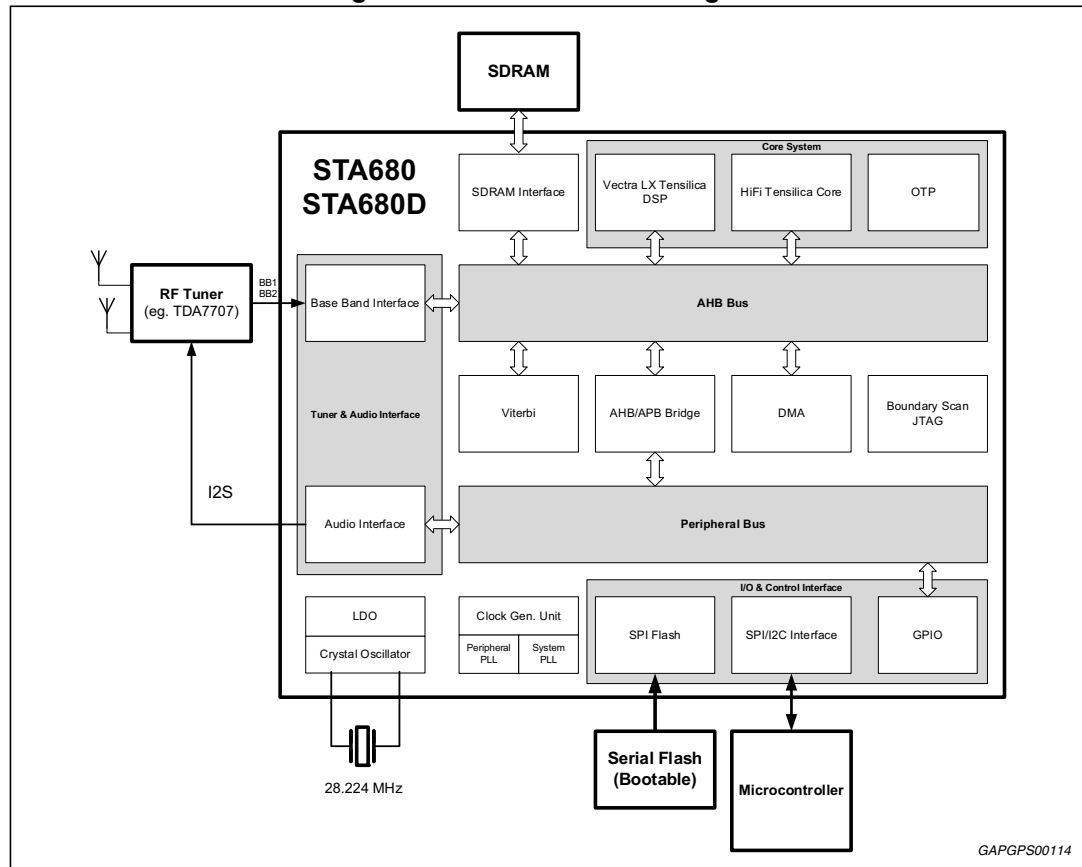
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1 Block diagram and pin description

1.1 Block diagram

Figure 1. Functional block diagram



1.2 Ball-out description

The STA680 is available in two different packages. It comes in a 12x12 mm LFBGA with 168 balls with 0.8 mm pitch and in 15x15 mm TFBGA with 289 balls with 0.8 mm pitch. TFBGA289 package option offers ball-to-ball compatibility with STA660 DAB/DRM digital decoder.

1.2.1 LFBGA description

Figure 2 presents the ball-out of the STA680 for the LFBGA package option. Different colors have been used for I/O signals from different interfaces according to Table 2 reported in Section 1.2.3.

Figure 2. LFBGA ball-out (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		GPIO6	BB2_BCK	BB2_I	GND_GEN_IO	IIC1_SDA	SPI1_MISO	SPI1_SCK	RESET_N	TXD_GPIO2	RTS_GPIO0	VDD_GEN_IO	TESTMODE	
B	GPIO5	BB1_Q	BLEND	BB2_WS	GND_GEN_IO	BB2_Q	IIC1_SCL	SPI1_MOSI	SPI1_SS0_N	RXD_GPIO3	CTS_GPIO1	VDD_GEN_IO	SDR_A3	TRST_N
C	BB1_WS	BB1_I	ADAT2	IIC2_SDA	GPIO7	IIC2_SCL	IIC1_DA	SPI3_MOSI	SPI3_MISO	SPI3_SCK	TDI	TCK	SDR_A1	SDR_A2
D	VDD_GEN_IO	VDD_GEN_IO	BB1_BCK	IIC2_DA	VDD	VDD			SPI3_SS_N	GPIO4	TDO	TMS	SDR_A10	SDR_A0
E	AUDIO_IN_ABCK	SPDIF	ADAT3	VDD_PLL_DIG							VDD	MODEOP_FSH	SDR_BA0	SDR_BA1
F	AUDIO_IN_ADAT	AUDIO_IN_AWS	GND_PLL_DIG	GND_PLL_DIG		GND	GND	GND	GND		VDD	MODEOP_GEN	SDR_RAS_N	SDR_CS_N
G	AWS	ADAT	DAC256X			GND	GND	GND	GND			SDR_CAS_N	SDR_WE_N	VDD_RAM_IO
H	GND_GEN_IO	GND_GEN_IO	ABCK			GND	GND	GND	GND			SDR_A4	SDR_A5	GND_RAM_IO
J	VDD_OSC	GND_OSC	GND_PLL1_ANA	GND_PLL0_ANA		GND	GND	GND	GND		VDD	VDD	SDR_A7	SDR_A6
K	OSC_OUT	CLK_IN	VDD	VDD_REG3V3							VDD	VDD	SDR_A9	SDR_A8
L	OSC_IN	GND_OSC	VDD	VDD_REG3V3	VDD_FSH_IO	GND_FSH_IO			VDD_RAM_IO_1V8	GND_RAM_IO_1V8	GND_RAM_IO	GND_RAM_IO	SDR_A12	SDR_A11
M	VDD_PLL1_ANA	VDD_PLL0_ANA	SPI2_SS1_N	SPI2_SS2_N	SPI2_SS3_N	RFU	SDR_D13	SDR_D10	VDD_RAM_IO	VDD_RAM_IO	GND_RAM_IO	GND_RAM_IO	SDR_DQM1	SDR_CKE
N	VDD_REG1V8	VDD_REG1V8	SPI2_MOSI	SPI2_SCK	SDR_CLK_RAM3V3	SDR_D15	SDR_D12	SDR_D9	SDR_D0	SDR_D2	SDR_D4	SDR_D6	SDR_DQM0	
P			SPI2_SS0_N	SPI2_MISO	SDR_FEED_CLK	SDR_D14	SDR_D11	SDR_D8	SDR_D1	SDR_D3	SDR_D5	SDR_D7		

Color legend:

Ball unused	Ball not present	JTAG interface	UART GPIO interface	Host micro-processor interface	Memory card interface	Flash interface	Base band input interface	Audio Input interface	Audio Output interface	SDRAM interface	

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1.2.2 TFBGA description

Figure 3 presents the ball-out of the STA680 for the TFBGA package option. Different colors have been used for I/O signals from different interfaces according to Table 2 reported in Section 1.2.3.

Figure 3. TFBGA ball-out (top view)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
A	GND			CLK_IN	VDD_PLL0_ANA	VDD_PLL_DIG				ADAT2	TXD_GPIO2	RTS_GPIO0					GND
B					GND_PLL0_ANA	GND_PLL_DIG	RB7				RXD_GPIO3						
C			SPI2_SS3_N	SPI2_SCK	SPI2_MISO	VDD_REG1V8	VDD_RAM_IO_1V8				CTS_GPIO1		TESTMODE	RESET_N			AUDIO_IN_ABCK
D			SPI2_MOSI	SPI2_SS0_N	GND_RAM_IO_1V8			GND_OSC	VDD_OSC	RD10			ADAT3	DAC256X	SPI3_MOSI		AUDIO_IN_AWS
E								OSC_IN	OSC_OUT				RD13	VDD_REG3V3		AUDIO_IN_ADAT	SPI3_SCK
F			SPI2_SS1_N	SPI2_SS2_N					VDDIO		VDD	IIC1_DA	IIC2_SDA	IIC2_SCL	IIC2_DA		
G						VSSIO	VDD	VSSIO	VDD	VDDIO	VSSIO	VDD					
H					TCK	TDO	VDDIO	GND	GND	GND	VDDIO	VDDIO					
J			BB1_Q	BB1_WS	TDI	TRST_N	VDD	GND	GND	GND	VSSIO	VDDIO					
K			BB1_BCK	BB1_I		TMS	VDDIO	GND	GND	GND	VDD	RK12		SPI1_MOSI		SPI1_SS0_N	
L			BB2_WS		RL5	RL6	VDD	VSSIO	VDDIO	VDD	VDDIO	VDD	SPI1_SCK	SPI1_MISO			
M			BB2_I	MODEOP_GEN						ABCK	AWS	SDR_FEED_CLK		GPIO5	GPIO4		
N			BB2_Q	IIC1_SCL							ADAT				GPIO7	GPIO6	SPI3_SS_N
P					SPDIF	SDR_A3	SDR_A7	SDR_A8	SDR_CKE	SDR_CLK_RAM3V3	VSSIO	SDR_D8	SDR_D14	SDR_D3	SDR_D4		SPI3_MISO
R				BLEND		SDR_A0	SDR_A6	SDR_A12	MODEOP_FSH	SDR_CS_N	SDR_CAS_N	SDR_D10	SDR_D13	SDR_D6	SDR_D0		
T	BB2_BCK			IIC1_SDA		SDR_A1	SDR_A5	SDR_A11	SDR_BA1	SDR_BA0	SDR_WE_N	SDR_D9	SDR_D15	SDR_D5	SDR_D2		
U	VDD				SDR_A2	SDR_A10	SDR_A4	SDR_A9	SDR_DQM1	SDR_DQM0	SDR_RAS_N	SDR_D11	SDR_D12	SDR_D7	SDR_D1		VDD

Color legend:

									
Flash interface	Audio Output interface	Memory card interface	Audio Input interface	Host micro-processor interface	JTAG interface	Bass band input interface	SDRAM interface	Ball unused	Ball Reserved

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1.2.3 Ball-out list

The [Table 2](#) describes the primary function and behavior of the STA680 pins.

Table 2. Ball-out description

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up/down ⁽¹⁾	Electrical	Supply group	Description
Test							
A13	C13	TESTMODE	I	Pull-down	3.3 V	Generic IO supply	Factory test mode enable
Standard 1149.1 JTAG interface							
B14	J6	TRST_N	I	Pull-up	3.3 V	Generic IO supply	JTAG active-low test reset
C12	H5	TCK	I	Pull-down	3.3 V	Generic IO supply	JTAG test clock
D12	K6	TMS	I	Pull-up	3.3 V	Generic IO supply	JTAG test mode state
C11	J5	TDI	I	Pull-up	3.3 V	Generic IO supply	JTAG test data in
D11	H6	TDO	O	-	3.3 V	Generic IO supply	JTAG test data out
GPIO & UART interfaces							
A11	A12	RTS_GPIO0	I/O	Pull-up	3.3 V	Generic IO supply	UART ready to send / GPIO bit 0
B11	C11	CTS_GPIO1	I/O	Pull-up	3.3 V	Generic IO supply	UART clear to send / GPIO bit 1
A10	A11	TXD_GPIO2	I/O	Pull-up	3.3 V	Generic IO supply	UART transmit data / GPIO bit 2
B10	B11	RXD_GPIO3	I/O	Pull-up	3.3 V	Generic IO supply	UART receive data / GPIO bit 3
D10	M15	GPIO4	I/O	Pull-up	3.3 V	Generic IO supply	GPIO bit 4
B1	M14	GPIO5	I/O	Pull-up	3.3 V	Generic IO supply	GPIO bit 5
A2	N16	GPIO6	I/O	Pull-up	3.3 V	Generic IO supply	GPIO bit 6

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up/down ⁽¹⁾	Electrical	Supply group	Description
C5	N15	GPIO7	I/O	Pull-up	3.3 V	Generic IO supply	GPIO bit 7
Reset							
A9	C14	RESET_N	I	Pull-up	3.3 V	Generic IO supply	Device active-low reset
Host microprocessor interfaces							
B9	K16	SPI1_SS0_N	I	Pull-up	3.3 V	Generic IO supply	SPI interface 1 active-low slave select
A8	L13	SPI1_SCK	I	Pull-up	3.3 V	Generic IO supply	SPI interface 1 serial clock
B8	K14	SPI1_MOSI	I	Pull-up	3.3 V	Generic IO supply	SPI interface 1 serial data master out/slave in
A7	L14	SPI1_MISO	O	Pull-up	3.3 V	Generic IO supply	SPI interface 1 serial data master in/slave out
B7	N4	IIC1_SCL	I/O	Pull-up	3.3 V	Generic IO supply	IIC interface 1 serial clock line
A6	T4	IIC1_SDA	I/O	Pull-up	3.3 V	Generic IO supply	IIC interface 1 serial data line
C7	F12	IIC1_DA	I/O	Pull-up	3.3 V	Generic IO supply	IIC interface 1 data acknowledged
C6	F14	IIC2_SCL	I/O	Pull-up	3.3 V	Generic IO supply	Reserved
C4	F13	IIC2_SDA	I/O	Pull-up	3.3 V	Generic IO supply	Reserved
D4	F15	IIC2_DA	I/O	Pull-up	3.3 V	Generic IO supply	Reserved

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up/down ⁽¹⁾	Electrical	Supply group	Description
IIS tuner interfaces							
C2	K4	BB1_I	I	Pull-down	3.3 V	Generic IO supply	Primary baseband interface serial I data or Primary baseband interface I/Q multiplexed data
B2	J3	BB1_Q	I	Pull-down	3.3 V	Generic IO supply	Primary baseband interface serial Q data (not used in case of Primary data multiplexed on BB1_I)
C1	J4	BB1_WS	I	Pull-down	3.3 V	Generic IO supply	Primary baseband interface word strobe
D3	K3	BB1_BCK	I	Pull-down	3.3 V	Generic IO supply	Primary baseband interface bit clock
A4	M3	BB2_I	I	Pull-down	3.3 V	Generic IO supply	Secondary baseband interface serial I data or Secondary baseband interface I/Q multiplexed data
B6	N3	BB2_Q	I	Pull-down	3.3 V	Generic IO supply	Secondary baseband interface serial Q data (not used in case of Secondary data multiplexed on BB2_I)
B4	L3	BB2_WS	I	Pull-down	3.3 V	Generic IO supply	Secondary baseband interface word strobe
A3	T1	BB2_BCK	I	Pull-down	3.3 V	Generic IO supply	Secondary baseband interface bit clock
IIS audio input interface							
F2	D17	AUDIO_IN_AWS	I/O	Pull-up	3.3 V	Generic IO supply	Digital audio input word strobe
E1	C17	AUDIO_IN_ABCK	I/O	Pull-up	3.3 V	Generic IO supply	Digital audio input clock
F1	E16	AUDIO_IN_ADAT	I	Pull-down	3.3 V	Generic IO supply	Digital audio input serial data
Audio output interfaces							
G1	M11	AWS	I/O	Pull-up	3.3 V	Generic IO supply	Digital audio output word strobe

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up/down ⁽¹⁾	Electrical	Supply group	Description
H3	M10	ABCK	I/O	Pull-up	3.3 V	Generic IO supply	Digital audio output clock
G2	N11	ADAT	O	-	3.3 V	Generic IO supply	Digital audio output serial data
C3	A10	ADAT2	O	-	3.3 V	Generic IO supply	Reserved
E3	D13	ADAT3	O	-	3.3 V	Generic IO supply	Reserved. Reference clock configuration pin, works in input mode till RESET_N release
E2	P5	SPDIF	O	-	3.3 V	Generic IO supply	Reserved
B3	R4	BLEND	O	-	3.3 V	Generic IO supply	Digital audio blend output. Reference clock configuration pin, works in input mode till RESET_N release
G3	D14	DAC256X	O	-	3.3 V	Generic IO supply	Digital audio output oversampling clock. Reference clock configuration pin, works in input mode till RESET_N release
Clock & oscillator							
K2	A4	CLK_IN	I	-	3.3 V	Generic IO supply	Reference digital clock
L1	E8	OSC_IN	ana	-	1.8 V	Osc supply	28,224MHz crystal in or digital clock input
K1	E9	OSC_OUT	ana	-	1.8 V	Osc supply	Crystal output
SPI Flash interface							
P4	C5	SPI2_MISO	I	Pull-up	3.3 V	Flash IO supply	SPI interface 2 serial data master in/slave out
N3	D4	SPI2_MOSI	O	Pull-up	3.3 V	Flash IO supply	SPI interface 2 serial data master out/slave in
P3	D5	SPI2_SS0_N	O	Pull-up	3.3 V	Flash IO supply	SPI interface 2 active-low slave select 0

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up/down ⁽¹⁾	Electrical	Supply group	Description
M3	F4	SPI2_SS1_N	O	Pull-up	3.3 V	Flash IO supply	Reserved
M4	F5	SPI2_SS2_N	O	Pull-up	3.3 V	Flash IO supply	Reserved
M5	C3	SPI2_SS3_N	O	Pull-up	3.3 V	Flash IO supply	Reserved
N4	C4	SPI2_SCK	O	Pull-up	3.3 V	Flash IO supply	SPI interface 2 serial clock
SPI SD/MMC interface							
C9	P17	SPI3_MISO	I	Pull-up	3.3 V	Generic IO supply	Reserved
C8	D15	SPI3_MOSI	O	Pull-up	3.3 V	Generic IO supply	Reserved
D9	N17	SPI3_SS_N	O	Pull-up	3.3 V	Generic IO supply	Reserved
C10	E17	SPI3_SCK	O	Pull-up	3.3 V	Generic IO supply	Reserved
SDRAM interface							
P5	M12	SDR_FEED_CLK	I	-	3.3 V	SDRAM IO supply	Feedback clock from SDRAM interface
N5	P10	SDR_CLK_RAM3V3	O	-	3.3 V	SDRAM IO supply	Clock to SDRAM for 3.3 V interface
N9	R15	SDR_D0	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 0
P9	U15	SDR_D1	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 1
N10	T15	SDR_D2	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 2
P10	P14	SDR_D3	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 3

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up/down ⁽¹⁾	Electrical	Supply group	Description
N11	P15	SDR_D4	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 4
P11	T14	SDR_D5	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 5
N12	R14	SDR_D6	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 6
P12	U14	SDR_D7	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 7
P8	P12	SDR_D8	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 8
N8	T12	SDR_D9	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 9
M8	R12	SDR_D10	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 10
P7	U12	SDR_D11	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 11
N7	U13	SDR_D12	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 12
M7	R13	SDR_D13	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 13
P6	P13	SDR_D14	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 14
N6	T13	SDR_D15	I/O	-	3.3 V	SDRAM IO supply	SDRAM bidirectional data bit 15
N13	U10	SDR_DQM0	O	-	3.3 V	SDRAM IO supply	Low-byte data input/output mask
M13	U9	SDR_DQM1	O	-	3.3 V	SDRAM IO supply	High-byte data input/output mask
G13	T11	SDR_WE_N	O	-	3.3 V	SDRAM IO supply	Active-low write enable

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up/down ⁽¹⁾	Electrical	Supply group	Description
G12	R11	SDR_CAS_N	O	-	3.3 V	SDRAM IO supply	Active-low column address strobe
F13	U11	SDR_RAS_N	O	-	3.3 V	SDRAM IO supply	Active-low row address strobe
M14	P9	SDR_CKE	O	-	3.3 V	SDRAM IO supply	Clock enable
F14	R10	SDR_CS_N	O	-	3.3 V	SDRAM IO supply	Active-low chip select
E13	T10	SDR_BA0	O	-	3.3 V	SDRAM IO supply	Bank select address 0
E14	T9	SDR_BA1	O	-	3.3 V	SDRAM IO supply	Bank select address 1
D14	R6	SDR_A0	O	-	3.3 V	SDRAM IO supply	Address bit 0 to SDRAM
C13	T6	SDR_A1	O	-	3.3 V	SDRAM IO supply	Address bit 1 to SDRAM
C14	U5	SDR_A2	O	-	3.3 V	SDRAM IO supply	Address bit 2 to SDRAM
B13	P6	SDR_A3	O	-	3.3 V	SDRAM IO supply	Address bit 3 to SDRAM
H12	U7	SDR_A4	O	-	3.3 V	SDRAM IO supply	Address bit 4 to SDRAM
H13	T7	SDR_A5	O	-	3.3 V	SDRAM IO supply	Address bit 5 to SDRAM
J14	R7	SDR_A6	O	-	3.3 V	SDRAM IO supply	Address bit 6 to SDRAM
J13	P7	SDR_A7	O	-	3.3 V	SDRAM IO supply	Address bit 7 to SDRAM
K14	P8	SDR_A8	O	-	3.3 V	SDRAM IO supply	Address bit 8 to SDRAM

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up/down ⁽¹⁾	Electrical	Supply group	Description
K13	U8	SDR_A9	O	-	3.3 V	SDRAM IO supply	Address bit 10 to SDRAM
D13	U6	SDR_A10	O	-	3.3 V	SDRAM IO supply	Address bit 10 to SDRAM
L14	T8	SDR_A11	O	-	3.3 V	SDRAM IO supply	Address bit 11 to SDRAM
L13	R8	SDR_A12	O	-	3.3 V	SDRAM IO supply	Address bit 12 to SDRAM
Supplies							
F12	M4	MODEOP_GEN	I	Pull-up	3.3 V	SDRAM IO supply	Define the operating voltage of the "Generic I/O" supply group. Value is 3.3V.
E12	R9	MODEOP_FSH	I	Pull-up	3.3 V	SDRAM IO supply	Define the operating voltage of the "Generic I/O" supply group. Value is 3.3V.
D5, D6, E11, F11, J11, J12, K3, K11, K12, L3	F11, G7, G9, G12, J7, K11, L7, L10, L12, U1, U17	VDD	n/a	-	1.2 V	Core supply	Power supply for core logic
F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9	A1, A17, H8, H9, H10, J8, J9, J10, K8, K9, K10,	GND	n/a	-	-	Core supply	Ground for core logic
A5, B5, H1, H2	-	GND_GEN_IO	n/a	-	-	Generic IO supply	Generic I/Os ground
A12, B12, D1, D2	-	VDD_GEN_IO	n/a	-	3.3 V	Generic IO supply	Generic I/Os power supply
L6	-	GND_FSH_IO	n/a	-	-	Flash IO supply	Ground for Flash Interface I/Os
L5	-	VDD_FSH_IO	n/a	-	3.3 V	Flash IO supply	Power supply for Flash Interface I/Os

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up/down ⁽¹⁾	Electrical	Supply group	Description
H14, L11, L12, M11, M12	-	GND_RAM_IO	n/a	-	-	SDRAM IO supply	Ground for SDRAM Interface I/Os
G14, M9, M10	-	VDD_RAM_IO	n/a	-	3.3 V	SDRAM IO supply	Power supply for SDRAM Interface I/Os
-	F9, G10, H7, H11, K7, L9, L11, H12, J12	VDDIO	n/a	-	3.3 V	I/O supply	Generic I/Os power supply
-	G6, G8, G11, J11, L8, P11	VSSIO	n/a	-	-	I/O supply	Generic I/Os ground
F3, F4	B6	GND_PLL_DIG	n/a	-	-	PLL digital supply	Ground for PLL digital part
E4	A6	VDD_PLL_DIG	n/a	-	1.2 V	PLL digital supply	Power supply for PLL digital part
J4	B5	GND_PLL0_ANA	n/a	-	-	PLL analog supply	Ground for PLL0 analog part
J3	-	GND_PLL1_ANA	n/a	-	-	PLL analog supply	Ground for PLL1 analog part
M2	A5	VDD_PLL0_ANA	n/a	-	1.8 V	PLL analog supply	Power supply for PLL0 analog part
M1	-	VDD_PLL1_ANA	n/a	-	1.8 V	PLL analog supply	Power supply for PLL1 analog part
J2, L2	D8	GND_OSC	n/a	-	-	Osc supply	Ground for oscillator core
J1	D9	VDD_OSC	n/a	-	1.8 V	Osc supply	Power supply for oscillator core
K4, L4	E14	VDD_REG3V3	n/a	-	3.3 V	LDO supply	Voltage regulator input power supply @ 3.3 V
N1, N2	C6	VDD_REG1V8	n/a	-	1.8 V	LDO supply	Voltage regulator output power supply @ 1.8 V
L9	C7	VDD_RAM_IO_1V8	n/a	-	1.8 V	n/a	Reserved - connect to 1.8 V supply
L10	D6	GND_RAM_IO_1V8	n/a	-	-	n/a	Reserved - Connect to ground
Others							
M6	-	RFU	n/a	-	n/a	n/a	Reserved for future use - do not connect

Table 2. Ball-out description (continued)

LFBGA Ball #	TFBGA Ball #	Signal name	Type	Pull-up/down ⁽¹⁾	Electrical	Supply group	Description
Reserved							
-	B7, D10, E13, K12, L5, L6	RB7, RD10, RE13, RK12, RL5, RL6	n/a	-	n/a	n/a	Reserved
Unused							
A1, A14, N14, P1, P2, P13, P14	A2, A3, A7, A8, A9, A13, A14, A15, A16, B1, B2, B3, B4, B8, B9, B10, B12, B13, B14, B15, B16, B17, C1, C2, C8, C9, C10, C12, C15, C16, D1, D2, D3, D7, D11, D12, D16, E1, E2, E3, E4, E5, E6, E7, E10, E11, E12, E15, F1, F2, F3, F6, F7, F8, F10, F16, F17, G1, G2, G3, G4, G5, G13, G14, G15, G16, G17, H1, H2, H3, H4, H13, H14, H15, H16, H17, J1, J2, J13, J14, J15, J16, J17, K1, K2, K5, K13, K15, K17, L1, L2, L4, L15, L16, L17, M1, M2, M5, M6, M7, M8, M9, M13, M16, M17, N1, N2, N5, N6, N7, N8, N9, N10, N12, N13, N14, P1, P2, P3, P4, P16, R1, R2, R3, R5, R16, R17, T2, T3, T5, T16, T17, U2, U3, U4, U16	Unused	n/a	-	n/a	n/a	Unused balls have to be left unconnected or connected to GND. Unused balls can be shorted together but they cannot be connected to any supply or other signal trace on the application PCB.

1. Each input pin has a pull-up/down resistor to its default value. Unless otherwise specified, signal balls not used in application can be left unconnected after verifying that the impedance value of the pull-up/down resistor (see [Table 20](#)) is sufficient to guarantee noise immunity in user application environment.

1.2.4 I/Os supply groups

The STA680 I/O signals can be grouped into three different supply domains, as shown in (see [Table 2](#)):

- Generic IO supply
- Flash IO supply
- SDRAM IO supply group

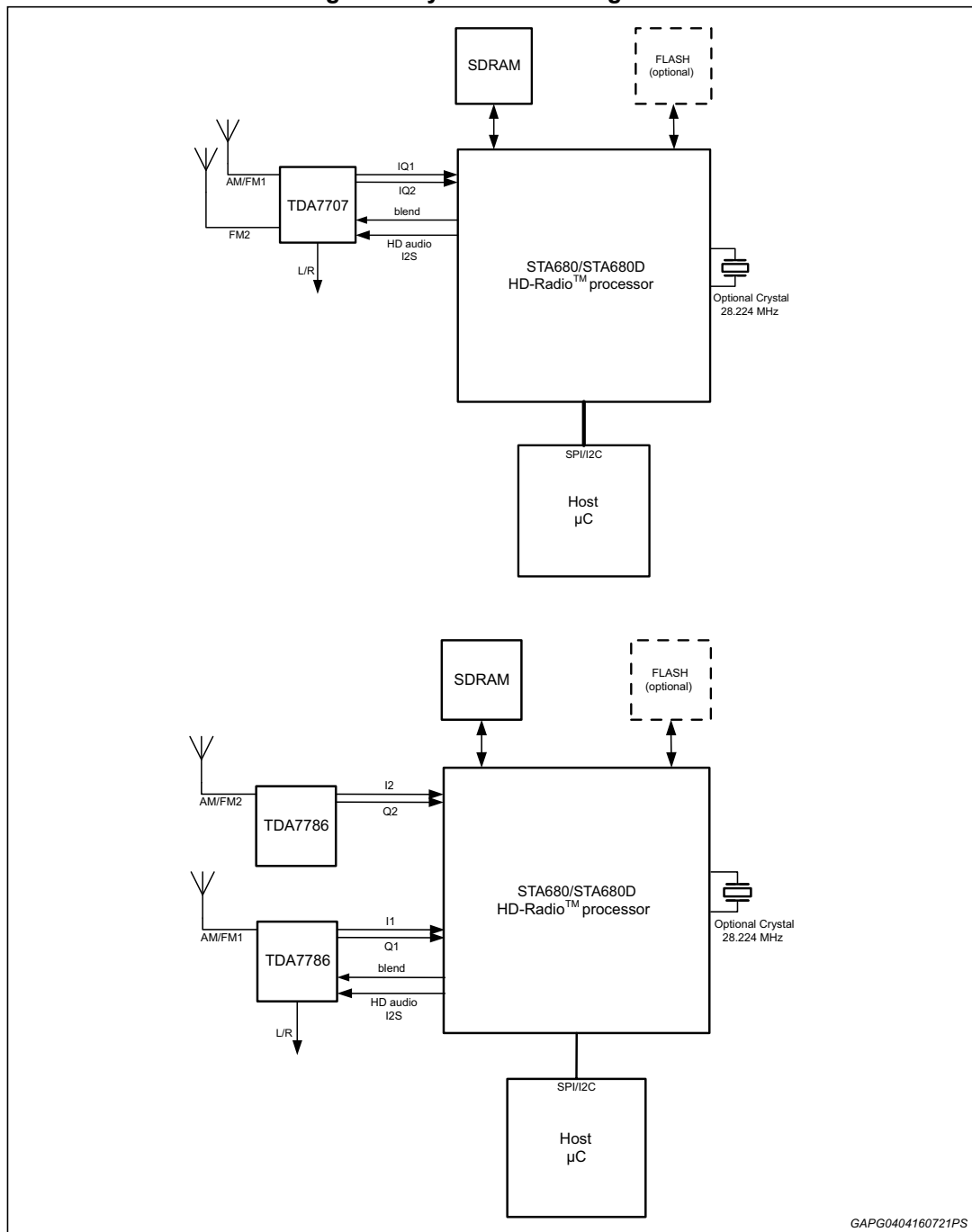
In the LFBGA and TFBGA packages the three supply groups operate at 3.3 V.

2 General description

The STA680 is a system-on-chip designed for demodulating and decoding HD Radio signals.

The STA680 is the base-band signal processor needed by an HD Radio receiver: it includes the OFDM demodulator, error correction, audio and data decoding of the digital channel.

Figure 4. System block diagrams



The architecture of STA680 consists of a mixed hardware/software implementation. Computation-intensive functional blocks are implemented using custom logic. Software implementation is more efficient for functional blocks where flexibility is needed.

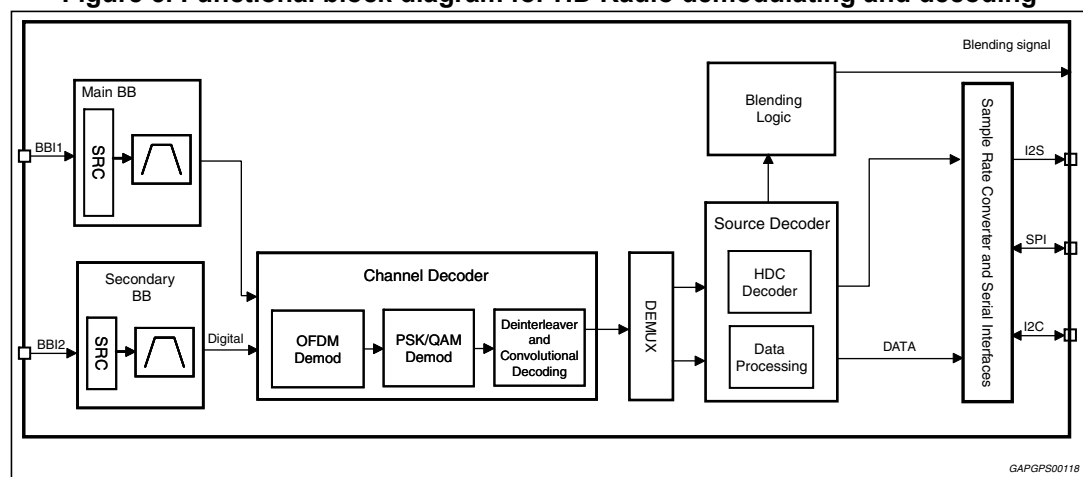
2.1 Receiver system overview

Such flexibility enables the STA680 to support both the HD 1.0 single-channel, and HD 1.5 double-channel applications, as shown in [Figure 4](#).

[Figure 5](#) shows the internal simplified block diagram of the STA680.

The STA680 receives the digital base-band signal from the digital tuner (e.g. TDA7786 or TDA7707) and extracts the HD-encoded audio and data services as shown in [Figure 5](#). STA680 is compatible with conventional base-band radio reception tuners (e.g. TDA7786 or TDA7707).

Figure 5. Functional block diagram for HD Radio demodulating and decoding



2.2 HD Radio processing

The STA680 HD Radio decoder performs the processing of the IBOC signal. The native internal processing data rate is 744.1875 kS/s for FM and 46.51171875 kS/s for AM.

The input I²S base-band interface accepts several input sample rates thanks to the availability of a reconfigurable sample rate converter. The supported rates are: 650 kS/s, 675 kS/s, 744.1875 kS/s and 912 kS/s.

The STA680 is responsible for the detection, acquisition and demodulation of the IBOC signal. This processing is mainly performed inside the Vectra DSP core. The demodulated signal is then passed to the Hi-Fi processor for decoding and handling of data services. The digital 44.1 kHz decompressed audio is streamed out by means of the Digital Audio Interface.

The STA680 requires a 4Mwords x16bits external SDRAM (with up to 32Mword x16bits supported) for data storage in order to process the HD Radio stream

2.3 Dual channel HD 1.5 Radio processing

The STA680 is capable of simultaneously demodulating two different HD Radio streams. This feature enables the device to decode the main HD Radio audio stream in parallel with the data service broadcasted by a different radio channel (for instance this feature allows to continue receiving traffic information provided by one radio station while listening to music from a different station).

An example of implementation of the dual stream HD Radio processing is shown in [Figure 4](#).

2.4 Overview of main functional blocks

2.4.1 Adjacent channel filter

This module performs digital filtering of the IBOC channel. It receives the complex base-band I/Q IBOC signal input from the tuner and pre-conditions the signal for subsequent modem processing.

2.4.2 HiFi2 core

The HiFi2 is a signal processing engine specifically designed to provide high quality 24-bit audio processing. The HiFi2 uses the Tensilica Xtensa LX engine with additional useful hardware capabilities such as:

- Specialized instructions for 24-bit Audio MAC & stream coding
- Dual MAC (each supports 24 x 24 and 32 x 16 bit format)
- Huffman Encode / Decode and truncate functions
- Two way Single-Instruction-Multiple-Data arithmetic and logic operations

2.4.3 Vectra core

The Vectra LX is an on-chip, powerful, 32-bit RISC engine optimized for DSP with VLIW capabilities. The Vectra LX includes eight MAC units, sixteen 160-bit vector operation registers, and a number of SIMD arithmetic instructions. Custom instructions in the Vectra are tailored to DSP applications such as filters and FFTs. The Vectra processor has been further configured with specific instructions for efficient performance on the HD Radio application.

2.4.4 DMA

A ten-channel DMA controller is attached to the AHB bus to allow the Vectra and HiFi2 processor cores to efficiently move large data-blocks.

2.4.5 Hardware accelerator (VITERBI)

The complex convolutional Viterbi hardware accelerator supports both K constants of 7 and 9, for IBOC digital FM and AM processing respectively.

3 Operation and general remarks

3.1 Clock schemes

The STA680 needs an external clock source to drive the internal Phase Locked Loops (PLLs) that generate the clocks needed by the DSP cores and their peripherals.

The STA680 accepts several external reference clock sources, as listed below:

- The reference clock can be supplied through the use of an external crystal or as a digital signal coming from an external IC.
- The reference clock can have different frequencies and different input pins can be used.

The selection of the clock input mode is performed during the power-on phase of the device by latching the value of the pins ADAT3, BLEND and DAC256X on the rising edge of the RESET_N signal (see [Section 3.2](#)); these values shall be selected according to [Table 3](#).

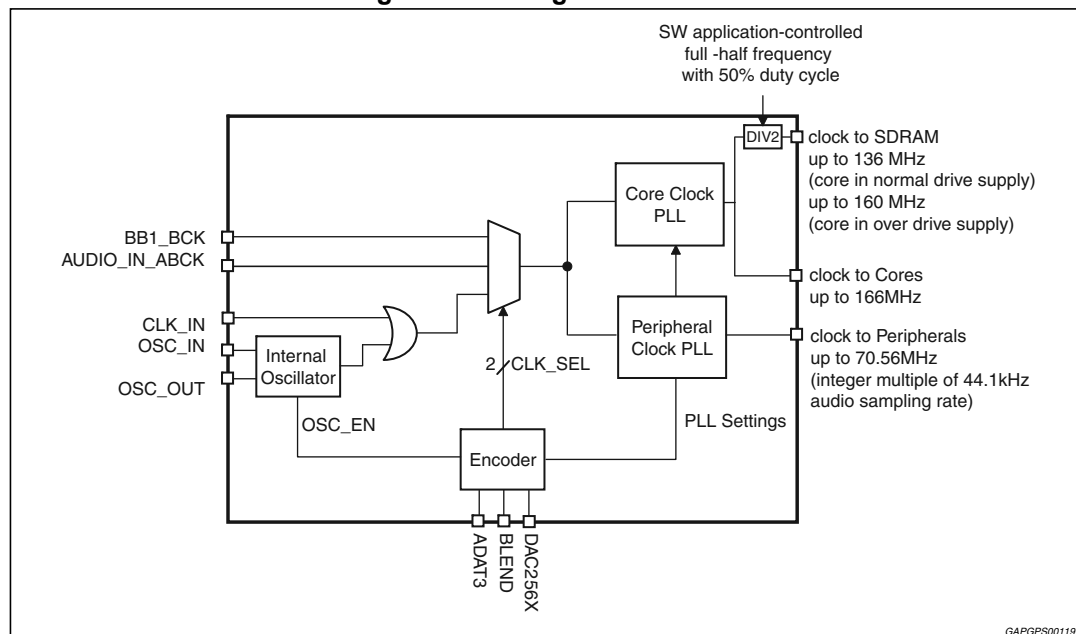
Table 3. Reference clock configuration

[ADAT3, BLEND, DAC256X]	Clock type	Input pin	Clock frequency (MHz)
[0,0,0] ⁽¹⁾	Crystal	OSC_IN	28.224
[0,0,1]	Digital	OSC_IN or CLK_IN ⁽²⁾	23.3472
[0,1,0]	Digital	OSC_IN or CLK_IN ⁽²⁾	36.48
[0,1,1]	Digital	OSC_IN or CLK_IN ⁽²⁾	2.9184
[1,0,0]	Digital	BB1_BCK ⁽³⁾	10.4
[1,0,1]	Digital	BB1_BCK ⁽³⁾	10.8

1. Default setting.
2. When using OSC_IN pin to input the reference clock the CLK_IN pin must be connected to ground and vice versa.
3. When using BB1_BCK to input the reference clock it is suggested to connect the OSC_IN to ground and to tie the CLK_IN pin to high value (3.3 V).

Figure 6 shows a simplified version of the internal clock generation unit.

Figure 6. Clock generation unit



Clock generation unit

Some remarks on the clock input pin follow:

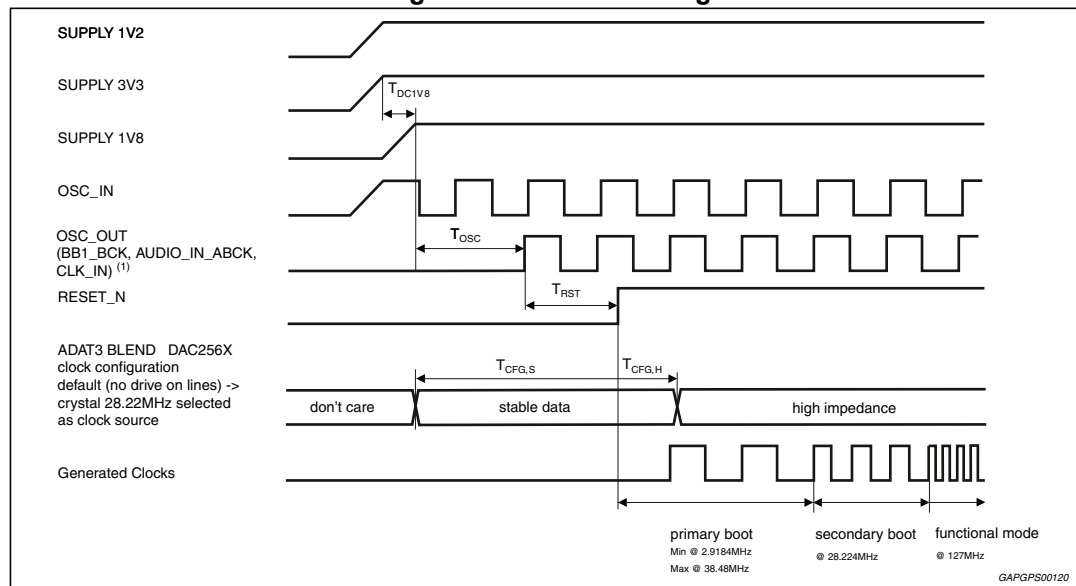
- OSC_IN is always a 1.8 V input pin;
- CLK_IN, BB1_BCK are 3.3 V;
- When the clock is fed through the CLK_IN pin, the OSC_IN pin must be connected to ground (and vice versa);
- The BB1_BCK pin is the bit clock of the digital interface to the baseband Tuner. When this pin is selected as input for the reference clock, the selected clock frequency must be chosen compatibly with the Primary baseband Interface settings (see [Section 5.2](#)):
 - $10.4 \text{ MHz} = 16 * 650 \text{ kHz} \rightarrow \text{BBI set to } 650 \text{ Ksample/s}$
 - $10.8 \text{ MHz} = 16 * 675 \text{ kHz} \rightarrow \text{BBI set to } 675 \text{ Ksample/s};$
- When the device reference clock comes from BB1_BCK it is suggested to connect the OSC_IN to ground and to tie the CLK_IN pin to its high value (3.3 V).

3.2 Power on

This chapter describes the power-on procedure for the cold start (i.e. when the device is not supplied before being turned on). [Figure 7](#) and [Table 4](#) show the timing for the cold start power up sequence.

Boot pins are latched at startup. Their default value is logic 0, in case logic 1 is needed a 6K2 pull-up resistor should be connected on the corresponding boot line. After reset release, the boot selection lines become outputs.

Figure 7. Power on timing



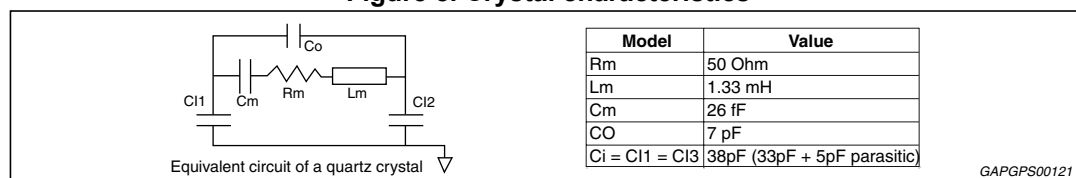
1. In case the Reference Clock is fed through BB1_BCK or CLK_IN the Power On timing diagram is the same as [Figure 7](#) where OSC_OUT is substituted by the external supplied stable reference clock.

Table 4. Power on timing parameters

Symbol	Parameter	Min	Max	Unit
$T_{\text{ramp-up}}$	External supply ramp-up time	Same ramp-up time for 3.3 V and 1.2 V supply		-
T_{DC1V8}	DC1V8 regulator start-up time	-	1	ms
$T_{\text{OSC}}^{(1)}$	Oscillator start-up time	-	400	μs
T_{RST}	Reset release time	2	-	ms
$T_{\text{CFG,S}}$	Setup time for clock configuration	0.1	-	μs
$T_{\text{CFG,H}}$	Hold time for clock configuration	10	-	ns

1. The oscillator start-up time depends on the crystal connected to the internal oscillator. The given value is estimated for a crystal with characteristic shown in [Figure 8](#).

Figure 8. Crystal characteristics



4 Power supply ramp-up phase

The external power supply circuit on the board has to ensure that all the power supplies are ramped up to their specified levels. The ramp up phase of each power domain should start at the same time.

The RESET_N pin must be kept low from the beginning.

For normal applications, the TESTMODE pin (Factory test mode enable) must be connected to ground.

4.1 Oscillator setting time

Once the power supply has reached the operating level, the internal voltage regulator gets functional after $T_{DC1V8} = 1\text{ms}$ (see [Table 4](#)) and starts supplying the 1.8 V voltage to internal IPs such as PLLs and Crystal Oscillator.

The PLL is powered up but not yet functional since the internal logic keeps it in bypass mode until a stable clock is available and STA680 has entered the secondary boot phase.

As shown in [Figure 7](#), if an external crystal is connected to the internal oscillator this will output a correct waveform after $T_{OSC} = 400\text{ }\mu\text{s}$ (see [Table 4](#)).

Alternatively, if no crystal is used, a digital clock must be supplied according to the instructions detailed in [Section 3.1](#). In this case the Power On timing diagram is the same as [Figure 7](#) where OSC_OUT is substituted by the external supplied stable reference clock (alternatively BB1_BCK or CLK_IN).

The RESET_N pin must be kept low for an additional $T_{RST} = 2\text{ ms}$ both when using a crystal and when using an external reference clock.

As described in [Section 3.1](#) the internal clock configuration is defined by the status of the pins ADAT3, BLEND and DAC256X; this is latched on the rising edge of the RESET_N signal.

The voltage of the three pins must be stable from at least $T_{CFG} = 0.1\text{ }\mu\text{s}$ before the rising edge of the RESET_N signal.

4.2 Boot sequence

Once the RESET_N signal has been released and the power up sequence correctly executed, the STA680 enters the boot procedure, which consists of two phases:

1. device setup
2. application authentication and download.

During the first phase, the STA680 executes the on-chip primary boot code contained in the Boot ROM.

The primary boot synchronizes the internal cores, initializes the SPI and IIC interfaces and automatically selects the secondary boot code source by looking for a pre-defined pattern into UART1, Flash (SPI2), IIC1.

Once the source of the secondary boot code has been identified, the STA680 executes the following steps:

1. code authentication
2. SDRAM initialization
3. secondary boot code download to SDRAM.

In order to decrease the boot time during the secondary phase, the STA680 performs the setup of the PLLs and sets the internal clock frequency to 28.224 MHz (see [Figure 7](#)). Subsequently it downloads and validates the application code either from the external Flash memory or from the host microcontroller. This ends the boot procedure.

4.3 Normal operation mode

After the execution of the boot code, the device enters the normal operation mode by jumping to the main program loop.

5 Digital I/O and memory interfaces

5.1 Interfaces: LFBGA vs. TFBGA

STA680 supported interfaces are listed in [Table 5](#)^(a).

Table 5. Interface list

Interface name	Direction	LFBGA	TFBGA
Baseband interface 1	I	√	√
Baseband interface 2 (data only)	I	√	√
I ² S audio input	I	√	√
I ² S audio output	O	√	√
I ² C primary interface (Micro)	I/O	√	√
I ² C secondary Interface	I/O	√	√
SPI micro interface	I/O	√	√
SPI Flash interface (double chip select)	I/O	√	√
SPI Flash interface extension (up to 4 chip select)	I/O	√	√
SDRAM interface	I/O	√	√
UART interface	I/O	√	√
4 GPIO lines	I/O	√	√
JTAG test interface (boundary scan only)	I/O	√	√

a. STA680 firmware determines actual feature availability. Refer to the STA680 firmware Release Notes.

5.2 Base-band I²S interface

The STA680 has two digital Base-Band Interfaces (BBI1 and BBI2).

The tuner receives the analog signal from the antenna, samples it, performs down conversion and channel selection, and transmits the digital base-band stream to the STA680 by means of BB1 and BB2.

Each BB interface consists of maximum four wires: up to two serial data lines I/Q (or one single data lines where I and Q data are multiplexed), one bit clock line and one frame clock line. The serial data is always transmitted with the MSB first and a 16-bit word length. The complex base-band signal needs to be at zero IF.

Most common data rates are supported by using the internal base-band sample rate converter. The allowed base-band interface data rates are:

- 650 kS/s,
- 675 kS/s,
- 744.1875 kS/s
- 912 kS/s.

[Table 6](#) describes the pin functionality of both BBI1 and BBI2.

Table 6. Baseband interfaces pin list

Pin name	Designation	Type
BB1_WS	Primary baseband interface word strobe	I
BB1_BCK	Primary baseband interface bit clock	I
BB1_I	Primary baseband interface serial I data (or Primary baseband data I/Q multiplexed)	I
BB1_Q	Primary baseband interface serial Q data	I
BB2_WS	Secondary baseband interface word strobe	I
BB2_BCK	Secondary baseband interface bit clock	I
BB2_I	Secondary baseband interface serial I data (or Secondary baseband data I/Q multiplexed)	I
BB2_Q	Secondary baseband interface serial Q data	I

The base-band interface supports the modes shown in [Figure 9](#) Timing information for the protocols shown in [Figure 9](#) is detailed in [Table 7](#).

Figure 9. BBI waveforms and timings

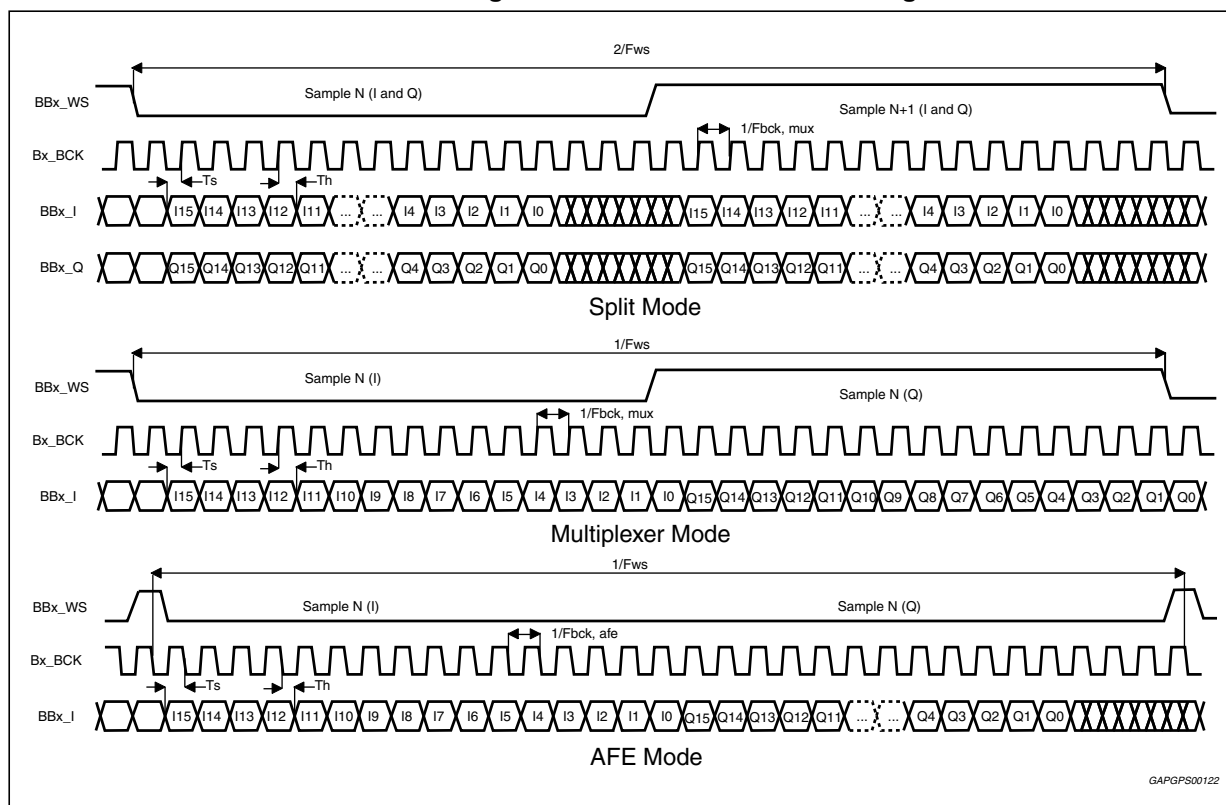


Table 7. BBI timing values

Symbol	Parameter	Working Rate				Unit
Fws	Word Strobe	650	675	744.1875	912	kHz
Fbck,split	Bit clock in SPLIT mode	16 x Fws				kHz
Fbck,mux	Bit clock in MUX mode	32 x Fws				kHz
Fbck,afe	Bit clock in AFE mode	32 x Fws				kHz
Th	Data hold time	4				ns
Ts	Data setup time	8				ns

5.3 Base-band I²S interface frequency diversity

When the STA680 is paired with the TDA7786 or any tuner of ST STAR family it can benefit from the supported base-band interface frequency diversity that allows to improve the EMI robustness of the system.

The frequency diversity technique allows the base-band data-rate to be varied at run-time depending on the frequency of the tuned station, thus moving the intrinsic radiation of the BBI digital lines away from the signal of interest.

5.4 Audio interface (AIF)

The STA680 uses a stereo I²S interface for sending the decoded digital audio back to the tuner, where the blending with the legacy AM/FM demodulated audio occurs.

The receivers and transmitters can be used either in master mode, running with the STA680 internal audio frequency of 44.1 kHz or in slave mode running with a frequency determined by the external device. In slave mode, the internal Audio Sample Rate Converter (ASRC, see [Chapter 5.4.3](#)) adapts the external data rate (from 44.1 to 48 kSps) to the internal one.

Table 8. AIF pin list

Pin name	Designation	Type	Drive
AUDIO_IN_AWS	Digital audio input word strobe	O	4mA
AUDIO_IN_ABCK	Digital audio input bit clock	O	4mA
AUDIO_IN_ADAT	Digital audio input serial data	I	-
AWS	Digital audio output word strobe	I/O	4mA
ABCK	Digital audio output clock	I/O	4mA
ADAT	Digital audio output serial data	O	4mA
DAC256X	Digital audio output oversampling clock (256 x Fs)	O	4mA
BLEND	Digital audio output blend output	O	4mA

5.4.1 Output serial audio interface (SAI)

The output serial audio interface is used to send the decoded audio from the HD Radio Decoder to an external IC (e.g. TDA7786 or TDA7707).

The output SAI is an I2S interface which provides audio samples in stereo at a 44.1 kS/s data rate in master mode. In slave mode, other sample rates (from 44.1 to 48 kS/s) are supported by means of the internal ASRC (see [Section 5.4.3](#)).

The output SAI interface is composed by three lines: one data line and two clock lines.

The output SAI supports a 32x or 64x bit clock with 16-bit precision audio data. The 32x clock mode has no bit padding. The 64x clock mode adds 16-bits zero padding at the end of the 16-bit audio data. [Figure 10](#) shows timing diagrams for the supported modes.

An oversampled audio master-clock is also available for directly interfacing the STA680 to an external DAC. [Table 8](#) shows the timing values for the output SAI interface.

Figure 10. Serial audio interface waveforms and timings

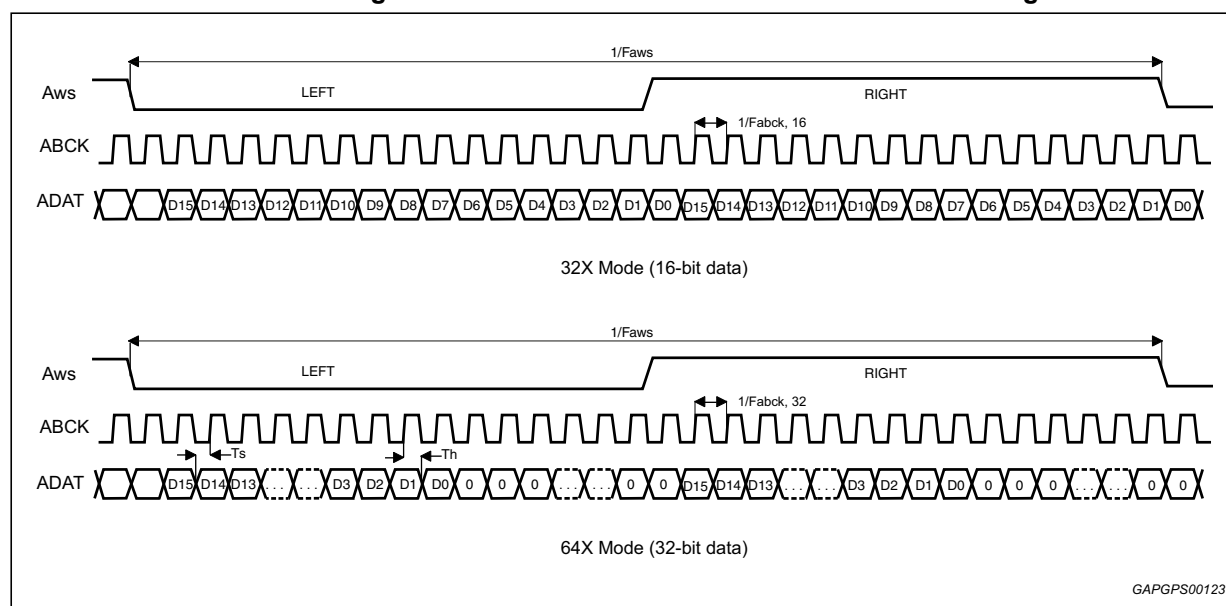


Table 9. Serial audio interface timing values

Symbol	Parameter	Working rate			Unit
Faws	Word strobe	44.1 ±10 Hz	45.6 ±15 Hz	48 ±15 Hz	kHz
Fabck,16	Bit clock for 16-bit data	32 x Faws			MHz
Fabck,32	Bit clock for 32-bit data	64 x Faws			MHz
Th	Data hold time	5			ns
Ts	Data setup time	20			ns

5.4.2 Input serial audio interface

The input serial audio interface is used to receive the legacy AM/FM demodulated audio samples from an external AM/FM Tuner for AAA algorithm purpose.

The input SAI is an I2S interface which accepts 16 bit audio samples in stereo at a 44.1 kS/s sample rate. For usage with AAA algorithm enabled SW the Input serial audio interface must be configured as master at 44.1 kS/s (in that case output SAI needs to be configured as slave).

5.4.3 Audio sample rate converter (ASRC)

The STA680 embeds a stereo channel sample rate converter to be used in combination with either the output (one single data-line) or the input SAI. The ASRC has a Total Harmonic Distortion plus Noise (THD+N) level at 1 kHz smaller than -85 dB (0.0056%).

The supported data rates are:

- 44.1 (± 10 Hz),
- 45.6 (± 15 Hz)
- 48 (± 15 Hz)

5.5 Serial peripheral interfaces (SPI)

The STA680 provides three serial peripheral interfaces:

- SPI1 is intended for communicating with the Host Microcontroller (slave);
- SPI2 interfaces the STA680 to the external flash memory (master);
- SPI3 - Reserved.

Figure 11 shows the timing diagrams and waveform for the three SPI interfaces.

Figure 11. SPI interface timings diagrams and waveforms

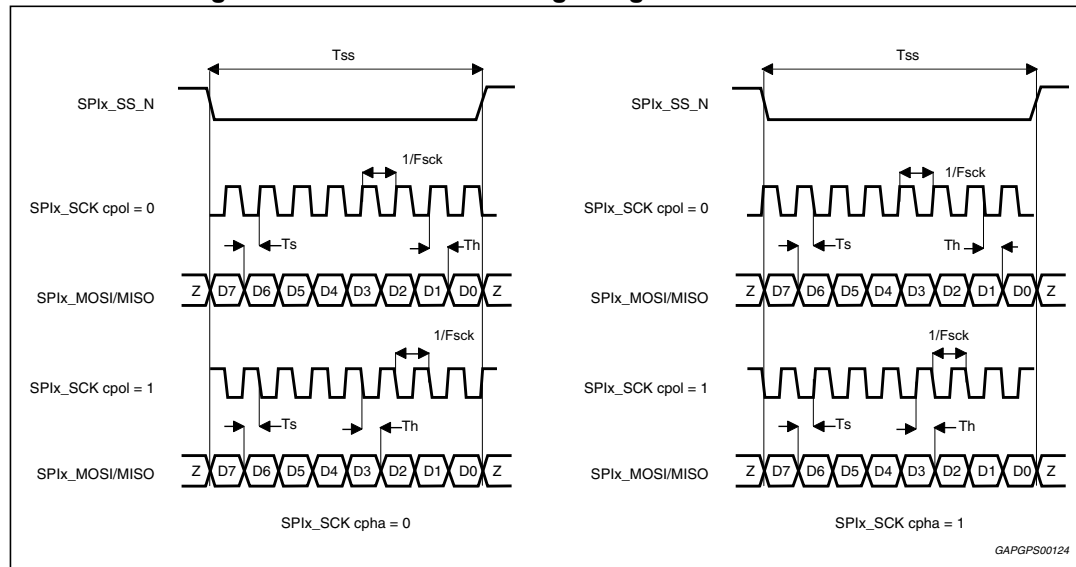


Table 10 shows the timing values for the SPI interface used in application.

Table 10. SPI interface timing values

Symbol	Parameter	Working rate		Unit
		Min.	Max.	
Tss	Chip select	8/Fsck	-	ns
Fsck	Serial bit clock, slave mode	-	7056	kHz
Fsck	Serial bit clock, master mode	-	28224	kHz
Th	Data hold time	7	-	ns
Ts	Data setup time	15	-	ns

5.5.1 Host micro serial peripheral interface (SPI1)

SPI1 is used to interface the STA680 with a host processor interface.

The communication with the host-microcontroller can alternatively be performed via I²C as described in [Section 5.6.1](#).

The Host Micro SPI is a slave only interface.

For the relevant pin description see [Table 11](#).

Table 11. Host micro SPI pin list

Pin name	Designation	Type	Drive
SPI1_MISO	Host Micro SPI data master in/slave out	O	4 mA ⁽¹⁾
SPI1_MOSI	Host Micro SPI data master out/slave in	I	-
SPI1_SCK	Host Micro SPI clock	I	-
SPI1_SS_N	Host Micro SPI active-low slave select 1	I	-

1. 4 mA driving capability is guaranteed on a maximum capacitive load of 20 pF.

5.5.2 Flash serial peripheral interface (SPI2)

SPI2 is typically used for connecting the STA680 to an external Flash memory where the boot code and configuration parameters could be stored. The minimum required capacity for this purpose is 1 Mbit. SPI2 is master-only.

Up to 4 chip select lines are available on the STA680. For the relevant pin description see [Table 12](#).

Table 12. Flash SPI pin list

Pin name	Designation	Type	Drive
SPI2_MISO	Flash SPI data master in/slave out	I	-
SPI2_MOSI	Flash SPI data master out/slave in	O	4 mA ⁽¹⁾
SPI2_SCK	Flash SPI clock	O	4 mA ⁽¹⁾
SPI2_SS_N	Flash SPI active-low slave select 1	O	4 mA ⁽¹⁾
SPI2_SS1_N	Flash SPI active-low slave select 2	O	4 mA ⁽¹⁾
SPI2_SS2_N	Flash SPI active-low slave select 3	O	4 mA ⁽¹⁾
SPI2_SS3_N	Flash SPI active-low slave select 4	O	4 mA ⁽¹⁾

1. 4 mA driving capability is guaranteed on a maximum capacitive load of 20 pF.

5.6 I²C interfaces

The STA680 features two I²C interfaces. For the relevant pin description see [Table 13](#).

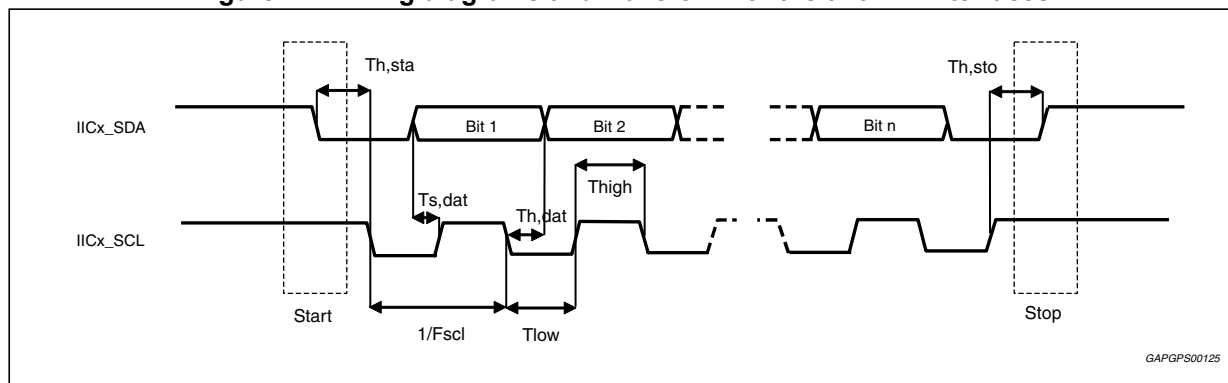
Table 13. Host and auxiliary I²C interface pin list

Pin name	Designation	Type	Drive
IIC1_SCL	Host Micro I ² C interface serial clock line	I/O	4mA
IIC1_SDA	Host Micro I ² C interface serial data line	I/O	4mA
IIC1_DA	Host Micro I ² C interface data acknowledged	I/O	4mA
IIC2_SCL	Auxiliary I ² C interface serial clock line	I/O	4mA
IIC2_SDA	Auxiliary I ² C interface serial data line	I/O	4mA
IIC2_DA	Auxiliary I ² C interface data acknowledged	I/O	4mA

The data pin of the I²C interface is an open drain driver and it needs a resistive pull-up as required by Philips® I²C specification.

[Figure 12](#) shows timing diagrams and waveform for the two I²C interface.

Figure 12. Timing diagrams and waveform for the two I²C interfaces



In [Table 14](#) the timing values for the I²C interfaces are reported.

Table 14. I²C interface timing values

Symbol	Parameter	Standard-mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
Fscl	SCL clock frequency	-	100	-	400	kHz
Tlow	Low period of SCL clock	4.7	-	1.3	-	μs
Thigh	High period of SCL clock	4	-	0.6	-	μs
Th, dat	Data hold time	5	-	-	-	μs
Ts, dat	Data setup time	250	-	100	-	μs
Th, sta	Hold time for start condition	4	-	0.6	-	μs
Ts, sto	Setup time for stop condition	4	-	0.6	-	μs

5.6.1 Host micro I²C interface (I2C1)

I2C1 is used to connect the STA680 to the host microcontroller to transmit commands, diagnostic information, and data.

The I2C1 interface is a standard bi-directional I²C interface.

The I2C1 interface supports 7-bit addressing and 8-bit data. It can run in both standard mode (serial clock frequency up to 100 kHz) and fast mode (up to 400 kHz). The I²C device addresses are reported in [Table 15](#).

An additional control line called IIC1_DA is provided as an extension of the I²C standard. This line is used as a flag to show the host controller that data is available and it can be polled by the host micro in either master or slave modes.

Table 15. I2C1 interface device address

I2C1	Primary address	Secondary address
Read Address	00101111b (0x2F)	00101101b (0x2D)
Write Address	00101110b (0x2E)	00101100b (0x2C)

5.7 SDRAM interface

The SDRAM interface supports up to 32M x 16 SDRAM; both standard and mobile protocols are accepted. For the relevant pin description see [Table 16](#).

Table 16. SDRAM Interface pin description

Pin Name	Designation	Type	Drive
SDR_D[0:15]	SDRAM interface data bus	I/O	4 mA
SDR_A[0:12]	SDRAM interface address bus	O	4 mA
SDR_BA[0:1]	Bank address	O	4 mA
SDR_CAS_N	Active-low column address strobe	O	8 mA
SDR_RAS_N	Active-low row address strobe	O	8 mA
SDR_WE_N	Active-low write enable	O	8 mA
SDR_CS_N	Active-low chip select	O	8 mA
SDR_DQM0	low-byte data input/output mask	O	4 mA
SDR_DQM1	high-byte data input/output mask	O	4 mA
SDR_CKE	Clock enable	O	4 mA
SDR_CLK_RAM3V3	Clock to SDRAM for 3.3 V interface	O	8 mA
SDR_FEED_CLK	Feedback clock from SDRAM	I	8 mA

The minimum required SDRAM size for single channel application is 64 Mbit (a specific FW is needed) while for a dual channel application at least 128 Mbit are needed.

[Figure 13](#) shows the timing diagrams and waveform for the SDRAM interface.

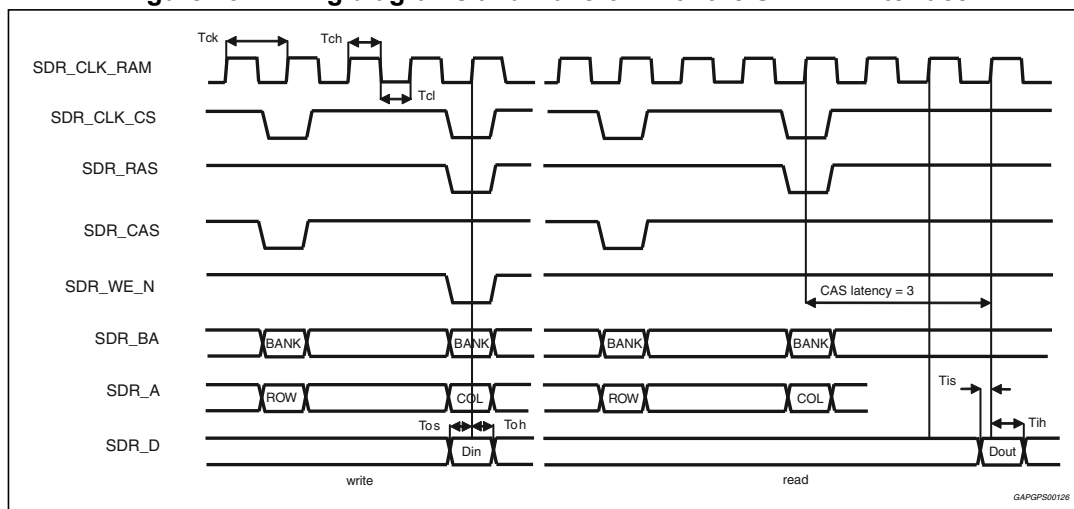
Figure 13. Timing diagrams and waveform for the SDRAM interface

Table 17 reports the timing values for the SDRAM interface

Table 17. SDRAM interface timing values

Symbol	Parameter	Condition	Software application	Min.	Max.	Unit
Tck	SCL clock period	Core in normal drive	Full rate	7.35	-	ns
			Half rate	12.05	-	
Tch	CLK high level width	-	-	2.5	-	ns
Tcl	CLK low level width	-	-	2.5	-	ns
Toh	Data out hold time	-	-	0.9	-	ns
Tos	Data out setup time	-	-	1.5	-	ns
Tis	Data In setup time	-	-	0.8	-	ns
Tih	Data In hold time	-	-	1.6	-	ns
Tt	Transition time	-	-	-	1.2	ns

For power saving and reduced interference on the board, the SDRAM speed can be programmed to work at half speed with respect to the internal data processing:

- Full Rate SW application: the SDRAM interface works at the same frequency as the internal data processing (HD 1.0 and HD 1.5 applications supported);
- Half Rate SW application: the SDRAM interface works at half frequency with respect to the internal data processing (only available for HD 1.0 application upon specific request).

6 Electrical specifications

6.1 Absolute maximum ratings

Table 18. Absolute maximum rating

Symbol	Parameter	Test condition	Min	Max	Units
VDD	Core supply voltage	-	-0.30	1.47	V
VDD_GEN_IO	Generic IO supply voltage	-	-0.30	3.60	V
VDD_FSH_IO	Flash IO supply voltage	-	-0.30	3.60	V
VDD_RAM_IO	SDRAM IO supply voltage	-	-0.30	3.60	V
VDD_OSC	Osc 1V8 supply voltage	-	-0.30	2.75	V
VDD_PLL_ANA	PLL analog supply voltage	-	-0.30	2.75	V
VDD_PLL_DIG	PLL digital supply voltage	-	-0.30	1.47	V
VDD_SAF	SAF core supply voltage	-	-0.30	1.47	V
V _i	Voltage on input pin	-	-0.50	VDDIO+0.5	V
V _o	Voltage on output pin	-	-0.50	VDDIO+0.5	V
VESD	ESD absolute minimum withstand voltage	R = 1.5 kΩ; C = 1.5 pF Human Body Model, LFBGA package	> ±1000		V
		Charged device mode, LFBGA package	> ±500		

6.2 Thermal data

Table 19. Thermal data

Symbol	Parameter	Test condition	Value	Unit
R _{th j-amb}	Thermal resistance junction-to-ambient	BGA package, JEDEC 2s2p PCB, free air	44	°C/W
T _{stg}	Storage temperature	-	-55 to 150	°C
T _{amb}	Operating ambient temperature	-	-40 to 85	°C
T _{j, max}	Maximum junction temperature	-	125	°C

6.3 Operating conditions

Table 20. DC electrical characteristics

Symbol	Parameter	Test condition			Min.	Typ.	Max.	Unit
VDD	Core supply voltage	Normal drive			1.14	1.2	1.26	V
VDD_GEN_IO	Generic IO supply voltage	-			3.14	3.3	3.46	V
VDD_FSH_IO	Flash IO supply voltage	-			3.14	3.3	3.46	V
VDD_RAM_IO	SDRAM IO supply voltage	-			3.14	3.3	3.46	V
VDD_RAM_IO_1V8 ⁽¹⁾	Supply for the SDRAM clock at 1.8V	-			1.71	1.8	1.89	V
VDD_OSC ⁽¹⁾	Oscillator analog supply voltage	-			1.71	1.8	1.89	V
VDD_PLL_ANA ⁽¹⁾	PLL analog supply voltage	-			1.71	1.8	1.89	V
VDD_PLL_DIG	PLL digital supply voltage	Normal drive			1.14	1.2	1.26	V
VDD_SAF	SAF supply voltage	Normal drive			1.14	1.2	1.26	V
I _{1V2}	Current from 1.2 V supply	HD 1.0 ⁽²⁾	T _{amb} = 25 °C	VDD = 1.20 V	-	90	-	mA
			T _{amb} = 85 °C	VDD = 1.26 V	-	-	149	mA
		HD 1.5 ⁽³⁾	T _{amb} = 25 °C	VDD = 1.20 V	-	110	-	mA
			T _{amb} = 85 °C	VDD = 1.26 V	-	-	180	mA
I _{3V3}	Current from 3.3 V supply	HD 1.0 ⁽²⁾	T _{amb} = 25 °C	VDD_IO ⁽⁴⁾ = 3.3 V	-	32	-	mA
			T _{amb} = 85 °C	VDD_IO = 3.46 V	-	-	41	mA
		HD 1.5 ⁽³⁾	T _{amb} = 25 °C	VDD_IO = 3.3 V	-	50	-	mA
			T _{amb} = 85 °C	VDD_IO = 3.46 V	-	-	70	mA
Pd	Power dissipation	HD 1.0 ⁽²⁾	T _{amb} = 25 °C	typical supply	-	214	-	mW
			T _{amb} = 85 °C	max supply	-	-	330	mW
		HD 1.5 ⁽³⁾	T _{amb} = 25 °C	typical supply	-	297	-	mW
			T _{amb} = 85 °C	max supply	-	-	469	mW
I _{il}	Low level input leakage current ⁽⁵⁾	Vi = 0 V			-	-	1.9	μA
I _{ih}	High level input leakage current ⁽⁵⁾	Vi = VDD_GEN_IO ⁽⁶⁾			-	-	1.9	μA
I _{lpu}	High level input leakage current on pull up ⁽⁷⁾	Vi = VDD_GEN_IO ⁽⁶⁾			-	-	2.9	μA

Table 20. DC electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I _l pd	Low level input leakage current on pull-down ⁽⁸⁾	V _i = 0 V	-	-	10	μA
R _{pu}	Equivalent pull-up resistance ⁽⁹⁾	3.3 V supply mode V _i = 0.1 V	52	-	180	kΩ
R _{pd}	Equivalent pull-down resistance ⁽¹⁰⁾	3.3 V supply mode V _i = 3.5 V	52	-	180	kΩ
V _{il}	Low level input voltage	3.3 V supply mode	-0.3	-	0.7	V
V _{ih}	High level input voltage	3.3 V supply mode	2.0	-	VDD_GEN_IO +0.3	V
V _{hyst}	Input hysteresis voltage	3.3 V supply mode	50	-	-	mV
V _{oh}	Output high voltage	I _{oh} = XmA ⁽¹¹⁾	VDD_GEN_IO - 0.4V	-	-	V
V _{ol}	Output low voltage	I _{ol} = XmA ⁽¹¹⁾	-	-	0.3	V
I _l latchup	Injection current	Maximum operating junction temperature	100	-	-	mA
I _{il} _ram	Low level input leakage current ⁽⁵⁾	V _i = 0V	-	-	4	μA
I _{ih} _ram	High level input leakage current ⁽⁵⁾	V _i = VDD_RAM_IO	-	-	4	μA
I _l pu_ram	High level input leakage current on pull up ⁽⁷⁾	V _i = VDD_RAM_IO	-	-	4	μA
I _{pu} _ram	Pull-up current	V _i = 0.1V	40	-	150	μA
R _{pu} _ram	Equivalent pull-up resistance ⁽⁹⁾	V _i = 0.1V	23	-	87	kΩ
V _{il} _ram	Low level input voltage	-	0.8	-	-	V
V _{ih} _ram	High level input voltage	-	-	-	2	V
V _{hyst} _ram	Schmitt trigger hysteresis	-	300	-	800	mV
V _{oh} _ram	High level output voltage	I _{oh} = -XmA ⁽¹¹⁾	VDD_RAM_IO -0.4	-	-	V
V _{ol} _ram	Low level output voltage	I _{ol} = XmA ⁽¹¹⁾	-	-	0.3	V
I _{dc}	3V3 to 1V8 DC regulator output current	-	-	-	100	mA

Table 20. DC electrical characteristics (continued)

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
C_L	Output load for triple voltage pads	3.3 V supply mode (for both 4 mA and 8 mA)	60 MHz	-	-	30	pF
			75 MHz	-	-	20	pF
$C_{L,3V3}$	Output load for 3.3 V pads	4 mA buffer	140 MHz	-	-	10	pF
		8 mA buffer	140 MHz	-	-	20	pF
$C_{L, DC}$	DC regulator output load ⁽¹²⁾	-		2.2	-	4.7	μF

1. DC operating voltage limits only apply for the case of external 1.8 V power supply. If connected to VDD_REG_1V8 supply pad, DC operating voltage limits are covered by manufacturing tests.
2. Current consumption and power dissipation measured for single channel software application (HD 1.0) running at 127 MHz on core and 65 MHz on SDRAM interface with FW version STA680-51001569-0D000003-C0004.000.
3. Current consumption and power dissipation measured for dual channel software application (HD 1.5) running at 127 MHz on core and 130 MHz on SDRAM interface with FW version STA680-51001569-0D000033-C0004.000.
4. VDD_IO generally refers to the supply of the VDD_GEN_IO, VDD_FSH_IO and VDD_RAM_IO groups.
5. Performed on all the input pins excluded the pull-down and pull-up ones.
6. VDD_GEN_IO may be VDD_FHS_IO or VDD_GEN_IO depending on interface considered.
7. Performed only on the Input pins with pull up.
8. Performed only on the Input pins with pull down.
9. Guaranteed by Ipu measurements.
10. Guaranteed by Ipd measurements.
11. XmA = 4mA for a BD4, 8 mA for BD8 pad type.
12. Dielectric = X7R ESR_{max} = 100 ohm, 2.2 μF ±5% or any above 3 μF±10% but less than 4.7 μF±10%. It is also recommended to distribute the 2.2 μF capacitance on the board by placing equivalent number of smaller capacitance value (for example, 470 nF) near each VDD_REG1V8 supply pad.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 LFBGA168 (12x12x1.4 mm) package information

Figure 14. LFBGA168 (12x12x1.4 mm) package outline

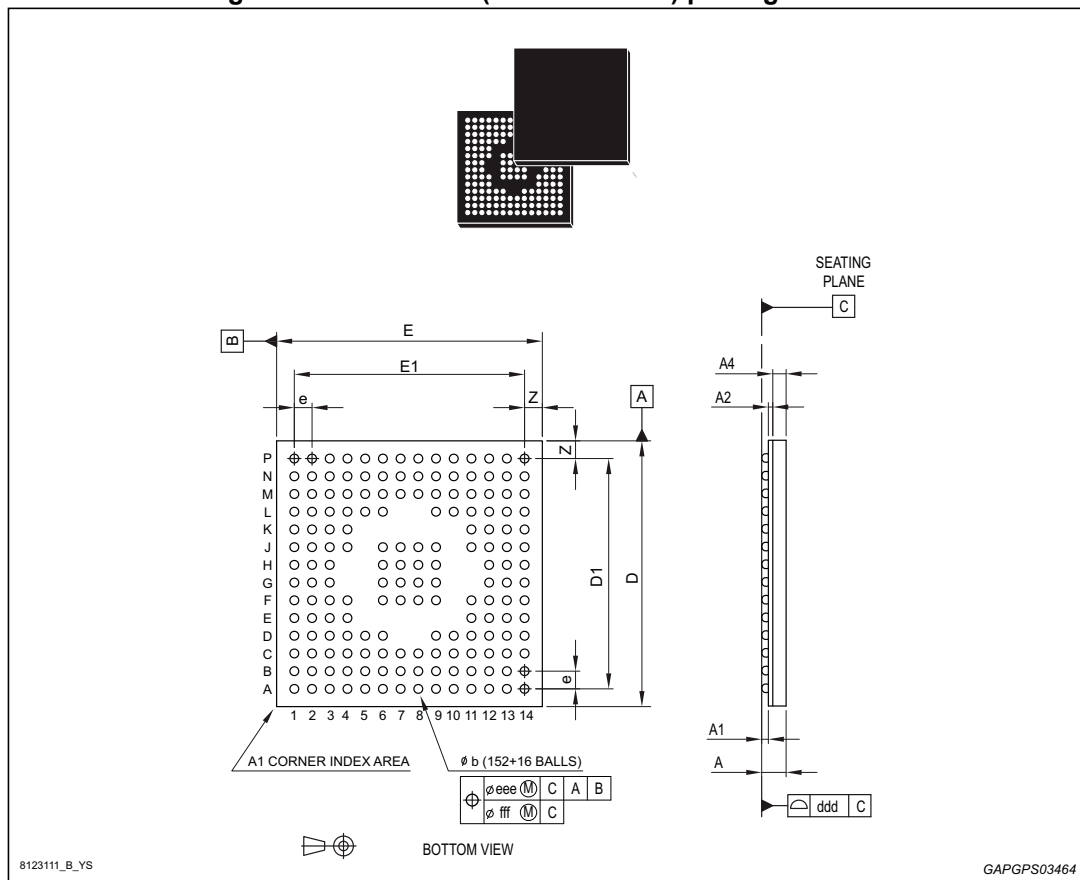


Table 21. LFBGA168 (12x12x1.4 mm) package mechanical data

Ref	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.400	-	-	0.0551
A1	0.210	-	-	0.0083	-	-
A2	-	0.200	-	-	0.0078	-
A4	-	-	0.800	-	-	0.0315
b	0.350	0.400	0.450	0.0138	0.0157	0.0177
D	11.850	12.000	12.150	0.4665	0.4724	0.4783
D1	-	10.400	-	-	0.4094	-
E	11.850	12.000	12.150	0.4665	0.4724	0.4783
E1	-	10.400	-	-	0.4094	-
e	-	0.800	-	-	0.0315	-
Z	-	0.800	-	-	0.0315	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

7.2 TFBGA289 (15x15x1.2 mm) package information

Figure 15. TFBGA289 (15x15x1.2 mm) package outline

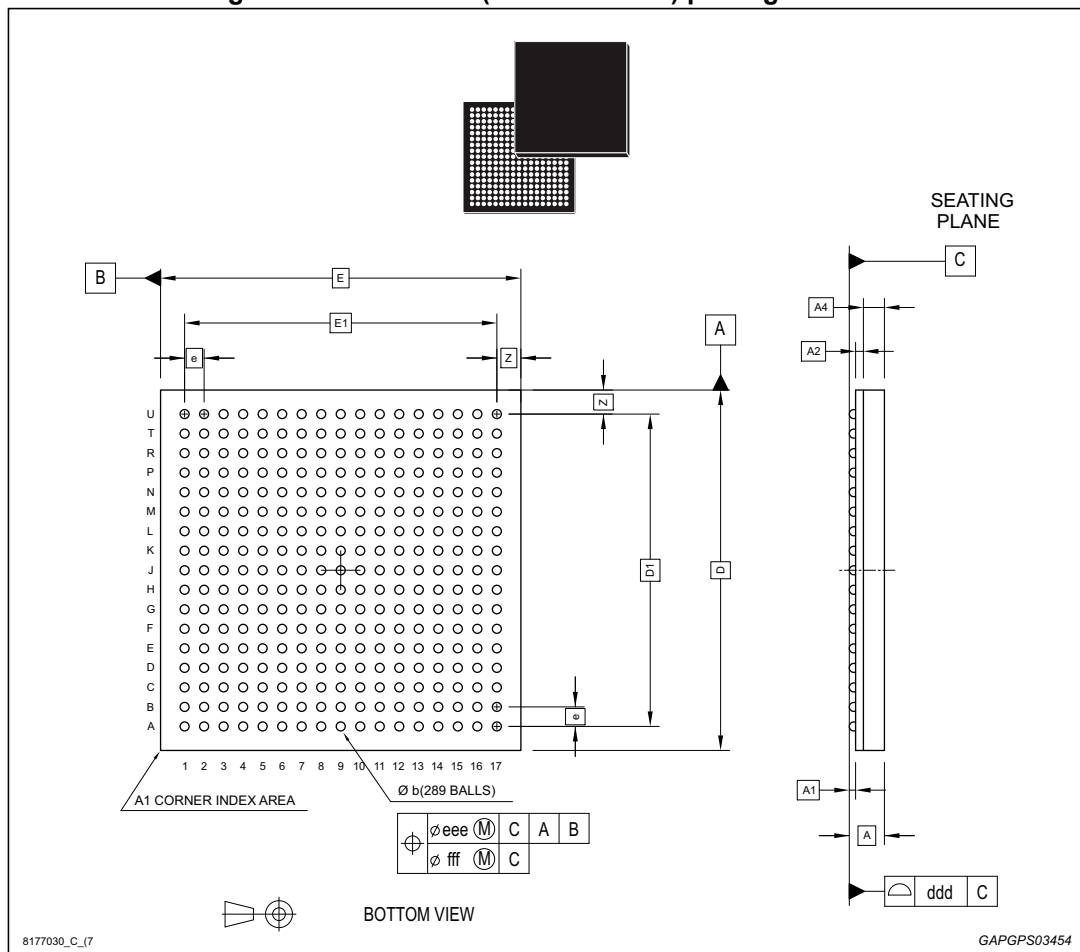


Table 22. TFBGA289 (15x15x1.2 mm) package mechanical data

Ref	Dimensions					
	Millimeters			Inches ⁽¹⁾		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.200	-	-	0.0472
A1	0.210	-	-	0.0083	-	-
A2	-	0.200	-	-	0.0079	-
A4	-	-	0.620	-	-	0.0244
b	0.350	0.400	0.480	0.0138	0.0157	0.0189
D	14.850	15.000	15.150	0.5846	0.5906	0.5965
D1	-	12.800	-	-	0.5039	-
E	14.850	15.000	15.150	0.5846	0.5906	0.5965
E1	-	12.800	-	-	0.5039	-
e	-	0.800	-	-	0.0315	-
Z	-	1.100	-	-	0.0433	-
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

8 Revision history

Table 23. Document revision history

Date	Revision	Changes
25-Jul-2008	1	Initial release.
19-Dec-2008	2	Update ECOPACK [®] information in Section 7 on page 42 .
31-Jul-2009	3	Added Section 2: HD Radio™ system on page 7 . Changed Table 2, 4, 7, 12, 13, 13, 17 and 20 ; Changed Figure 14, 15, 6, 3, 8 and 11 . Add Figure 10: Crystal characteristics on page 26 .
09-Nov-2010	4	Document status promoted from preliminary data to datasheet. Modified Features . and Description on page 1 . Modified the flow of the sections. Modified Section 1: Block diagram and pin description . Add Section 2: General description . Changed Figure 7: Power on timing and updated Table 4: Power on timing parameters . Modified Section 5.5: Serial peripheral interfaces (SPI) . Updated Section 6: Electrical specifications .
01-Feb-2011	5	Updated Table 20: DC electrical characteristics .
23-Mar-2012	6	Modified Section 2.1: Receiver system overview on page 21 . Modified Section 2.3: Dual channel HD 1.5 Radio processing on page 22 . Modified Figure 7: Power on timing on page 25 ; Section 4.1: Oscillator setting time on page 26 ; Table 6: Baseband interfaces pin list on page 29 ; Table 11: Host micro SPI pin list on page 34 ; Section 5.6: I²C interfaces on page 35 Table 15: I2C1 interface device address on page 36 .
26-Nov-2012	7	Modified Table 18: Absolute maximum ratings on page 38 . Modified Table 19: Thermal data on page 38 . Modified Table 20: DC electrical characteristics on page 39 .
17-Sep-2013	8	Updated disclaimer.
18-Dec-2013	9	Updated Table 1: Device summary on page 1 .
01-Jul-2015	10	Updated: Table 1: Device summary on page 1 ; Section 1.2: Ball-out description ; Table 5: Interface list on page 28 ; Table 19: Thermal data on page 38 and Section 7: Package information .

Table 23. Document revision history (continued)

Date	Revision	Changes
14-Apr-2016	11	Updated document Title. Added: "AEC-Q100 qualified" as first <i>Features</i> in cover page. Removed LQFP144 package image and 'STA680Q' Order code in <i>Table 1: Device summary</i>. Updated: <i>Section 1.2: Ball-out description</i>; <i>Figure 4: System block diagrams on page 20</i>; <i>Section 2.1: Receiver system overview</i>; <i>Section 2.2: HD Radio processing</i>; <i>Section 3.1: Clock schemes</i>; <i>Section 3.2: Power on</i>; <i>Section 4: Power supply ramp-up phase</i>; <i>Section 5.1: Interfaces: LFBGA vs. TFBGA</i>; <i>Section 5.2: Base-band I²S interface</i>; <i>Section 5.3: Base-band I²S interface frequency diversity</i>; <i>Section 5.4.1: Output serial audio interface (SAI)</i>; <i>Section 5.5.2: Flash serial peripheral interface (SPI2)</i>; <i>Section 5.6: I²C interfaces</i>; <i>Section 5.7: SDRAM interface</i>; <i>Section 6.1: Absolute maximum ratings</i>; <i>Section 6.2: Thermal data</i>. <i>Section 6.3: Operating conditions</i>; and <i>Section 7: Package information</i>.
17-Mar-2017	12	Updated: – <i>Features</i> and <i>Description</i> in cover page; – <i>Table 2: Ball-out description</i>; – <i>Section 4.2: Boot sequence</i>; – <i>Table 6: Baseband interfaces pin list</i>; – <i>Table 8: AIF pin list</i>; – <i>Section 5.4.1: Output serial audio interface (SAI)</i>; – Added paragraph title <i>Section 5.4.2: Input serial audio interface</i>; – <i>Section 5.4.3: Audio sample rate converter (ASRC)</i> – <i>Section 5.5: Serial peripheral interfaces (SPI)</i>; – <i>Table 11: Host micro SPI pin list</i>; – <i>Table 12: Flash SPI pin list</i>; – <i>Section 5.7: SDRAM interface</i>.
22-Mar-2019	13	Updated: – <i>Table 18: Absolute maximum rating on page 38</i>; – <i>Table 20: DC electrical characteristics on page 39</i>.

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