IXYS

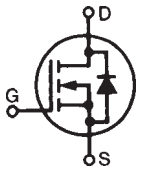
PolarHV™ HiPerFET Power MOSFET ISOPLUS247™

(Electrically Isolated Back Surface)

IXFR 48N60P

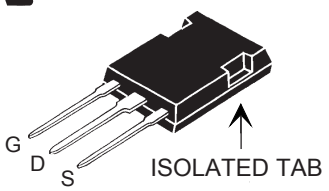
V_{DSS} = 600 V
I_{D25} = 32 A
$R_{DS(on)}$ ≤ 150 mΩ
t_{rr} ≤ 200 ns

N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25° C to 150° C	600	V
V_{DGR}	T_J = 25° C to 150° C; R_{GS} = 1 MΩ	600	V
V_{GSS}	Continuous	±30	V
V_{GSM}	Transient	±40	V
I_{D25}	T_C = 25° C	32	A
I_{DM}	T_C = 25° C, pulse width limited by T_{JM}	110	A
I_{AR}	T_C = 25° C	32	A
E_{AR}	T_C = 25° C	70	mJ
E_{AS}	T_C = 25° C	2.0	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤100 A/μs, $V_{DD} \le V_{DSS}$, T_J ≤150° C, R_G = 4 Ω	20	V/ns
P_D	T_C = 25° C	300	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
V_{ISOL}	50/60 Hz, RMS, 1 minute	2500	V~
F_C	Mounting Force	20..120 / 4.5..26	N/lb.
Weight		5	g

ISOPLUS247 (IXFR)
E153432



G = Gate D = Drain
S = Source

Symbol (T_J = 25° C, unless otherwise specified)	Test Conditions	Characteristic Values Min.	Typ.	Max.	
BV_{DSS}	V_{GS} = 0 V, I_D = 250 μA	600			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 8 mA	3.0		5.0	V
I_{GSS}	V_{GS} = ±30 V_{DC}, V_{DS} = 0			±200	nA
I_{DSS}	$V_{DS} = V_{DSS}$			25	μA
	V_{GS} = 0 V, T_J = 125° C			1000	μA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = I_T$			150	mΩ

Features

- International standard isolated package
- UL recognized package
- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic diode

Advantages

- Easy to mount
- Space savings
- High power density

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Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 20 V; I_D = I_T, Notes 1, 2	35	53		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		8860		pF
C_{oss}			850		pF
C_{rss}			60		pF
$t_{d(on)}$	V_{DS} = 0.5 V_{DSS}, I_D = I_T, V_{GS} = 10 V R_G = 2 Ω (External)		30		ns
t_r			25		ns
$t_{d(off)}$			85		ns
t_f			22		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = I_T		150		nC
Q_{gs}			50		nC
Q_{gd}			50		nC
R_{thJC}				0.42	°C/W
R_{thCS}			0.15		°C/W

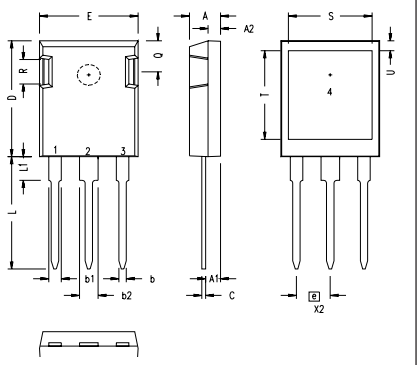
Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0 V			32	A
I_{SM}	Repetitive			110	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Note 1			1.5	V
t_{rr}	I_F = 20A, -di/dt = 100 A/µs V_R = 480V			200	ns
Q_{RM}			0.8		µC
I_{RM}			6.0		A

Notes:

1. Pulse test, t ≤300 µs, duty cycle d ≤ 2 %;
2. Test current I_T = 24 A.

ISOPLUS247 Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or moreof the following U.S. patents: 4,835,592 4,850,072 4,881,106 4,931,844 5,017,508 5,034,796 5,049,961 5,063,307 5,187,117 5,237,481 5,381,025 5,486,715 6,162,665 6,259,123 B1 6,306,728 B1 6,404,065 B1 6,534,343 6,583,505 6,683,344 6,710,405B2 6,710,463 6,727,585 6,759,692 6,771,478 B2

Fig. 1. Output Characteristics @ 25°C

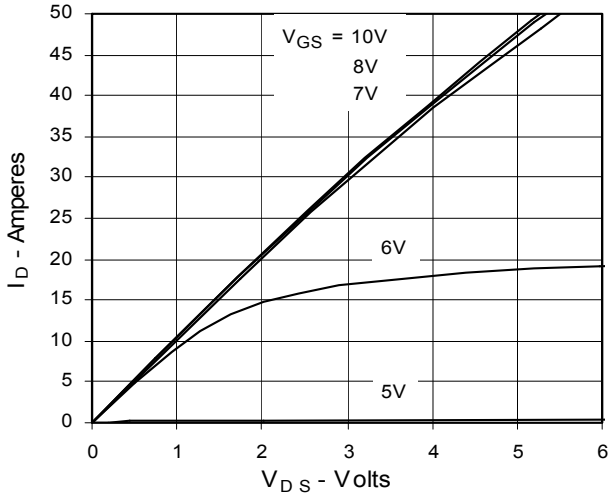


Fig. 2. Extended Output Characteristics @ 25°C

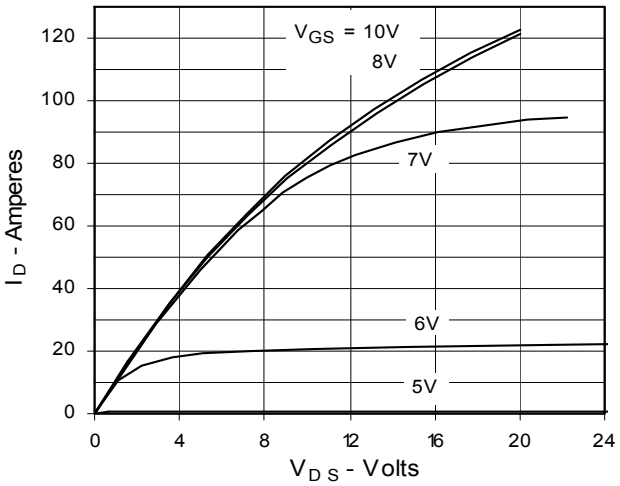


Fig. 3. Output Characteristics @ 125°C

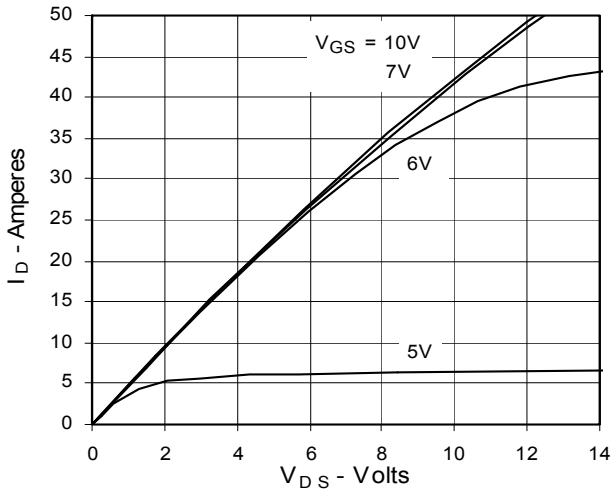


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 24A Value vs. Junction Temperature

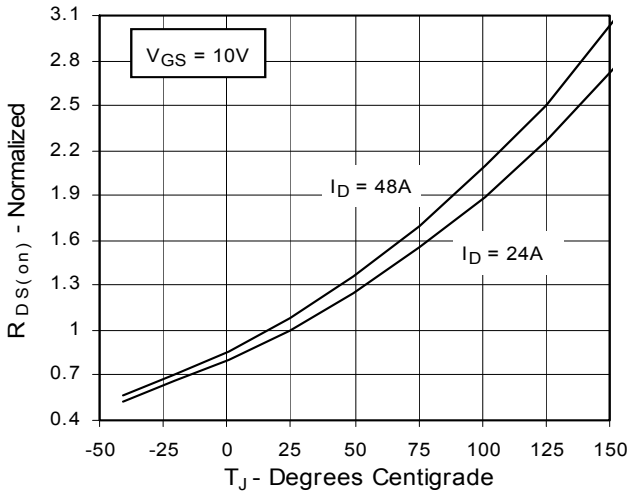


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 24A Value vs. Drain Current

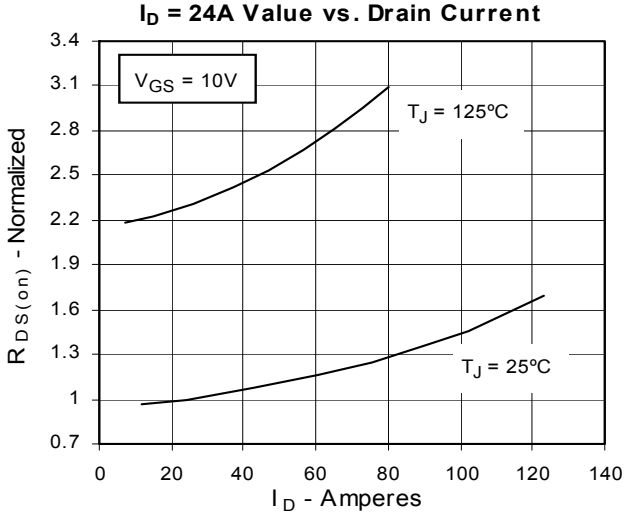
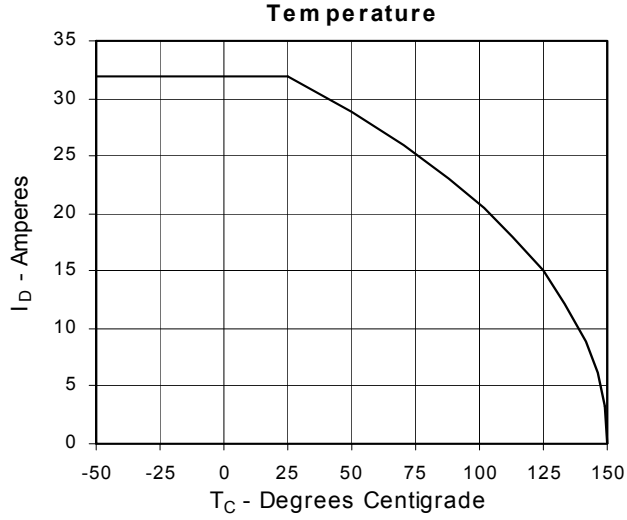


Fig. 6. Drain Current vs. Case Temperature



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Fig. 7. Input Admittance

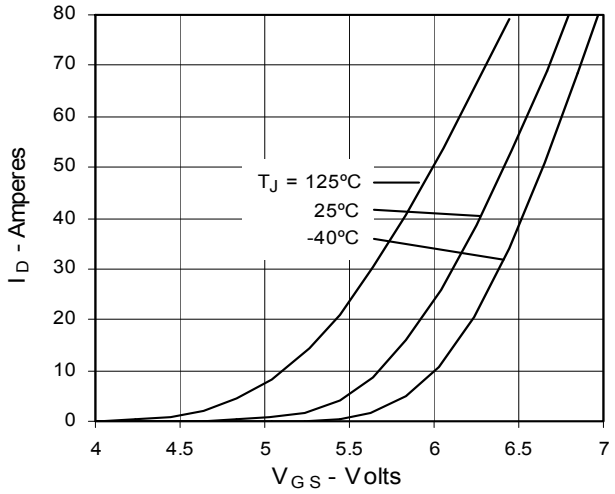


Fig. 8. Transconductance

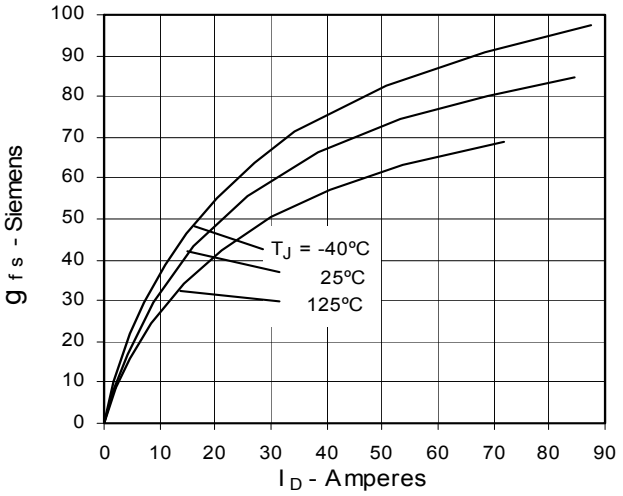


Fig. 9. Source Current vs. Source-To-Drain Voltage

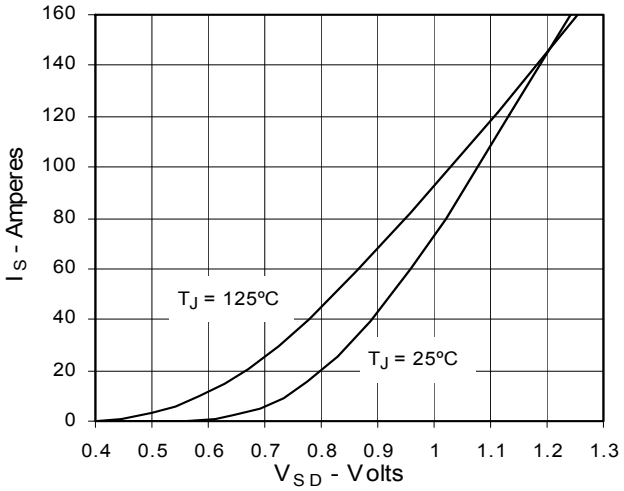


Fig. 10. Gate Charge

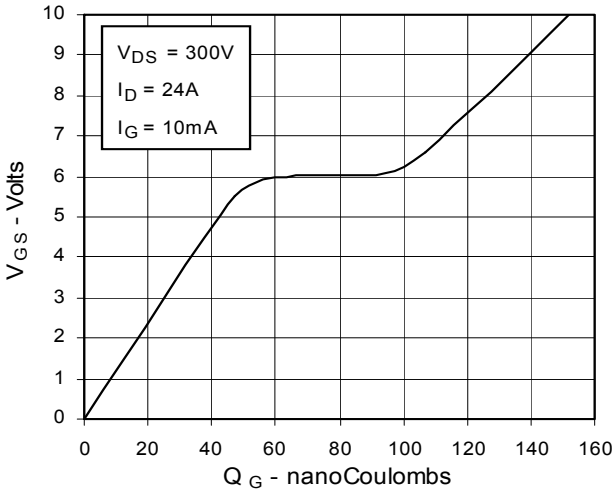


Fig. 11. Capacitance

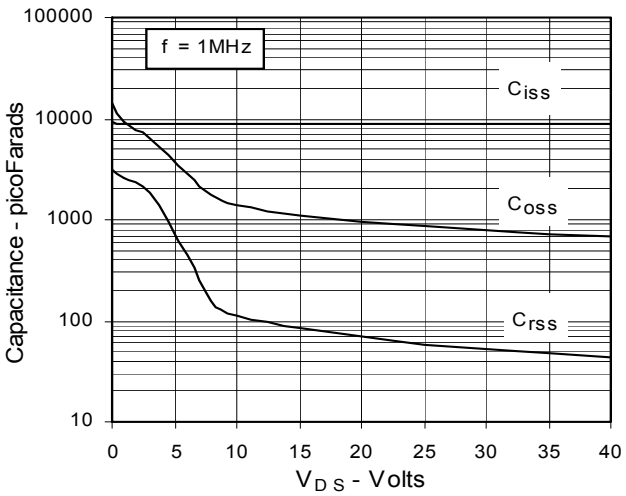
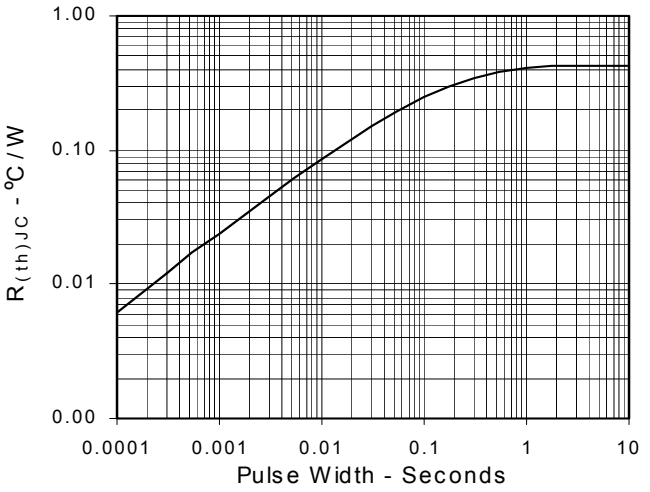


Fig. 13. Maximum Transient Thermal Resistance



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