

LTM4604A

2.375V_{IN(MIN)}, 4A Step-Down μModule Regulator

DESCRIPTION

Demonstration circuit 1392A features the LTM®4604AEV, the high efficiency, high density switch mode step-down μModule® regulator. The input voltage range is from 2.375V to 5.5V with a jumper selectable output voltage from 0.8V to 3.3V. The rated load current is 4A, while derating is necessary for certain V_{IN}, V_{OUT} and thermal conditions. By using the TRACK pin, the output can be set to coincidentally or ratiometrically track to another voltage rail.

The LTM4604A data sheet must be read in conjunction with this demo manual prior to working on or modifying demo circuit DC1392A.

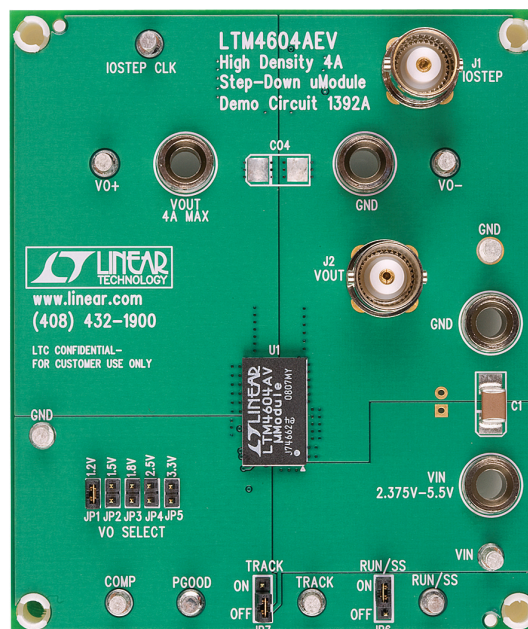
Design files for this circuit board are available at <http://www.linear.com/demo>

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PERFORMANCE SUMMARY (T_A = 25°C)

PARAMETER	CONDITION	VALUE
Input Voltage Range		2.375V to 5.5V
Output Voltage, V _{OUT}	Jumper Selectable (Open for 0.8V)	1.2V, 1.5V, 1.8V, 2.5V, 3.3V; ±2%
Maximum Continuous Output Current	Derating is Necessary for Certain V _{IN} , V _{OUT} and Thermal Conditions	4A DC
Default Operating Frequency		1.25MHz
Efficiency	V _{IN} = 5V, V _{OUT} = 3.3V, I _{OUT} = 4A	88% Typical, See Figure 3

BOARD PHOTO



dc1392af

DEMO MANUAL DC1392A

QUICK START PROCEDURE

Demonstration circuit 1392A is an easy way to evaluate the performance of the LTM4604AEV. Please refer to Figure 1 for proper measurement equipment setup and follow the procedure below:

1. Place jumpers in the following positions for a typical $1.2V_{OUT}$ application:

VO SELECT	TRACK	RUN/SS
1.2V	OFF	ON

2. With power off, connect the input power supply, load and meters as shown in Figure 1. Preset the load to 0A and V_{IN} supply within the operating range of the LTM4604A.
3. Turn on the power at the input. The output voltage should be $1.2V \pm 2\%$.

4. Once the proper output voltage is established, adjust the load within the operating range and observe the output voltage regulation, ripple voltage, efficiency and other parameters
5. To measure input and output ripple, please refer to Figure 2 for proper setup.
6. For optional load transient test, apply adjustable pulse signal between IOSTEP CLK and GND pins. Pulse amplitude sets the current step. The pulse signal should have very small duty cycle ($<5\%$) to limit the thermal stress on the transient load circuit. The output transient current can be monitored at BNC connector J1 (10mV/A), the output voltage can be monitored at BNC connector J2.

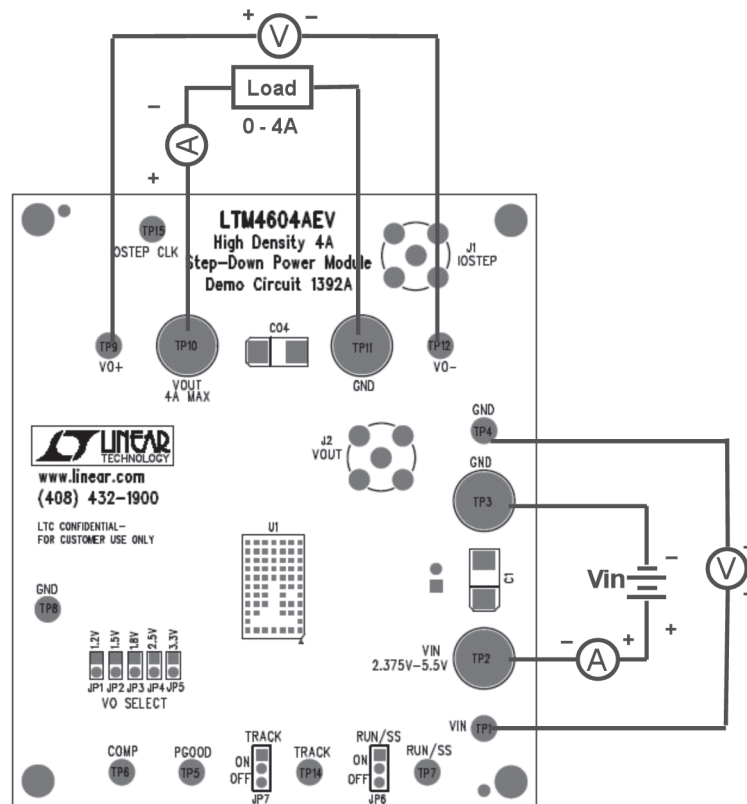


Figure 1. Test Setup of DC1392A

QUICK START PROCEDURE

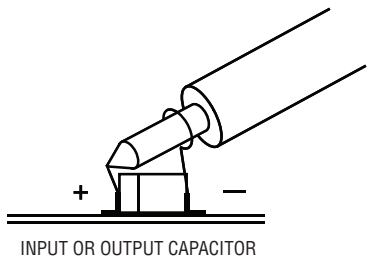


Figure 2. Scope Probe Placements for Measuring Input or Output Ripple

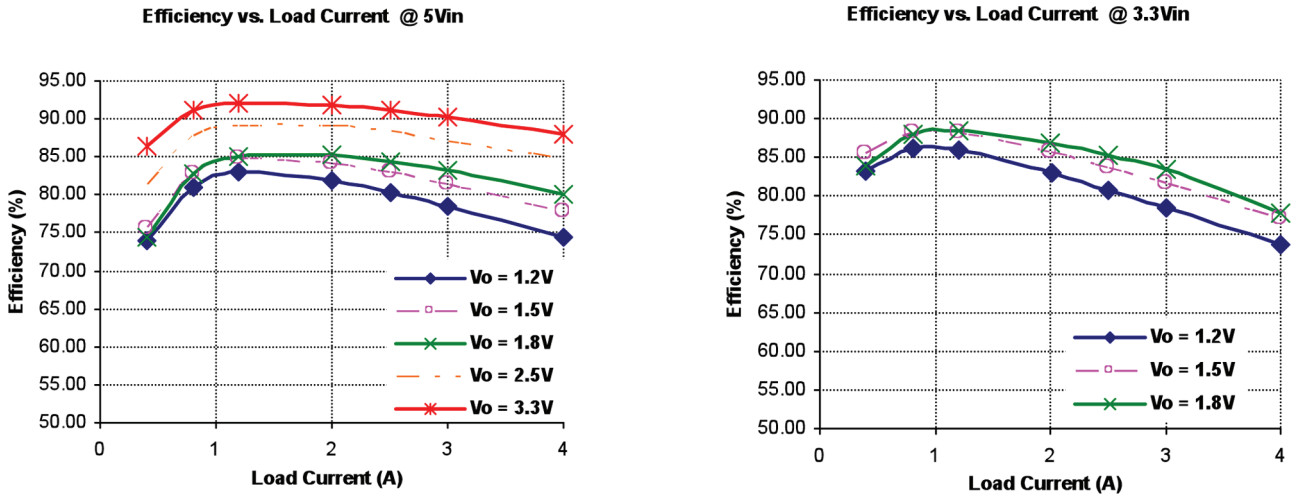


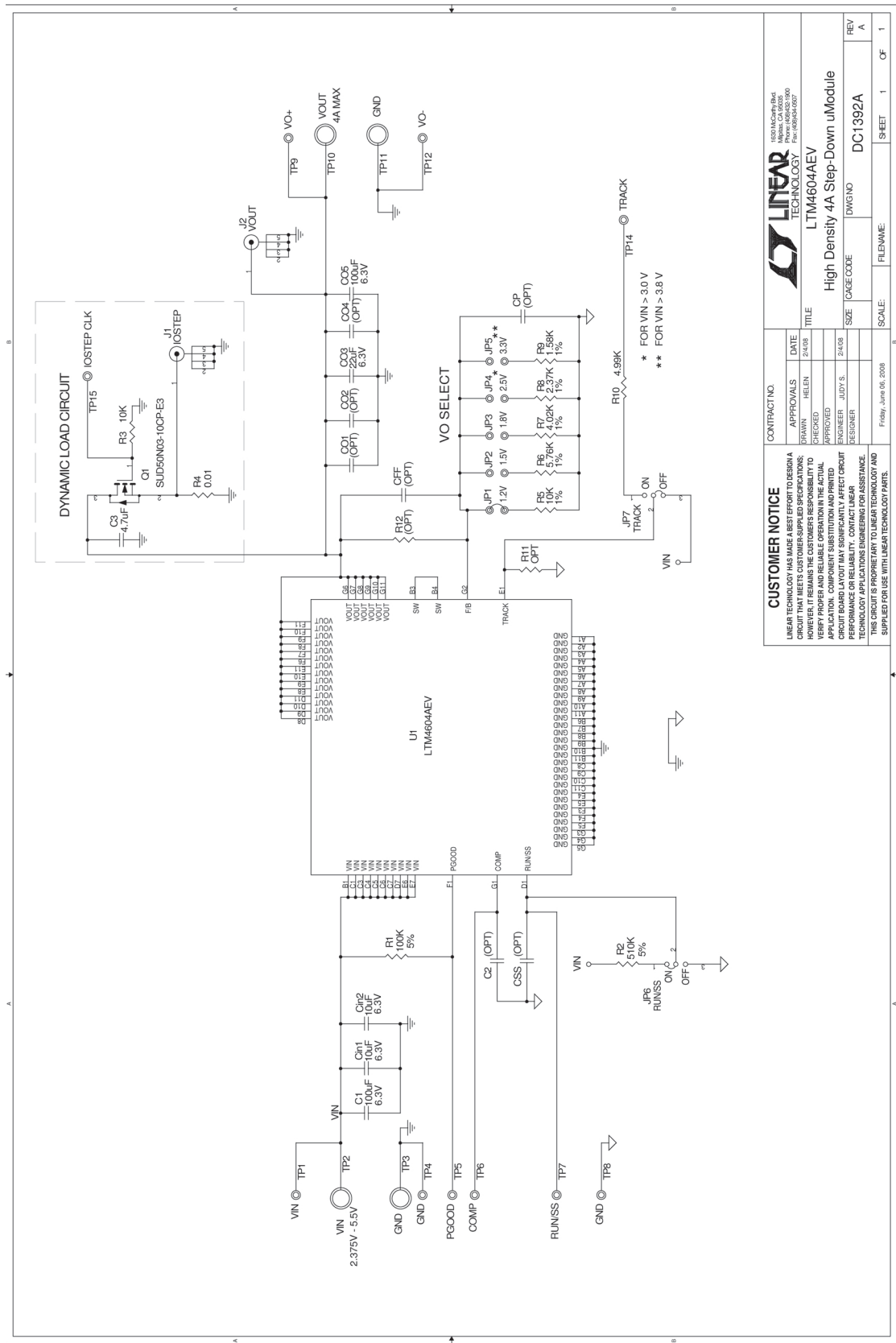
Figure 3. Measured Supply Efficiency with Different V_{IN} and V_{OUT}

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PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	C1, C05	CAP, X5R, 100 μ F, 6.3V, 20%, 1812	TDK, C4532X5R0J107M
2	2	CIN1, CIN2	CAP, X5R, 10 μ F, 6.3V, 10%, 1206	AVX, 12066D106KAT2A
3	1	C03	CAP, X5R, 22 μ F, 6.3V, 10%, 1206	AVX, 12066D226KAT2A
4	1	R5	RES., CHIP, 10k, 1/16W, 1%, 0603	VISHAY, CRCW060310K0FKEA
5	1	R2	RES., CHIP, 510k, 1/16W, 5%, 0603	VISHAY, CRCW0603510KJNEA
6	1	U1	I.C., LTM4604AEV	LINEAR TECH., LTM4604AEV#PBF
Additional Demo Board Circuit Components				
1	0	C2 (OPT)	CAP, 0603	
2	1	C3	CAP, X5R, 4.7 μ F, 6.3V, 10%, 0603	AVX, 06036D475KAT2A
3	0	C01, C02 (OPT)	CAP, 1210	
4	0	C04 (OPT)	CAP, 1812	
5	0	CSS, CP, CFF (OPT)	CAP, 0603	
6	1	Q1	N-CHANNEL 30V MOSFET, TO-252	VISHAY, SUD50N03-10CP-E3
7	1	R1	RES., CHIP, 100K, 1/16W, 5%, 0603	VISHAY, CRCW0603100KJNEA
8	1	R3	RES., CHIP, 10K, 1/16W, 1%, 0603	VISHAY, CRCW060310K0FKEA
9	1	R4	RES., CHIP, 0.01 Ω , 0.5W, 1%, 1206	VISHAY, WSL1206R0100FEA18
10	1	R6	RES., CHIP 5.76k, 1/16W, 1%, 0603	VISHAY, CRCW06035K76FKEA
11	1	R7	RES., CHIP 4.02k, 1/16W, 1%, 0603	VISHAY, CRCW06034K02FKEA
12	1	R8	RES., CHIP, 2.37k, 1/16W, 1%, 0603	VISHAY, CRCW06032K37FKEA
13	1	R9	RES., CHIP, 1.58k, 1/16W, 1%, 0603	VISHAY, CRCW06031K58FKEA
14	0	R10-R12 (OPT)	RES., 0603	
Hardware—For Demo Board Only				
1	2	J1, J2	CONN, BNC, 5-PINS	CONNEX, 112404
2	5	JP1-JP5	2MM SINGLE ROW HEADER, 2-PIN	SAMTEC, TMM-102-02-L-S
3	2	JP6, JP7	2MM SINGLE ROW HEADER, 3-PIN	SAMTEC, TMM-103-02-L-S
4	3	JP1, JP6, JP7	SHUNT	SAMTEC, 2SN-BK-G
5	10	TP1, TP4-TP9, TP12, TP14, TP15	TESTPOINT, TURRET, 0.095"	MILL-MAX, 2501-2-00-80-00-00-07-0
6	4	TP2, TP3, TP10, TP11	BANANA JACK	KEYSTONE, 575-4
7	4	STAND OFF	STAND-OFF, NYLON 0.50" TALL	KEYSTONE, 8833 (SNAP ON)

SCHEMATIC DIAGRAM



CUSTOMER NOTICE		CONTRACT NO.	DATE
LINEAR TECHNOLOGY HAS MADE A BEST EFFORT TO DESIGN A CIRCUIT THAT MEETS CUSTOMER-SUPPLIED SPECIFICATIONS. CUSTOMER AGREES TO HOLD LINEAR TECHNOLOGY HARMLESS FROM AND AGAINST ALL CLAIMS, DAMAGES, LOSSES AND EXPENSES, INCLUDING REASONABLE ATTORNEY'S FEES, ARISING OUT OF OR RESULTING FROM THE APPLICATION OF THIS CIRCUIT. COMPONENT SUBSTITUTION AND PRINTED CIRCUIT BOARD LAYOUT MAY SIGNIFICANTLY AFFECT CIRCUIT PERFORMANCE OR RELIABILITY. CONTACT LINEAR TECHNOLOGY FOR ASSISTANCE.		APPROVALS	DATE
THIS CIRCUIT IS PROPRIETARY TO LINEAR TECHNOLOGY AND SUPPLIED FOR USE WITH LINEAR TECHNOLOGY PARTS.		DRAWN	2/4/08
		CHECKED	HELEN
		APPROVED	JUDY S.
		DESIGNER	JUDY S.
		SCALE	1 OF 1
		FILE NAME	DC1392A
		REV	A

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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