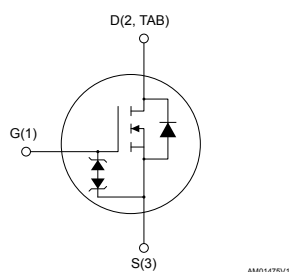


N-channel 1000 V, 5.4 Ω typ., 2.5 A SuperMESH™ Power MOSFETs in DPAK and TO-220FP packages



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	Package
STD3NK100Z	1000 V	6 Ω	2.5 A	DPAK
STF3NK100Z				TO-220FP

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

These high-voltage devices are Zener-protected N-channel Power MOSFETs developed using the SuperMESH™ technology by STMicroelectronics, an optimization of the well-established PowerMESH™. In addition to a significant reduction in on-resistance, these devices are designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link

[STD3NK100Z](#)
[STF3NK100Z](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		DPAK	TO-220FP	
V_{DS}	Drain-source voltage	1000		V
V_{GS}	Gate-source voltage	± 30		V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	2.5	2.5 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	1.57	1.57 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current (pulsed)	10	10	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	90	25	W
ESD	Gate-source human body model ($C = 100\text{ pF}$, $R = 1.5\text{ k}\Omega$)	3		kV
dv/dt ⁽³⁾	Peak diode recovery voltage slope	4.5		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ }^{\circ}\text{C}$)		2.5	kV
T_j	Operating junction temperature range	-55 to 150		$^{\circ}\text{C}$
T_{stg}	Storage temperature range			

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 2.5\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		DPAK	TO-220FP	
$R_{thj-case}$	Thermal resistance junction-case	1.39	5	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}$ ⁽¹⁾	Thermal resistance junction-pcb	50		
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	

1. When mounted on FR-4 board of 1 inch², 2 oz Cu.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR} ⁽¹⁾	Avalanche current, repetitive or not-repetitive	2.5	A
E_{AS} ⁽²⁾	Single pulse avalanche energy	110	mJ

1. Pulse width limited by T_{jmax} .
2. Starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V, I _D = 1 mA	1000			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 1000 V			1	μA
		V _{GS} = 0 V, V _{DS} = 1000 V, T _C = 125 °C ⁽¹⁾			50	μA
I _{GSS}	Gate-body leakage current	V _{DS} = 0 V, V _{GS} = ±30 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DS} = V _{GS} , I _D = 50 μA	3	3.75	4.5	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 1.25 A		5.4	6	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0 V	-	601	-	pF
C _{oss}	Output capacitance			53		
C _{rss}	Reverse transfer capacitance			12		
C _{oss eq.} ⁽¹⁾	Equivalent output capacitance	V _{GS} = 0 V, V _{DS} = 0 V to 800 V	-	15	-	pF
R _G	Gate input resistance	f = 1 MHz, open drain	-	8.6	-	Ω
Q _g	Total gate charge	V _{DD} = 800 V, I _D = 2.5 A,	-	18	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 0 to 10 V		3.6		
Q _{gd}	Gate-drain charge	(see Figure 16. Test circuit for gate charge behavior)		9.2		

1. C_{oss eq.} is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t _{d(on)}	Turn-on delay time	V _{DD} = 500 V, I _D = 1.25 A, R _G = 4.7 Ω, V _{GS} = 10 V	-	15	-	ns
t _r	Rise time			7.5		
t _{d(off)}	Turn-off delay time	(see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)		39		
t _f	Fall time			32		

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		2.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		10	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.5 \text{ A}$, $V_{GS} = 0 \text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 2.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	584		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100 \text{ V}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	2.3		μC
I_{RRM}	Reverse recovery current		-	8		A
t_{rr}	Reverse recovery time	$I_{SD} = 2.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$	-	628		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 100 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	2.5		μC
I_{RRM}	Reverse recovery current		-	8.1		A

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$, $I_D = 0 \text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

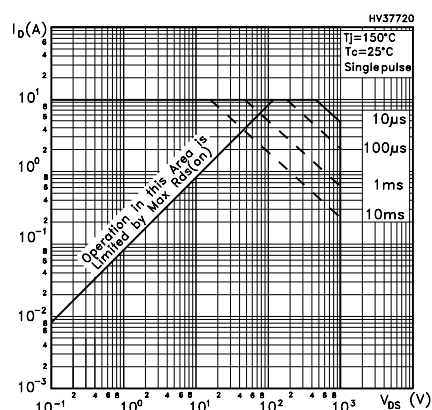
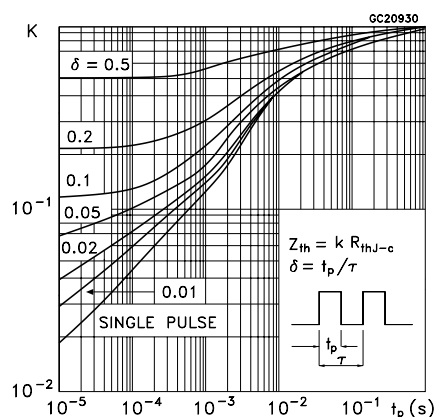
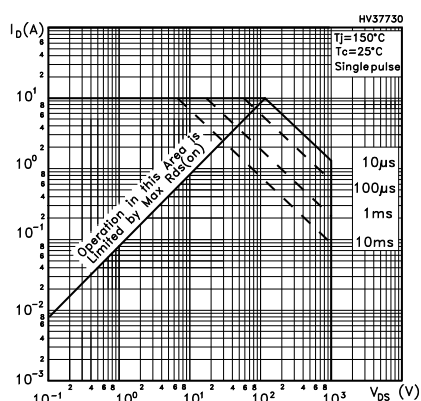
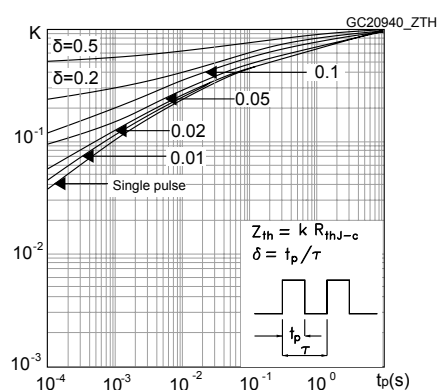
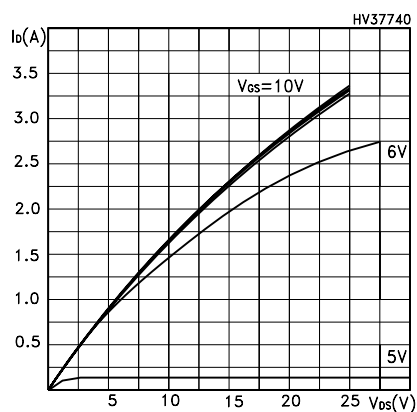
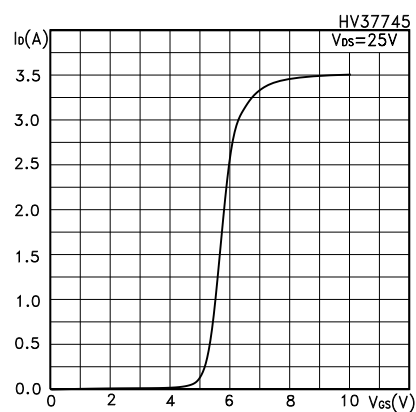
Figure 1. Safe operating area for DPAK

Figure 2. Thermal impedance for DPAK

Figure 3. Safe operating area for TO-220FP

Figure 4. Thermal impedance for TO-220FP

Figure 5. Output characteristics

Figure 6. Transfer characteristics


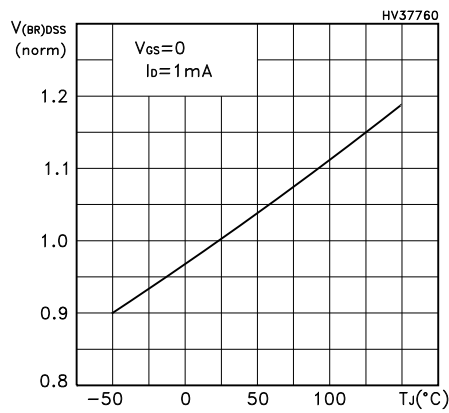
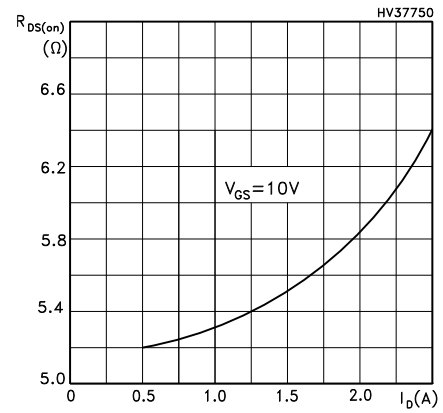
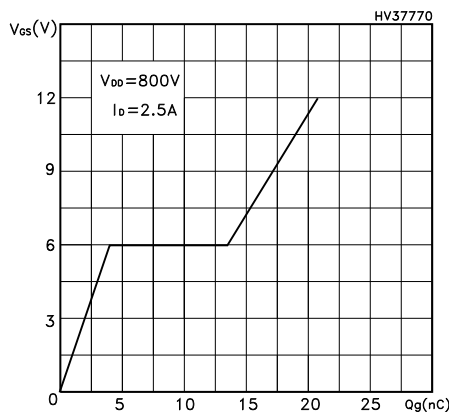
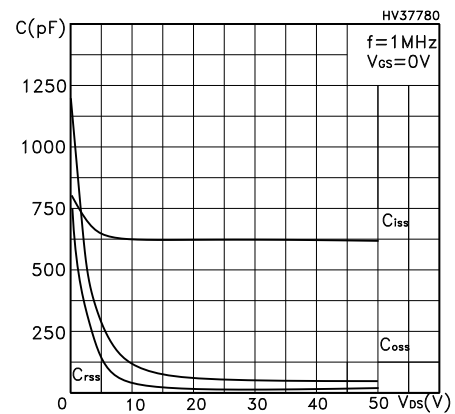
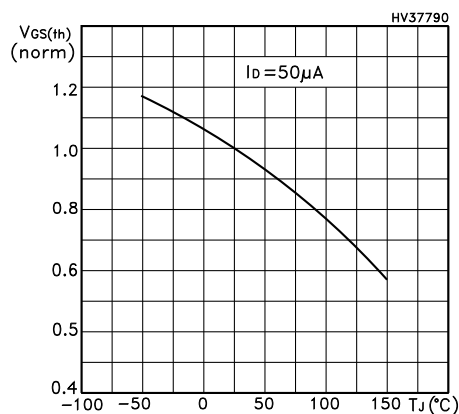
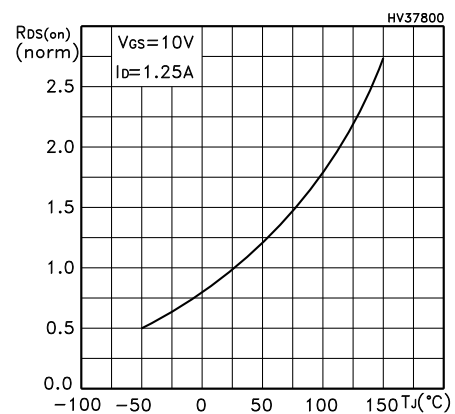
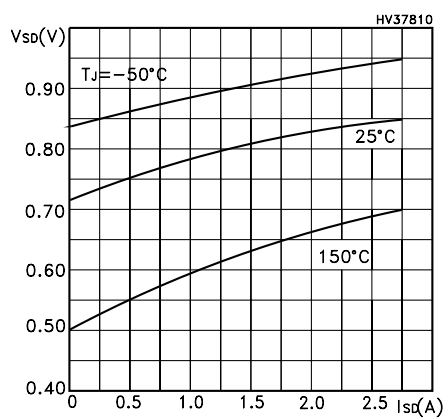
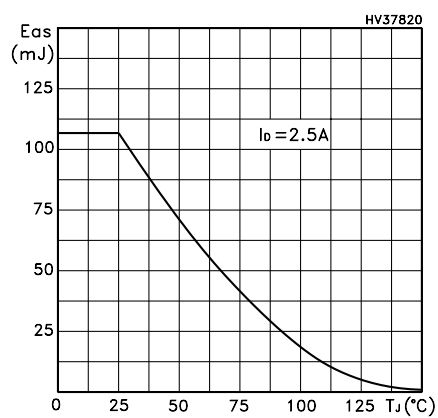
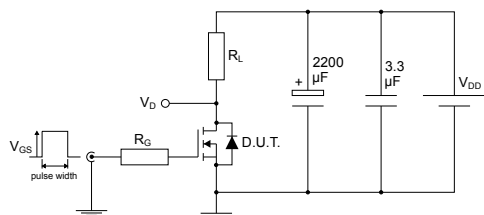
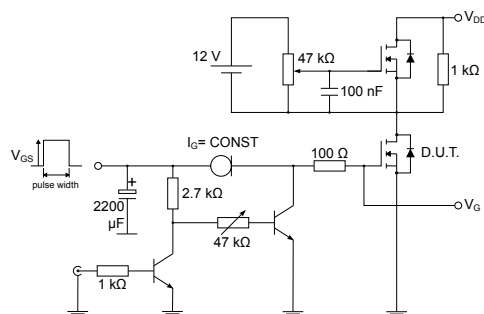
Figure 7. Normalized $V_{(BR)DSS}$ vs temperature

Figure 8. Static drain-source on resistance

Figure 9. Gate charge vs gate-source voltage

Figure 10. Capacitance variations

Figure 11. Normalized gate threshold voltage vs temperature

Figure 12. Normalized on resistance vs temperature


Figure 13. Source-drain diode forward characteristics

Figure 14. Maximum avalanche energy vs temperature


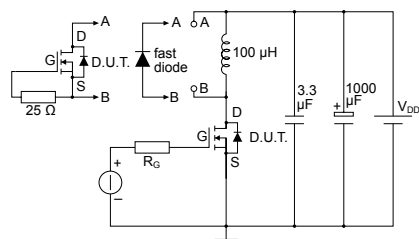
3 Test circuits

Figure 15. Test circuit for resistive load switching times


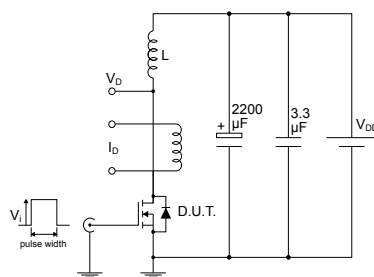
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Figure 16. Test circuit for gate charge behavior


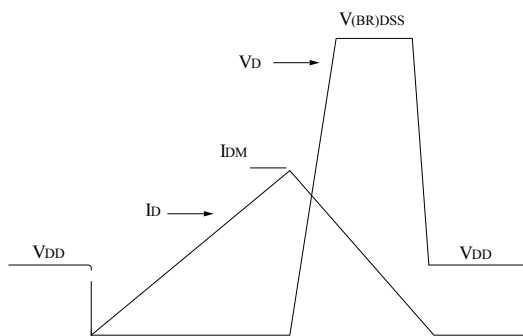
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Figure 17. Test circuit for inductive load switching and diode recovery times


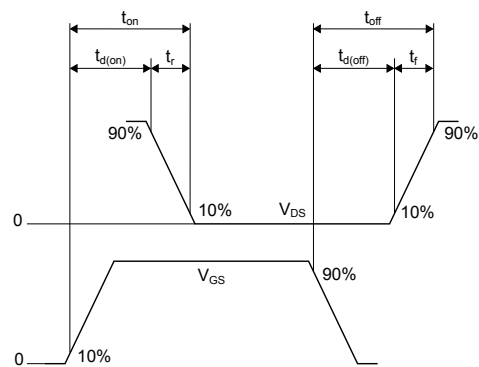
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Figure 18. Unclamped inductive load test circuit


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Figure 19. Unclamped inductive waveform


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Figure 20. Switching time waveform


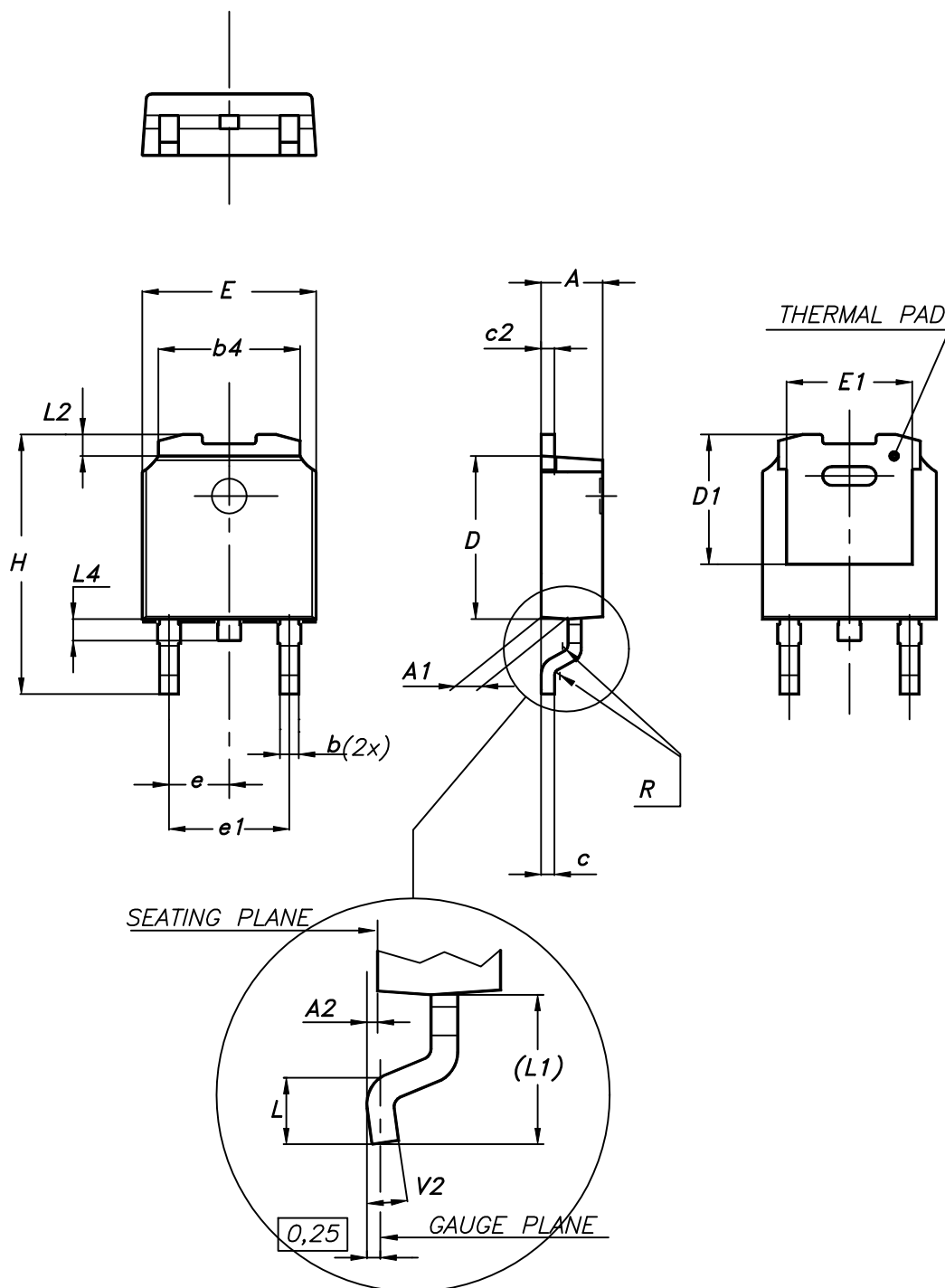
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 21. DPAK (TO-252) type A2 package outline



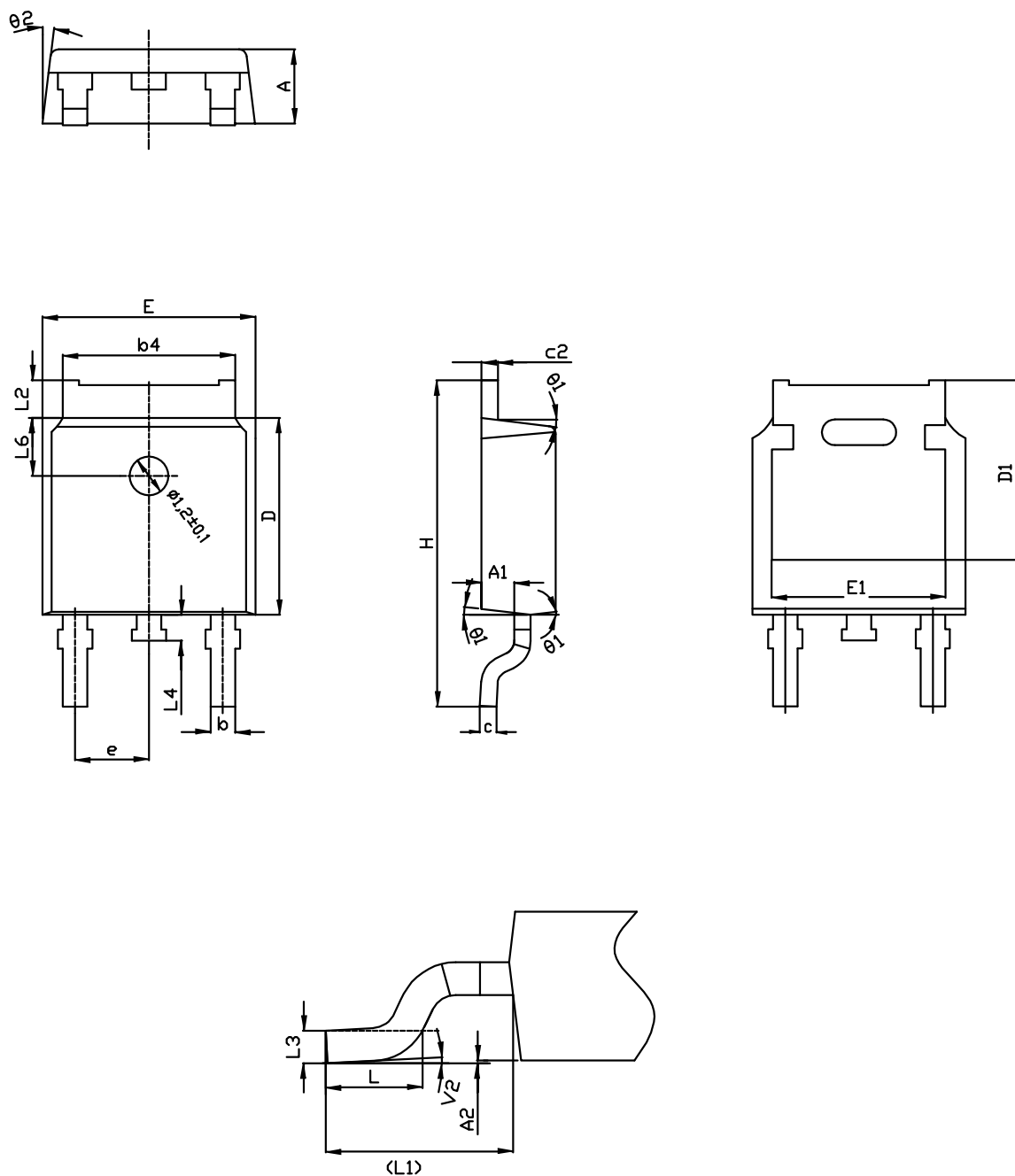
0068772_type-A2_rev25

Table 9. DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C2 package information

Figure 22. DPAK (TO-252) type C2 package outline

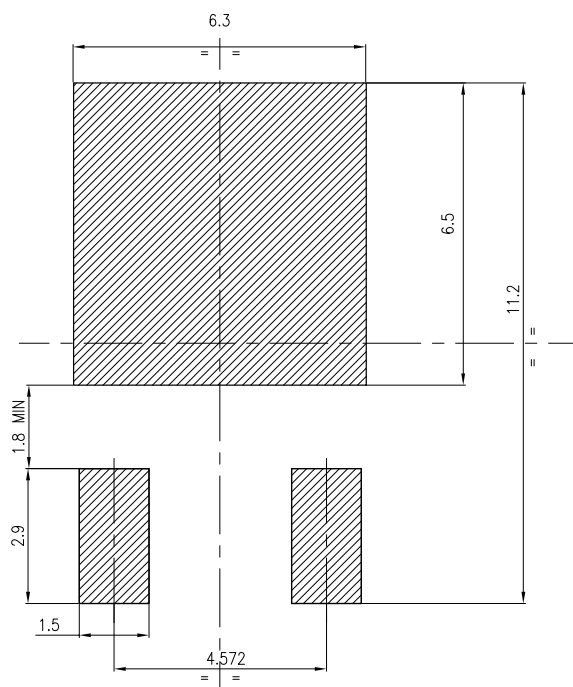


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Table 10. DPAK (TO-252) type C2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

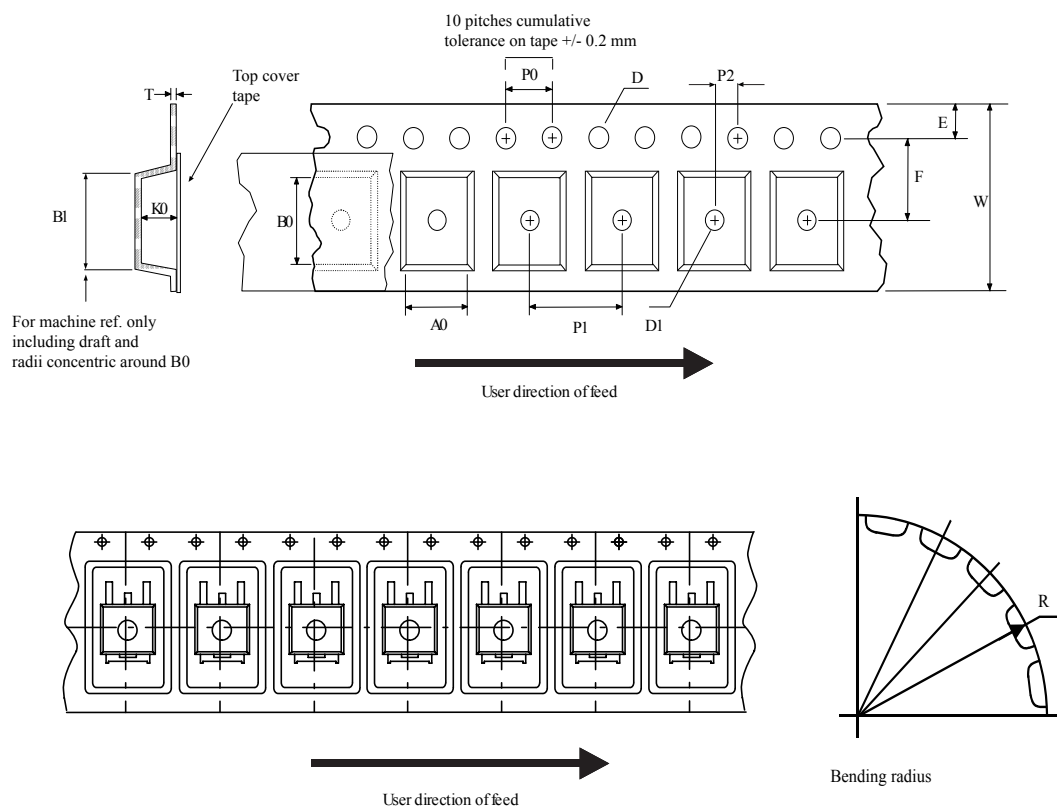
Figure 23. DPAK (TO-252) recommended footprint (dimensions are in mm)



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4.3 DPAK (TO-252) packing information

Figure 24. DPAK (TO-252) tape outline



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Figure 25. DPAK (TO-252) reel outline

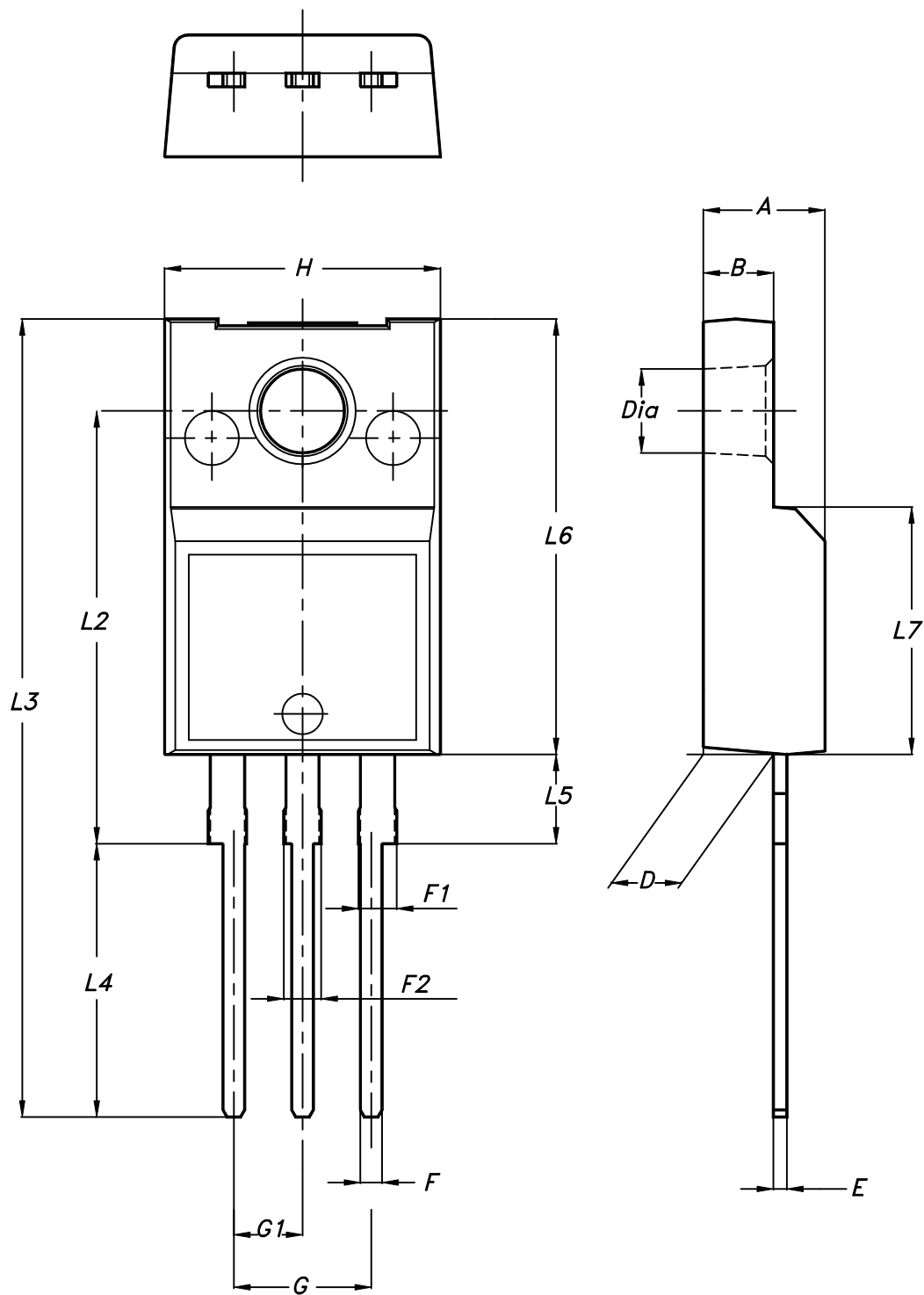

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Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220FP package information

Figure 26. TO-220FP package outline



7012510_Rev_12_B

Table 12. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Ordering information

Table 13. Order codes

Order code	Marking	Package	Packing
STD3NK100Z	D3NK100Z	DPAK	Tape and reel
STF3NK100Z	F3NK100Z	TO-220FP	Tube

Revision history

Table 14. Document revision history

Date	Version	Changes
17-May-2007	1	First release
18-Oct-2007	2	Added DPAK
02-Jul-2018	3	The part number STP3NK100Z has been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated title in cover page, Section 1 Electrical ratings, Section 2 Electrical characteristics and Section 4 Package information. Minor text changes.

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