TPS61256A 3.5-MHz HIGH EFFICIENCY STEP-UP CONVERTER FEATURING 2.3A CURRENT LIMIT IN CHIP SCALE PACKAGING

1 Features

- 93% Efficiency at 3.5MHz Operation
- 36µA Quiescent Current
- Wide V_{IN} Range From 2.5V to 5.5V
- I_{OUT} ≥1000mA at V_{OUT} = 5.0V, V_{IN} ≥3.3V
- ±2% Total DC Voltage Accuracy
- Light-Load PFM Mode
- True Load Disconnect During Shutdown
- Thermal Shutdown and Overload Protection
- Only Three Surface-Mount External Components Required
- Total Solution Size <35mm^2
- 9-Pin NanoFree^{TM} (CSP) Packaging

2 Applications

- Cell Phones, Smart-Phones
- Tablet PCs
- Mono and Stereo APA Applications

3 Description

The TPS61256A device provides a power supply solution for battery-powered portable applications. Intended for low-power applications, the TPS61256A supports up to 800-mA load current from a battery discharged as low as 2.7V and allows the use of low cost chip inductor and capacitors.

With a wide input voltage range of 2.5V to 5.5V, the device supports applications powered by Li-Ion batteries with extended voltage range and delivers a fixed 5.0V output voltage.

The TPS61256A operates at a regulated 3.5-MHz switching frequency and enters power-save mode operation at light load currents to maintain high efficiency over the entire load current range. The PFM mode extends the battery life by reducing the quiescent current to 36µA (typ) during light load operation. Input current in shutdown mode is less than 5µA, which maximizes battery life.

The TPS61256A offers a very small solution size due to minimum amount of external components. It allows the use of small inductors and input capacitors to achieve a small solution size. During shutdown, the load is completely disconnected from the battery.

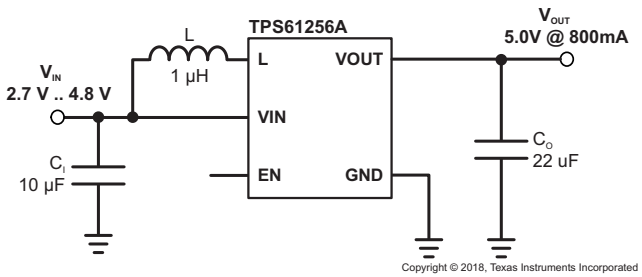
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Device Information(1)

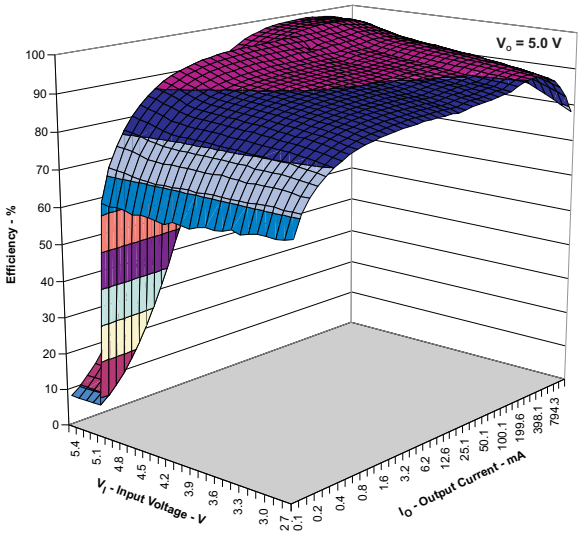
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS61256A	YFF	1.206 mm × 1.306 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Smallest Solution Size Application



Efficiency vs. Load Current



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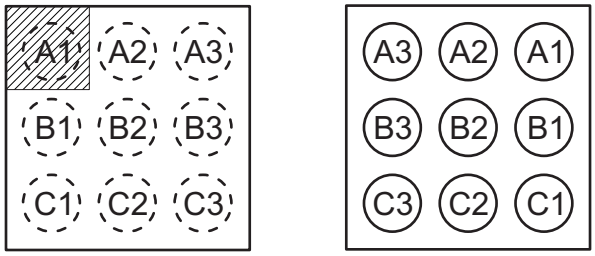
4 Revision History

Changes from Original (July 2011) to Revision A **Page**

- *First public release of data sheet.* ... 1
- *See Table of Contents for new data sheet format and added sections.* ... 2

5 Pin Configuration and Functions

YFF Package
9-Bump DSBGA
Top View



Pin Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	B3	I	This is the enable pin of the device. Connecting this pin to ground forces the device into shutdown mode. Pulling this pin high enables the device. This pin must not be left floating and must be terminated.
GND	C1, C2, C3		Ground pin.
SW	B1, B2	I/O	This is the switch pin of the converter and is connected to the drain of the internal Power MOSFETs.
VIN	A3	I	Power supply input.
VOUT	A1, A2	O	Boost converter output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
Input voltage	Voltage at VIN(2), VOUT(2), SW(2), EN(2)	–0.3 to 7	V
Input current	Steady state DC current into SW	2.3	A
Power dissipation		Internally limited	
Temperature range	Operationg temperature range, T_A (3)	–40 to 85	°C
	Operating virtual junction, T_J	–40 to 150	°C
	Storage temperature range, T_{stg}	–65 to 150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to network ground terminal.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max)} - (\theta_{JA} \times P_{D(max)})$. To achieve optimum performance, it is recommended to operate the device with a maximum junction temperature of 105°C.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ (1)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (2)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (3)	±1000	V
		Machine Model - (MM)	±200	V

(1) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin. The machine model is a 200-pF capacitor discharged directly into each pin.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(3) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_I	Input voltage range	2.5		4.85	V
R_L	Minimum resistive load for start-up	55			Ω
L	Inductance	0.7	1.0	2.9	µH
C_O	Output capacitance	10	20	50	µF
T_A	Ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC		TPS61256A YFF 9 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	18	
ψ_{JT}	Junction-to-top characterization parameter	4.2	
ψ_{JB}	Junction-to-board characterization parameter	17.9	

6.5 Electrical Characteristics

Minimum and maximum values are at V_{IN} = 2.5V to 5.5V, V_{OUT} = 5.0V (or V_{IN}, whichever is higher), EN = 1.8V, T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 5.0V, EN = 1.8V, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Operating quiescent current into V_{IN}	I_{OUT} = 0mA, V_{OUT} = 5.0V, V_{IN} = 3.6V EN = V_{IN} Device not switching		33	45	µA
	Operating quiescent current into V_{OUT}			7	15	µA
I_{SD}	Shutdown current	EN = GND		0.85	5.0	µA
V_{UVLO}	Under-voltage lockout threshold	Falling		2.0	2.1	V
		Hysteresis		0.1		V
ENABLE						
V_{IL}	Low-level input voltage				0.4	V
V_{IH}	High-level input voltage		1.0			V
I_{lkg}	Input leakage current	Input connected to GND or V_{IN}			0.5	µA

Electrical Characteristics (continued)

Minimum and maximum values are at V_{IN} = 2.5V to 5.5V, V_{OUT} = 5.0V (or V_{IN}, whichever is higher), EN = 1.8V, T_A = –40°C to 85°C; Circuit of Parameter Measurement Information section (unless otherwise noted). Typical values are at V_{IN} = 3.6V, V_{OUT} = 5.0V, EN = 1.8V, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_{OUT}	DC output voltage accuracy	2.5V ≤ V_{IN} ≤ 4.85V, I_{OUT} = 0mA PWM operation. Open Loop	4.92	5.0	5.08	V
		2.5V ≤ V_{IN} ≤ 4.85V, 0mA ≤ I_{OUT} ≤ 650mA 3.3V ≤ V_{IN} ≤ 4.85V, 0mA ≤ I_{OUT} ≤ 1000mA PFM/PWM operation	4.9	5.0	5.2	V
ΔV_{OUT}	Power-save mode output ripple voltage	PFM operation, I_{OUT} = 1mA		30		mVpk
	PWM mode output ripple voltage	PWM operation, I_{OUT} = 200mA		15		mVpk
POWER SWITCH						
$r_{DS(on)}$	High-side MOSFET on resistance			170		mΩ
	Low-side MOSFET on resistance			100		mΩ
I_{lkg}	Reverse leakage current into VOUT	EN = GND			3.5	µA
I_{LIM}	Pre-charge current limit		165	215	265	mA
	Switch valley current limit	EN = V_{IN}. Open Loop	1900	2400	2900	mA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C
OSCILLATOR						
f_{OSC}	Oscillator frequency	V_{IN} = 3.6V		3.5		MHz
TIMING						
	Start-up time	I_{OUT} = 0mA Time from active EN to V_{OUT}		700		µs

6.6 Typical Characteristics

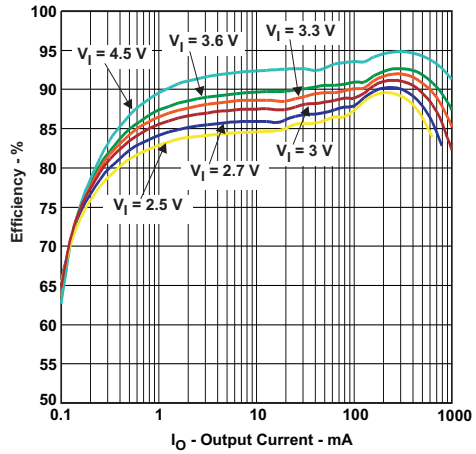


Figure 1. Efficiency vs Output Current

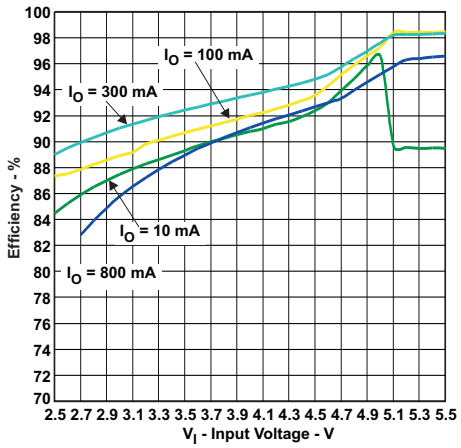


Figure 2. Efficiency vs Input Voltage

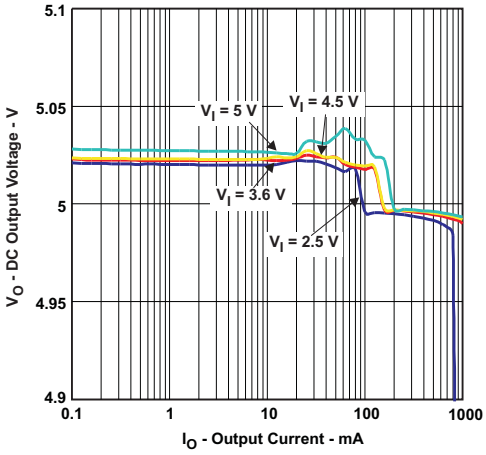


Figure 3. DC Output Voltage vs Output Current

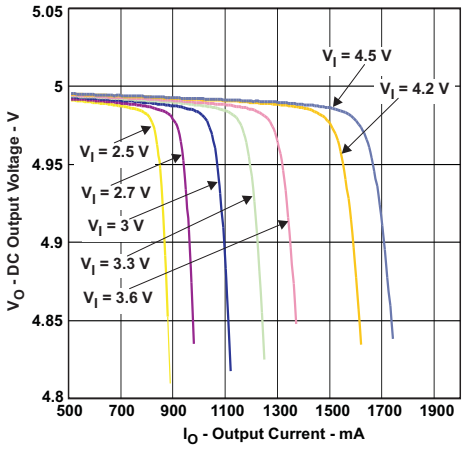


Figure 4. DC Output Voltage vs Output Current

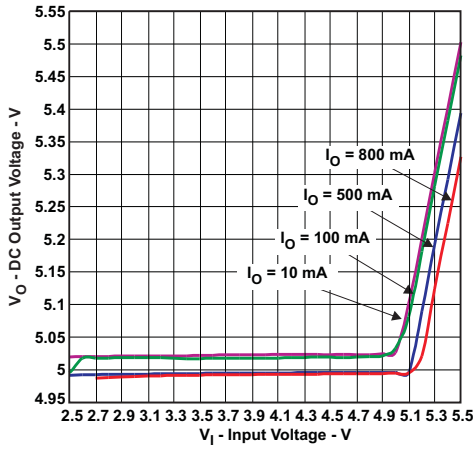


Figure 5. DC Output Voltage vs Input Voltage

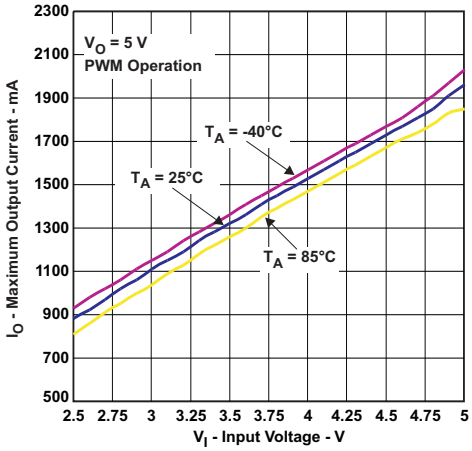


Figure 6. Maximum Output Currentvs Input Voltage

Typical Characteristics (continued)

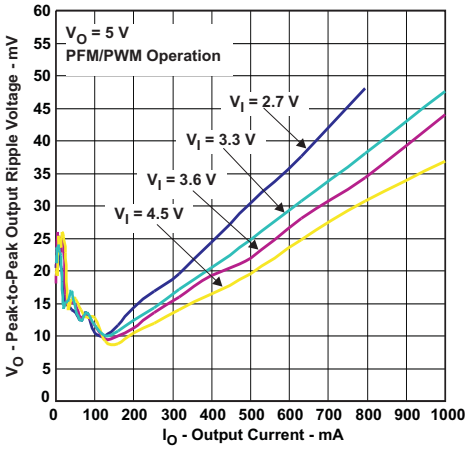


Figure 7. Peak-To-Peak Output Ripple Voltage vs Output Current

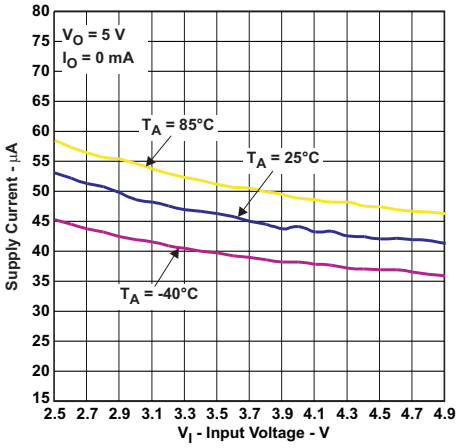


Figure 8. Supply Currentvs Input Voltage

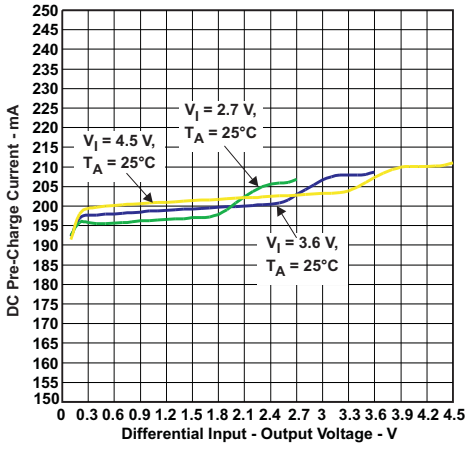


Figure 9. DC Pre-Charge Currentvs Differential Input-Output Voltage

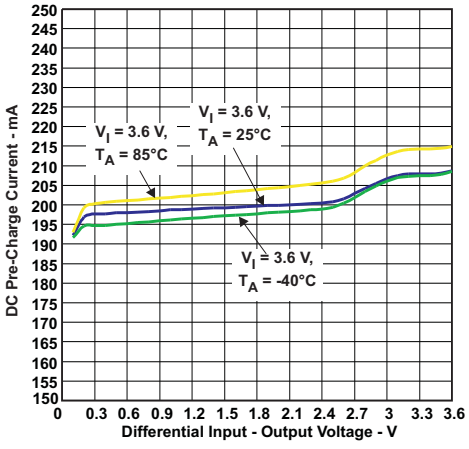


Figure 10. DC Pre-Charge Currentvs Differential Input-Output Voltage

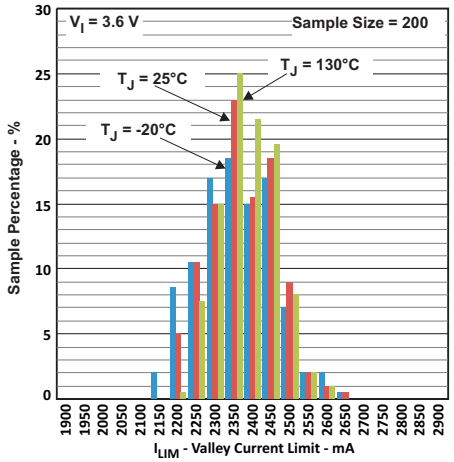


Figure 11. Valley Current Limit

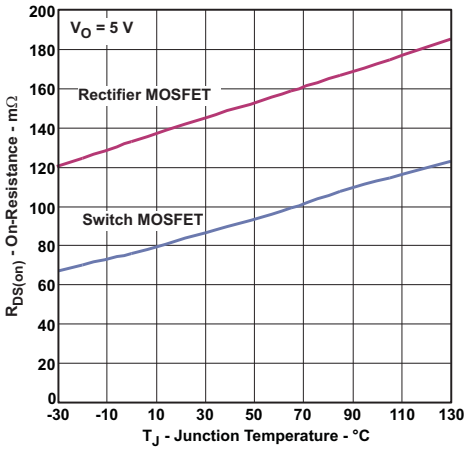


Figure 12. MOSFET Rds(On) vs Temperature

7 Parameter Measurement Information

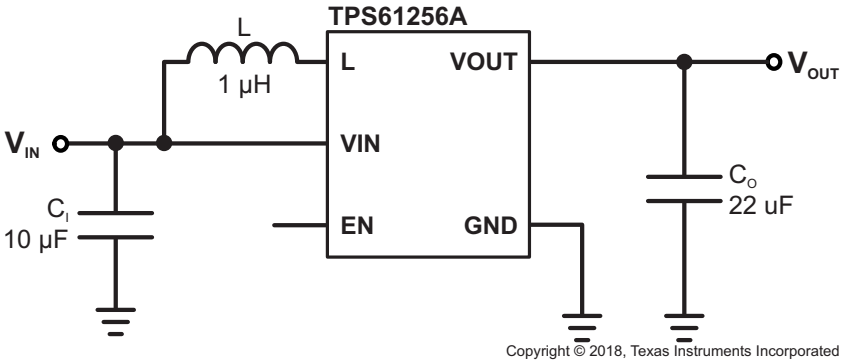


Table 1. List of Components

REFERENCE	DESCRIPTION	PART NUMBER, MANUFACTURER
L	1.0µH, 2.5A, 50mΩ, 3.2 x 2.5 x 1.2mm max. height	DFE322512C-1R0N, TOKO
C_I	10µF, 6.3V, 0603, X5R ceramic	GRM188R60J106ME84, muRata
C_O	22µF, 10V, 1210, X5R ceramic	GRM32ER71A226K, muRata

8 Detailed Description

8.1 Overview

The TPS61256A synchronous step-up converter typically operates at a quasi-constant 3.5-MHz frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the TPS61256A converter operates in power-save mode with pulse frequency modulation (PFM).

During PWM operation, the converter uses a novel quasi-constant on-time valley current mode control scheme to achieve excellent line/load regulation and allows the use of a small ceramic inductor and capacitors. Based on the V_{IN}/V_{OUT} ratio, a simple circuit predicts the required on-time.

At the beginning of the switching cycle, the low-side N-MOS switch is turned-on and the inductor current ramps up to a peak current that is defined by the on-time and the inductance. In the second phase, once the on-timer has expired, the rectifier is turned-on and the inductor current decays to a preset valley current threshold. Finally, the switching cycle repeats by setting the on timer again and activating the low-side N-MOS switch.

In general, a dc/dc step-up converter can only operate in "true" boost mode, i.e. the output “boosted” by a certain amount above the input voltage. The TPS61256A device operates differently as it can smoothly transition in and out of zero duty cycle operation. Therefore the output can be kept as close as possible to its regulation limits even though the converter is subject to an input voltage that tends to be excessive. Refer to the typical characteristics section (DC Output Voltage vs. Input Voltage) for further details.

The current mode architecture with adaptive slope compensation provides excellent transient load response, requiring minimal output filtering. Internal soft-start and loop compensation simplifies the design process while minimizing the number of external components.

8.2 Softstart

The TPS61256A device has an internal softstart circuit that limits the inrush current during start-up. The first step in the start-up cycle is the pre-charge phase. During pre-charge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch is current limited (approx. 200mA) during this phase. This mechanism is used to limit the output current under short-circuit condition.

Once the output capacitor has been biased to the input voltage, the converter starts switching. The soft-start system progressively increases the on-time as a function of the input-to-output voltage ratio. As soon as the output voltage is reached, the regulation loop takes control and full current operation is permitted.

8.3 Undervoltage Lockout

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. It disables the output stage of the converter once the falling V_{IN} trips the under-voltage lockout threshold V_{UVLO} which is typically 2.0V. The device starts operation once the rising V_{IN} trips V_{UVLO} threshold plus its hysteresis of 100 mV at typ. 2.1V.

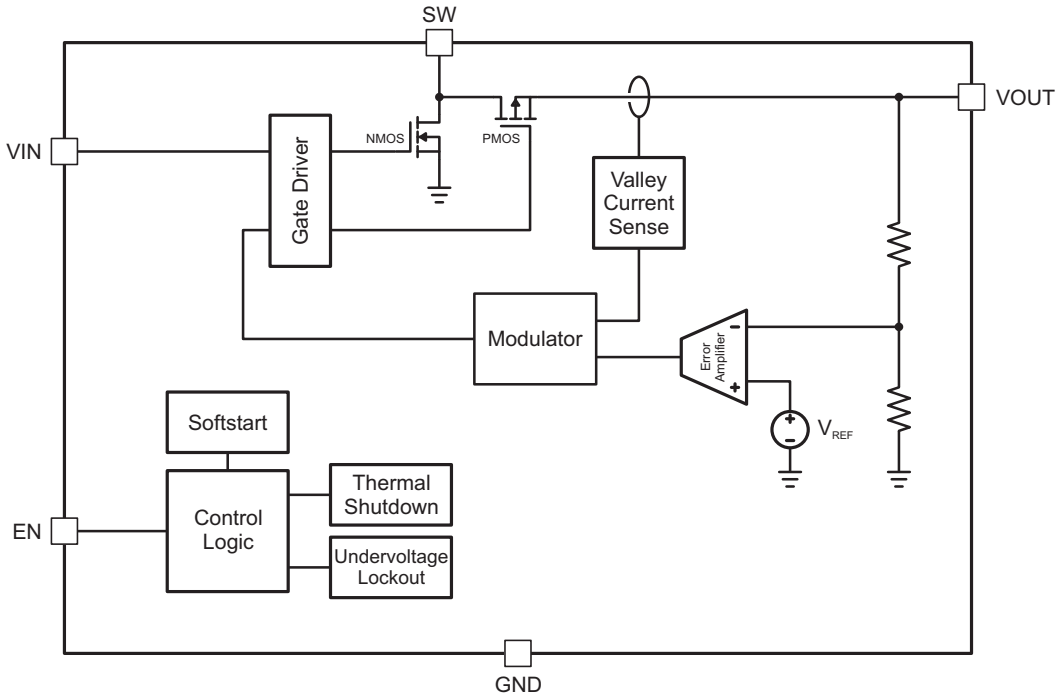
8.4 Thermal Regulation

The TPS61256A device contains a thermal regulation loop that monitors the die temperature during the pre-charge phase. If the die temperature rises to high values of about 110 °C, the device automatically reduces the current to prevent the die temperature from increasing further. Once the die temperature drops about 10 °C below the threshold, the device will automatically increase the current to the target value. This function also reduces the current during a short-circuit condition.

8.5 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typ.) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned-off. When the junction temperature falls below the thermal shutdown minus its hysteresis, the device continuous the operation.

8.6 Functional Block Diagram



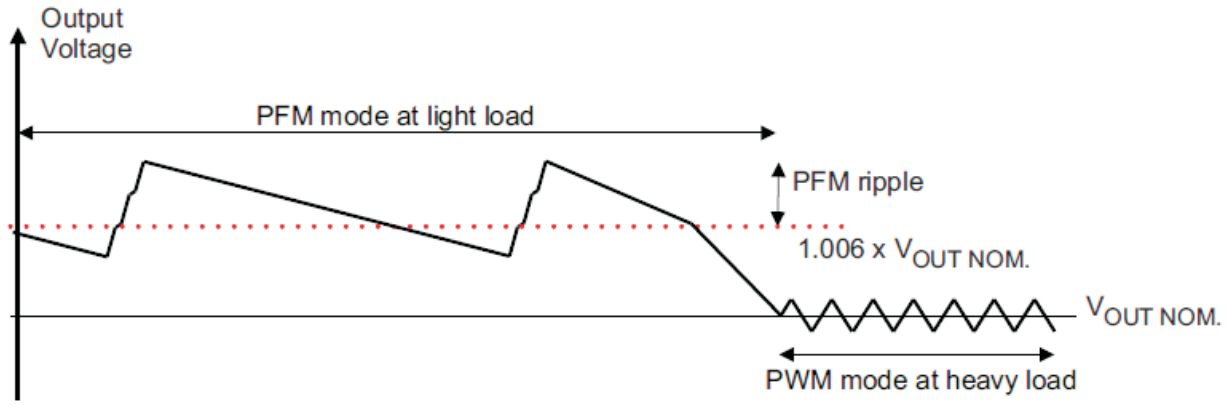
8.7 Feature Description

8.7.1 Power-Save Mode

The TPS61256A integrates a power-save mode to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage.

It ramps up the output voltage with several pulses and goes into power save mode once the output voltage exceeds the set threshold voltage.

The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode.



Feature Description (continued)

8.7.2 Current Limit Operation

The TPS61256A device employs a valley current limit sensing scheme. Current limit detection occurs during the off-time by sensing of the voltage drop across the synchronous rectifier.

The output voltage is reduced as the power stage of the device operates in a constant current mode. The maximum continuous output current ($I_{OUT(CL)}$), before entering current limit (CL) operation, can be defined by Equation 1.

$$I_{OUT(CL)} = (1 - D) \cdot \left(I_{VALLEY} + \frac{1}{2} \Delta I_L\right) \quad (1)$$

The duty cycle (D) can be estimated by Equation 2

$$D = 1 - \frac{V_{IN} \cdot \eta}{V_{OUT}} \quad (2)$$

and the peak-to-peak current ripple (ΔI_L) is calculated by Equation 3

$$\Delta I_L = \frac{V_{IN}}{L} \cdot \frac{D}{f} \quad (3)$$

The output current, $I_{OUT(DC)}$, is the average of the rectifier ripple current waveform. When the load current is increased such that the lower peak is above the current limit threshold, the off-time is increased to allow the current to decrease to this threshold before the next on-time begins (so called frequency fold-back mechanism). When the current limit is reached the output voltage decreases during further load increase.

illustrates the inductor and rectifier current waveforms during current limit operation.

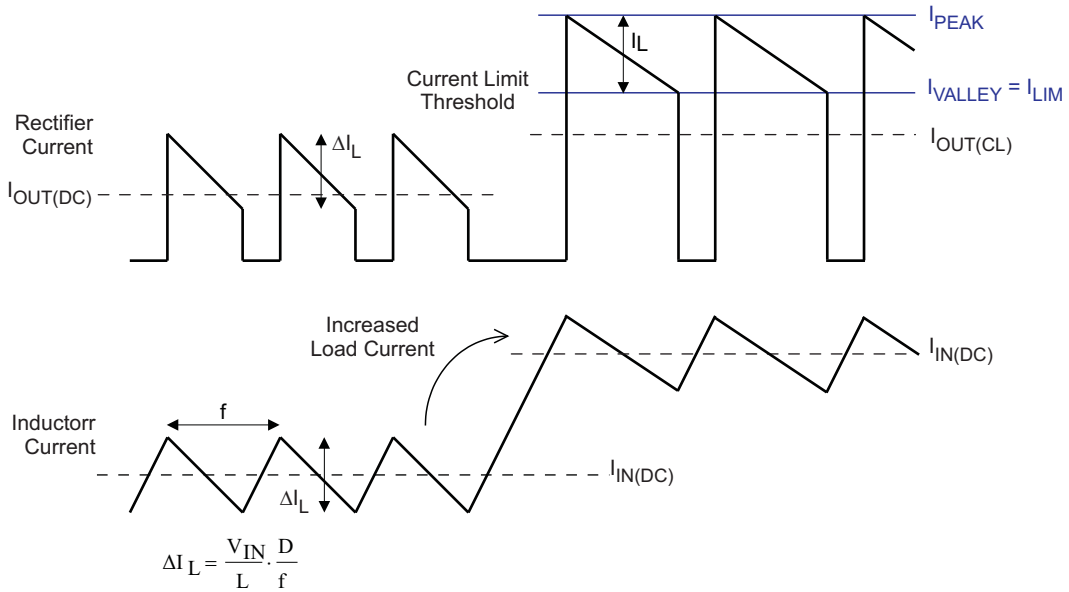


Figure 13. Inductor/Rectifier Currents In Current Limit Operation

8.7.3 Enable

The TPS61256A device starts operation when EN is set high and starts up with the soft-start sequence. For proper operation, the EN pin must be terminated and must not be left floating.

Pulling the EN pin low forces the device in shutdown, with a shutdown current of typically 1µA. In this mode, true load disconnect between the battery and load prevents current flow from V_{IN} to V_{OUT}, as well as reverse flow from V_{OUT} to V_{IN}.

Feature Description (continued)

8.7.4 Load Disconnect And Reverse Current Protection

Regular boost converters do not disconnect the load from the input supply and therefore a connected battery will be discharge during shutdown. The advantage of TPS61256A is that this converter is disconnecting the output from the input of the power supply when it is disabled (so called true shutdown mode). In case of a connected battery it prevents it from being discharge during shutdown of the converter.

8.8 Device Functional Modes

8.8.1 Load Disconnect And Reverse Current Protection

Regular boost converters do not disconnect the load from the input supply and therefore a connected battery will be discharge during shutdown. The advantage of TPS61256A is that this converter is disconnecting the output from the input of the power supply when it is disabled (so called true shutdown mode). In case of a connected battery it prevents it from being discharge during shutdown of the converter.

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The TPS61256A device has an internal softstart circuit that limits the inrush current during start-up. The first step in the start-up cycle is the pre-charge phase. During pre-charge, the rectifying switch is turned on until the output capacitor is charged to a value close to the input voltage. The rectifying switch is current limited (approx. 200mA) during this phase. This mechanism is used to limit the output current under short-circuit condition.

Once the output capacitor has been biased to the input voltage, the converter starts switching. The soft-start system progressively increases the on-time as a function of the input-to-output voltage ratio. As soon as the output voltage is reached, the regulation loop takes control and full current operation is permitted.

8.8.3 Undervoltage Lockout

The under voltage lockout circuit prevents the device from malfunctioning at low input voltages and the battery from excessive discharge. It disables the output stage of the converter once the falling V_{IN} trips the under-voltage lockout threshold V_{UVLO} which is typically 2.0V. The device starts operation once the rising V_{IN} trips V_{UVLO} threshold plus its hysteresis of 100 mV at typ. 2.1V.

8.8.4 Thermal Regulation

The TPS61256A device contains a thermal regulation loop that monitors the die temperature during the pre-charge phase. If the die temperature rises to high values of about 110 °C, the device automatically reduces the current to prevent the die temperature from increasing further. Once the die temperature drops about 10 °C below the threshold, the device will automatically increase the current to the target value. This function also reduces the current during a short-circuit condition.

8.8.5 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 140°C (typ.) the device goes into thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned-off. When the junction temperature falls below the thermal shutdown minus its hysteresis, the device continuous the operation.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

With a wide input voltage range of 2.5 V to 5.5 V, the TPS61256A supports applications powered by Li-Ion batteries with extended voltage range. Intended for low-power applications, it supports up to 800-mA load current from a battery discharged as low as 2.7 V and allows the use of low cost chip inductor and capacitors. Different fixed voltage output versions are available from 3.15 V to 5.0 V. The TPS61256A offers a very small solution size due to minimum amount of external components. It allows the use of small inductors and input capacitors to achieve a small solution size. During shutdown, the load is completely disconnected from the battery.

9.2 Typical Application

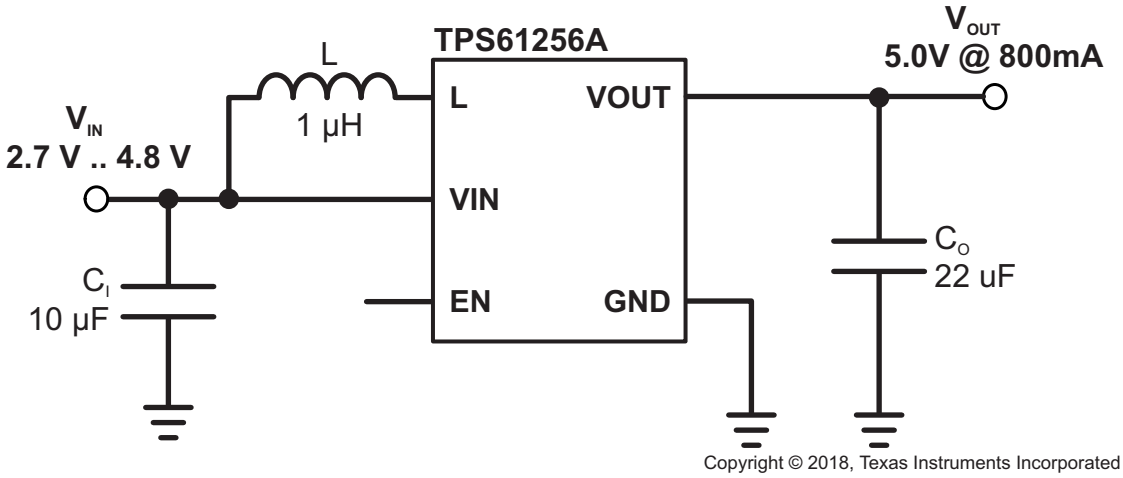


Figure 14. Typical Application

9.2.1 Design Requirements

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage Range	2.5 V to 4.5 V
Output Voltage	5 V
Output Voltage Ripple	±3% VOUT
Transient Response	±15% VOUT
Input Voltage Ripple	±200 mV
Output Current	800 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

A boost converter normally requires two main passive components for storing energy during the conversion, an inductor and an output capacitor are required. It is advisable to select an inductor with a saturation current rating higher than the possible peak current flowing through the power switches.

The inductor peak current varies as a function of the load, the input and output voltages and can be estimated using Equation 4.

$$I_{L(PEAK)} = \frac{V_{IN} \cdot D}{2 \cdot f \cdot L} + \frac{I_{OUT}}{(1-D) \cdot \eta} \quad \text{with} \quad D = 1 - \frac{V_{IN} \cdot \eta}{V_{OUT}} \tag{4}$$

Selecting an inductor with insufficient saturation performance can lead to excessive peak current in the converter. This could eventually harm the device and reduce it's reliability.

When selecting the inductor, as well as the inductance, parameters of importance are: maximum current rating, series resistance, and operating temperature. The inductor DC current rating should be greater (by some margin) than the maximum input average current, refer to Equation 5 and Current Limit Operation section for more details.

$$I_{L(DC)} = \frac{V_{OUT}}{V_{IN}} \cdot \frac{1}{\eta} \cdot I_{OUT} \tag{5}$$

The TPS61256A series of step-up converters have been optimized to operate with a effective inductance in the range of 0.7µH to 2.9µH and with output capacitors in the range of 22µF to 47µF. The internal compensation is optimized for an output filter of L = 1µH and C_O = 22µF. Larger or smaller inductor values can be used to optimize the performance of the device for specific operating conditions. For more details, see the Checking Loop Stability section.

9.2.2.1.1 High-frequency Converter Applications

In high-frequency converter applications, the efficiency is essentially affected by the inductor AC resistance (i.e. quality factor) and to a smaller extent by the inductor DCR value. To achieve high efficiency operation, care should be taken in selecting inductors featuring a quality factor above 25 at the switching frequency. Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

The total losses of the coil consist of both the losses in the DC resistance, $R_{(DC)}$, and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)
- Radiation losses

The following inductor series from different suppliers have been used with the TPS61256A converters.

Table 2. List Of Inductors

MANUFACTURER(1)	SERIES	DIMENSIONS (in mm)
MURATA	LQH44PN1R0NP0	4.0 x 4.0 x 1.8 max. height
HITACHI METALS	KSLI-322512BL1-1R0	3.2 x 2.5 x 1.2 max. height
TOKO	DFE322512C-1R0N	3.2 x 2.5 x 1.2 max. height

(1) See Third-party Products Disclaimer

9.2.2.2 Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the V_{OUT} and GND pins of the IC. To get an estimate of the recommended minimum output capacitance, Equation 6 can be used.

$$C_{MIN} = \frac{I_{OUT} \cdot (V_{OUT} - V_{IN})}{f \cdot \Delta V \cdot V_{OUT}} \quad (6)$$

Where f is the switching frequency which is 3.5MHz (typ.) and ΔV is the maximum allowed output ripple.

With a chosen ripple voltage of 20mV, a minimum effective capacitance of 9µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using Equation 7

$$V_{ESR} = I_{OUT} \cdot R_{ESR} \quad (7)$$

An MLCC capacitor with twice the value of the calculated minimum should be used due to DC bias effects. This is required to maintain control loop stability. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. There are no additional requirements regarding minimum ESR. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients but the total output capacitance value should not exceed ca. 50µF.

DC bias effect: high cap. ceramic capacitors exhibit DC bias effects, which have a strong influence on the device's effective capacitance. Therefore the right capacitor value has to be chosen very carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and it's effective capacitance. For instance, a 22µF X5R 6.3V 0805 MLCC capacitor would typically show an effective capacitance of less than 8µF (under 5V bias condition).

9.2.2.3 Input Capacitor

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 10µF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_I and the power source lead to reduce ringing than can occur between the inductance of the power source leads and C_I.

9.2.2.4 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signals:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

These are the basic signals that need to be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop may be unstable. This is often a result of board layout and/or L-C combination.

As a next step in the evaluation of the regulation loop, the load transient response is tested. The time between the application of the load transient and the turn on of the P-channel MOSFET, the output capacitor must supply all of the current required by the load. V_{OUT} immediately shifts by an amount equal to $\Delta I_{(LOAD)}$ x ESR, where ESR is the effective series resistance of C_{OUT}. $\Delta I_{(LOAD)}$ begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. The results are most easily interpreted when the device operates in PWM mode.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot or ringing that helps judge the converter's stability. Without any ringing, the loop has usually more than 45° of phase margin. Because the damping factor of the circuitry is directly related to several resistive parameters (e.g., MOSFET $r_{DS(on)}$) that are temperature dependant, the loop stability analysis has to be done over the input voltage range, load current range, and temperature range.

9.2.3 Application Curves

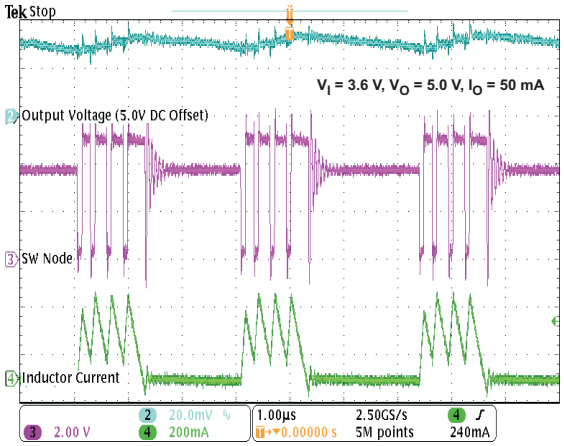


Figure 15. Power-Save Mode Operation

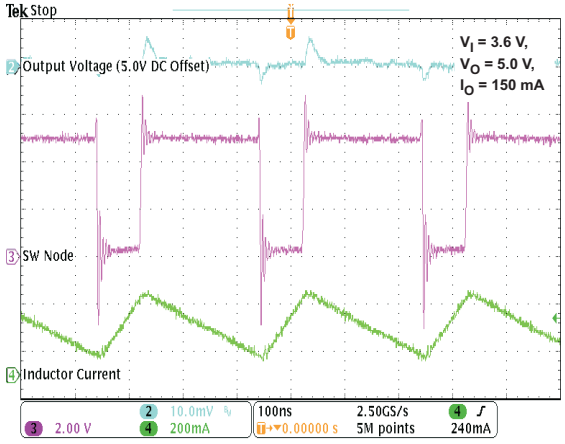


Figure 16. PWM Operation

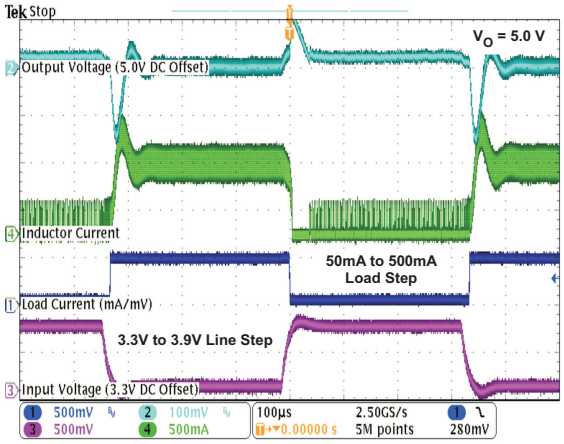


Figure 17. Combined Line/Load Transient Response

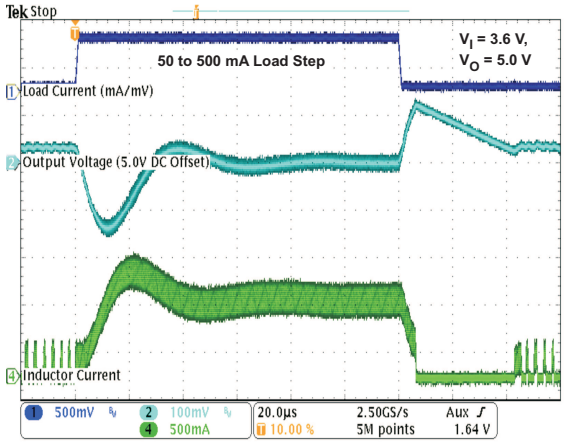


Figure 18. Load Transient Response InPFM/PWM Operation

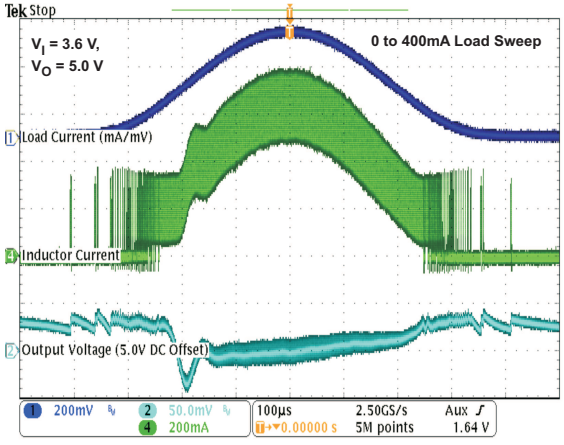


Figure 19. AC Load Transient Response

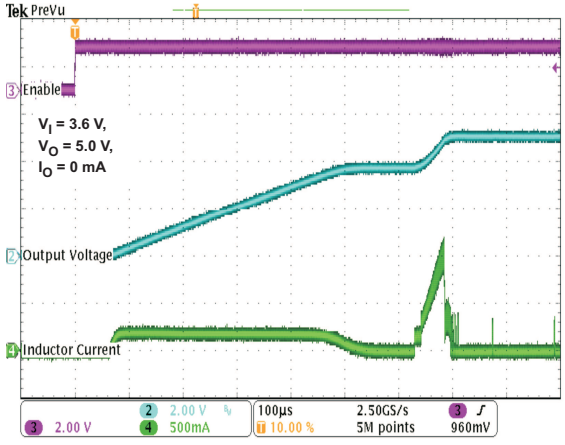


Figure 20. Start-Up

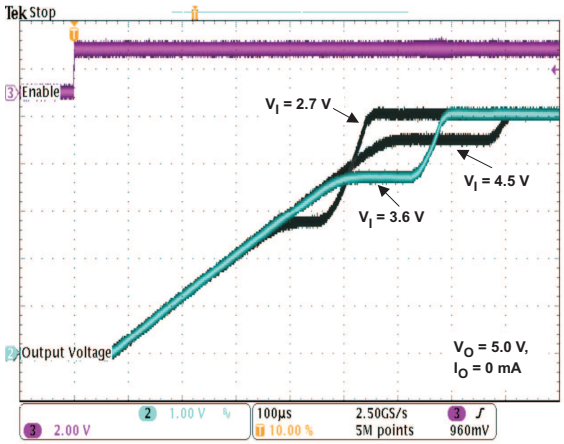


Figure 21. Start-Up

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 2.5 V and 4.5 V. This input supply must be well regulated. If the input supply is located more than a few inches from the converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to the ground pins of the IC.

11.2 Layout Example

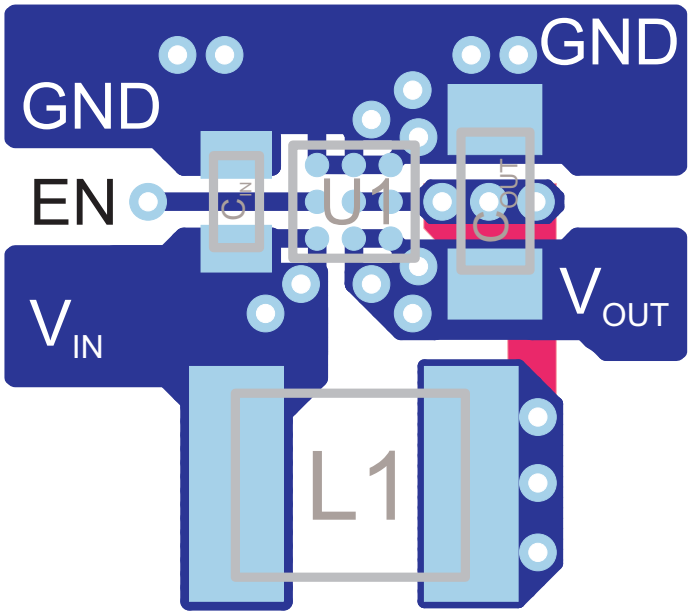


Figure 22. Suggested Layout (Top)

11.3 Thermal Information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

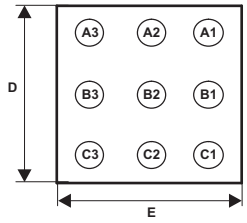
Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

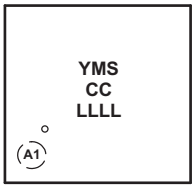
Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. The maximum junction temperature (T_J) of the TPS61256A is 125°C.

12 Package Summary

CHIP SCALE PACKAGE
(BOTTOM VIEW)



CHIP SCALE PACKAGE
(TOP VIEW)



Code:

- YM - 2 digit date code
- S - assembly site code
- CC - chip code (see ordering table)
- LLLL - lot trace code

12.1 Package Dimensions

The dimensions for the YFF-9 package are shown in Table 3. See the package drawing at the end of this data sheet.

Table 3. YFF-9 Package Dimensions

Packaged Devices	D	E
TPS61256AYFF	1.206 ±0.03 mm	1.306 ±0.03 mm

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.4 Trademarks

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

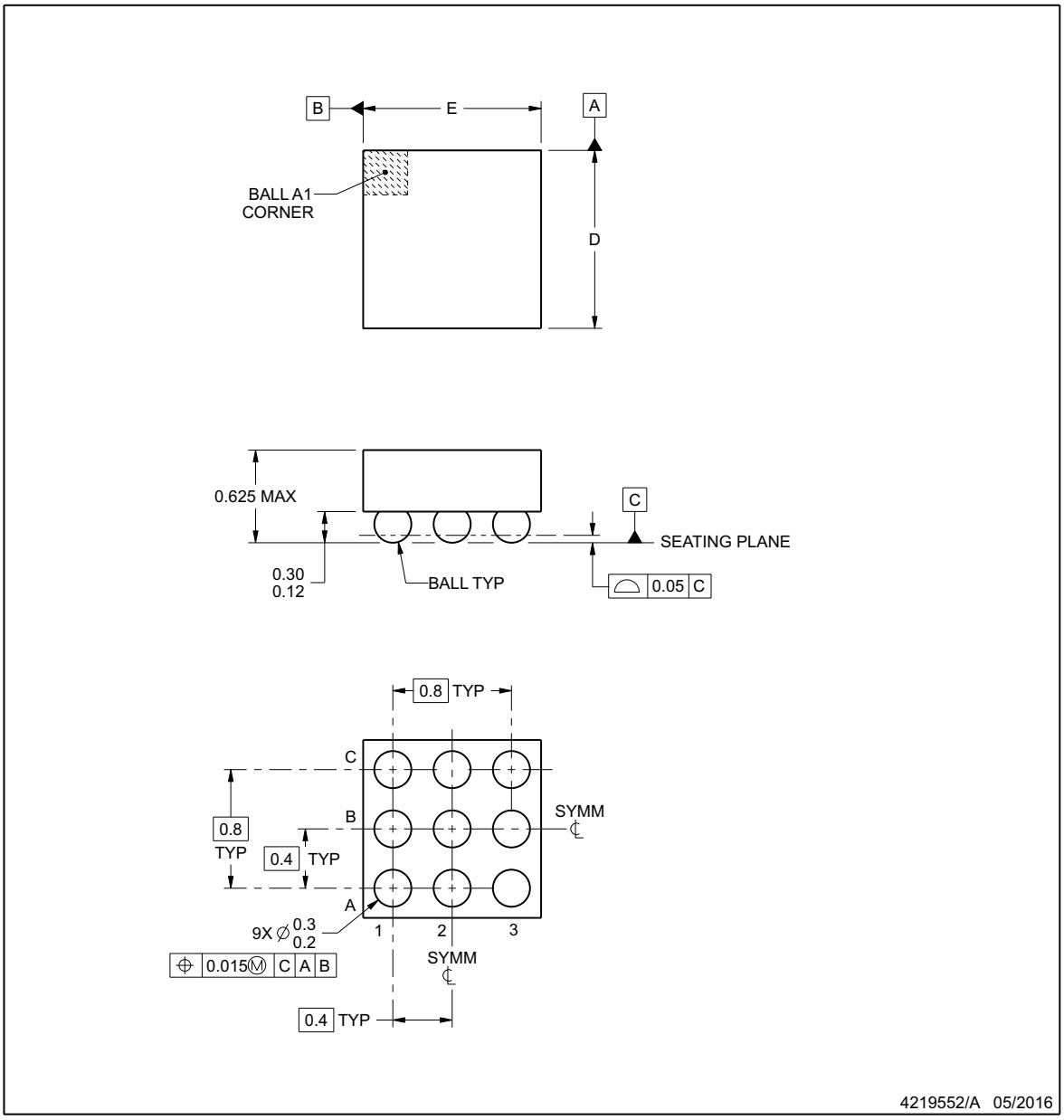
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

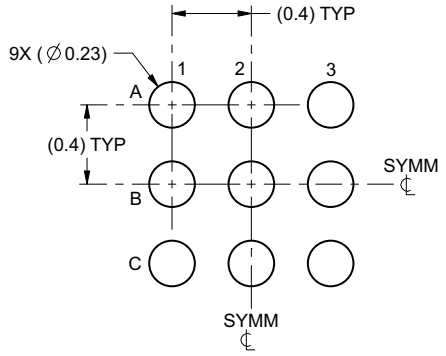
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

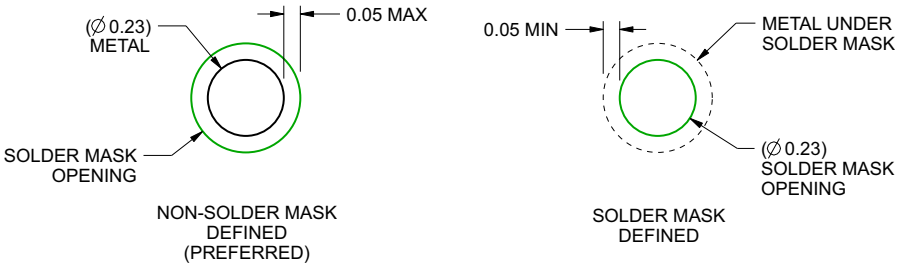
YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

4219552/A 05/2016

NOTES: (continued)

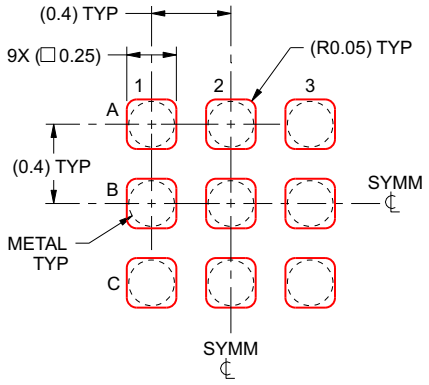
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61256AYFFR	ACTIVE	DSBGA	YFF	9	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	QXA	Samples
TPS61256AYFFT	ACTIVE	DSBGA	YFF	9	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	QXA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

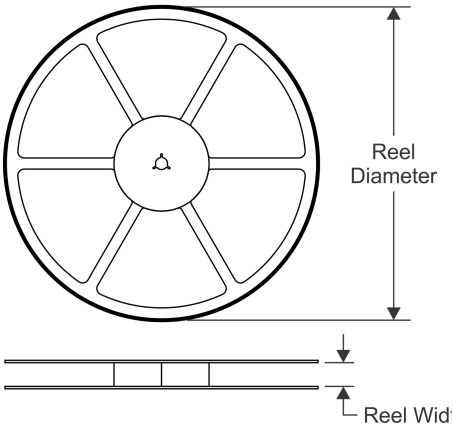
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

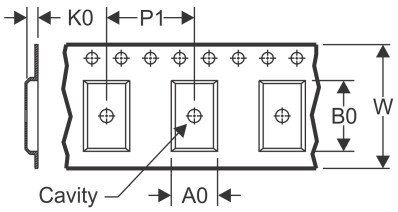
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

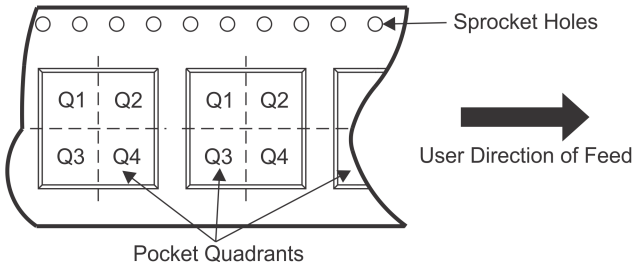


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

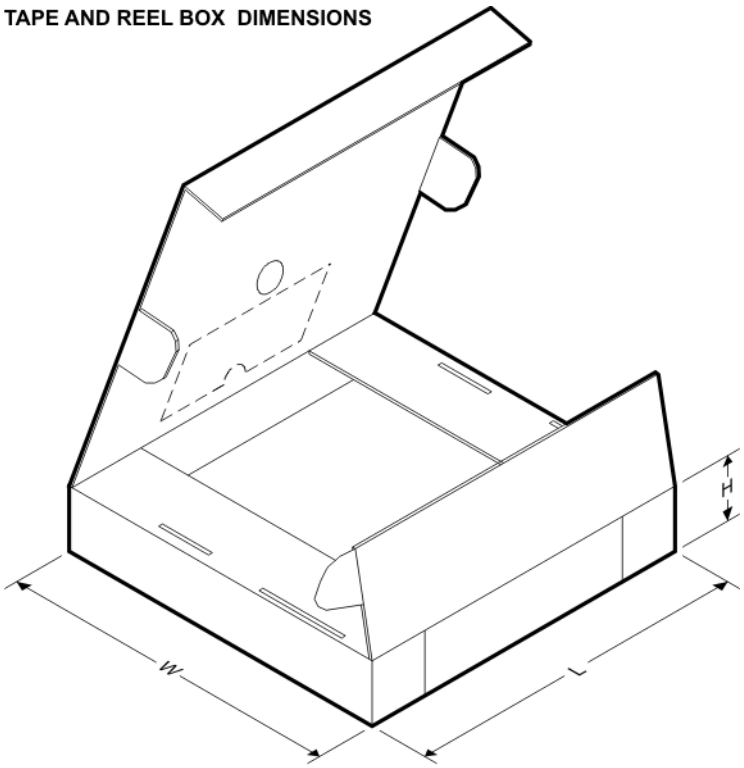
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61256AYFFR	DSBGA	YFF	9	3000	180.0	8.4	1.41	1.31	0.69	4.0	8.0	Q1
TPS61256AYFFT	DSBGA	YFF	9	250	180.0	8.4	1.41	1.31	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

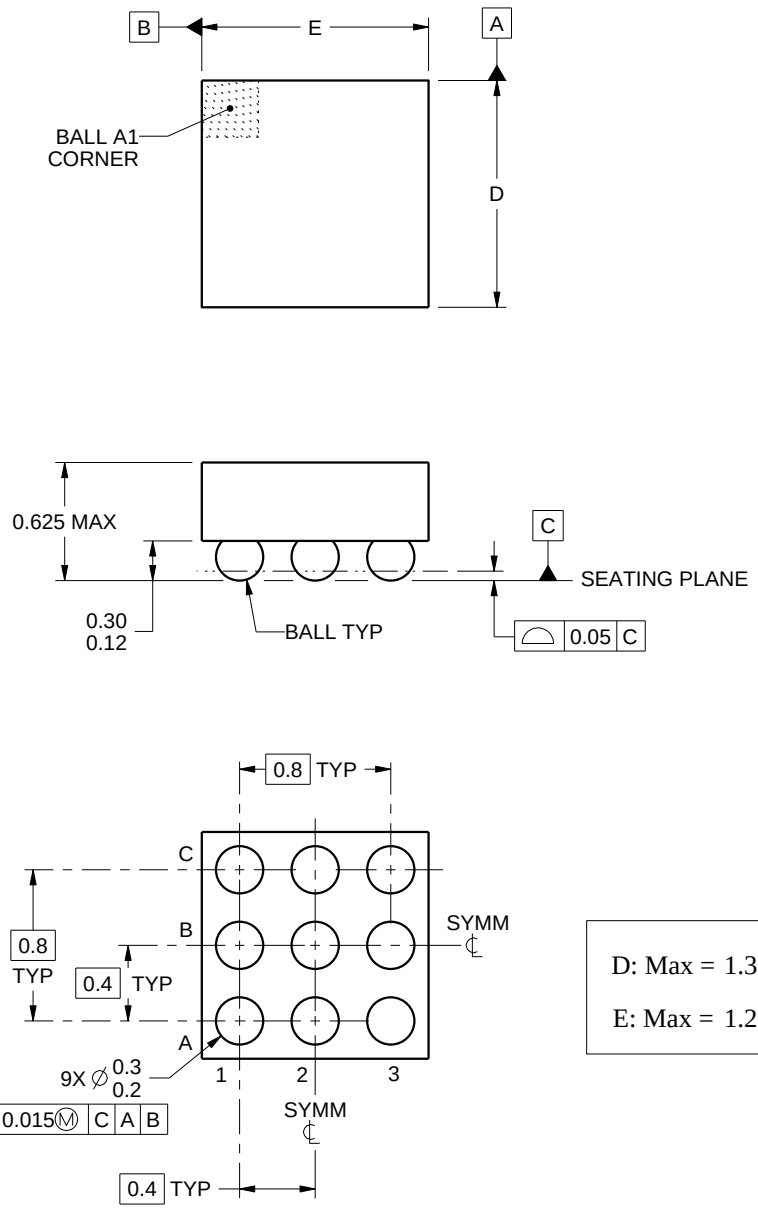
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61256AYFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0
TPS61256AYFFT	DSBGA	YFF	9	250	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



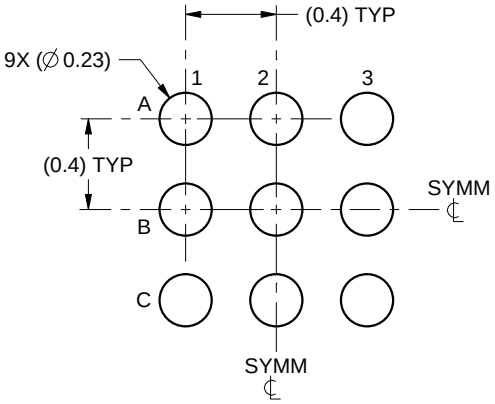
D: Max = 1.336 mm, Min =1.276 mm

E: Max = 1.236 mm, Min =1.176 mm

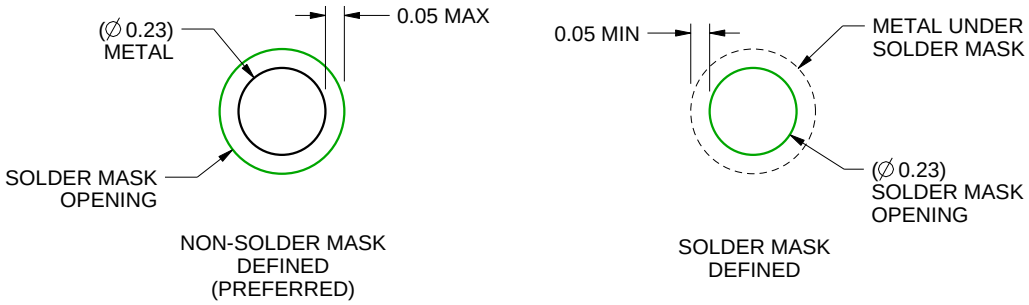
4219552/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

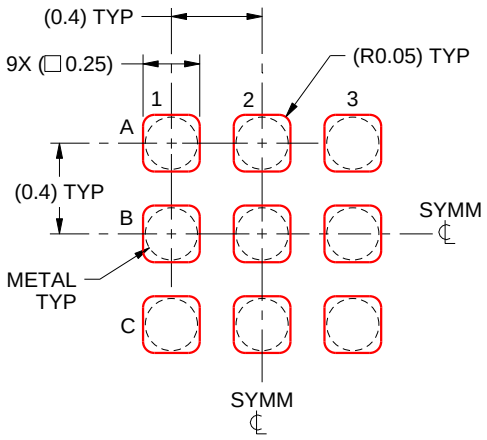


SOLDER MASK DETAILS
NOT TO SCALE

4219552/A 05/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219552/A 05/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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